ALPHA & OMEGA SEMICONDUCTOR

AO4918

Asymmetric Dual N-Channel Enhancement Mode Field Effect Transistor

General Description

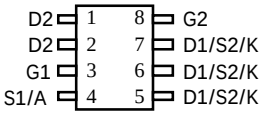
The AO4918 uses advanced trench technology to provid excellent $R_{DS(ON)}$ and low gate charge. The two MOSFETs make a compact and efficient switch and synchronous rectifier combination for use in DC-DC converters. A Schottky diode is co-packaged in parallel with the synchronous MOSFET to boost efficiency furthe *Standard Product AO4918 is Pb-free (meets ROHS & Sony 259 specifications). AO4918L is a Green Product ordering option. AO4918 and AO4918L are electrically identical.*

Features

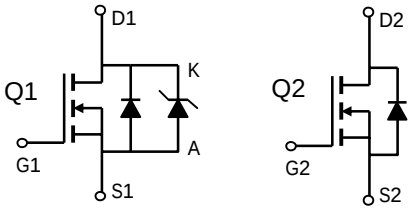
Q1	Q2	
V_{DS} (V) = 30V	V_{DS}(V) = 30V	
I_D = 9.3A (V_{GS} = 10V)	I_D=8.3A	(V_{GS} = 10V
$R_{DS(ON)}$ < 14.5mΩ	<18mΩ	(V_{GS} = 10V)
$R_{DS(ON)}$ < 16mΩ	<27mΩ	(V_{GS} = 4.5V)

SCHOTTKY

V_{DS} (V) = 30V, I_F = 3A, V_F<0.5V@1A



SOIC-8



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Max Q1	Max Q2	Units
Drain-Source Voltage		V_{DS}	30	30	V
Gate-Source Voltage		V_{GS}	±12	±20	V
Continuous Drain Current [A]	T_A=25°C	I_D	9.3	8.3	A
	T_A=70°C		7.4	6.7	
Pulsed Drain Current [B]		I_{DM}	40	40	
Power Dissipation	T_A=25°C	P_D	2	2	W
	T_A=70°C		1.28	1.28	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	-55 to 150	°C

Parameter		Symbol	Maximum Schottky	Units
Reverse Voltage		V_{DS}	30	V
Continuous Forward Current [A]	T_A=25°C	I_F	3	A
	T_A=70°C		2.2	
Pulsed Diode Forward Current [B]		I_{FM}	20	
Power Dissipation [A]	T_A=25°C	P_D	2	W
	T_A=70°C		1.28	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Parameter: Thermal Characteristics MOSFET Q1		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	53	62.5	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		81.9	110	
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	30.5	40	

Parameter: Thermal Characteristics MOSFET Q2		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	53	62.5	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		81.9	110	
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	30.5	40	

Thermal Characteristics Schottky					
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	50.4	62.5	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		86	110	
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	26.6	40	

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

D. The static characteristics in Figures 1 to 6 are obtained using 80 μs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

F. The Schottky appears in parallel with the MOSFET body diode, even though it is a separate chip. Therefore, we provide the net forward drop, capacitance and recovery characteristics of the MOSFET and Schottky. However, the thermal resistance is specified for each chip separately.

Rev4: August 2005

Q1 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current. (Set by Schottky leakage)	V_R=30V		0.007	0.05	mA
		V_R=30V, T_J=125°C		3.2	10	
		V_R=30V, T_J=150°C		12	20	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±12V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	0.6	1.1	2	V
$I_{D(ON)}$	On state drain current	V_{GS}=4.5V, V_{DS}=5V	40			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=9.3A		11.7	14.5	mΩ
		T_J=125°C		15.4	19	
		V_{GS}=4.5V, I_D=8.8A		13.1	16	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=9.3A	30	37		S
V_{SD}	Diode+Schottky Forward Voltage	I_S=1A		0.46	0.5	V
I_S	Maximum Body-Diode+Schottky Continuous Current				3.5	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		3740	4488	pF
C_{oss}	Output Capacitance (FET + Schottky)			295		pF
C_{rss}	Reverse Transfer Capacitance			186		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		0.86	1.1	Ω
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	V_{GS}=4.5V, V_{DS}=15V, I_D=9.3A		30.5	37	nC
Q_{gs}	Gate Source Charge			4.5		nC
Q_{gd}	Gate Drain Charge			8.5		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=1.6Ω, R_{GEN}=3Ω		6	9	ns
t_r	Turn-On Rise Time			8.2	12	ns
$t_{D(off)}$	Turn-Off DelayTime			54.5	75	ns
t_f	Turn-Off Fall Time			10.5	15	ns
t_{rr}	Body Diode + Schottky Reverse Recovery Time	I_F=9.3A, dI/dt=100A/µs		23.5	28	ns
Q_{rr}	Body Diode + Schottky Reverse Recovery Charge	I_F=9.3A, dI/dt=100A/µs		13.3	16	nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in ^{2} FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

D. The static characteristics in Figures 1 to 6,12,14 are obtained using 80 µs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in ^{2} FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

F. The Schottky appears in parallel with the MOSFET body diode, even though it is a separate chip. Therefore, we provide the net forward drop, capacitance and recovery characteristics of the MOSFET and Schottky. However, the thermal resistance is specified for each chip separately

Rev4: August 2005.

Q1 TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

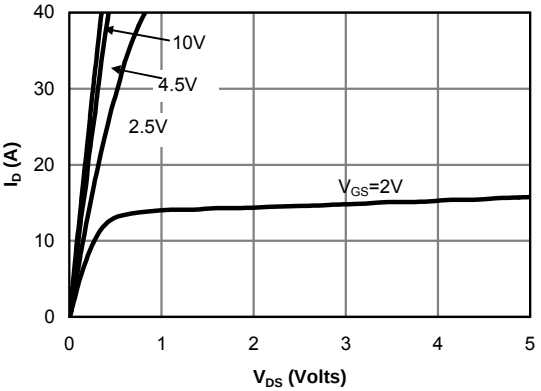


Fig 1: On-Region Characteristics

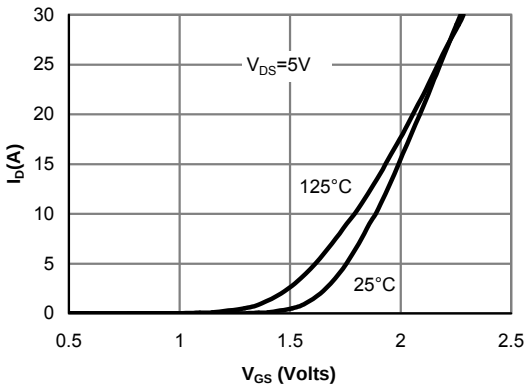


Figure 2: Transfer Characteristics

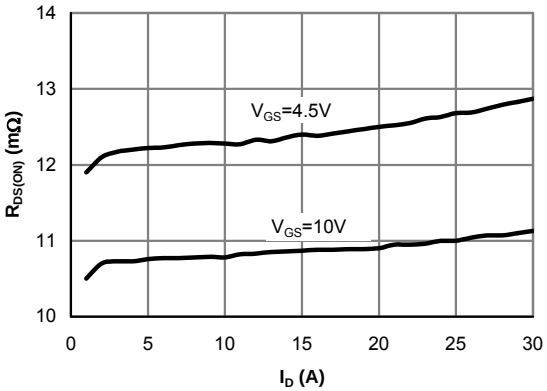


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

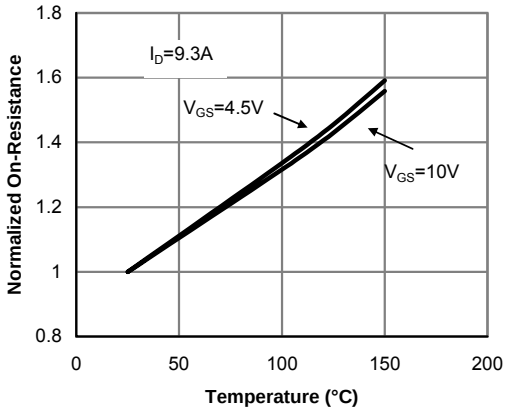


Figure 4: On resistance vs. Junction Temperature

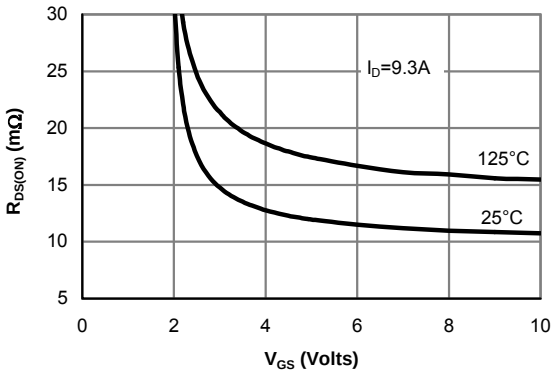


Figure 5: On resistance vs. Gate-Source Voltage

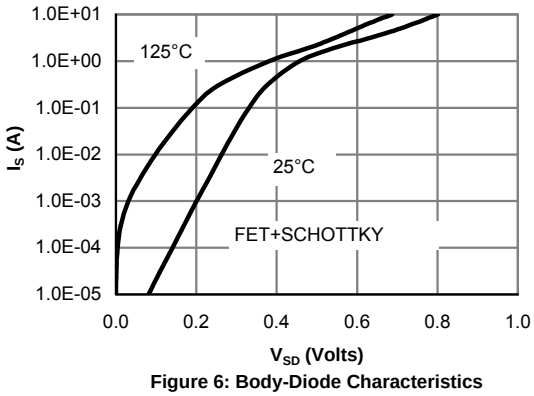


Figure 6: Body-Diode Characteristics (Note F)

Q1 TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

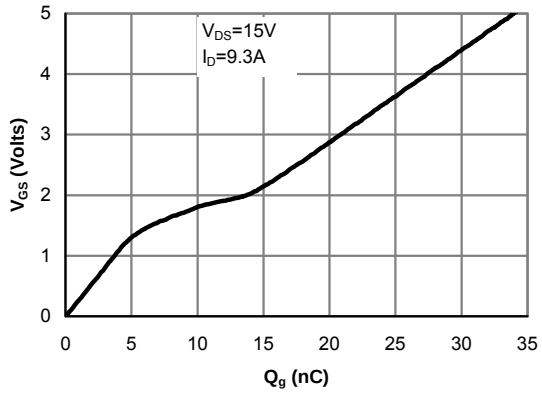


Figure 7: Gate-Charge Characteristics

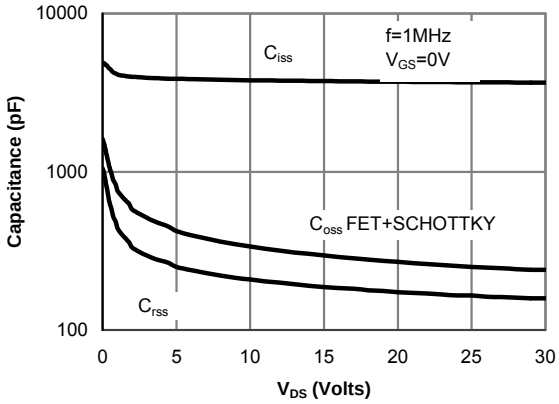


Figure 8: Capacitance Characteristics

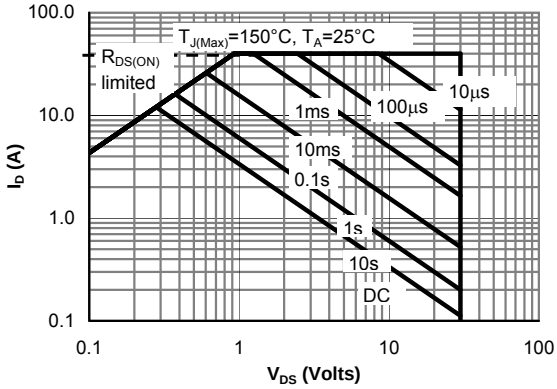


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

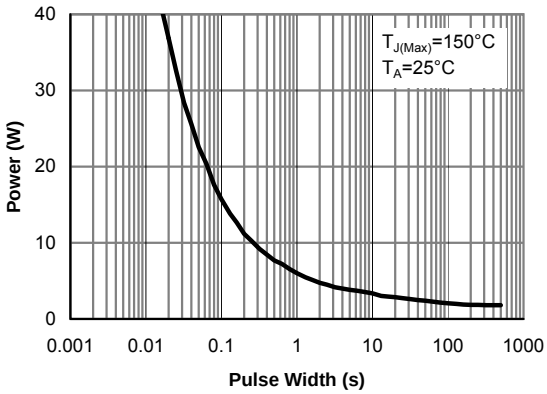


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

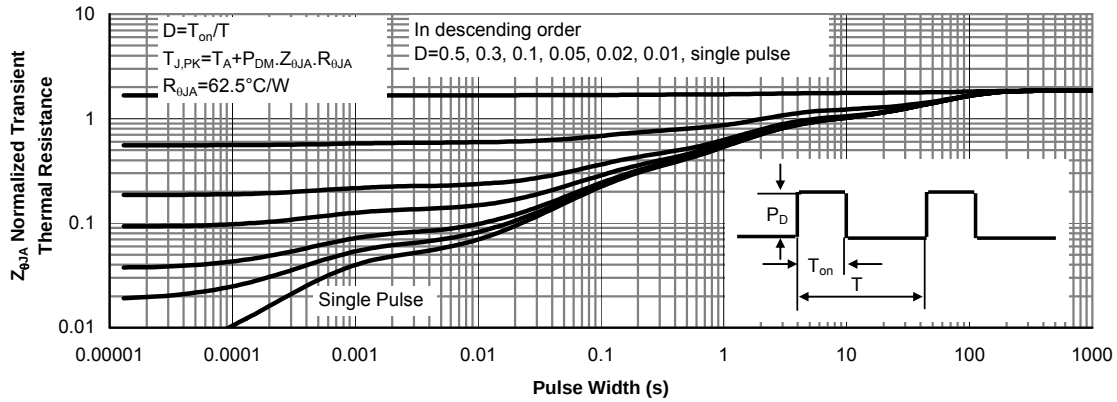


Figure 11: Normalized Maximum Transient Thermal Impedance

Q2 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=24V, V_{GS}=0V		0.004	1	µA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	1	1.8	3	V
$I_{D(ON)}$	On state drain current	V_{GS}=4.5V, V_{DS}=5V	30			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=8.3A		14.9	18	mΩ
		T_J=125°C		22	27	
		V_{GS}=4.5V, I_D=7A		21.6	27	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=8.3A		23		S
V_{SD}	Diode+Schottky Forward Voltage	I_S=1A		0.45	0.5	V
I_S	Maximum Body-Diode+Schottky Continuous Current				3	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		1040	1250	pF
C_{oss}	Output Capacitance			180		pF
C_{rss}	Reverse Transfer Capacitance			110		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		0.7	0.85	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=8.3A		19.2	24	nC
Q_g	Total Gate Charge			9.36	12	nC
Q_{gs}	Gate Source Charge			2.6		nC
Q_{gd}	Gate Drain Charge			4.2		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=1.8Ω, R_{GEN}=3Ω		5.2	7.5	ns
t_r	Turn-On Rise Time			4.4	6.5	ns
$t_{D(off)}$	Turn-Off DelayTime			17.3	25	ns
t_f	Turn-Off Fall Time			3.3	5	ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=8.5A, dI/dt=100A/µs		16.7	21	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=8.5A, dI/dt=100A/µs		6.7	10	nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

D. The static characteristics in Figures 1 to 6,12,14 are obtained using 80µs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

Rev4: August 2005

Q2 Electrical Characteristics (T_J=25°C unless otherwise noted)

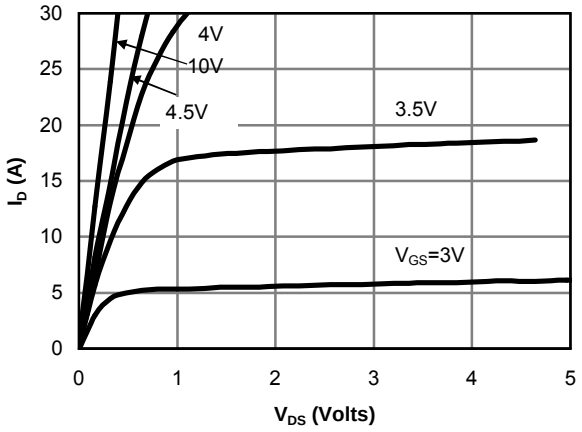


Fig 1: On-Region Characteristics

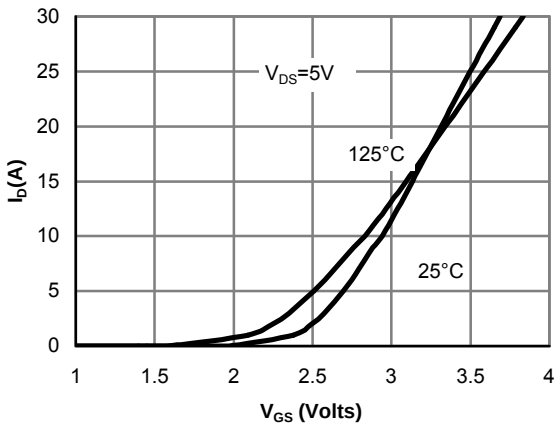


Figure 2: Transfer Characteristics

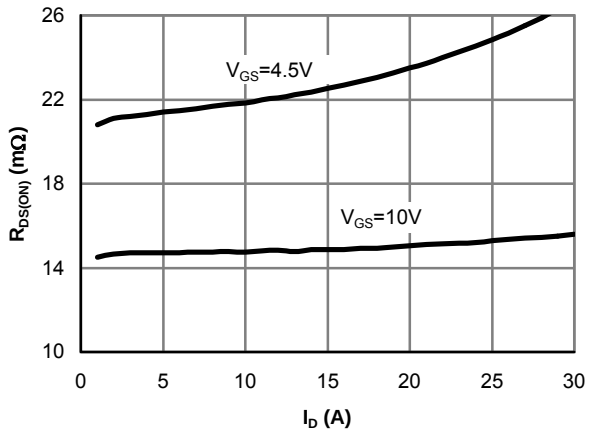


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

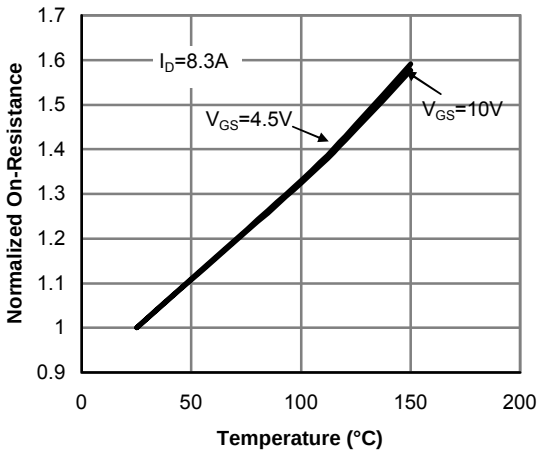


Figure 4: On resistance vs. Junction Temperature

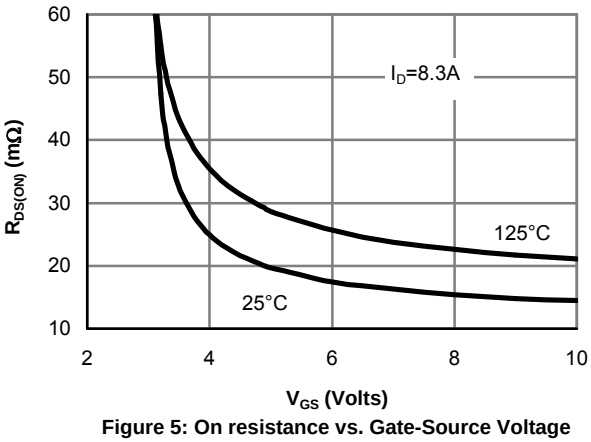


Figure 5: On resistance vs. Gate-Source Voltage

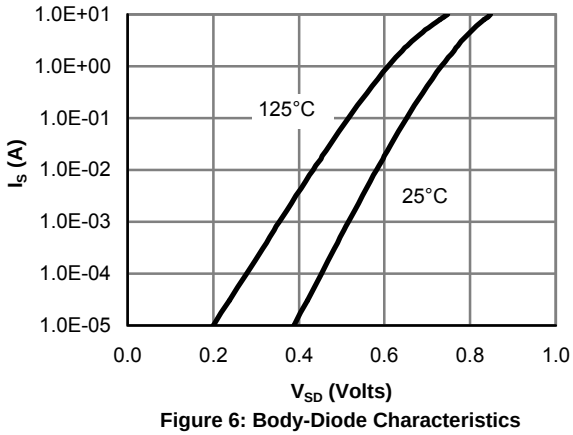


Figure 6: Body-Diode Characteristics

Q2 Electrical Characteristics (T_J=25°C unless otherwise noted)

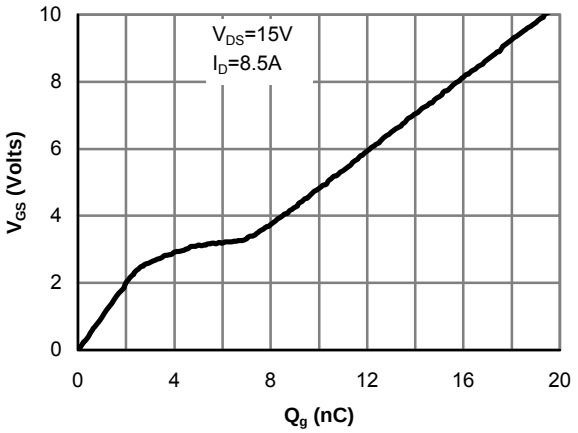


Figure 7: Gate-Charge Characteristics

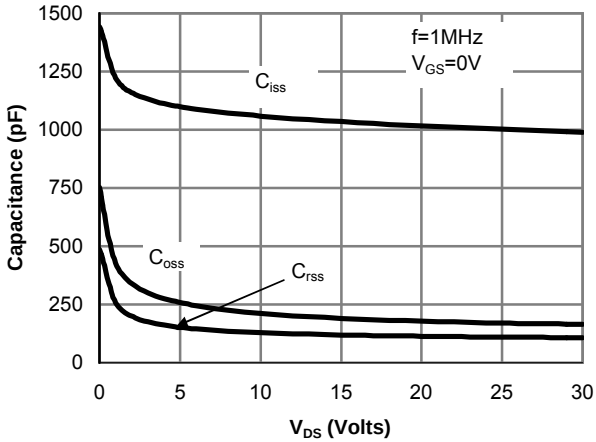


Figure 8: Capacitance Characteristics

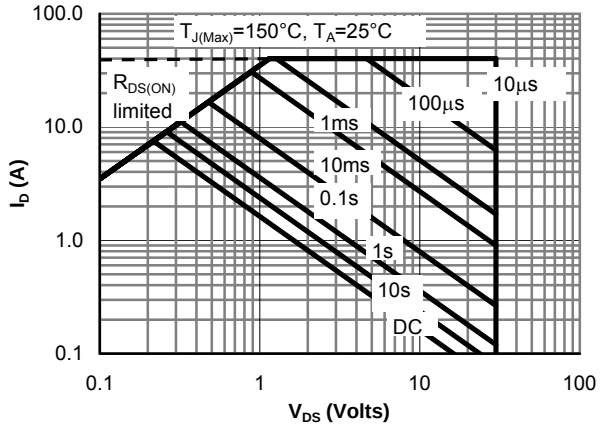


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

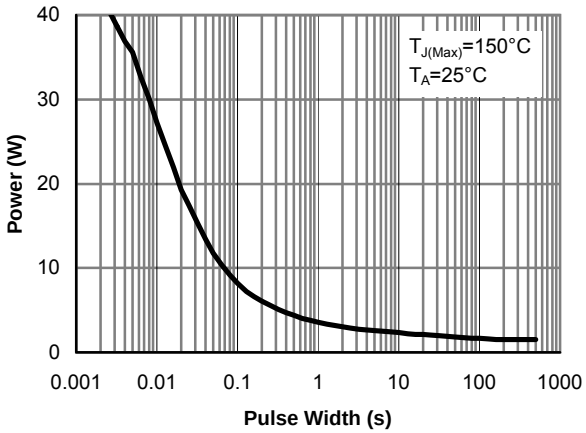


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

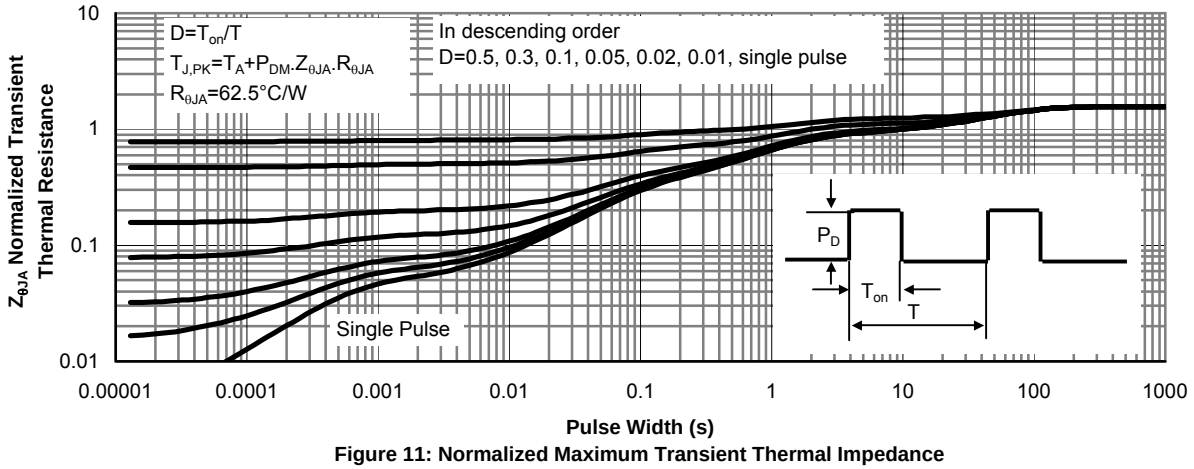


Figure 11: Normalized Maximum Transient Thermal Impedance