Fortune
Semiconductor Corporation
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FS9168

8-bit MCU with 1k program ROM, 64-byte RAM, 1 R2F module and 3 × 13 LCD driver.

Data Sheet

TD-0410001

Rev. 1.2

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1. General Description

The FS9168 is an 8-bit high performance, low cost microcontroller. The device is suited for use in low power LCD applications such as: capacitor scales, toys, thermometer, hand held LCD products…etc.

2. Features

- **Embedded 1K x 14 program memory, 64-byte data memory, 8-bit microcontroller.**
- **1.5V battery operation, with about 40μA (Typ.) operation current, and 0.2μA (Typ.) sleep mode current .**
- **Build-in voltage doubler for LCD driver.**
- **1/3 duty, 1/2 bias 3x13 LCD driver.**
- **One resistance to frequency conversion module for thermistor and reference resistor.**
- **One high-speed comparator and one 16-bit counter with programmable gate time select.**
- **Two buzzer outputs.**
- **One 4-bit input port, one 4-bit I/O port.**
- **Build in low battery detector.**
- **Package: Dice form (36 pins), 44-pin LQFP.**

3. Applications

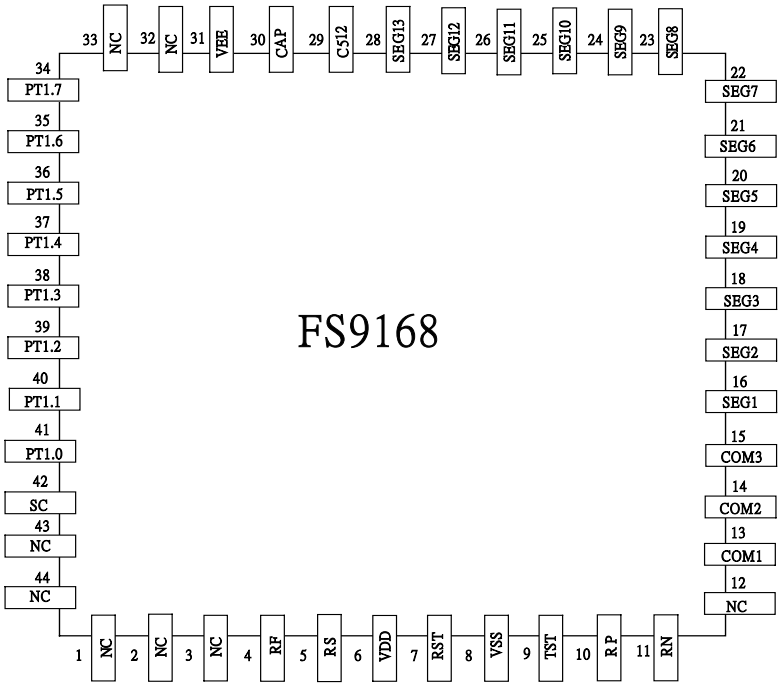
- **Thermometer.**
- **Hygrometer.**
- **Capacitor Scale.**
- **R/C Type Sensor Measurement.**

4. Ordering Information

Product Number	Package Type
FS9168-nnnV	Dice form of 36 pin, or 44 pin LQFP

Note1: Code number ”nnnV” is assigned for customer; ”nnn” = 001~999; ”V” means Version = A~Z.

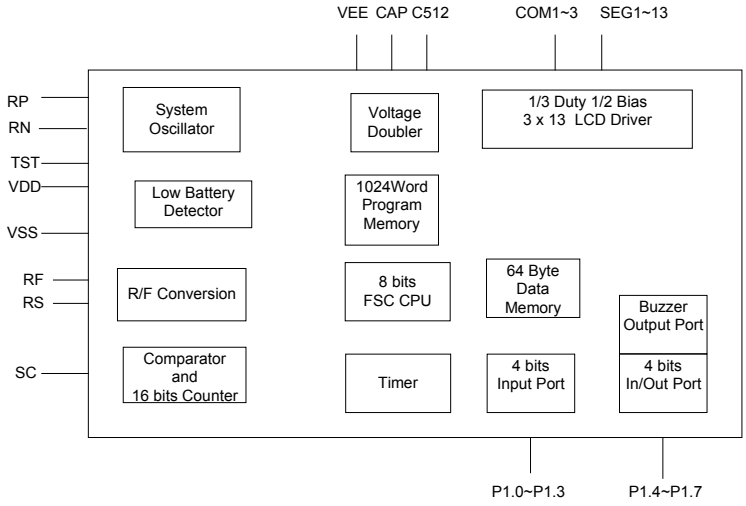
5. Pin Configuration



6. Pin Description

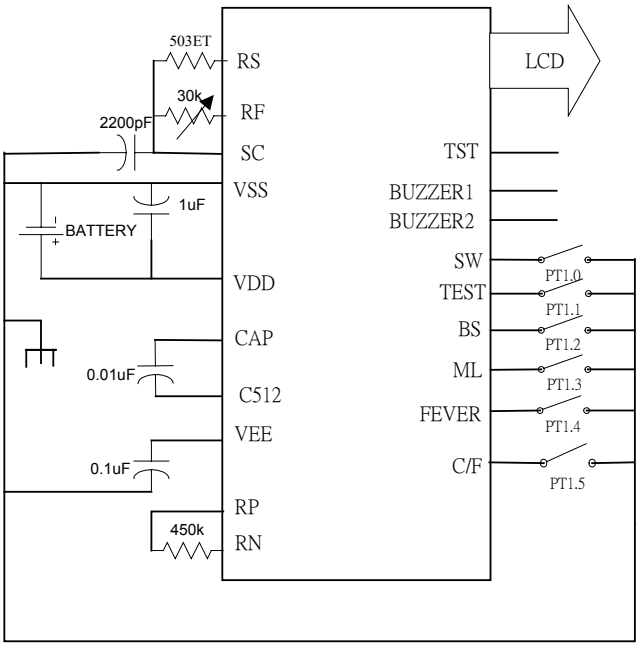
Name	In/Out	Pad NO.	Description
VDD	I	3	Positive input of power supply (1.5V)
VSS	I	5	Negative input of power supply
TST	I	6	Test pin for IC
RP	I/O	7	System oscillator external resistor connection (450k)
RN	I/O	8	System oscillator external resistor connection (450k)
VEE	I/O	27	Voltage doubler output (+3.0V)
CAP	I/O	26	Voltage doubler capacitor positive terminal
C512	I/O	25	Voltage doubler capacitor negative terminal
COM1~3	O	9~11	LCD common driver
SEG1~13	O	12~24	LCD segment driver
RF	I	1	Reference resistor connection
RS	I	2	Sensor resistor connection
SC	I	36	Comparator input
P1.0~P1.3	I	32~35	Input Ports
P1.4~P1.7	I/O	28~31	In/Out Ports
RST	I	4	CPU Reset Pin

7. Functional Block Diagram



8. Typical Application Circuit

8.1 Digital Clinical Thermometer



9. Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage to Ground Potential	-0.3 to 1.65	V
Applied Input/Output Voltage	-0.3 to VDD+0.15	V
Ambient Operating Temperature	0 to +70	°C
Storage Temperature	-55 to +150	°C
Soldering Temperature, Time	260°C, 10 Sec	

10. Electrical Characteristics

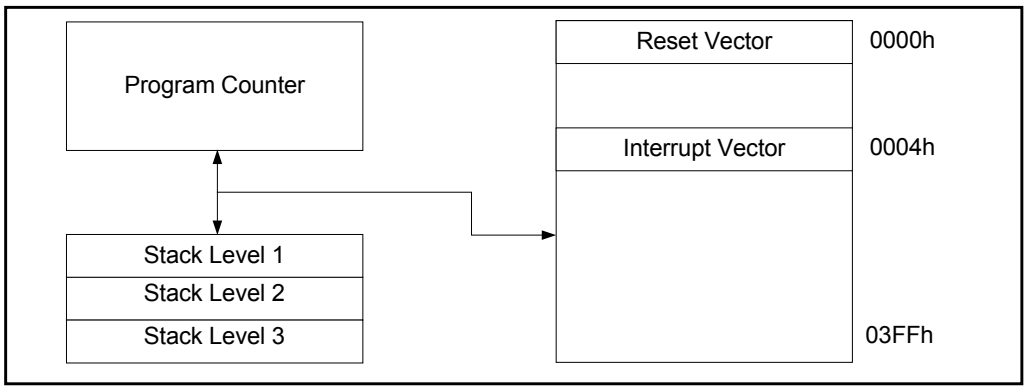
Symbol	Parameter	Test Condition	Min	Typ	Max	Units
VDD	Recommended Operation Voltage		1.2	1.5	1.65	V
IDD	Supply Current	CPU, R2F ADC On		40	60	μA
IPO	Power off Current	At Sleep mode	0.1	0.2	1.0	μA
FOSC	System Clock	ROSC=350k, VDD=1.5V	25.6	32	38.4	KHz
RNE	Resistance Non-Linearity Error	Rin=22k~38k			0.2	%

11. Function Description

11.1 CPU Core

11.1.1 Program Memory Organization

CPU has a 10-bit program counter capable of addressing 1K x 14 program memory space. The reset vector is at 0000h and the interrupt vector is at 0004h.



11.1.2 Data Memory Organization

Address	Name	Content							
000H	IND0	Use contents of FSR0 to address data memory							
001H	IND1	Use contents of FSR1 to address data memory							
002H	FSR0		Indirect data memory, address point 00H; **7-bit only.**						
003H	FSR1		Indirect data memory, address point 01H; **7-bit only.**						
004H	STATUS				PD			C	Z
005H	WORK	WORK register							
006H	INTF							E0IF	TMIF
007H	INTE	GIE						EOIE	TMIE
008H	PT1	PT1[7:0]							
009H	PT1EN	PT1EN[7:4]							
00AH	PT1PU	PT1PU[7:0]							
00EH	PT1MR	BPE2	BPE1	CH_S	RF_EN				
010H	LCD0		LCDEN	SEG2[2:0]			SEG1[2:0]		
011H	LCD1			SEG4[2:0]			SEG3[2:0]		
012H	LCD2			SEG6[2:0]			SEG5[2:0]		
013H	LCD3			SEG8[2:0]			SEG7[2:0]		
014H	LCD4			SEG10[2:0]			SEG9[2:0]		
015H	LCD5			SEG12[2:0]			SEG11[2:0]		
016H	LCD6						SEG13[2:0]		
018H	CKCON	LCD_S	PMPEN	PCK_S	BP_S	TMRST	GT_S		
019H	TMCNTH	TMCNT[15:8]							
01AH	TMCNTL	TMCNT[7:0]							
01BH	RSCNTH	RSCNT[15:8]							
01CH	RSCNTL	RSCNT[7:0]							
01DH	LowBatDct	lbEN	lowPwr	0	0	0	0	BiasSEL1	BiasSEL0
40H~7FH		General Data Memory							

- IND0: Indirect addressing mode address 0.
- IND1: Indirect addressing mode address 1.
- FSR0: Indirect addressing mode point 0.
- FSR1: Indirect addressing mode point 1.
- PD: Power down flag, which can be cleared by writing 0 or power-on reset, and set by sleep instruction.
- C: Carry flag.
- Z: Zero flag.
- E0IF, E0IE: PT1.0 external interrupt flag and enable.
- TMIF, TMIE: 8-bit Timer interrupt flag and enable.
- GIE: Global interrupt enable.

11.1.3 Instruction Set

Instruction	Operation	Cylce	Flag
NOP	No operation	1	None
CLRF f	f=0	1	Z
ADDWF f, d	d=f+W	1	C, DC, Z
INCF f, d	d=f+1	1	Z
INCFSZ f, d	d=f+1 skip if d=0	1,2	None
DECF f, d	d=f-1	1	Z
DECFSZ f, d	d=f-1 skip if d=0	1,2	None
SUBWF f, d	d=f-W	1	C, DC, Z
COMF f, d	d=~f	1	Z
MOVWF f	f=W	1	None
MOVFW f	W=f	1	None
ADDWFC f, d	d=f+W+C	1	C, DC, Z
ANDWF f, d	d=f&W	1	Z
IORWF f, d	d=f|W	1	Z
XORWF f, d	d=f^W	1	Z
RLF f, d	C, d [7:0]=f [7:0], C	1	C
SUBWFC f, d	d=f-W- (~C)	1	C, DC, Z
RRF f, d	d [7:0], c=C, f [7:0]	1	C
ADDLW k	W=k+W	1	C, DC, Z
SUBLW k	W=k-W	1	C, DC, Z
ANDLW k	W=k&W	1	Z
IORLW k	W=k|W	1	Z
XORLW k	W=k^W	1	Z
MOVLW k	W=k	1	None
RETLW k	RETURN and W=k	2	None
CALL k	Push PC+1 and GOTO k	2	None
GOTO k	PC=k	2	None
RETFIE	Pop PC and GIE=1	2	None
RETURN	Pop PC	2	None
SLEEP	Stop OSC	1	PD
ADDPCW	PC=PC+1+{6{W [7], W [6:0]}	2	None
BCF f, b	f [b]=0	1	None
BSF f, b	f [b]=1	1	None
BTFSC f, b	Skip if f[b]=0	1,2	None
BTFSS f, b	Skip if f[b]=1	1,2	None

*****FS9168 does not have HALT instruction to avoid the system error occurred when fast releasing and plugging-in the battery repeatedly.**

- f: memory address (00h ~ 7Fh).
- w: work register.
- k: literal field, constant data or label
- d: destination select:. “d=0” saves result in W, “d=1” saves result in memory address f.
- b: bit select (0~7).
- M (f): the content of memory address f.
- PC: program counter

11.1.4 Instruction Description

NOP	**No Operation**
Syntax	NOP
Operation	No Operation
Status Affected	None
Description	No operation. NOP is used for one instruction cycle delay.

CLRF	**Clear f**
Syntax	CLRF f
Operation	0 => M (f)
Status Affected	1=> Z
Description	Reset memory address f content.

ADDWF	**Add W to f**
Syntax	ADDWF f, d
Operation	W + M (f) => (destination)
Status Affected	DC, C, Z
Description	Add the content of the W register and M (f). If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f).

INCF	**Increment f**
Syntax	INCF f, d
Operation	M (f) + 1 => (destination)
Status Affected	Z
Description	M (f) is incremented. If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f).

INCFSZ	**Increment f, skip if zero**
Syntax	INCFSZ f, d
Operation	M (f) + 1 => (destination), skip if result is zero
Status Affected	None
Description	M (f) is incremented. If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f). If the result is 0, then the next fetched instruction is discarded and a NOP is executed instead making it a two-cycle instruction.

DECF	**Decrement f**
Syntax	DECF f, d
Operation	M (f) - 1 => (destination)
Status Affected	Z
Description	M (f) is decremented. If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f).

DECFSZ	**Decrement f, skip if zero**
Syntax	DECFSZ f, d
Operation	M (f) - 1 => (destination), skip if result is zero
Status Affected	None
Description	M (f) is decremented. If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f). If the result is 0, then the next fetched instruction is discarded and a NOP is executed instead making it a two-cycle instruction.

SUBWF	**Subtract W from f**
Syntax	SUBWF f, d
Operation	M (f) + NOT (W) + 1 => (destination)
Status Affected	DC, C, Z
Description	Subtract the content of the W register from M (f). If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f),

COMF	**Complement f**
Syntax	COMF f, d
Operation	NOT (M (f)) => M (f)
Status Affected	Z
Description	M (f) is complemented. If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f)

MOVWF	**Move W to f**
Syntax	MOVWF f
Operation	W => M (f)
Status Affected	None
Description	Move data from the W register to M (f).

MOVFW	**Move f to W**
Syntax	MOVFW f
Operation	M (f) => W
Status Affected	None
Description	Move data from M (f) to the W register.

ADDWFC	**Add W, f and Carry**
Syntax	ADDWFC f, d
Operation	W + M (f) + C => (destination)
Status Affected	DC, C, Z
Description	Add the content of the W register, M (f) and Carry bit. If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f).

ANDWF	**And W and f**
Syntax	ANDWF f, d
Operation	W AND M (f) => (destination)
Status Affected	Z
Description	AND the content of the W register with M (f). If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f).

IORWF	Inclusive OR W and f
Syntax	IORWF f, d
Operation	W OR M (f) => (destination)
Status Affected	Z
Description	Inclusive OR the content of the W register and M (f). If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f).

XORWF	Exclusive OR W and f
Syntax	XORWF f, d
Operation	W XOR M (f) => (destination)
Status Affected	Z
Description	Exclusive OR the content of the W register and M (f). If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f).

RLF	Rotate left M (f) through Carry
Syntax	RLF f, d
Operation	M (f) [6:0], C => (destination)
Status Affected	C
Description	M (f) is rotated one bit to the left through the Carry bit. If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f).

SUBWFC	Subtract W and Carry from f
Syntax	SUBWFC f, d
Operation	M (f) + NOT (W) + C => (destination)
Status Affected	DC, C, Z
Description	Subtract the content of the W register from M (f). If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f).

RRF	Rotate right M (f) through Carry
Syntax	RRF f, d
Operation	C, M (f) [7:1] => (destination)
Status Affected	C
Description	M (f) is rotated one bit to the right through the Carry bit. If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f).

ADDLW	ADD literal to W
Syntax	ADDLW k
Operation	W + k => W
Status Affected	DC, C, Z
Description	Add the content of the W register and the eight-bit literal "k". The result is stored in the W register.

SUBLW	Subtract literal from W
Syntax	SUBLW k
Operation	k + NOT (W) + 1 => W
Status Affected	DC, C, Z
Description	Subtract the eight-bit literal "k" from the content of the W register. The result is stored in the W register.

ANDLW	**AND literal with W**
Syntax	ANDLW k
Operation	W AND k => W
Status Affected	Z
Description	AND the content of the W register with the eight-bit literal "k". The result is stored in the W register.

IORLW	**Inclusive OR literal with W**
Syntax	IORLW k
Operation	W OR k => W
Status Affected	Z
Description	Inclusive OR the content of the W register and the eight-bit literal "k". The result is stored in the W register.

XORLW	**Exclusive OR literal with W**
Syntax	XORLW k
Operation	W XOR k => W
Status Affected	Z
Description	Exclusive OR the content of the W register and the eight-bit literal "k". The result is stored in the W register.

MOVLW	**Move literal to W**
Syntax	MOVLW k
Operation	k => W
Status Affected	None
Description	Move the eight-bit literal "k" to the content of the W register.

RETLW	**Return and move literal to W**
Syntax	RETLW k
Operation	k => W [Top Stack] => PC Pop Stack
Status Affected	None
Description	Move the eight-bit literal "k" to the content of the W register. The program counter is loaded from the top stack, then pop stack.

CALL	**Subroutine CALL**
Syntax	CALL k
Operation	Push Stack PC + 1 => [Top Stack] k => PC
Status Affected	None
Description	Subroutine Call. First, return address PC + 1 is pushed onto the stack. The immediate address is loaded into PC.

GOTO	Unconditional Branch
Syntax	GOTO k
Operation	k => PC
Status Affected	None
Description	The immediate address is loaded into PC.

Return	Return from Subroutine
Syntax	RETURN
Operation	[Top Stack] => PC Pop Stack
Status Affected	None
Description	The program counter is loaded from the top stack, then pop stack.

RETFIE	Return from Interrupt
Syntax	RETFIE
Operation	[Top Stack] => PC Pop Stack 1 => GIE
Status Affected	None
Description	The program counter is loaded from the top stack, then pop stack. Setting the GIE bit enables interrupts.

ADDPCW	ADD W to Program Counter
Syntax	ADDPCW
Operation	PC + 1 + W => PC
Status Affected	None
Description	The relative address PC + 1 + W is loaded into PC. The working register must less than 80h (128d).

SLEEP	Oscillator stop
Syntax	SLEEP
Operation	CPU oscillator is stopped
Status Affected	PD
Description	CPU oscillator is stopped. CPU can be waked up by external interrupt sources.

PS. Please make sure all interrupt flags are cleared before running SLEEP; "NOP" command must follow SLEEP commands.

BSF	Bit Set f
Syntax	BSF f, b
Operation	1 => M (f) [b]
Status Affected	None
Description	Bit b in M (f) is set to 1.

BCF	Bit Clear f
Syntax	BCF f, b
Operation	0 => M (f) [b]
Status Affected	None
Description	Bit b in M (f) is reset to 0.

BTFSC	Bit Test skip if Clear
Syntax	BTFSC f, b
Operation	Skip if M (f) [b] = 0
Status Affected	None
Description	If bit 'b' in M (f) is 0, the next fetched instruction is discarded and a NOP is executed instead making it a two-cycle instruction.

BTFSS	Bit Test skip if Set
Syntax	BTFSS f, b
Operation	Skip if M (f) [b] = 1
Status Affected	None
Description	If bit 'b' in M (f) is 1, the next fetched instruction is discarded and a NOP is executed instead making it a two-cycle instruction.

11.2 Low Battery Detection

Address	Name	Content							
1dH	LowBatDct	lbEN	lowPwr	0	0	0	0	BiasSEL1	BiasSEL0

When resetting, lbEN=1, BiasSEL=00.

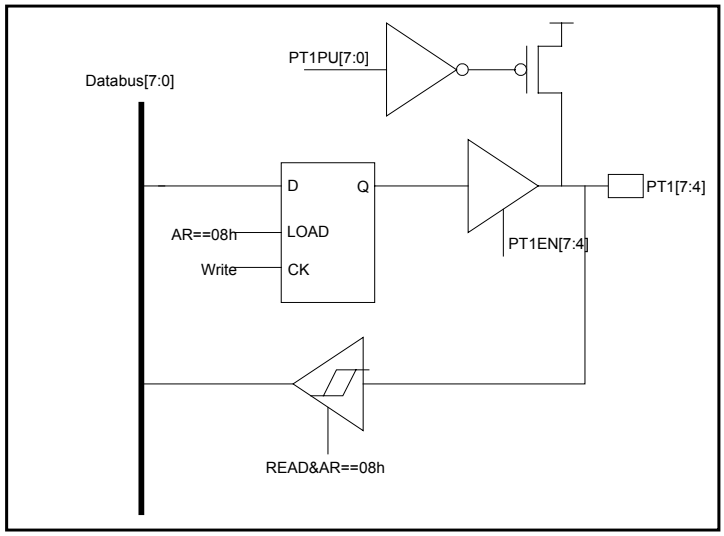
- "lbEN=1" enables low batery detection, "lbEN=0" disables low batery detection.
- BiasSEL is low voltage potential option.
- When reading LowBatDct, lowPwr=1 is normal, lowPwr=0 indicates it is under preset low voltage.

*****For various Low Voltage Detection option, the voltage detected might be different due to the slight variation of the IC process. The following table provides several voltage values for reference.**

BiasSEL1	BiasSEL0	Detect Voltage
0	0	1.329V
0	1	1.293V
1	0	1.260V
1	1	1.224V

11.3 I/O Port

Address	Name	Content							
008H	PT1	PT1[7:0]							
009H	PT1EN	PT1EN[7:4]							
00AH	PT1PU	PT1PU[7:0]							
00EH	PT1MR	BPE2	BPE1	CH_S	RF_EN				



- PT1[0:3] is input port, PT1[4:7] is I/O port, with pull-up resistor enable control.
- PT1[4:7] is an input port when PT1EN[4:7]=0, an output port when PT1EN[4:7]=1; system reset or initial start-up is 0.
- When PT1PU[N]=0, PT1[N] has no pull-up resistor; When PT1PU[N]=1, PT1[N] has a pull-up resistor; system reset or initial start-up is 0.
- PT1 has Schmitt-trigger input.
- When PT1.0 is set as interrupt input, negative edge interrupt has absolute high priority, independent of GIE's control.
- BPE2 =1 & PT1EN[7]=1: PT1[7] is used as the positive input for a buzzer. BPE1=1 & PT1EN[6]=1: PT1[6] is used as negative input of the buzzer. System reset or initial start-up is 0.

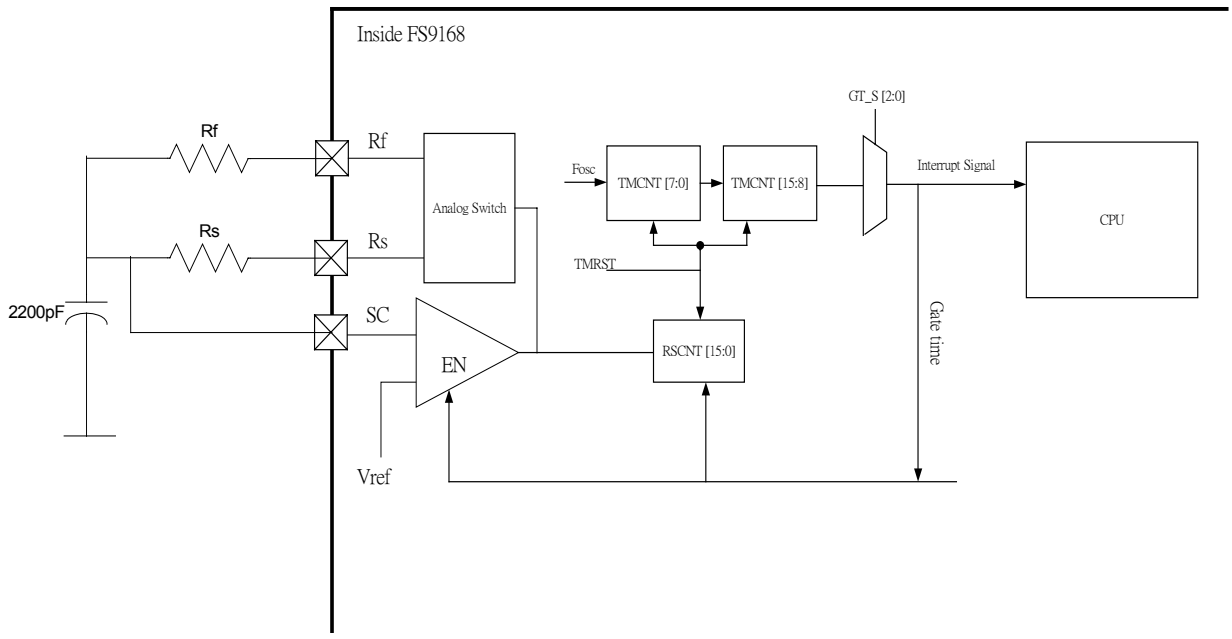
*RF_EN enables R/F (Resistor/Frequency) switch mode, CH_S=1 selects reference resistor (RF part) oscillator, CH_S=0 selects sensor resistor (RS part) oscillator.

11.4 RF Conversion Module

Address	Name	Content					
018H	CKCON	LCD_S	PMPEN	PCK_S	BP_S	TMRST	GT_S
019H	TMCNTH	TMCNT[15:8]					
01AH	TMCNTL	TMCNT[7:0]					
01BH	RSCNTH	RSCNT[15:8]					
01CH	RSCNTL	RSCNT[7:0]					

- LCD_S : LCD clock setup.
- PMPEN: Clock enable in step-up circuit.
- PCK_S: Clock setup in step-up circuit.
- BP_S : Buzzer clock setup.
- TMCNT is the Timer for Gate time; RSCNT is The Counter for RF module.
- GT_S is for Gate time setting of RF module, please reference the table below.
- TMRST: ” 0 ” clear all counter and stop counting;” 0→1” start to count until Gate time interrupt occurred.

  When TMCNT re-counts, TMRST must be set as 0 first, so TMCNT and RSCNT will be cleared as 0. When TMRST is set as 1, TMCNT and RSCNT start counting until TMCNT[N]1 → 0. Then TMCNT and RSCNT stop counting and store the value at the same time.



■ Table for RF module Gate time setting.

GT_S	TMCNT[N]	Gate time(Hz)
0	8	64
1	9	32
2	10	16
3	11	8
4	12	4
5	13	2
6	14	1
7	15	0.5

11.5 LCD Driver

Address	Name	Content			
010h	LCD0		LCDEN	SEG2[2:0]	SEG1[2:0]
011h	LCD1			SEG4[2:0]	SEG3[2:0]
012h	LCD2			SEG6[2:0]	SEG5[2:0]
013h	LCD3			SEG8[2:0]	SEG7[2:0]
014h	LCD4			SEG10[2:0]	SEG9[2:0]
015h	LCD5			SEG12[2:0]	SEG11[2:0]
016h	LCD6				SEG13[2:0]

LCDEN=1, LCD display enable; LCDEN=0, LCD display disable。

12. Application Note

12.1 Current Consumption

To reduce the current consumption, please note the following when executing the program：

A. Turn on (lbEN=1) only when detecting the low battery, and turn off (lbEN=0) immediately after the detection.

B. When entering SLEEP mode, and the Port is in input status or is set as input status, detect the Port status first. Turn off Pull-up if Port=0; turn on Pull-up if Port=1 (Pull-up must be always turned on in Port 1.0)

C. When entering SLEEP mode, and Port is set as output status, Port should be cleared as 0.

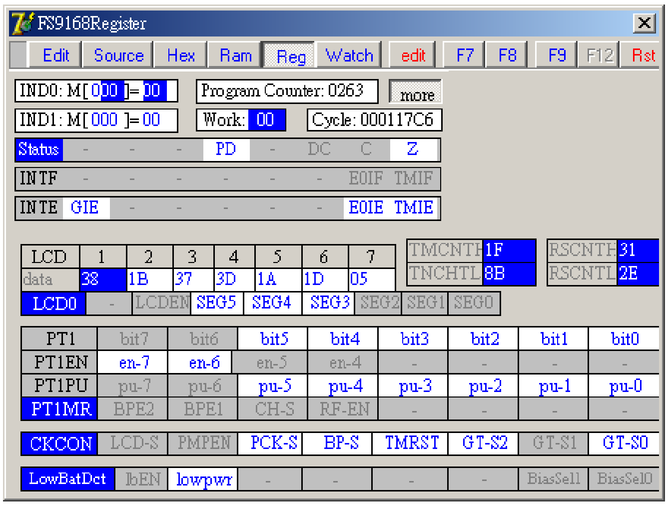
D. When entering SLEEP mode, and not detecting the resistor, RF_EN must be turned off.

E. After completing the above procedures, the current consumption will be less than 1μA in SLEEP mode.

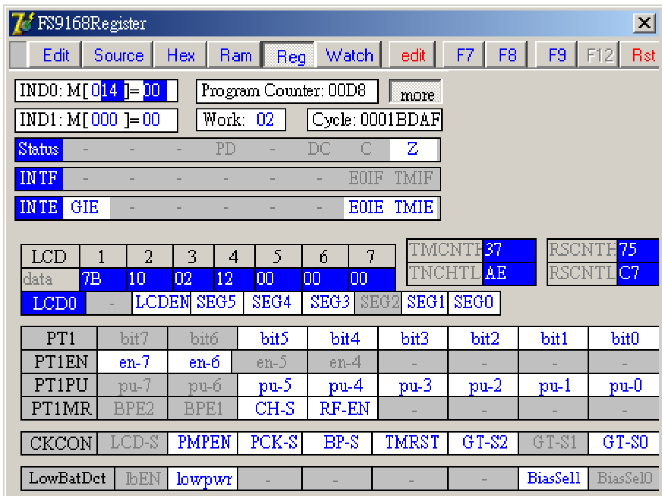
- Example Program:

```
tovsleepa:
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
        ;give the input port a constant state (the status cannot be "floating")
        movfw   pt1             ;read I/O port
        iorlw   00000001b       ;pt1.0 is exernal interrupt, it must be pulled high, and execute
                                OR operation with the value read by the last line, pull high when
                                the state is High, do not turn on the pull high circuit if the state is
                                Low
        andlw   00111111b       ;pull high when the state is High so to prevent the current
                                leakage of pull high resistor caused by Input port's Low state;
                                preset bit0~bit5 as input
        movwf   pt1pu

;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
        bcf     pt1mr ,rfen     ;turn off rfen
        clrf    pt1             ;I/O port output is low
        clrf    lbdct           ;turn off low battery detector
        bcf     ckcon,6         ;turn off chrage pump
        bcf     lcd0,6          ;turn off lcd
        movlw   10000010b       ;choose external interrupt
        movwf   inte
        sleep
```

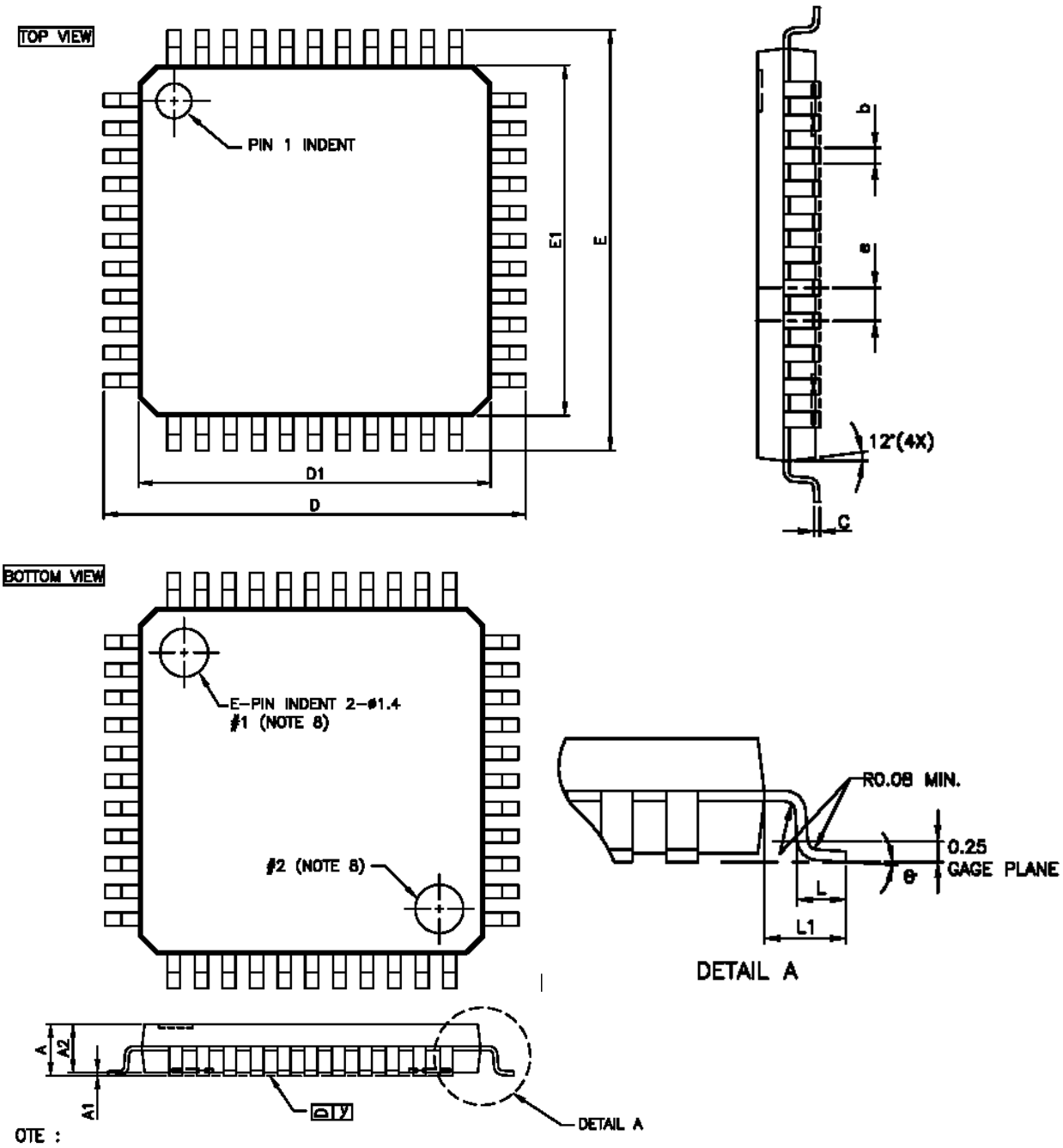


Sleep Mode



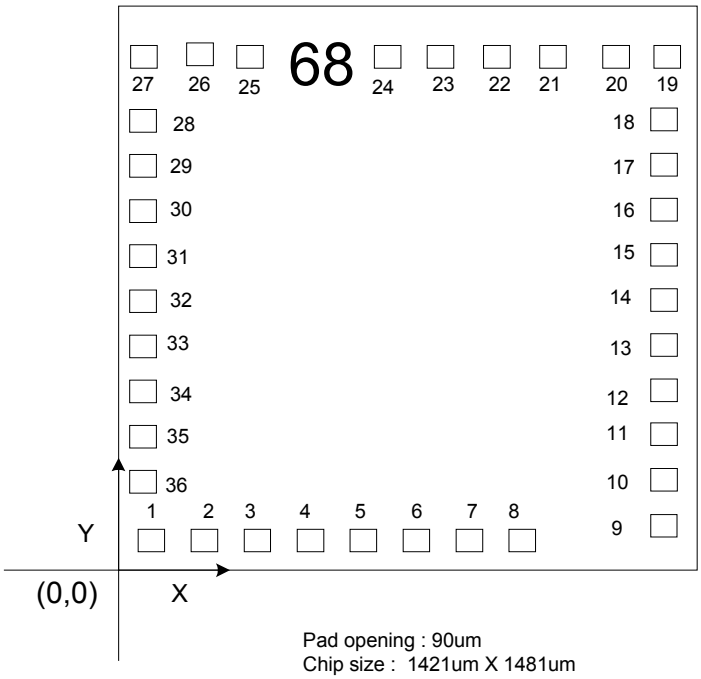
Operation Mode

13. Package Outline



SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A	——	——	1.60
A1	0.05	——	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
C	0.09	——	0.20
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
e	——	0.80	——
L	0.45	0.60	0.75
L1	——	1.00	——
θ°	0°	3.5°	7°
y	0.0	——	0.08

14. Pad Assignment



Pad opening : 90um
Chip size : 1421um X 1481um
Substrate should be connected to VSS

15. Pad Coordinate

※PAD NO: 36 pads ※Die Size:1421 um x 1481 um

Pad No.	Name	X[um]	Y[um]	Pad No.	Name	X[um]	Y[um]
1	RF	85	74	19	SEG<8>	1335	1406
2	RS	205	74	20	SEG<9>	1205	1406
3	VDD	329	74	21	SEG<10>	1095	1406
4	RST	449	74	22	SEG<11>	975	1406
5	VSS	569	74	23	SEG<12>	855	1406
6	TST	689	74	24	SEG<13>	738	1406
7	RP	809	74	25	C512	331	1406
8	RN	929	74	26	CAP	200	1406
9	COM<1>	1346	87	27	VEE	74	1406
10	COM<2>	1346	205	28	PT1<7>	74	1262
11	COM<3>	1346	324	29	PT1<6>	74	1142
12	SEG<1>	1346	441	30	PT1<5>	74	1021
13	SEG<2>	1346	561	31	PT1<4>	74	902
14	SEG<3>	1346	681	32	PT1<3>	74	772
15	SEG<4>	1346	802	33	PT1<2>	74	650
16	SEG<5>	1346	924	34	PT1<1>	74	531
17	SEG<6>	1346	1041	35	PT1<0>	74	411
18	SEG<7>	1346	1162	36	SC	74	291