SBAS287A − JUNE 2003 − REVISED SEPTEMBER 2003

Low-Power, 24-Bit Analog-to-Digital Converter

FEATURES

- 20-Bit Effective Resolution
- High-Impedance Buffered Input
- ±2.5V Differential Input Range
- Pin-Compatible with ADS1244
- 0.0006% INL (typ), 0.0015% INL (max)
- Simple Two-Wire Serial Interface
- Simultaneous 50Hz and 60Hz Rejection
- Single Conversions with Sleep Mode
- Single-Cycle Settling
- Self-Calibration
- Well Suited for Multi-Channel Systems
- Easily Connects to the MSP430
- Current Consumption: 158μA
- Analog Supply: 2.5V to 5.25V
- Digital Supply: 1.8V to 3.6V

APPLICATIONS

- Hand-Held Instrumentation
- Portable Medical Equipment
- Industrial Process Control
- Test and Measurement Systems

DESCRIPTION

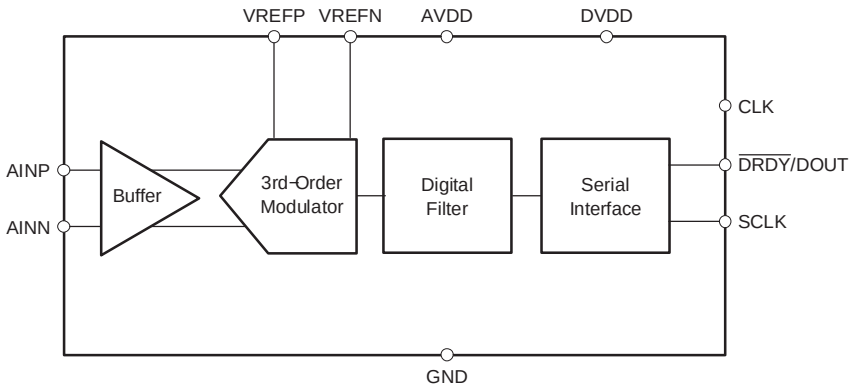
The ADS1245 is a 24-bit, delta-sigma analog-to-digital converter (ADC). It offers excellent performance and very low power in an MSOP-10 package and is well suited for demanding high-resolution measurements, especially in portable and other space- and power-constrained systems.

The buffered input presents an impedance of 3GΩ, minimizing measurement errors when using high-impedance sources. The ADS1245 is compatible with ADS1244 and offers a direct upgrade path for designs requiring higher input impedance.

A third-order delta-sigma (ΔΣ) modulator and digital filter form the basis of the ADC. The analog modulator has a ±2.5V differential input range. The digital filter rejects both 50Hz and 60Hz signals, completely settles in one cycle, and outputs data at 15 samples per second (SPS).

A simple, two-wire serial interface provides all the necessary control. Data retrieval, self-calibration, and Sleep mode are handled with a few simple waveforms. When only single conversions are needed, the ADS1245 can be shut down (Sleep mode) while idle between measurements to dramatically reduce the overall power dissipation. Multiple ADS1245s can be connected together to create a synchronously sampling multichannel measurement system. The ADS1245 is designed to easily connect to microcontrollers, such as the MSP430.

The ADS1245 supports 2.5V to 5.25V analog supplies and 1.8V to 3.6V digital supplies. Power is typically less than 470μW in normal operation and less than 1μW during Sleep mode.



ORDERING INFORMATION

PRODUCT	PACKAGE−LEAD	PACKAGE DESIGNATOR(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS1245	MSOP-10	DGS	−40°C to +85°C	BHI	ADS1245IDGST	Tape and Reel, 250
					ADS1245IDGSR	Tape and Reel, 2500

(1) For the most current specifications and package information, refer to our web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	ADS1245	UNIT
AVDD to GND	−0.3 to +6	V
DVDD to GND	−0.3 to +3.6	V
Input Current	100, momentary	mA
Input Current	10, continuous	mA
Analog Input Voltage to GND	−0.5 to AVDD + 0.5	V
Analog Input Voltage to GND	−0.3 to DVDD + 0.3	V
Digital Output Voltage to GND	−0.3 to DVDD + 0.3	V
Maximum Junction Temperature	+150	°C
Operating Temperature Range	−40 to +85	°C
Storage Temperature Range	−60 to +150	°C
Lead Temperature (soldering, 10s)	+300	°C

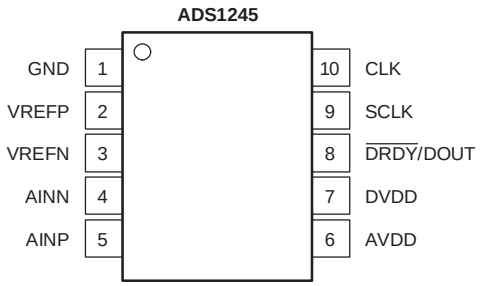
(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN ASSIGNMENTS

DGS PACKAGE
MSOP
(TOP VIEW)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
GND	1	Analog and digital ground
VREFP	2	Positive reference input
VREFN	3	Negative reference input
AINN	4	Negative analog input
AINP	5	Positive analog input
AVDD	6	Analog power supply, 2.5V to 5.25V
DVDD	7	Digital power supply, 1.8V to 3.6V
$\overline{\text{DRDY}}$/DOUT	8	Dual-purpose output: Data ready: indicates valid data by going low. Data output: outputs data, MSB first, on the first rising edge of SCLK.
SCLK	9	Serial clock input: clocks out data on the rising edge. Used to initiate calibration and Sleep mode (see text for more details).
CLK	10	System clock input: typically 2.4576MHz

ELECTRICAL CHARACTERISTICS

All specifications at T_A = −40°C to +85°C, AVDD = +5V, DVDD = +3V, f_{CLK} = 2.4576MHz, and V_{REF} = +1.25V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog Input						
Full-scale input voltage range		AINP − AINN		±2V_{REF}		V
Absolute input range		AINP, AINN with respect to GND	GND + 0.1		AVDD − 1.25	V
Differential input impedance		f_{CLK} = 2.4576MHz		3		GΩ
System Performance						
Resolution		No missing codes	24			Bits
Data rate		f_{CLK} = 2.4576MHz		15		SPS(1)
Integral nonlinearity (INL)		Differential input signal, end point fit		±0.0006	±0.0015	%FSR(2)
Offset error				1	14	ppm of FSR
Offset error drift(3)				0.01		ppm of FSR/°C
Gain error(4)				0.005	0.1	%
Gain error drift(3)				0.5		ppm/°C
Common-mode rejection		At DC	90	100		dB
		f_{CM}(5) = 50 ± 1Hz, f_{CLK} = 2.4576MHz	100			dB
		f_{CM} = 60 ± 1Hz, f_{CLK} = 2.4576MHz	100			dB
Normal-mode rejection		f_{SIG}(6) = 50 ± 1Hz, f_{CLK} = 2.4576MHz	60			dB
		f_{SIG} = 60 ± 1Hz, f_{CLK} = 2.4576MHz	70			dB
Input referred noise				2		ppm of FSR, RMS
Analog power-supply rejection		At DC, ΔAVDD = 5%		100		dB
Digital power-supply rejection		At DC, ΔAVDD = 5%		100		dB
Voltage Reference Input						
Reference input voltage (V_{REF})		V_{REF} ≡ VREFP − VREFN	0.5	1.25	AVDD(7)	V
Negative reference input (VREFN)			GND − 0.1		VREFP − 0.5	V
Positive reference input (VREFP)			VREFN + 0.5		AVDD + 0.1	V
Voltage reference impedance		f_{CLK} = 2.4576MHz		1		MΩ
Digital Input/Output						
Logic levels	V_{IH} (CLK, SCLK)		0.8 DVDD		5.25	V
	V_{IL} (CLK, SCLK)		GND		0.2 DVDD	V
	V_{OH} ($\overline{DRDY}$, DOUT)	I_{OH} = 1mA	DVDD − 0.4		DVDD	V
	V_{OL} ($\overline{DRDY}$, DOUT)	I_{OL} = 1mA	GND		DVDD + 0.4	V
Input leakage (CLK, SCLK)		0 < (CLK, SCLK) < DVDD			±10	µA
CLK frequency (f_{CLK})					6	MHz
CLK duty cycle			30		70	%
Power Supply						
AVDD			2.7		5.25	V
DVDD			1.8		3.6	V
AVDD current		Sleep mode		0.1	1	µA
		AVDD = 3V		152		µA
		AVDD = 5V		158	250	µA
DVDD current		Sleep mode, CLK stopped		0.1		µA
		Sleep mode, 2.4576MHZ CLK running		1.6	5	µA
		DVDD = 3V		5	10	µA
Total power dissipation		AVDD = DVDD = 3V		0.47		mW

(1) SPS = samples per second.
(2) FSR = full-scale range = 4V_{REF}.
(3) Recalibration can reduce these errors to the level of the noise.
(4) Achieving specified gain error performance requires that calibration be performed with reference voltage input between (GND + 0.1V) and (AVDD − 1.25V). See *Voltage Reference Inputs* section.
(5) f_{CM} is the frequency of the common-mode input.
(6) f_{SIG} is the frequency of the input signal.
(7) It will not be possible to reach the digital output full-scale code when V_{IN} > 2V_{REF}.

TYPICAL CHARACTERISTICS

At T_A = +25°C, AVDD = +5V, DVDD = +3V, f_{CLK} = 2.4576MHz, and V_{REF} = +1.25V, unless otherwise specified.

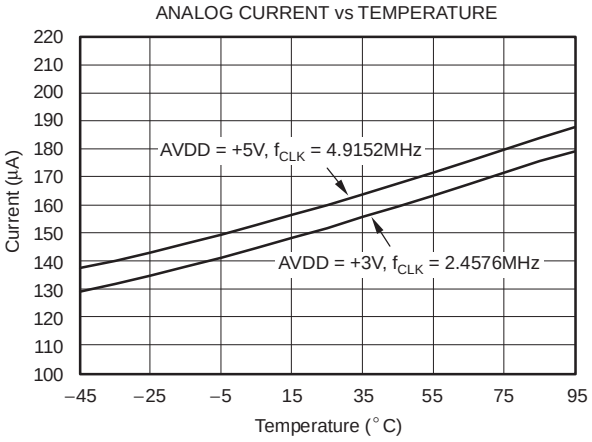


Figure 1

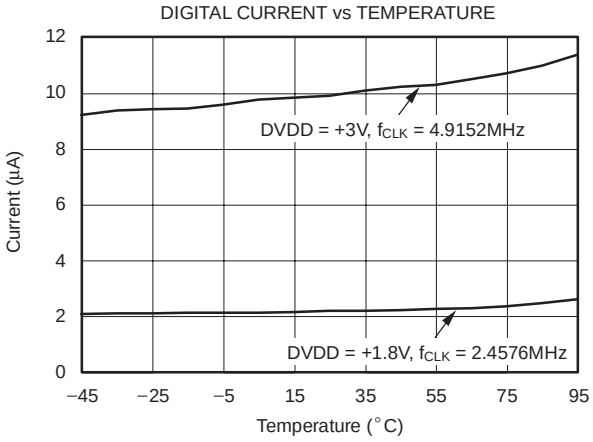


Figure 2

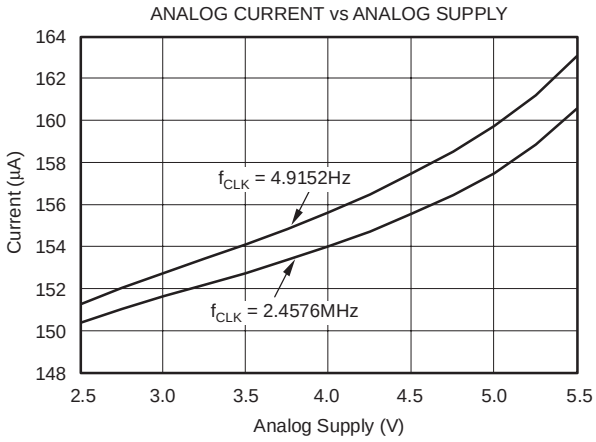


Figure 3

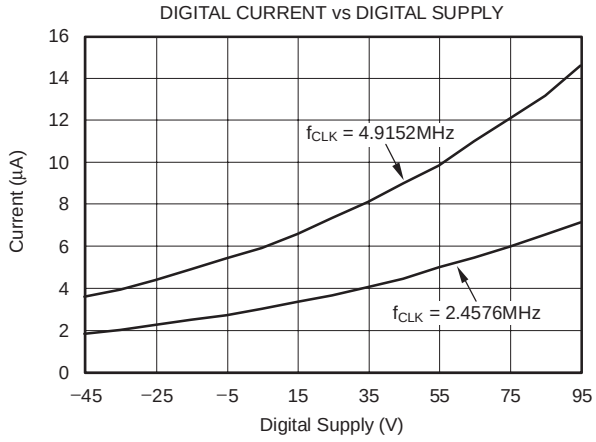


Figure 4

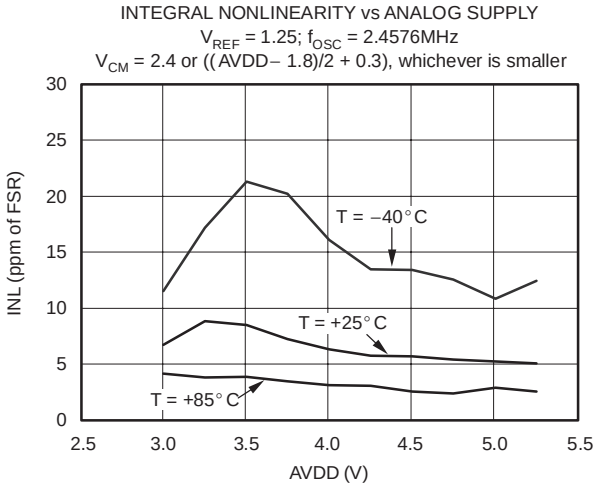


Figure 5

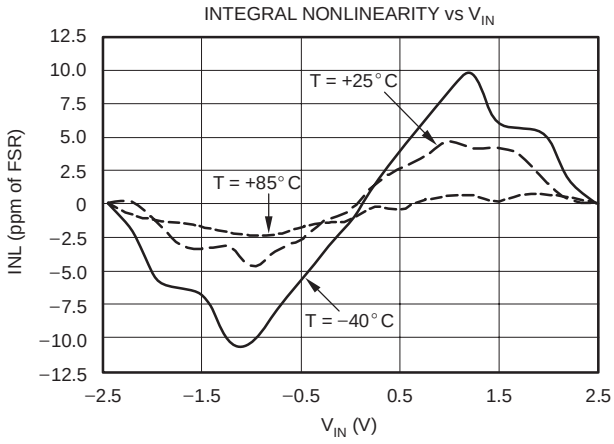


Figure 6

TYPICAL CHARACTERISTICS

At T_A = +25°C, AVDD = +5V, DVDD = +3V, f_{CLK} = 2.4576MHz, and V_{REF} = +1.25V, unless otherwise specified.

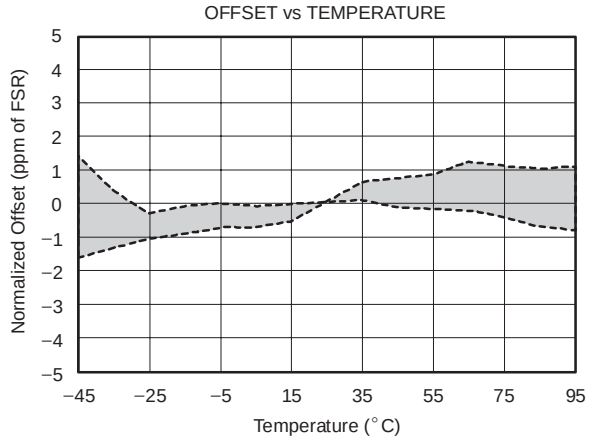


Figure 7

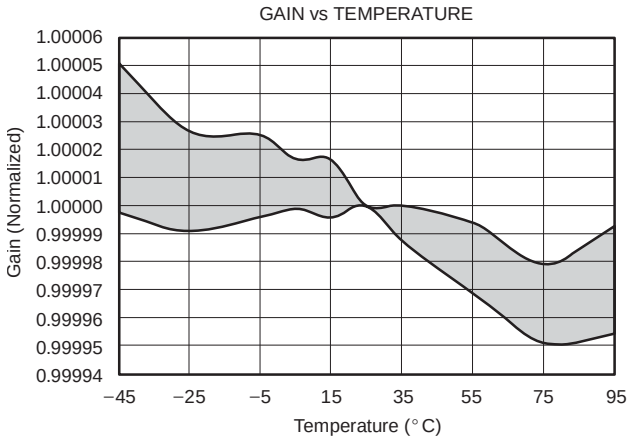


Figure 8

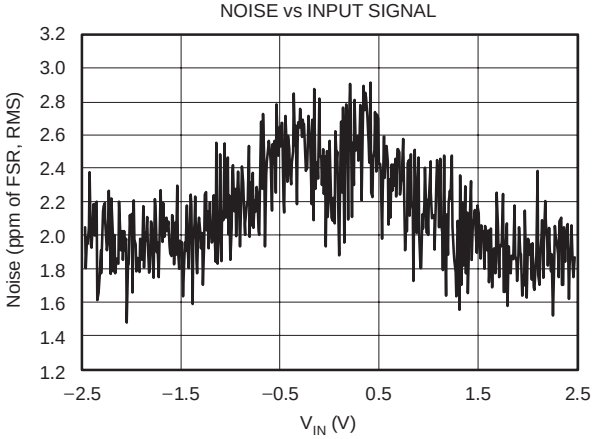


Figure 9

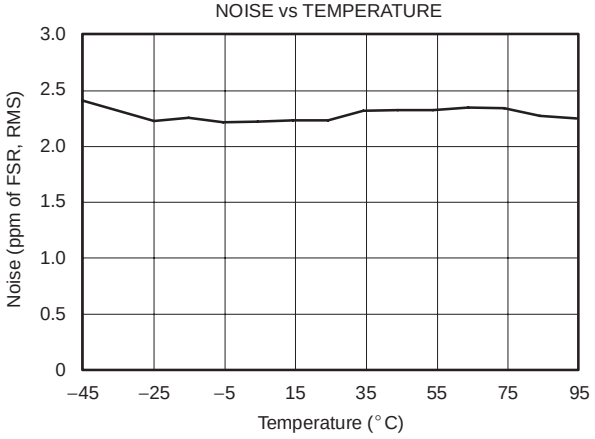


Figure 10

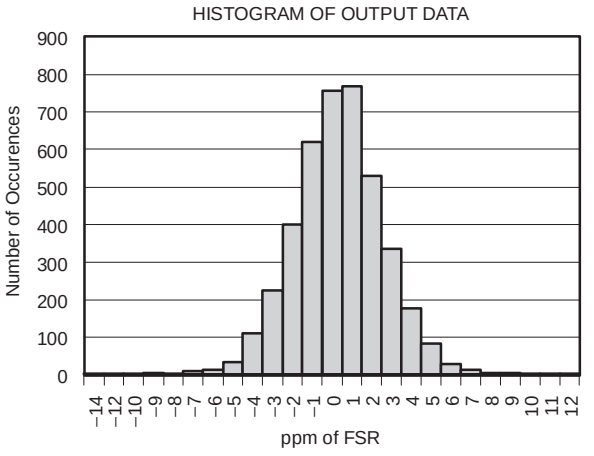


Figure 11

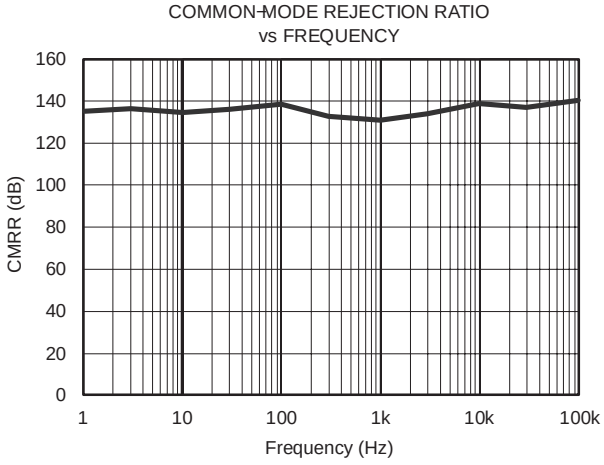


Figure 12

TYPICAL CHARACTERISTICS

At T_A = +25°C, AVDD = +5V, DVDD = +3V, f_{CLK} = 2.4576MHz, and V_{REF} = +1.25V, unless otherwise specified.

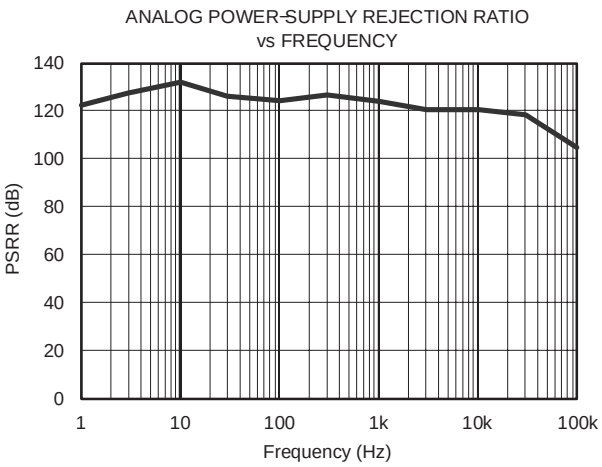


Figure 13

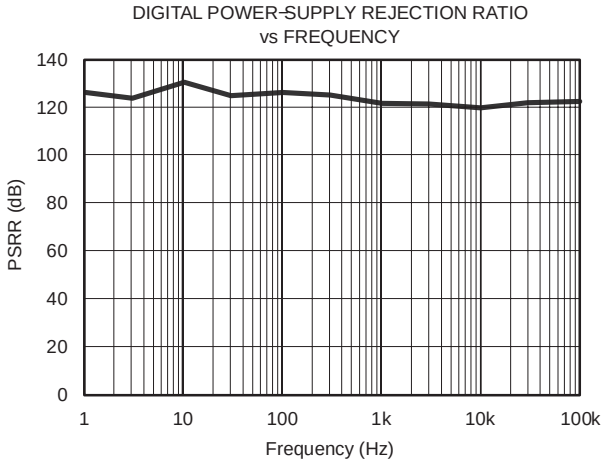


Figure 14

OVERVIEW

The ADS1245 is an ADC comprised of a 3rd-order modulator followed by a digital filter. The modulator measures the differential input signal V_{IN} = (AINP – AINN) against the differential reference V_{REF} = (VREFP – VREFN). Figure 15 shows a conceptual diagram. The differential reference is scaled internally so that the full-scale input range is $\pm 2V_{REF}$. The digital filter receives the modulator signal and provides a low-noise digital output. The filter also sets the frequency response of the converter and provides 50Hz and 60Hz rejection while settling in a single conversion cycle. A two-wire serial interface indicates conversion completion and provides the user with the output data.

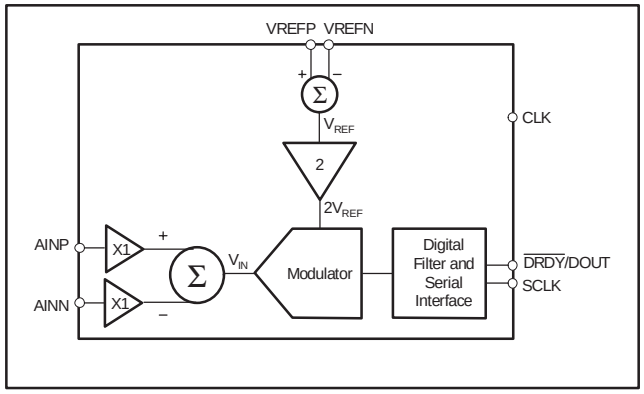


Figure 15. Conceptual Diagram of the ADS1245

ANALOG INPUTS (AINP, AINN)

The input signal to be measured is applied to the input pins AINP and AINN. The ADS1245 features a low-drift chopper-stabilized buffer to achieve very high input impedance. The input impedance can be modeled by resistors, as shown in Figure 16. The impedance scales inversely with f_{CLK} frequency. For example, if the frequency of f_{CLK} is reduced by a factor of two, the impedances $Zeff_A$ and $Zeff_B$ will double.

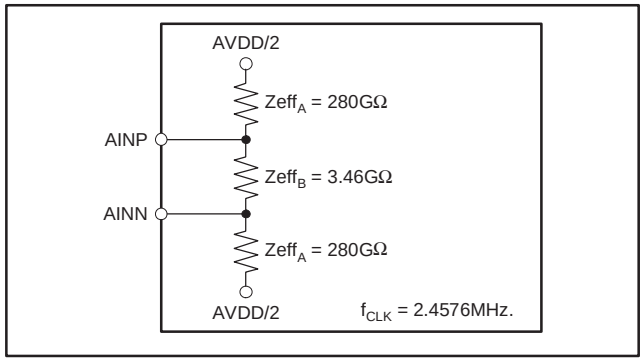


Figure 16. Effective Analog Input Impedances

The ADS1245 accepts differential input signals, but can also measure unipolar signals. Note that the analog inputs (listed in the Electrical Characteristics table as *Absolute Input Range*) must remain between GND + 0.1V to AVDD − 1.25V. Exceeding this range will degrade linearity and result in performance outside specified limits.

VOLTAGE REFERENCE INPUTS (VREFP, VREFN)

The voltage reference used by the modulator is generated from the voltage difference between VREFP and VREFN: V_{REF} = VREFP – VREFN. A simplified diagram of the circuitry on the reference inputs is shown in Figure 17. The switches and capacitors can be modeled with an effective impedance equal to:

$$\left(\frac{t_{SAMPLE}}{2}\right)/25pF = 1M\Omega \text{ for } f_{CLK} = 2.4576MHz$$

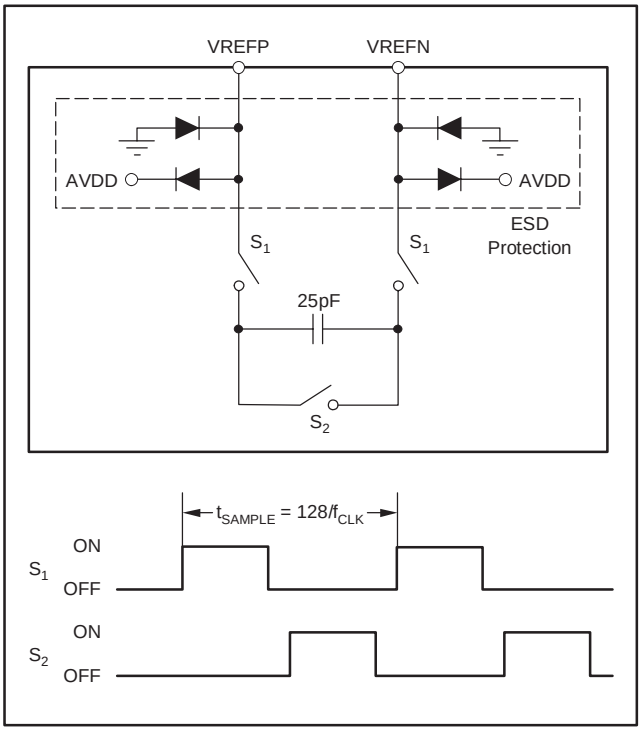


Figure 17. Simplified Reference Input Circuitry

The ADS1245 is specified for operation with V_{REF} = 1.25V, resulting in a full−scale input value of ±2.5V. However, the buffered analog inputs can accept voltages within the range of 0.10V to 3.75V, resulting in a maximum V_{IN} of ±3.65V. Input voltages can be accurately measured over this entire range if a voltage reference of 1.825V is provided. In any case, digital output codes will clip to the full scale value if the absolute input voltage range exceeds $2V_{REF}$.

To achieve optimal gain error performance, the reference input should be maintained within the range GND + 0.1V to AVDD − 1.25V when performing a self-calibration. A calibration based on a reference input outside this voltage range will result in gain errors exceeding specified values, but not more than 0.5%. Errors due to drift will remain within specified limits regardless of the calibration procedure.

For best performance, bypass the voltage reference inputs with a 0.1µF capacitor between VREFP and VREFN. Place the capacitor as close as possible to the pins.

ESD diodes protect the inputs. To keep these diodes from turning on, make sure the voltages on the input pins do not go below GND by more than 100mV, and likewise do not exceed AVDD by 100mV.

CLOCK INPUT (CLK)

This digital input supplies the system clock to the ADS1245. The recommended CLK frequency is 2.4576MHz. This places the notches of the digital filter at 50Hz and 60Hz and sets the data rate at 15SPS. The CLK frequency can be increased to speed up the data rate, but the frequency notches will move proportionally in frequency. CLK must be left running during normal operation. It can be turned off during Sleep Mode to save power, but this is not required. The CLK input can be driven with 5V logic, regardless of the DVDD or AVDD voltage. Minimize the overshoot and undershoot on CLK for the best analog performance. A small resistor in series with CLK (10Ω to 100Ω) can often help. CLK can be generated from a number of sources including stand-alone crystal oscillators and microcontrollers. The MSP430, an ultra low power microcontroller, is especially well-suited for this task. Using the MSP430 FLL clock generator available on the 4xx family, it is easy to produce a 2.4576MHz clock from a 32.768kHz crystal.

DATA READY/DATA OUTPUT ($\overline{\text{DRDY}}$/DOUT)

The digital output pin on the ADS1245 serves two purposes. It indicates when new data is ready by going low. Afterwards, on the first rising edge of SCLK, the $\overline{\text{DRDY}}$/DOUT pin changes function and begins outputting the conversion data, MSB first. Data is shifted out on each subsequent SCLK rising edge. After all 24 bits have been retrieved, the pin can be forced high with an additional SCLK. It will then stay high until new data is ready. This is useful when polling on the status of $\overline{\text{DRDY}}$/DOUT to determine when to begin data retrieval.

SERIAL CLOCK INPUT (SCLK)

This digital input shifts serial data out with each rising edge. As with CLK, this input may be driven with 5V logic regardless of the DVDD or AVDD voltage. There is hysteresis built into this input, but care should still be taken to ensure a clean signal. Glitches or slow-rising signals can cause unwanted additional shifting. For this reason, it is best to make sure the rise-and-fall times of SCLK are less than 50ns.

FREQUENCY RESPONSE

The ADS1245 frequency response for f_{CLK} = 2.4576MHz is shown in Figure 18. The frequency response repeats at multiples of 19.2kHz. The overall response is that of a low-pass filter with a –3dB cutoff frequency of 13.7Hz. As can be seen, the ADS1245 does a good job attenuating out to 19kHz. For the best resolution, limit the input bandwidth to below this value to keep higher frequency noise from affecting performance. Often, a simple RC filter on the ADS1245 analog inputs is all that is needed.

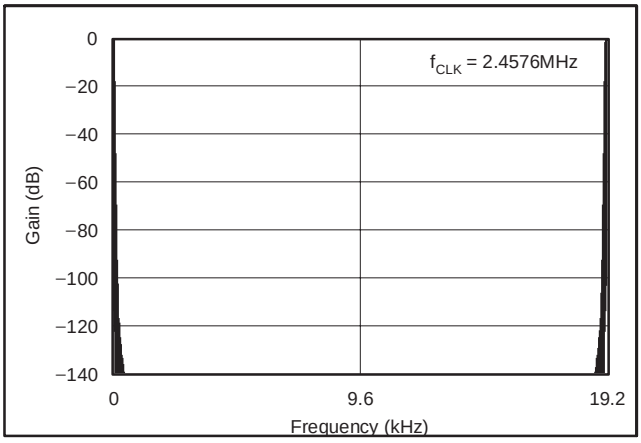


Figure 18. Frequency Response

To help see the response at lower frequencies, Figure 19 illustrates the response out to 180Hz. Notice that both 50Hz and 60Hz signals are rejected. This feature is very useful for eliminating power line cycle interference during measurements. Figure 20 shows the ADS1245 response around these frequencies.

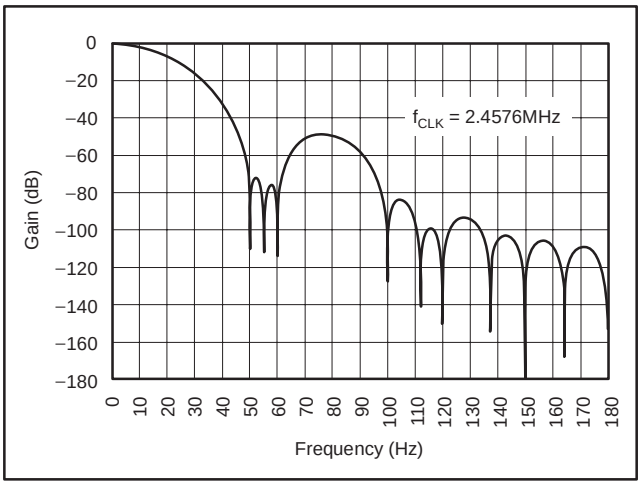


Figure 19. Frequency Response to 180Hz

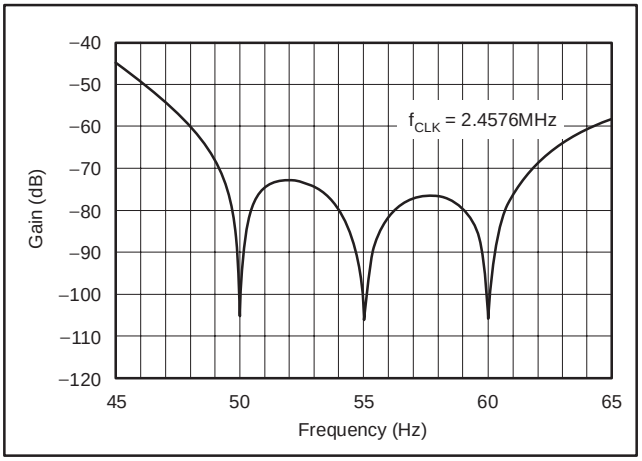


Figure 20. Frequency Response Near 50Hz and 60Hz

The ADS1245 data rate and frequency response scale directly with CLK frequency. For example, if fCLK increases from 2.4576MHz to 4.9152MHz, the data rate increases from 15sps to 30sps while the notches in the response at 50Hz and 60Hz move out to 100Hz and 120Hz.

SETTLING TIME

The ADS1245 has single-cycle settling. That is, the output data is fully settled after a single conversion—there is no need to wait for additional conversions before retrieving the data when there is a change on the analog inputs.

In order to realize single-cycle settling, synchronize changes on the analog inputs to the conversion beginning, which is indicated by the falling edge of $\overline{\text{DRDY}}$/DOUT. For example, when using a multiplexer in front of the ADS1245, change the multiplexer inputs when $\overline{\text{DRDY}}$/DOUT goes low. Increasing the time between the conversion beginning and the change on the analog inputs (t_{DELAY}) results in a settling error in the conversion data, as shown in Figure 21. The settling error versus delay time is shown in Figure 22. If the input change is delayed to the point where the settling error is too high, simply ignore the first data result and wait for the second conversion, which will be fully settled.

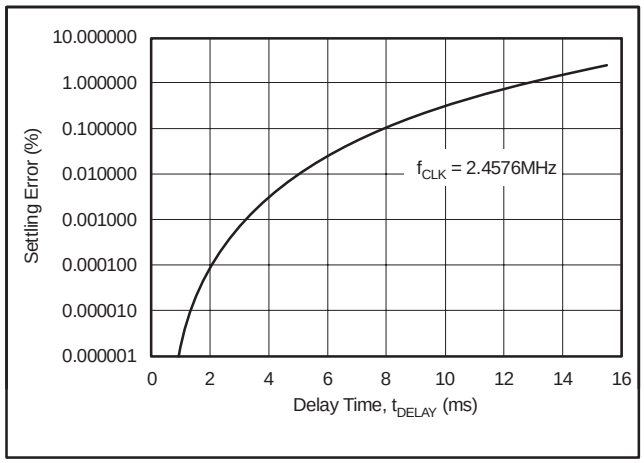


Figure 21. Settling Error vs Delay Time

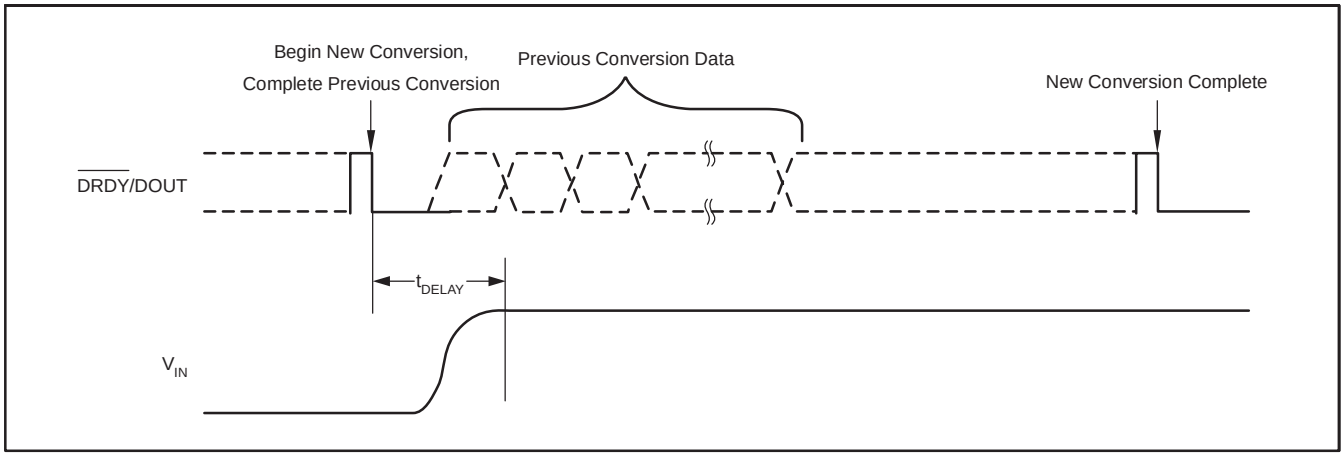
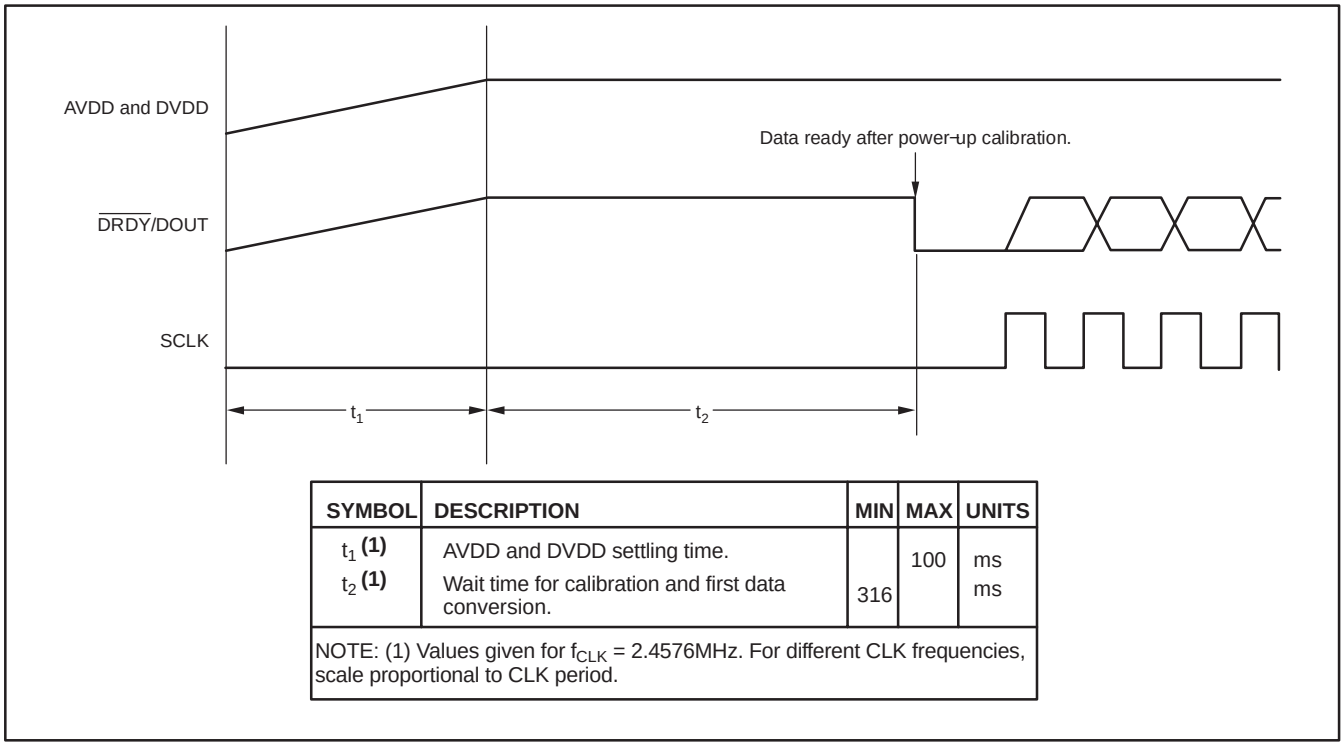


Figure 22. Analog Input Change Timing

POWER−UP

Self-calibration is performed at power-up to minimize offset and gain errors. In order for the self-calibration at power-up to work properly, make sure that both AVDD and DVDD increase monotonically and are settled by t_1, as shown in Figure 23. SCLK must be held low during this time. Once calibration is complete, $\overline{DRDY}$/DOUT goes low, indicating data is ready for retrieval. The time required before the first data is ready (t_6) depends on how fast AVDD and DVDD ramp to their final value (t_1). For most ramp rates, $t_1 + t_2 \approx 350$ms (f_{CLK} = 2.4576MHz). If the system environment is not stable during power-up (the temperature is varying or the supply voltages are moving around), it is recommended that a self-calibration be issued after everything is stable.



SYMBOL	DESCRIPTION	MIN	MAX	UNITS
t_1 **(1)**	AVDD and DVDD settling time.		100	ms
t_2 **(1)**	Wait time for calibration and first data conversion.	316		ms

NOTE: (1) Values given for f_{CLK} = 2.4576MHz. For different CLK frequencies, scale proportional to CLK period.

Figure 23. Power-Up Timing

DATA FORMAT

The ADS1245 outputs 24 bits of data in Binary Two's Complement format. The least significant bit (LSB) has a weight of $(2V_{REF})/(2^{23} - 1)$. A positive full-scale input produces an output code of 7FFFFFh and the negative full-scale input produces an output code of 8000000h. The output clips at these codes for signals exceeding full-scale. Table 1 summarizes the ideal output codes for different input signals.

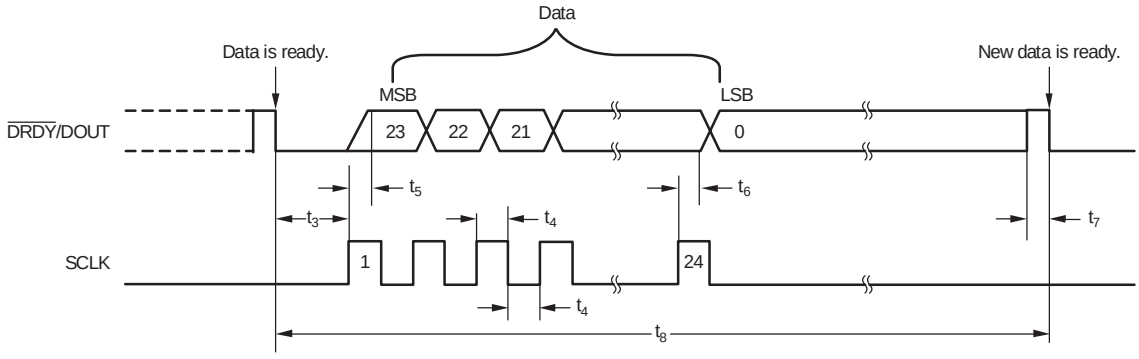
Table 1. Ideal Output Code vs Input Signal

INPUT SIGNAL V_{IN} (AINP − AINN)	IDEAL OUTPUT CODE(1)
$\geq +2V_{REF}$	$7FFFFF_H$
$\frac{+ 2V_{REF}}{(2^{23}) - 1}$	000001_H
0	000000_H
$\frac{- 2V_{REF}}{(2^{23}) - 1}$	$FFFFFF_H$
$\leq - 2V_{REF}\left(\frac{2^{23}}{(2^{23}) - 1}\right)$	800000_H
NOTE: (1) Excludes effects of noise, INL, offset, and gain errors.	

DATA RETRIEVAL

The ADS1245 continuously converts the analog input signal. To retrieve data, wait until $\overline{DRDY}$/DOUT goes low, as shown in Figure 24. After this occurs, begin shifting out the data by applying SCLKs. Data is shifted out most significant bit (MSB) first. It is not required to shift out all the 24 bits of data, but the data must be retrieved before the new data is updated (see t_3) or else it will be overwritten. Avoid data retrieval during the update period. $\overline{DRDY}$/DOUT remains at the state of the last bit shifted out until it is taken high (see t_7), indicating that new data is being updated.

To avoid having $\overline{DRDY}$/DOUT remain in the state of the last bit, shift a 25th SCLK to force $\overline{DRDY}$/DOUT high; see Figure 25. This technique is useful when a host controlling the ADS1245 is polling $\overline{DRDY}$/DOUT to determine when data is ready.



SYMBOL	DESCRIPTION	MIN	MAX	UNITS
t_3	$\overline{DRDY}$/DOUT low to first SCLK rising edge.	0		ns
t_4	SCLK positive or negative pulse width.	100		ns
t_5 (1)	SCLK rising edge to new data bit valid; propagation delay.	50		ns
t_6	SCLK rising edge to old data bit valid: hold time.	0		ns
t_7	Data updating, no read back allowed.	152	152	µs
t_8 (2)	Conversion time (1/data rate).	66.667	66.667	ms

NOTES: (1) Load on $\overline{DRDY}$/DOUT = 20pF||100kΩ.
(2) Values given for f_{CLK} = 2.4576MHz. For different CLK frequencies, scale proportional to CLK period. For example, for f_{CLK} = 4.9152MHz, $t_8 \rightarrow$33.333ms.

Figure 24. Data Retrieval Timing

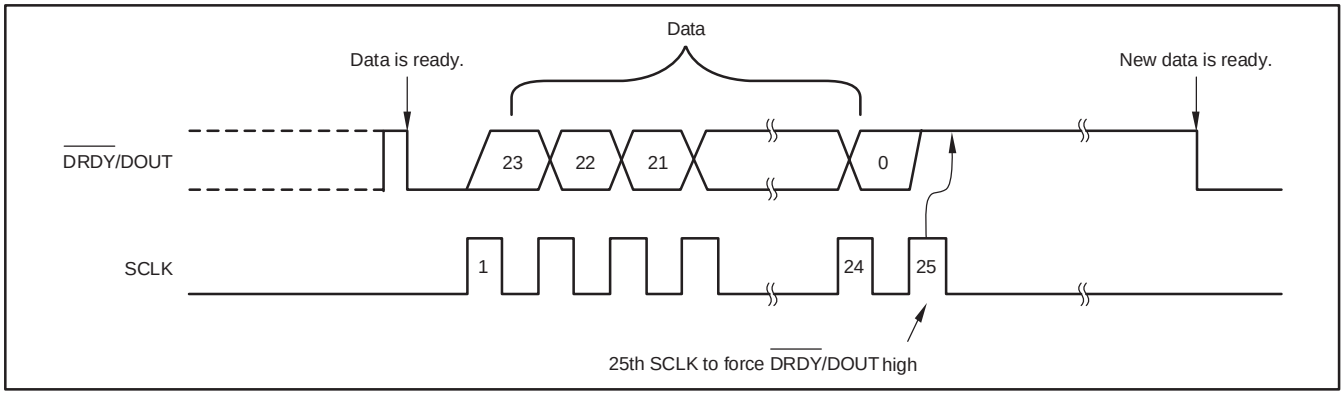
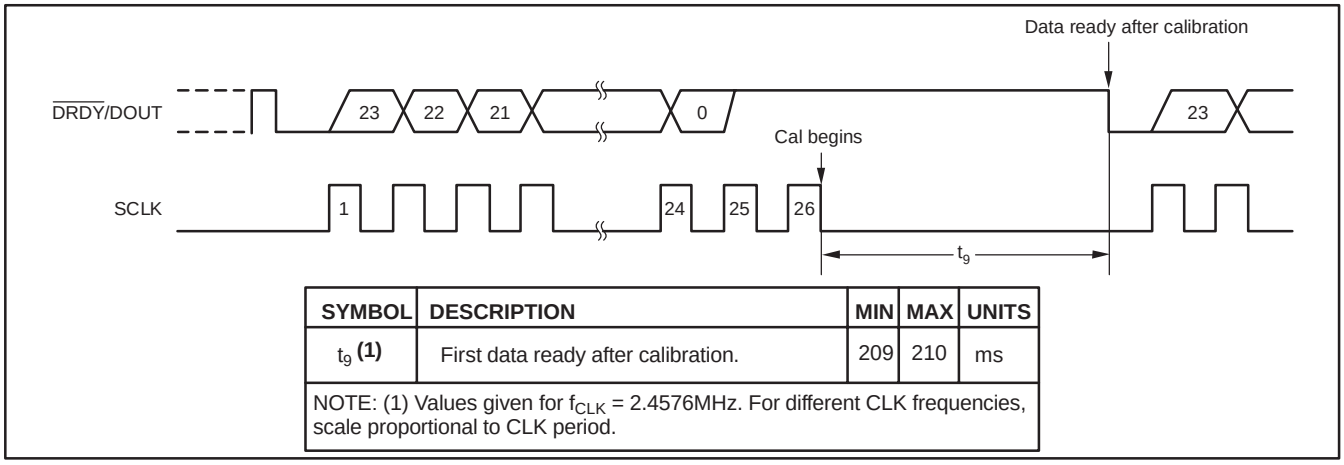


Figure 25. Data Retrieval with $\overline{\text{DRDY}}$/DOUT Forced High Afterwards

SELF-CALIBRATION

The user can initiate self-calibration at any time, though in many applications the ADS1245 drift performance is good enough that the self-calibration performing automatically at power-up is all that is needed. To initiate a self-calibration, apply at least two additional SCLKs after retrieving 24 bits of data. Figure 26 shows the timing pattern. The 25th SCLK will send $\overline{\text{DRDY}}$/DOUT high. The falling edge of the 26th SCLK will begin the calibration cycle. Additional SCLK pulses may be sent after the 26th SCLK, but minimizing activity on SCLK during calibration provides best results.

When the calibration is complete, $\overline{\text{DRDY}}$/DOUT will go low, indicating that new data is ready. There is no need to alter the analog input signal applied to the ADS1245 during calibration; the inputs pins are disconnected within the ADC and the appropriate signals are automatically applied internally. The first conversion after a calibration is fully settled and valid for use. The time required for a calibration depends on two independent signals: the falling edge of SCLK and an internal clock derived from CLK. Variations in the internal calibration values will change the time required for calibration (t_9) within the range given by the MIN/MAX specs. t_{12} and t_{13} described in the next section are likewise affected.



SYMBOL	DESCRIPTION	MIN	MAX	UNITS
t_9 (1)	First data ready after calibration.	209	210	ms

NOTE: (1) Values given for f_{CLK} = 2.4576MHz. For different CLK frequencies, scale proportional to CLK period.

Figure 26. Self-Calibration Timing

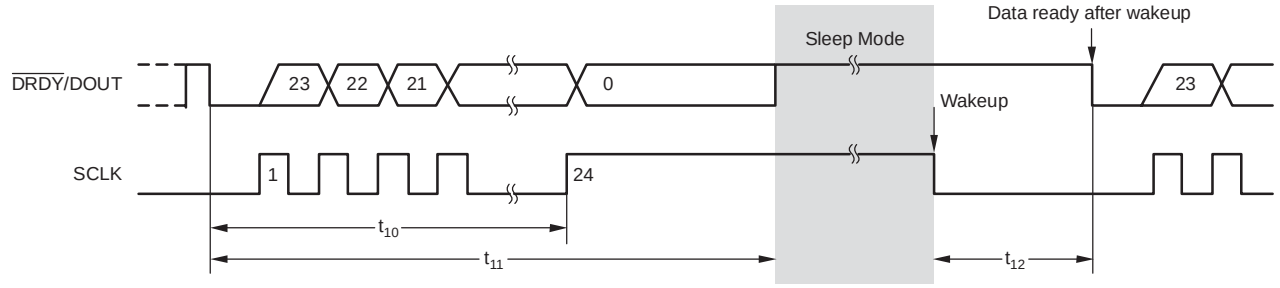
SLEEP MODE

Sleep mode dramatically reduces power consumption (typically < 1μW with CLK stopped) by shutting down all of the active circuitry. To enter Sleep mode, simply hold SCLK high after DRDY/DOUT goes low, as shown in Figure 27. Sleep Mode can be initiated at any time during read-back; it is not necessary to retrieve all 24 bits of data beforehand. Once t_{11} has passed with SCLK held high, Sleep mode will activate. DRDY/DOUT stays high once Sleep mode begins. SCLK must remain high to stay in Sleep mode. To exit Sleep mode (wakeup), set SCLK low. The first data after exiting Sleep Mode is valid. It is not necessary to stop CLK during Sleep mode, but doing so will further reduce the digital supply current.

Sleep Mode with Self-Calibration

Self-calibration can be set to run immediately after exiting Sleep mode. This is useful when the ADS1245 is put in Sleep mode for long periods of time and self-calibration is desired afterwards to compensate for temperature or supply voltage changes.

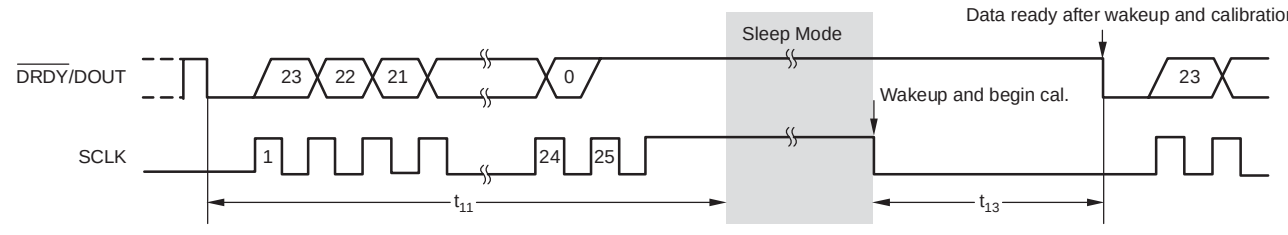
To force a self-calibration with Sleep mode, shift 25 bits out before taking SCLK high to enter Sleep mode. Self-calibration begins after wakeup. Figure 28 shows the appropriate timing. Note the extra time needed after wakeup for calibration before data is ready. The first data after Sleep mode with self-calibration is fully settled and can be used.



SYMBOL	DESCRIPTION	MIN	MAX	UNITS
t_{10}(1)	SCLK HIGH after DRDY/DOUT goes low to activate Sleep Mode.	0	63.7	ms
t_{11}(1)	Sleep Mode activation time.	66.5	66.5	ms
t_{12}(1)	Data ready after wakeup.	71	72	ms

NOTES: (1) Values given for f_{CLK} = 2.4576MHz. For different CLK frequencies, scale proportional to CLK period.

Figure 27. Sleep-Mode Timing; Can Be Used for SIngle Conversions



SYMBOL	DESCRIPTION	MIN	MAX	UNITS
t_{13}(1)	Data ready after wakeup and calibration.	210	211	ms

NOTE: (1) Values given for f_{CLK} = 2.4576MHz. For different CLK frequencies, scale proportional to CLK period.

Figure 28. Sleep-Mode with Self-Calibration on Wakeup Timing; Can Be Used for SIngle Conversions

SINGLE CONVERSIONS

When only single conversions are needed, Sleep mode can be used to start and stop the ADS1245. To make a single conversion, first enter the Sleep Mode holding SCLK high. Now, when ready to start the conversion, take SCLK low. The ADS1245 will wake up and begin the conversion. Wait for $\overline{\text{DRDY}}$/DOUT to go low, and then retrieve the data. Afterwards, take SCLK high to stop the ADS1245 from converting and re−enter Sleep mode. Continue to hold SCLK high until ready to start the next conversion. Operating in this fashion greatly reduces power consumption since the ADS1245 is shut down while idle between conversions. Self−calibrations can be performed prior to the start of the single conversions by using the waveform shown in Figure 28.

SINGLE-SUPPLY OPERATION

It is possible to operate the ADS1245 with a single supply. For a 3V supply, simply connect AVDD and DVDD together. Figure 29 shows an example of the ADS1245 running on a single 5V supply. An external resistor, R_1, is used to drop 5V supply down to a desired voltage level of DVDD. For example, if the desired DVDD supply voltage is 3V and AVDD is 5V, the value of R_1 should be:

$$R_1 = (5V - 3V)/5\mu A \approx 400k\Omega \quad (1)$$

where 5mA is a typical digital current consumption when DVDD = 3V (refer to the typical characteristic *Digital Current vs Digital Supply*). A buffer on $\overline{\text{DRDY}}$/DOUT can provide level−shifting if required.

DVDD can be set to a desired voltage by choosing a proper value of R_1, but keep in mind that DVDD must be set between 1.8V and 3.6V. Note that the maximum logic high output of $\overline{\text{DRDY}}$/DOUT is equal to DVDD, but both CLK and SCLK inputs can be driven with 5V logic regardless of the DVDD or AVDD voltage. Use 0.1mF capacitors to bypass both AVDD and DVDD.

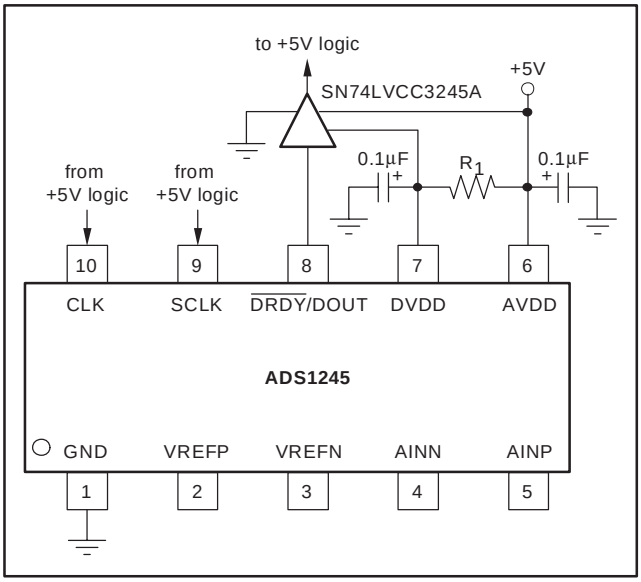
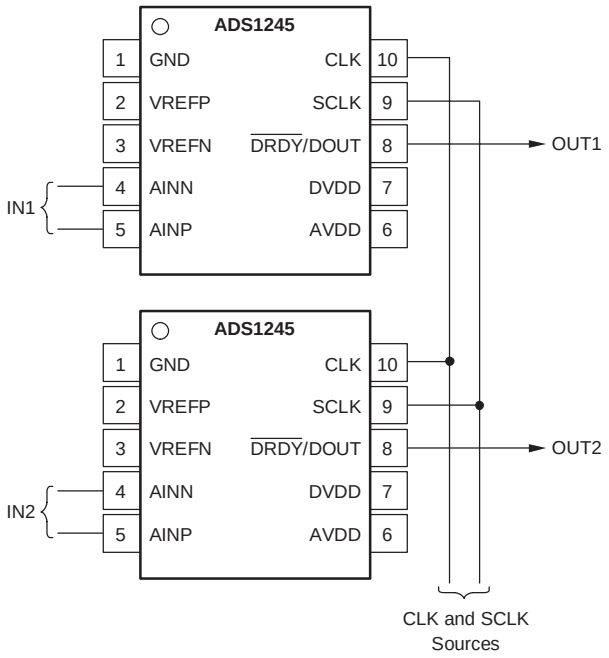


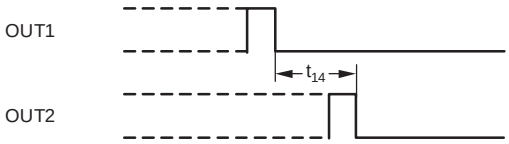
Figure 29. Example of the ADS1244 Running on a Single 5V Supply

MULTI-CHANNEL SYSTEMS

Multiple ADS1245s can be operated in parallel to measure multiple input signals. Figure 30 shows an example of a two-channel system. For simplicity, the supplies and reference circuitry were not included. The same CLK signal should be applied to all devices. To be able to synchronize the ADS1245s, connect the same SCLK signal to all devices as well. When ready to synchronize, place all the devices in Sleep mode. Afterwards, a wakeup command will synchronize all the ADS1245s; that is, they will sample the input signals simultaneously

The $\overline{\text{DRDY}}$/DOUT outputs will go low at approximately the same time after synchronization. The falling edges, indicating that new data is ready, will vary with respect to each other no more than timing specification t_{14}. This variation is due to possible differences in the ADS1245 internal calibration settings. To account for this when using multiple devices, either wait for t_{14} to pass after seeing one device $\overline{\text{DRDY}}$/DOUT go low, or wait until all $\overline{\text{DRDY}}$/DOUTs have gone low before retrieving data.





SYMBOL	DESCRIPTION	MIN	MAX	UNITS
t_{14}	Difference between $\overline{DRDY}$/DOUTs going low in multichannel systems.		± 500	µs

Figure 30. Example of Using Multiple ADS1245s in Parallel

SUMMARY OF SERIAL INTERFACE WAVEFORMS

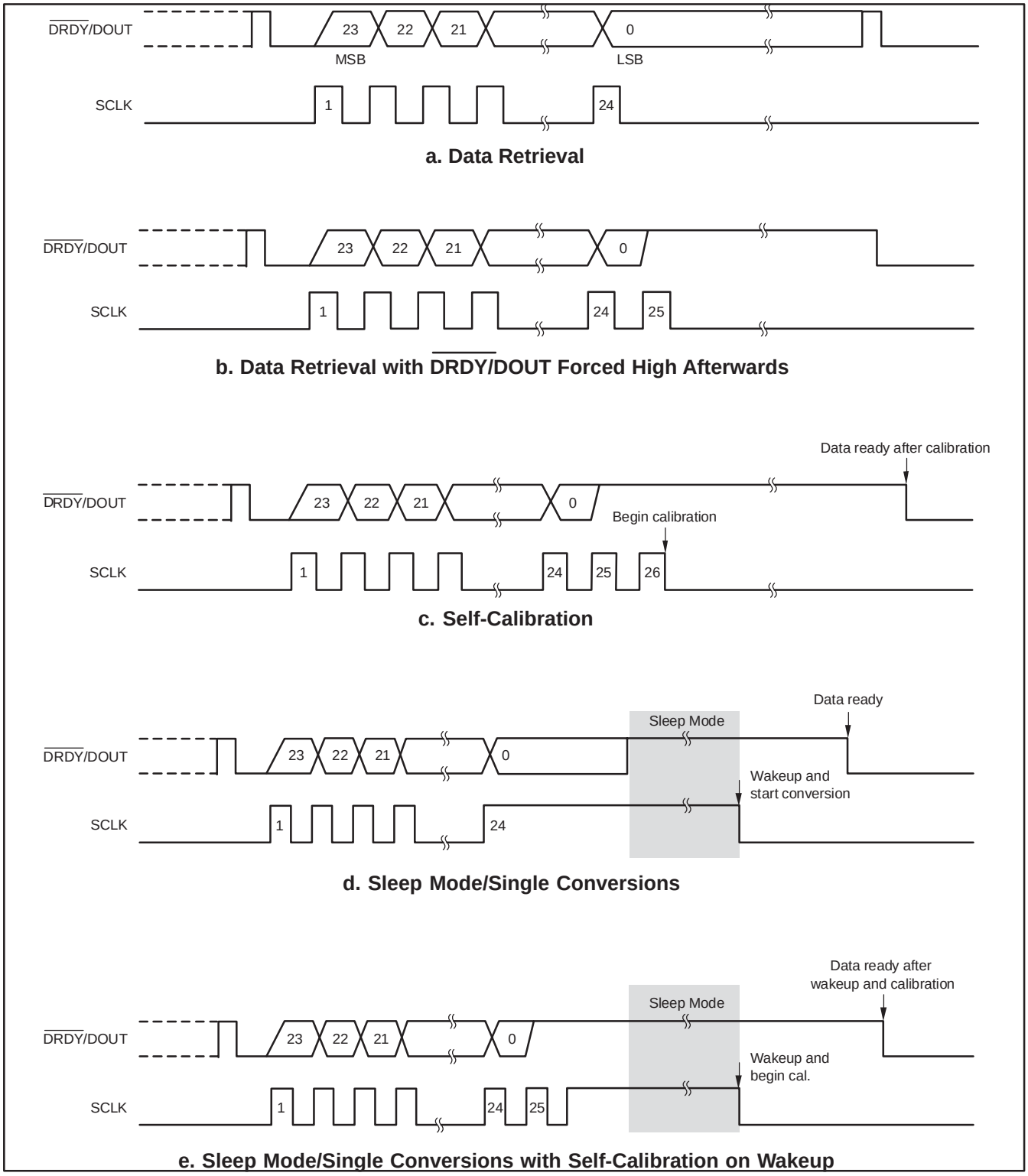


Figure 31. Summary of Serial Interface Waveforms

PACKAGING INFORMATION

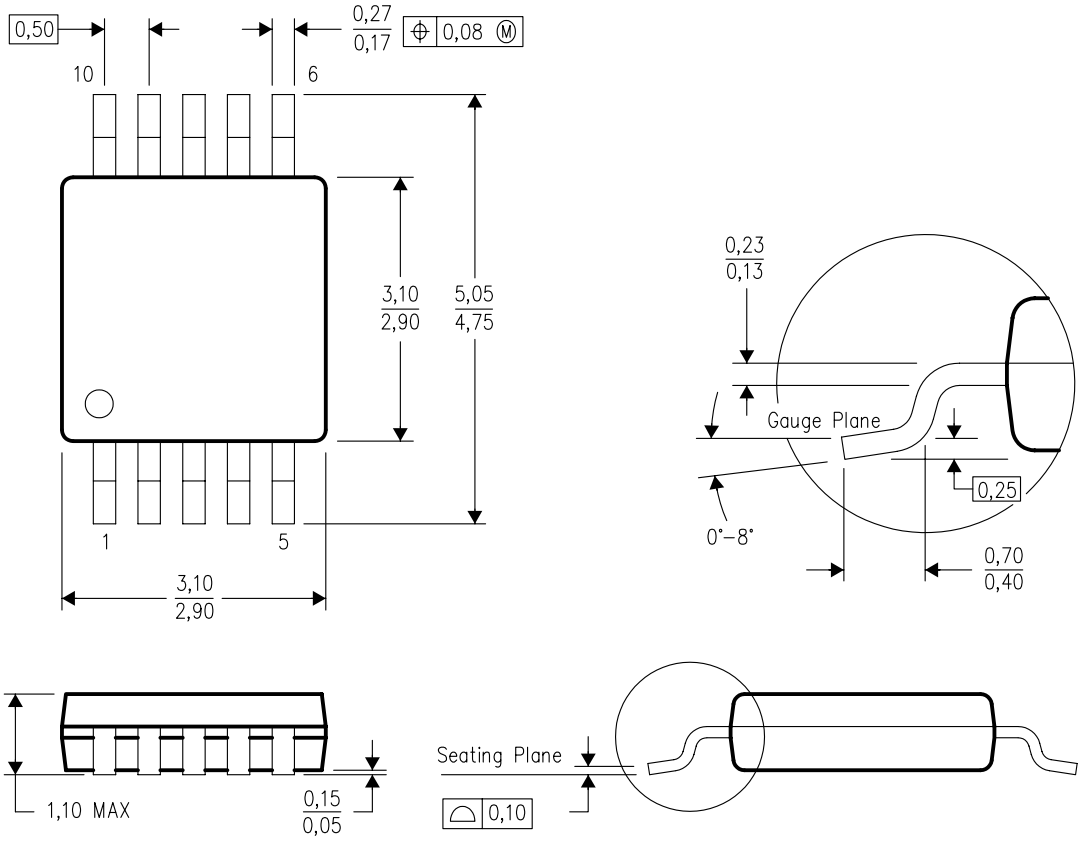
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ADS1245IDGSR	ACTIVE	MSOP	DGS	10	2500	TBD	Call TI	Call TI
ADS1245IDGST	ACTIVE	MSOP	DGS	10	250	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



4073272/C 02/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

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