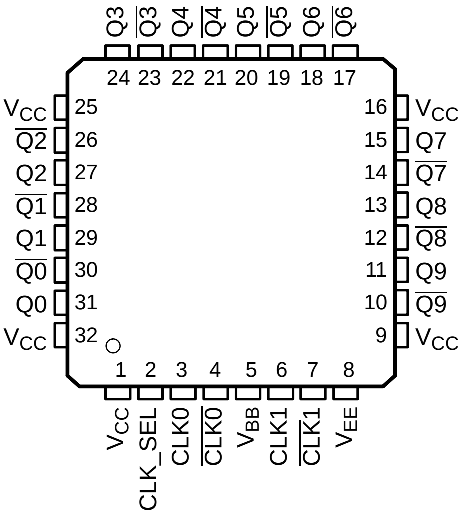
LOW-VOLTAGE 1:10 LVPECL/HSTL WITH SELECTABLE INPUT CLOCK DRIVER

FEATURES

- **Distributes One Differential Clock Input Pair LVPECL/HSTL to 10 Differential LVPECL Clock Outputs**
- **Fully Compatible With LVECL/LVPECL/HSTL**
- **Single Supply Voltage Required, ±3.3-V or ±2.5-V Supply**
- **Selectable Clock Input Through CLK_SEL**
- **Low-Output Skew (Typ 15 ps) for Clock-Distribution Applications**
- **VBB Reference Voltage Output for Single-Ended Clocking**
- **Available in a 32-Pin LQFP Package**
- **Frequency Range From DC to 3.5 GHz**
- **Pin-to-Pin Compatible With MC100 Series EP111, ES6111, LVEP111, PTN1111**

LQFP PACKAGE
(TOP VIEW)



DESCRIPTION

The CDCLVP110 clock driver distributes one differential clock pair of either LVPECL or HSTL (selectable) input, (CLK0, CLK1) to ten pairs of differential LVPECL clock (Q0, Q9) outputs with minimum skew for clock distribution. The CDCLVP110 can accept two clock sources into an input multiplexer. The CLK0 input accepts either LVECL/LVPECL input signals, while CLK1 accepts an HSTL input signal when operated under LVPECL conditions. The CDCLVP110 is specifically designed for driving 50-Ω transmission lines.

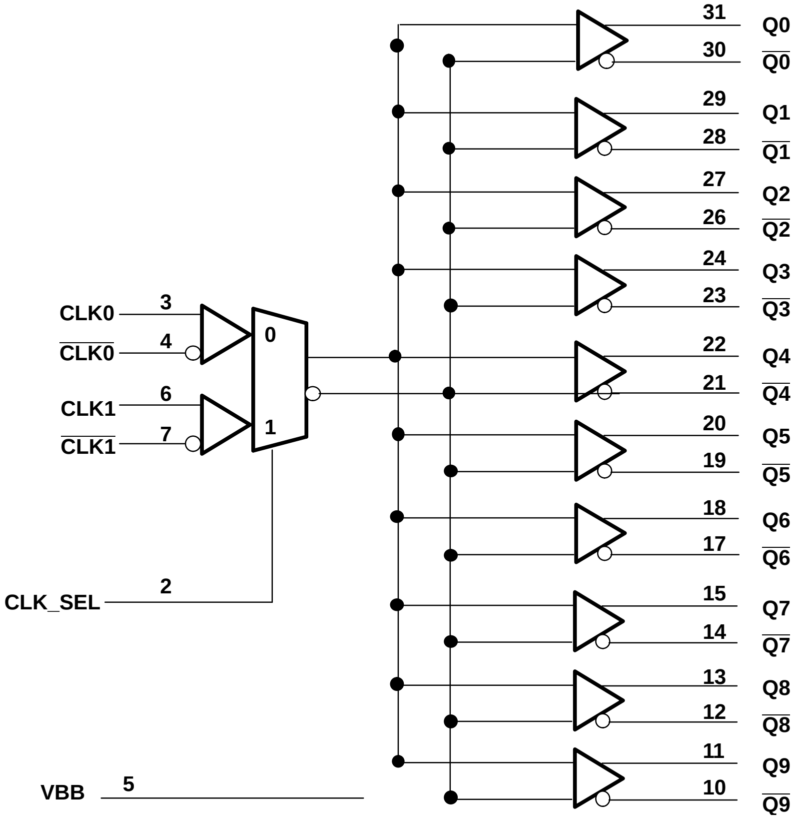
The VBB reference voltage output is used if single-ended input operation is required. In this case the VBB pin should be connected to $\overline{\text{CLK0}}$ and bypassed to GND via a 10-nF capacitor.

However, for high-speed performance up to 3.5 GHz, the differential mode is strongly recommended.

The CDCLVP110 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

CLK_SEL	ACTIVE CLOCK INPUT
0	CLK0, $\overline{\text{CLK0}}$
1	CLK1, $\overline{\text{CLK1}}$



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
CLK_SEL	2	Clock select. Used to select between CLK0 and CLK1 input pairs.
CLK0, $\overline{\text{CLK0}}$	3, 4	Differential LVECL/LVPECL input pair
CLK1, $\overline{\text{CLK1}}$	6, 7	Differential HSTL input pair
Q [9:0]	11, 13, 15, 18, 20, 22, 24, 27, 29, 31	LVECL/LVPECL clock outputs, these outputs provide low-skew copies of CLKn.
$\overline{\text{Q}}$[9:0]	10, 12, 14, 17, 19, 21,23, 26, 28, 30	LVECL/LVPECL complementary clock outputs, these outputs provide copies of $\overline{\text{CLKn}}$.
V_{BB}	5	Reference voltage output for single-ended input operation
V_{CC}	1, 9, 16, 25, 32	Supply voltage
V_{EE}	8	Device ground or negative supply voltage in ECL mode

ABSOLUTE MAXIMUM RATINGS(1)

V_{CC}	Supply voltage	-0.3 V to 4.6 V
V_I	Input voltage	-0.3 V to V_{CC} + 0.5 V
V_O	Output voltage	-0.3 V to V_{CC} + 0.5 V
I_{IN}	Input current	±20 mA
V_{EE}	Negative supply voltage	-0.3 V to 4.6 V
I_{BB}	Sink/source current	-1 to 1 mA
I_O	DC output current	-50 mA
T_{stg}	Storage temperature range	-65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (relative to V_{EE})	2.375	2.5/3.3	3.8	V
T_A(1)	Operating free-air temperature	-40		85	°C

(1) Operating junction temperature affects device lifetime. The continuous operation junction temperature is recommended to be at max 110°C. The device ac and dc parameters are specified up to 85°C ambient temperature. See the *PCB Layout Guidelines for CDCLVP110* application note, literature number SCAA057 for more details.

PACKAGE THERMAL IMPEDANCE

		TEST CONDITION	MIN	MAX	UNIT
Θ_{JA}	Thermal resistance junction to ambient(1)	0 LFM		78	°C/W
		150 LFM		73	°C/W
		250 LFM		71	°C/W
		500 LFM		68	°C/W
Θ_{JC}	Thermal resistance junction to case			51	°C/W

(1) According to JESD 51-7 standard.

LVECL DC ELECTRICAL CHARACTERISTICS

Vsupply: V_{CC} = 0 V, V_{EE} = -2.375 V to -3.8 V

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{EE}	Supply internal current	Absolute value of current	-40°C	40		78	mA
			25°C	45		82	
			85°C	48		85	
I_{CC}	Output and internal supply current	All outputs terminated 50 Ω to V_{CC} - 2 V	-40°C			343	mA
			25°C			370	
			85°C			380	
I_{IN}	Input current	Includes pullup/pulldown resistors	-40°C, 25°C, 85°C			150	µA
V_{BB}	Internally generated bias voltage	For V_{EE} = -3 to -3.8 V, I_{BB} = -0.2 mA	-40°C	-1.38		-1.26	V
			25°C	-1.42		-1.26	
			85°C	-1.45		-1.26	
		V_{EE} = -2.375 to -2.75 V, I_{BB} = -0.2 mA	-40°C, 25°C, 85°C	-1.38		-1.16	
V_{IH}	High-level input voltage (CLK_SEL)		-40°C, 25°C, 85°C	-1.165		-0.88	V

LVECL DC ELECTRICAL CHARACTERISTICS (continued)

Vsupply: V_{CC} = 0 V, V_{EE} = -2.375 V to -3.8 V

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage (CLK_SEL)		-40°C, 25°C, 85°C	-1.81		-1.475	V
VIN_{PP}	Input amplitude (CLK0, $\overline{\text{CLK0}}$)	Difference of input 9 V_{IH}-V_{IL} , See Note (1)	-40°C, 25°C, 85°C	0.5		1.3	V
V_{CM}	Common-mode voltage (CLK0, $\overline{\text{CLK0}}$)	Cross point of input 9 average (V_{IH}, V_{IL})	-40°C, 25°C, 85°C	V_{EE} + 1		-0.3	V
V_{OH}	High-level output voltage	I_{OH} = -21 mA	-40°C	-1.26		-0.9	V
			25°C	-1.2		-0.9	
			85°C	-1.15		-0.9	
V_{OL}	Low-level output voltage	I_{OL} = -5 mA	-40°C	-1.85		-1.5	V
			25°C	-1.85		-1.45	
			85°C	-1.85		-1.4	
V_{OD}	Differential output voltage swing	Terminated with 50 Ω to V_{CC} - 2 V, See Figure 3	-40°C, 25°C, 85°C	600			V

(1) VIN_{PP} minimum and maximum is required to maintain ac specifications, actual device function tolerates a minimum VIN_{PP} of 100 mV.

LVPECL/HSTL DC ELECTRICAL CHARACTERISTICS

Vsupply: V_{CC} = 2.375 V to 3.8 V, V_{EE}= 0 V

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{EE}	Supply internal current	Absolute value of current	-40°C	40		78	mA
			25°C	45		82	
			85C	48		85	
I_{CC}	Output and internal supply current	All outputs terminated 50 Ω to V_{CC} - 2 V	-40°C			343	mA
			25°C			370	
			85°C			380	
I_{IN}	Input current	Includes pullup/pulldown resistors	-40°C, 25°C, 85°C			150	µA
V_{BB}	Internally generated bias voltage	V_{EE} = -3 to -3.8 V, I_{BB}= -0.2 mA	-40°C	V_{CC} - 1.38		V_{CC} - 1.26	V
			25°C	V_{CC} - 1.42		V_{CC} - 1.26	
			85°C	V_{CC} - 1.45		V_{CC} - 1.26	
		V_{EE} = -2.375 to -2.75 V, I_{BB} = -0.2 mA	-40°C, 25°C, 85°C	V_{CC} - 1.38		V_{CC} - 1.16	
V_{IH}	High-level input voltage (CLK_SEL)	-40°C, 25°C, 85°C		V_{CC} - 1.165		V_{CC} - 0.88	V
V_{IL}	Low-level input voltage (CLK_SEL)	-40°C, 25°C, 85°C		V_{CC} - 1.81		V_{CC} - 1.475	V
VIN_{PP}	Input amplitude (CLK0, $\overline{\text{CLK0}}$)	Difference of input 9 V_{IH}-V_{IL}, see Note (1)	-40°C, 25°C, 85°C	0.5		1.3	V
V_{IC}	Common-mode voltage (CLK0, $\overline{\text{CLK0}}$)	Cross point of input 9 average (V_{IH}, V_{IL})	-40°C, 25°C, 85°C	1		V_{CC} - 0.3	V

(1) VIN_{PP} minimum and maximum is required to maintain ac specifications, actual device function tolerates a minimum VIN_{PP} of 100 mV.

LVPECL/HSTL DC ELECTRICAL CHARACTERISTICS (continued)

Vsupply: V_{CC} = 2.375 V to 3.8 V, V_{EE}= 0 V

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{ID}	Differential input voltage (CLK1, $\overline{\text{CLK1}}$)	Difference of input V_{IH}-V_{IL}, See Note (1)	-40°C, 25°C, 85°C	0.4		1.9	V
$V_{I(x)}$	Input crossover voltage (CLK1, $\overline{\text{CLK1}}$)	Cross point of input 9 average (V_{IH}, V_{IL})	-40°C, 25°C, 85°C	0.68		0.9	V
V_{OH}	High-level output voltage	I_{OH} = -21 mA	-40°C	V_{CC} - 1.26		V_{CC} - 0.9	V
			25°C	V_{CC} - 1.2		V_{CC} - 0.9	
			85°C	V_{CC} - 1.15		V_{CC} - 0.9	
V_{OL}	Low-level output voltage	I_{OL} = -5 mA	-40°C	V_{CC} - 1.85		V_{CC} - 1.5	V
			25°C	V_{CC} - 1.85		V_{CC} - 1.45	
			85°C	V_{CC} - 1.85		V_{CC} - 1.4	
V_{OD}	Differential output voltage swing	Terminated with 50 Ω to V_{CC} - 2 V, See Figure 4	-40°C, 25°C, 85°C	600			mV

AC ELECTRICAL CHARACTERISTICS

Vsupply: V_{CC} = 2.375 V to 3.8 V, V_{EE} = 0 V or LVECL/LVPECL input V_{CC} = 0 V, V_{EE} = -2.375 V to -3.8 V

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd}	Differential propagation delay CLK0, $\overline{\text{CLK0}}$ to all Q0, $\overline{\text{Q0}}$… Q9, $\overline{\text{Q9}}$	Input condition: VCM = 1 V, V_{PP} = 0.5 V	-40°C, 25°C, 85°C	230		350	ps
$t_{sk(pp)}$	Part-to-part skew	See Note B and Figure 1	-40°C, 25°C, 85°C			70	ps
$t_{sk(o)}$	Output-to-output skew	See Note A and Figure 1	-40°C, 25°C, 85°C		15	30	ps
$t_{(JITTER)}$	Cycle-to-cycle RMS jitter		-40°C, 25°C, 85°C			< 1	ps
$f_{(max)}$	Maximum frequency	Functional up to 3.5 GHz, timing specifications apply at 1 GHz, see Figure 3	-40°C, 25°C, 85°C			3500	MHz
t_r/t_f	Output rise and fall time (20%, 80%)		-40°C, 25°C, 85°C	100		200	ps

HSTL INPUT

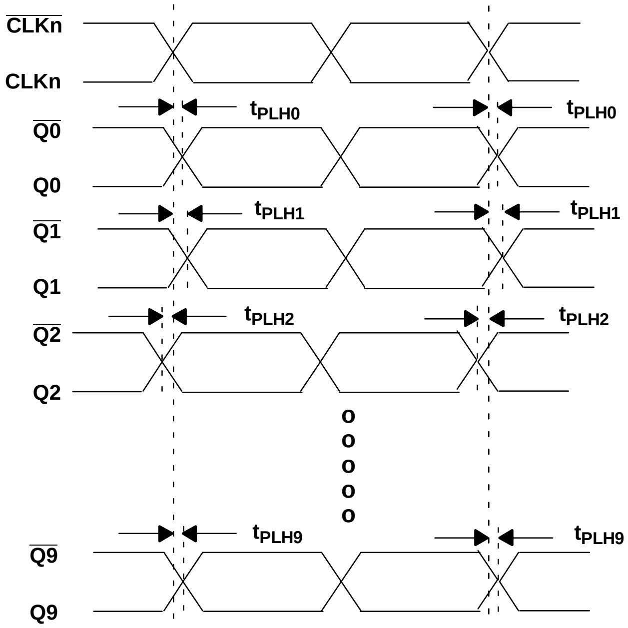
Vsupply: V_{CC} = 2.375 V to 3.8 V, V_{EE} = 0 V

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd}	Differential propagation delay CLK0, $\overline{\text{CLK0}}$ to all Q0, $\overline{\text{Q0}}$… Q9, $\overline{\text{Q9}}$	Input condition: V_x = 0.68 V, V_{dif} = 0.4 V	-40°C, 25°C, 85°C	290		370	ps
$t_{sk(pp)}$	Part-to-part skew	See Note B and Figure 1	-40°C, 25°C, 85°C			70	ps
$t_{sk(o)}$	Output to output skew	See Note A and Figure 1	-40°C, 25°C, 85°C		10	30	ps
$t_{(JITTER)}$	Cycle-to-cycle RMS jitter		-40°C, 25°C, 85°C			<1	ps

HSTL INPUT (continued)

Vsupply: V_{CC} = 2.375 V to 3.8 V, V_{EE} = 0 V

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{(max)}$	Maximum frequency	Functional up to 3.5 GHz, timing specifications apply at 1 GHz, See Figure 4	-40°C, 25°C, 85°C			3500	MHz
t_r/t_f	Output rise and fall time (20%, 80%)		-40°C, 25°C, 85°C	100		200	ps



A. Output skew is calculated as the greater of: The difference between the fastest and the slowest t_{PLHn} (n = 0, 1,...9) or the difference between the fastest and the slowest t_{PHLn} (n = 0, 1,...9).

B. Part-to-part skew, is calculated as the greater of: The difference between the fastest and the slowest t_{PLHn} (n = 0, 1,...9) across multiple devices or the difference between the fastest and the slowest t_{PHLn} (n = 0, 1,...9) across multiple devices.

Figure 1. Waveform for Calculating Both Output and Part-to-Part Skew

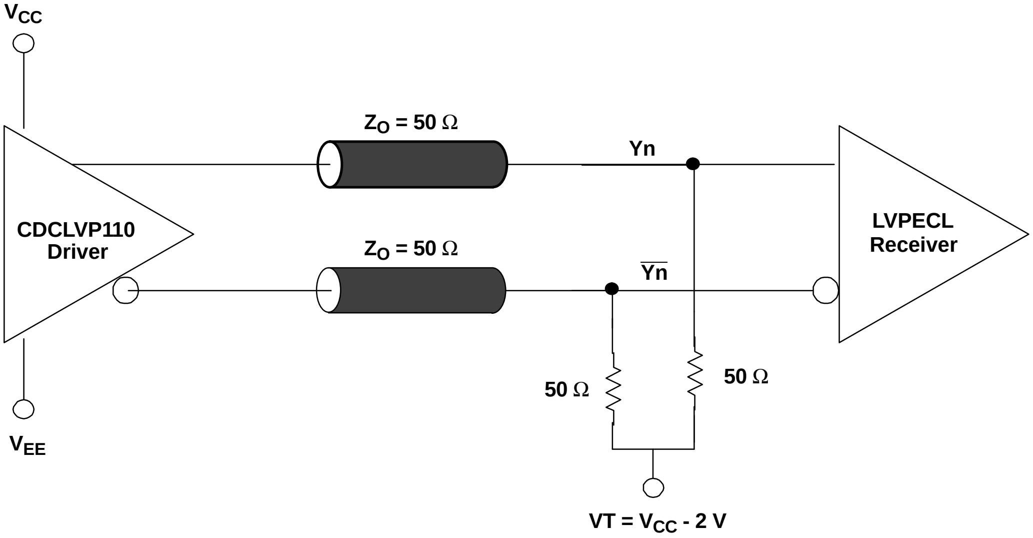


Figure 2. Typical Termination for Output Driver (See the Interfacing Between LVPECL, LVDS, and CML Application Note, Literature Number SCAA056)

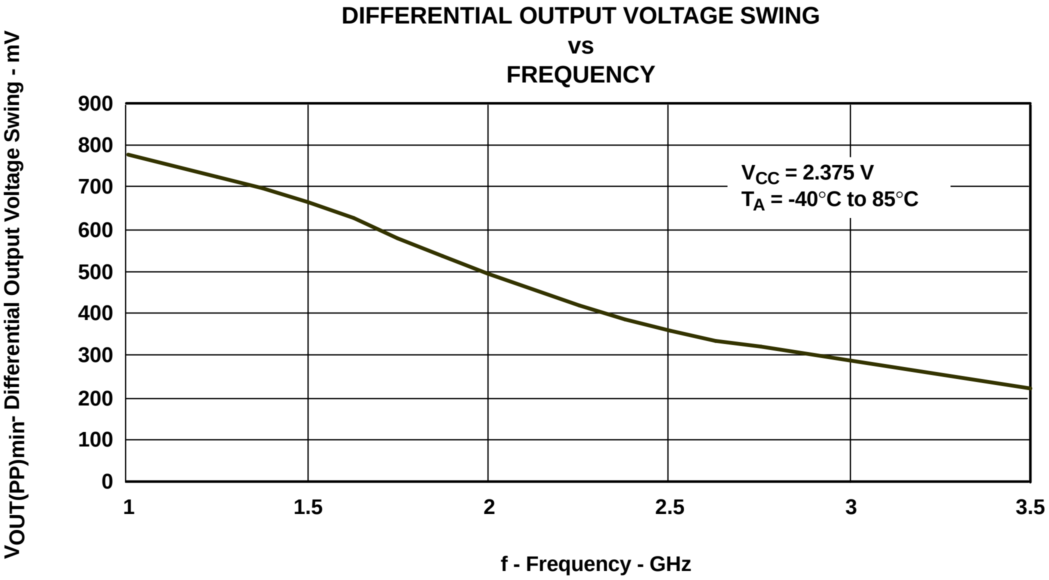


Figure 3. LVPECL Input Using CLK0 Pair, VCM = 1 V, $VIN_{dif} = 0.5\ V$

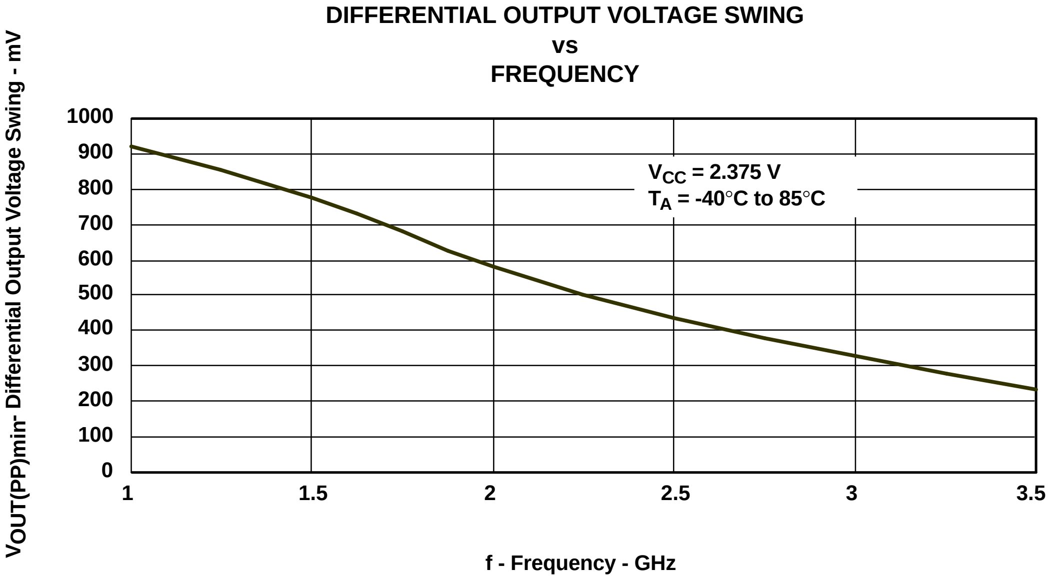


Figure 4. HSTL Input Using CLK1 Pair, VCM = 0.68 V, VIN_{dif} = 0.4 V

PACKAGE OPTION ADDENDUM

4-Mar-2005

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
CDCLVP110VF	ACTIVE	LQFP	VF	32	250	None	CU NIPDAU	Level-2-220C-1 YEAR
CDCLVP110VFR	ACTIVE	LQFP	VF	32	1000	None	CU NIPDAU	Level-2-220C-1 YEAR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
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Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
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[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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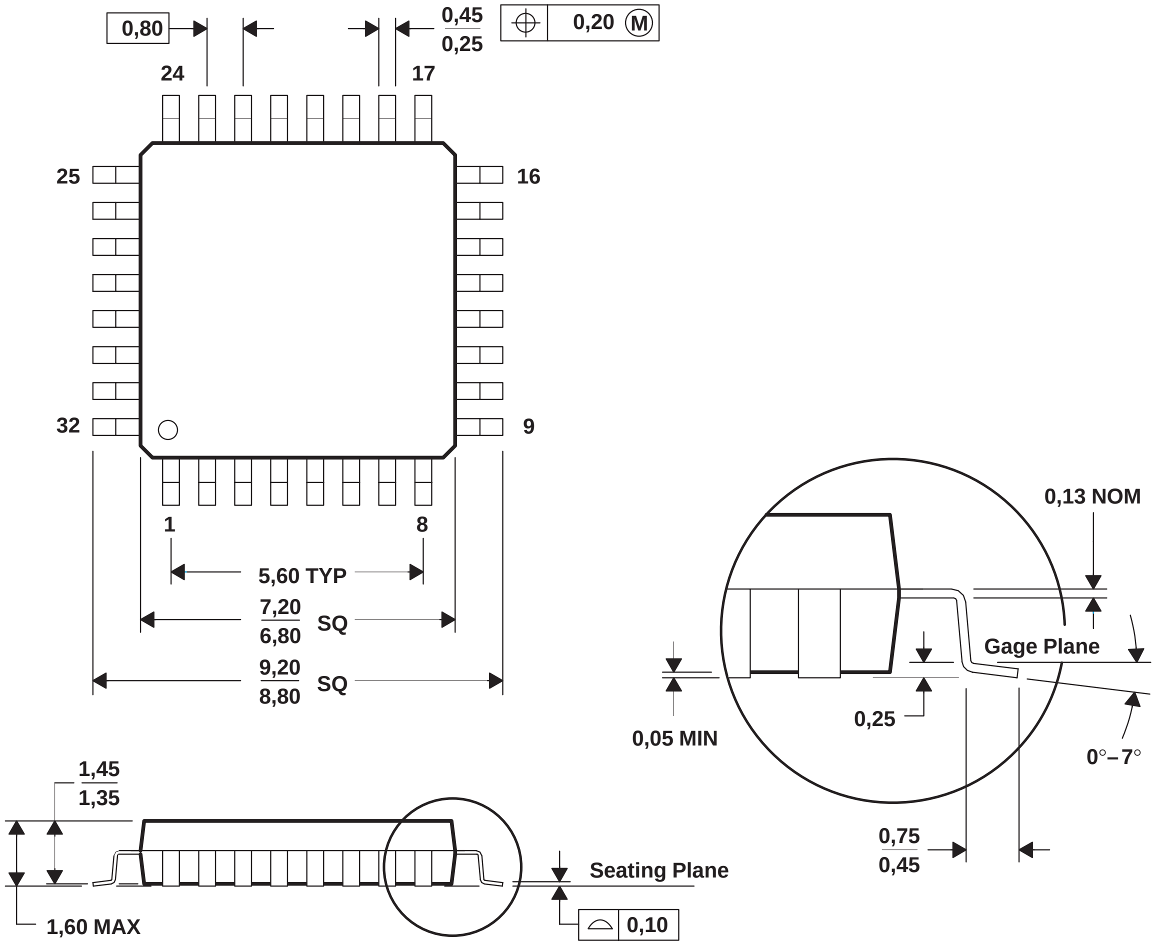
VF (S-PQFP-G32) **PLASTIC QUAD FLATPACK**



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NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.

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