7. External Memory Interfaces in HardCopy III Devices

HIII51007-3.2

This chapter describes the hardware features that support high-speed memory interfacing for each double data rate (DDR) memory standard in HardCopy® III devices. HardCopy III devices feature delay-locked loops (DLLs), phase-locked loops (PLLs), dynamic on-chip termination (OCT), read-and-write leveling, and deskew circuitry.

This chapter contains the following sections:

Similar to the Stratix® III I/O structure, the HardCopy III I/O structure has been redesigned to provide flexible and high-performance support for existing and emerging external memory standards. These include high-performance DDR memory standards such as DDR3, DDR2, DDR SDRAM, QDRII+, QDRII SRAM, and RLDRAM II.

HardCopy III devices offer the same external memory interface features found in Stratix III devices. These features include DLLs, PLLs, dynamic OCT, trace mismatch compensation, read-and-write leveling, deskew circuitry, half data rate (HDR) blocks, 4- to 36-bit DQ group widths, and DDR external memory support on all sides of the HardCopy III device. HardCopy III devices provide an efficient architecture to quickly and easily fit wide external memory interfaces with the small modular I/O bank structure.

HardCopy III devices are designed to support the same I/O standards and implementation guidelines for external memory interfaces as Stratix III devices.

In addition, the Quartus® II timing analysis tool (TimeQuest Timing Analyzer) provides a complete solution for the highest reliable frequency of operation across process, voltage, and temperature (PVT) variations.

PLL reconfiguration is not required for AltMEMPHY-based designs. The AltMEMPHY megafunction has an auto calibration feature so implementing PLL reconfiguration does not add value.

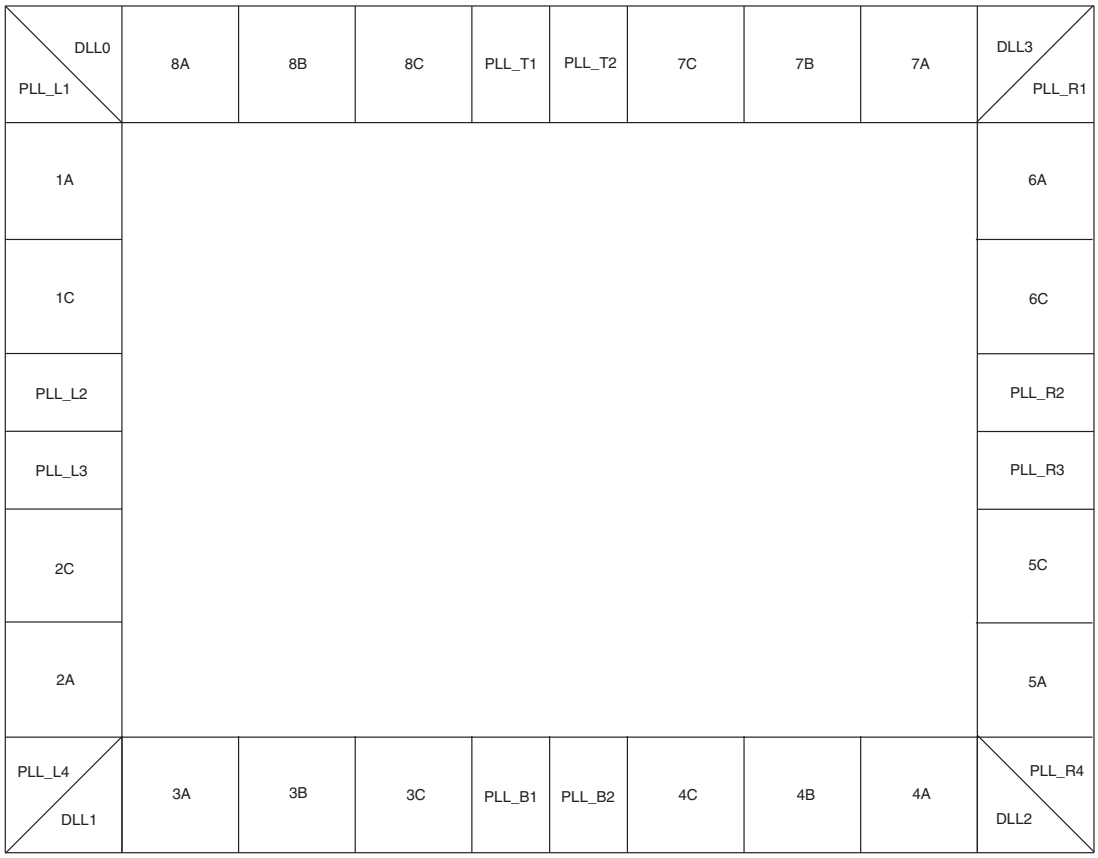
For more information about the ALTMEMPHY megafunction, refer to the *External Memory Interface Handbook*.

Altera recommends enabling the PLL reconfiguration feature and the DLL phase offset feature (DLL reconfiguration) for HardCopy III devices. Because HardCopy III devices are mask programmed, they cannot be changed after the silicon is fabricated. By implementing these two features, you can perform timing adjustments to improve or resolve timing issues after the silicon is fabricated.

For information about the clock rate support for Hardcopy III devices, refer to the *System Performance Specifications* section of the *External Memory Interface Handbook*.

Figure 7–1 shows a package-bottom view for HardCopy III external memory support.

Figure 7–1. Package-Bottom View for HardCopy III Devices *(Note 1)*, *(2)*, *(3)*



Notes to Figure 7–1:

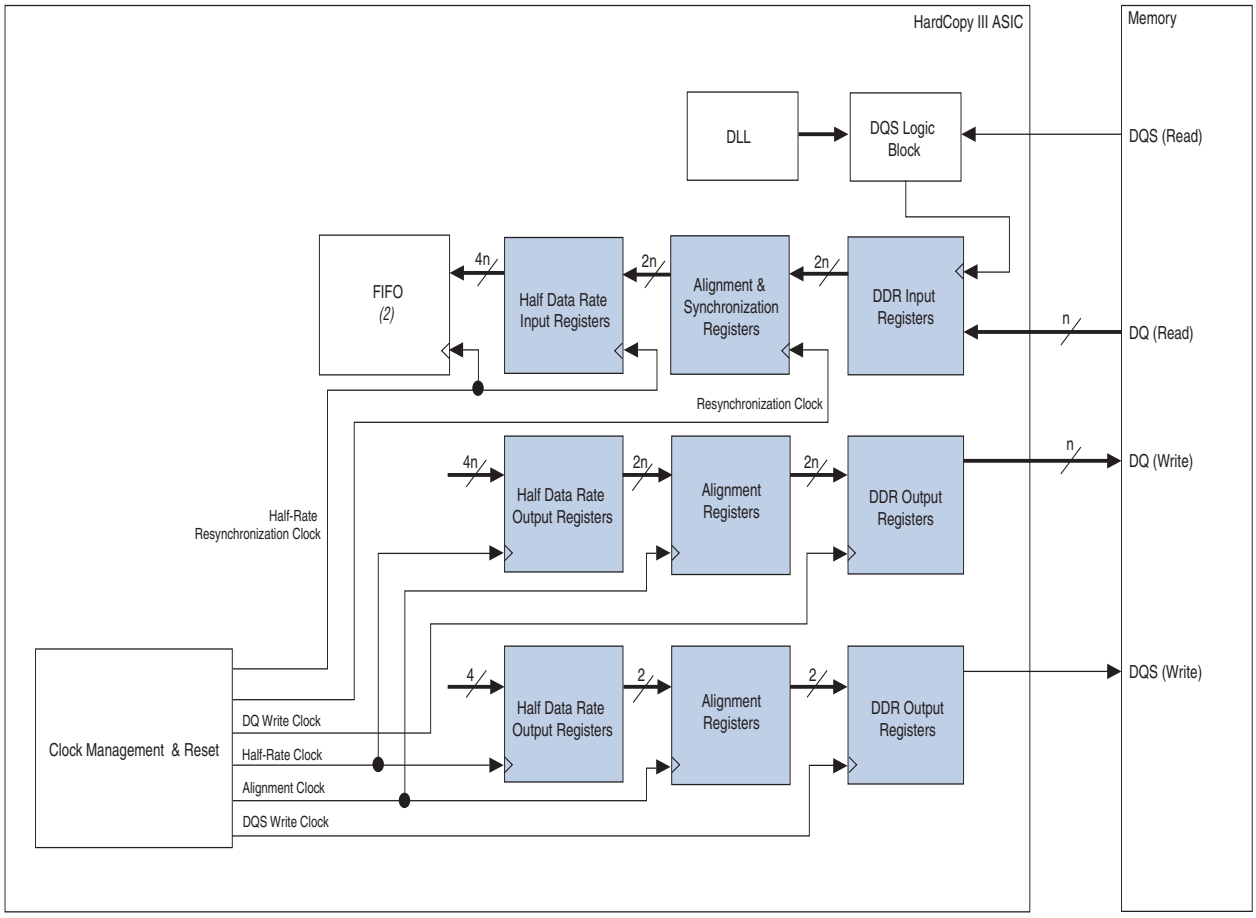
(1) The number of I/O banks and PLLs available depend on the device density.

(2) Not all HardCopy III devices support I/O banks 1B, 2B, 5B, and 6B.

(3) There is only one PLL on each side of the HC325W and HC325F devices. These devices do not support I/O banks 3B, 4B, 7B, and 8B.

Figure 7–2 shows the memory interface data path that uses all the HardCopy III I/O element (IOE) features.

Figure 7–2. External Memory Interface Data Path Overview ***(Note 1)***, ***(2)***, ***(3)***



Notes to Figure 7–2:

(1) Each register block can be bypassed.

(2) The blocks for each memory interface may differ slightly.

(3) These signals may be bidirectional or unidirectional, depending on the memory standard. When bidirectional, the signal is active during both read and write operations.

Memory Interfaces Pin Support

A typical memory interface requires data (D, Q, or DQ), data strobe (DQS and DQSn/CQn), address, command, and clock pins. Some memory interfaces use data mask (DM) pins to enable write masking and QVLD pins to indicate that the read data is ready to be captured. This section describes how HardCopy III devices support these pins.

Data and Data Clock/Strobe Pins

HardCopy III DDR memory interface read data-strobes or clocks are called DQS pins. Depending on the memory specifications, the DQS pins can be bidirectional single-ended signals (in DDR2 and DDR SDRAM), bidirectional differential signals (DDR3 and DDR2 SDRAM), unidirectional differential signals (in RLDRAM II), or unidirectional complementary signals (QDRII+ and QDRII SRAM). Connect the unidirectional read-and-write data-strobes or clocks to HardCopy III DQS pins.

HardCopy III devices offer differential input buffers for differential read data-strobe/clock operations and provide an independent DQS logic block for each CQn pin for complementary read data-strobe/clock operations. In the HardCopy III pin tables, the differential DQS pin-pairs are denoted as DQS and DQSn pins; the complementary DQS signals are denoted as DQS and CQn pins. DQSn and CQn pins are marked separately in the pin table. Each CQn pin connects to a DQS logic block and the shifted CQn signals go to the negative-edge input registers in the DQ IOE registers.

☞ Use differential DQS signaling for DDR2 SDRAM interfaces running higher than 333 MHz.

HardCopy III DDR memory interface data pins are called DQ pins. The DQ pins can be bidirectional signals, as in DDR3, DDR2, and DDR SDRAM, and RLDRAM II common I/O (CIO) interfaces, or unidirectional signals, as in QDRII+, QDRII SRAM, and RLDRAM II separate I/O (SIO) devices. Connect the unidirectional read data signals to HardCopy III DQ pins and the unidirectional write data signals to a DQS/DQ group other than the read DQS/DQ group. Furthermore, the write clocks must be assigned to the DQS/DQSn pins associated with this write DQS/DQ group. Do not use the DQS/CQn pin-pair for write clocks.

☞ Using a DQS/DQ group for the write data signals minimizes output skew and allows access to the write leveling circuitry (for DDR3 SDRAM interfaces). These pins also have access to deskewing circuitry that can compensate for delay mismatch between signals on the bus.

Table 7–1 lists the pin connections between a HardCopy III device and an external memory device.

Table 7–1. Memory Interfaces Pin Utilization for HardCopy III Devices (Part 1 of 2)

Pin Description	Memory Standard	HardCopy III Pin Utilization
Read Data	All	DQ
Write Data	All	DQ *(1)*
Parity, DM, BWSn, NWSn, QVLD, ECC	All	DQ *(1)*, *(2)*

Table 7–1. Memory Interfaces Pin Utilization for HardCopy III Devices (Part 2 of 2)

Pin Description	Memory Standard	HardCopy III Pin Utilization
Read Strobes/Clocks	DDR3 SDRAM DDR2 SDRAM (with differential DQS signaling) *(3)* RLDRAM II	Differential DQS/DQSn
	DDR2 SDRAM (with single-ended DQS signaling) *(3)* DDR SDRAM	Single-ended DQS
	QDRII+ SRAM QDRII SRAM	Complementary DQS/CQn
Write Clocks	QDRII+ SRAM *(4)* QDRII SRAM *(4)* RLDRAM II SIO	Any unused DQS and DQSn pin pairs *(1)*
Memory Clocks	DDR3 SDRAM	Any unused DQ or DQS pins with `DIFFIO_RX` capability for the `mem_clk[0]` and `mem_clk_n[0]` signals.
		Any unused DQ or DQS pins with `DIFFOUT` capability for the `mem_clk[n:1]` *and* `mem_clk_n[n:1]` signals (where n is greater than or equal to 1).
	DDR2 SDRAM (with differential DQS signaling)	Any `DIFFIO_RX` pins for the `mem_clk[0]` and `mem_clk_n[0]` signals.
		Any unused `DIFFOUT` pins for the `mem_clk[n:1]` and `mem_clk_n[n:1]` signals (where n is greater than or equal to 1).
	DDR2 SDRAM (with single-ended DQS signaling) DDR SDRAM RLDRAM II	Any `DIFFOUT` pins
	QDRII+ SRAM *(4)* QDRII SRAM *(4)*	Any unused DQSn pin pairs *(1)*

Notes to Table 7–1:

(1) If the write data signals are unidirectional including the data mask pins, connect them to a separate DQS/DQ group other than the read DQS/DQ group. Connect the write clock to the DQS and DQSn pin-pair associated with that DQS/DQ group. Do not use the DQS and CQn pin-pair as write clocks.

(2) The BWSn, NWSn, and DM pins must be part of the write DQS/DQ group. Parity, QVLD, and ECC pins must be part of the read DQS/DQ group.

(3) DDR2 SDRAM supports either single-ended or differential DQS signaling.

(4) QDRII+/QDRII SRAM devices typically use the same clock signals for both write and memory clock pins (K/K# clocks) to latch data and address, and command signals. The clocks must be part of the DQS/DQ group in this case.

The DQS and DQ pin locations are fixed in the pin table. Memory interface circuitry is available in every HardCopy III I/O bank. All memory interface pins support the I/O standards required to support DDR3, DDR2, DDR SDRAM, QDRII+, QDRII SRAM, and RLDRAM II devices.

HardCopy III devices support DQS and DQ signals with DQ bus modes of x4, x8/x9, x16/x18, or x32/x36, although not all devices support DQS bus mode x32/x36. When any of these pins are not used for memory interfacing, you can use them as user I/Os. In addition, you can use any DQSn or CQn pin not used for clocking as DQ (data) pins. Table 7–2 lists pin support per DQS/DQ bus mode, including the DQS and DQSn/CQn pin pair.

Table 7–2. DQS/DQ Bus Mode Pins for HardCopy III Devices ***(Note 1)***, ***(2)***, ***(3)***, ***(4)***, ***(5)***

Mode	DQSn Support	CQn Support	Parity or DM (Optional)	QVLD (Optional)	Typical Number of Data Pins per Group	Maximum Number of Data Pins per Group
x4	Yes	No	No	No	4	5
x8/x9	Yes	Yes	Yes	Yes	8 or 9	11
x16/x18	Yes	Yes	Yes	Yes	16 or 18	23
x32/x36	Yes	Yes	Yes	Yes	32 or 36	47

Notes to Table 7–2:

(1) The QVLD pin is not used in the ALTMEMPHY megafunction.

(2) This represents the maximum number of DQ pins (including parity, data mask, and QVLD pins) connected to the DQS bus network with single-ended DQS signaling. When you use differential or complementary DQS signaling, the maximum number of data per group decreases by one. This number may vary per DQS/DQ group in a particular device. Check the pin table for the accurate number per group.

(3) Two x4 DQS/DQ groups are stitched to make a x8/x9 group, so there are a total of 12 pins in this group.

(4) Four x4 DQS/DQ groups are stitched to make a x16/x18 group.

(5) Eight x4 DQS/DQ groups are stitched to make a x32/x36 group.

You can also use DQS/DQSn pins in some of the x4 groups as R_{UP}/R_{DN} pins (listed in the pin table). You cannot use a x4 DQS/DQ group for memory interfaces if any of its pin members are being used as R_{UP} and R_{DN} pins for OCT calibration. You may use the x8/x9 group that includes this x4 DQS/DQ group, if either of the following circumstances apply:

- You are not using DM pins with your differential DQS pins
- You are not using complementary or differential DQS pins

You can do this because a DQS/DQ x8/x9 group is comprised of 12 pins, as the groups are formed by stitching two DQS/DQ groups in x4 mode with six total pins each (Table 7–2). A typical x8 memory interface contains 10 pins, consisting of one DQS, one DM, and eight DQ pins. If you choose your pin assignment carefully, you can use the two extra pins for R_{UP} and R_{DN}. In a DDR3 SDRAM interface, you must use differential DQS, which means that you only have one extra pin. In this case, pick different pin locations for the R_{UP} and R_{DN} pins (for example, in the bank that contains the address and command pins).

You cannot use the R_{UP} and R_{DN} pins shared with DQS/DQ group pins when using x9 QDRII+/QDRII SRAM devices, as the R_{UP} and R_{DN} pins have a dual purpose with the CQn pins. In this case, pick different pin locations for the R_{UP} and R_{DN} pins to avoid conflict with memory interface pin placement. You have the choice of placing the R_{UP} and R_{DN} pins in the data-write group or in the same bank as the address and command pins. There is no restriction for using x16/x18 or x32/x36 DQS/DQ groups that include the x4 groups in which the pin members are used as R_{UP} and R_{DN} pins. These groups contain enough extra pins that they can be used as DQS pins.

You must pick your DQS and DQ pins manually for the ×8/×9, ×16/×18, or ×32/×36 DQS/DQ group in which the members are used for R_{UP} and R_{DN}. Otherwise, the Quartus II software might not be able to place these pins correctly if there are no specific pin assignments and might give you a "no-fit" error instead.

Table 7–3 lists the maximum number of DQS/DQ groups per side of the HardCopy III device.

Table 7–3. Number of DQS/DQ Groups in HardCopy III Devices per Side

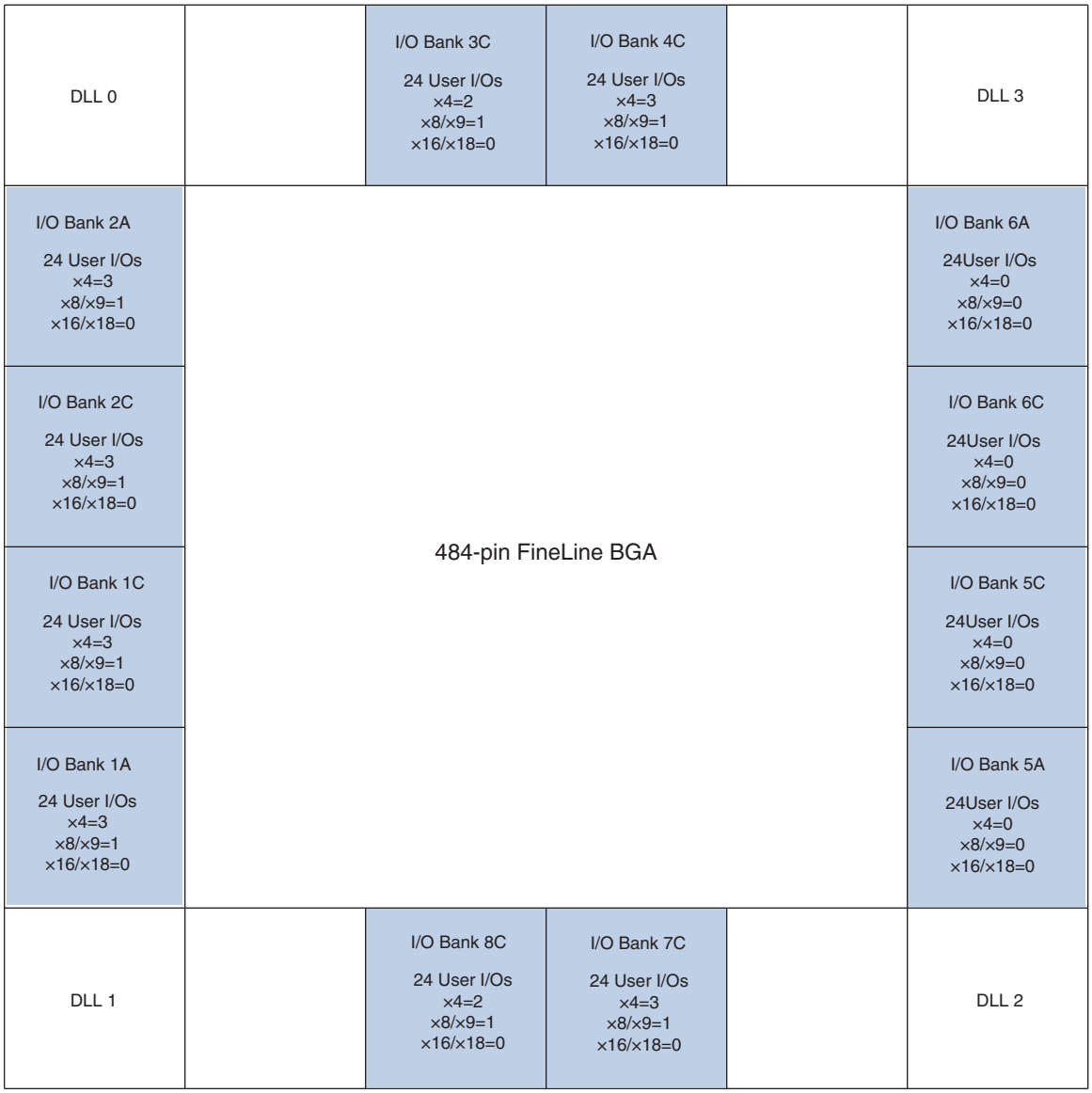
Device	Package	Side	x4 *(1)*	x8/x9	x16/x18	x32/x36
HC325W HC325F	484-pin FineLine BGA	Left	12	4	0	0
		Bottom	5	2	0	0
		Right	12	4	0	0
		Top	5	2	0	0
	780-pin FineLine BGA	Left	14	6	2	0
		Bottom	17	8	2	0
		Right	14	6	2	0
		Top	17	8	2	0
HC335L HC335F	FineLine BGA 1152-pin	Left	26	12	4	0
		Bottom	26	12	4	0
		Right	26	12	4	0
		Top	26	12	4	0
	1517-pin FineLine BGA	Left	26	12	4	0
		Bottom	38	18	8	4
		Right	26	12	4	0
		Top	38	18	8	4

Note to Table 7–3:

(1) In some x4 groups, DQS/DQ pins can also be used as R_{UP}/R_{DN} pins. You cannot use these x4 groups if the pins are used as R_{UP} and R_{DN} pins for OCT calibration. Make sure that the DQS/DQ groups that you chose are not also used for OCT calibration.

Figure 7–3 through Figure 7–6 show the number of DQS/DQ groups available per bank in each HardCopy III device. These figures present the package-bottom view of the specified HardCopy III devices.

Figure 7–3. Number of DQS/DQ Groups per Bank in HC4E25W and HC325F Devices in a 484-pin FineLine BGA Package *(Note 1)*, *(2)*

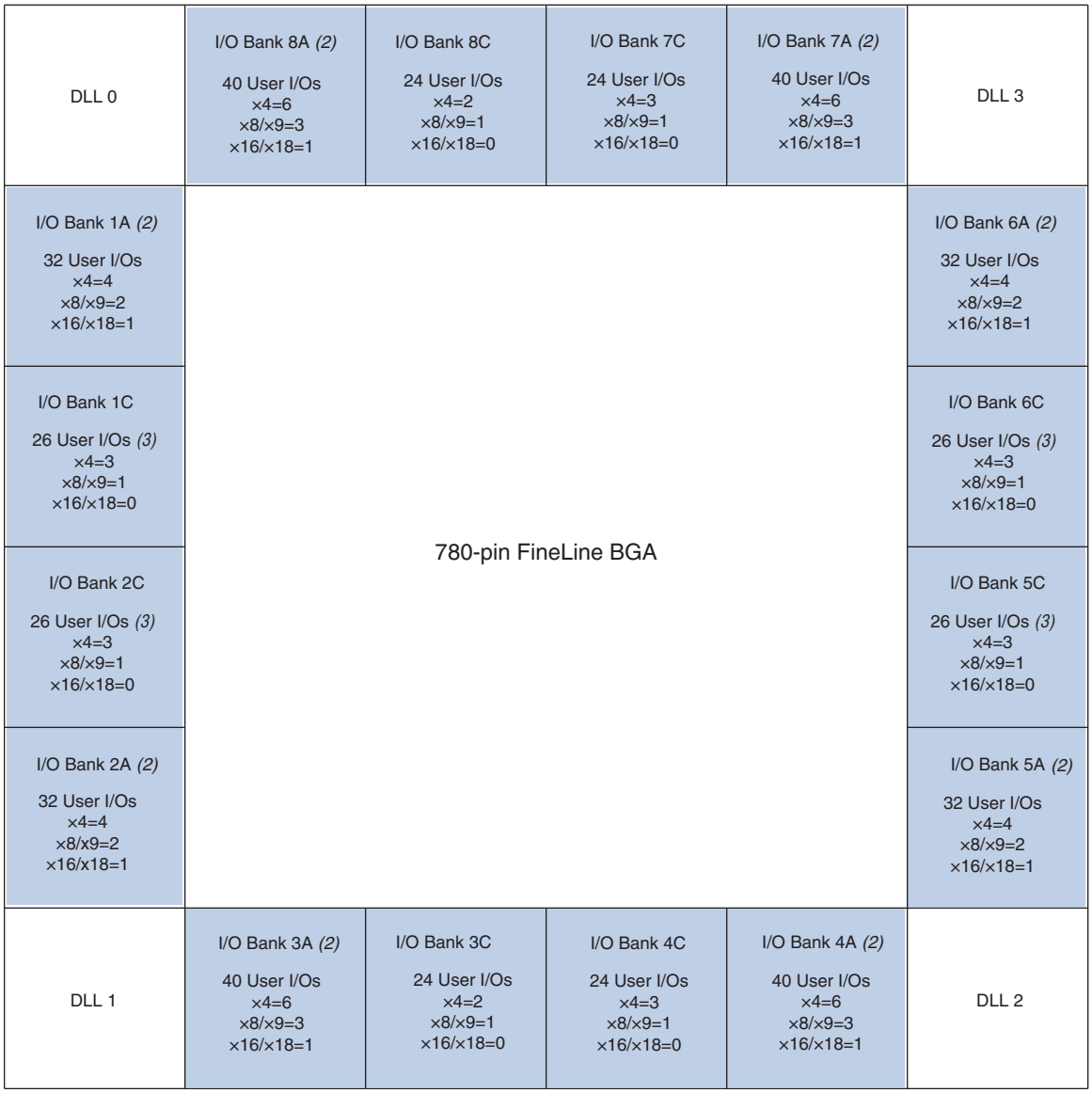


Notes to Figure 7–3:

(1) These devices do not support ×32/×36 mode.

(2) All I/O pin counts include eight dedicated clock inputs (`CLK1p`, `CLK1n`, `CLK3p`, `CLK3n`, `CLK8p`, `CLK8n`, `CLK10p`, and `CLK10n`).

Figure 7–4. Number of DQS/DQ Groups per Bank in HC325W and HC325F Devices in a 780-pin FineLine BGA Package *(Note 1)*



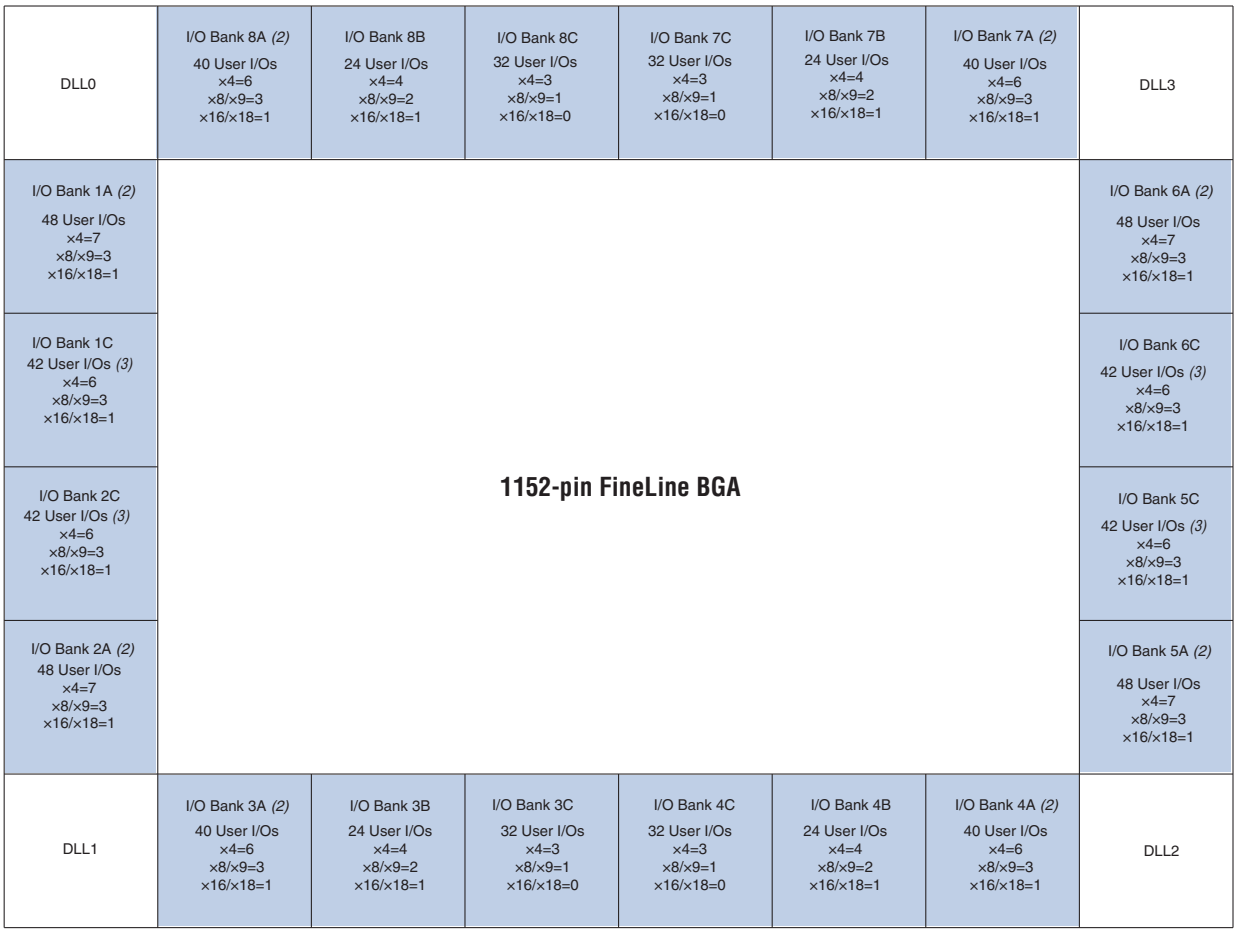
Notes to Figure 7–4:

(1) These devices do not support ×32/×36 mode.

(2) You can use DQS/DQSn pins in some of the ×4 groups as R_{UP}/R_{DN} pins. You cannot use a ×4 group for memory interfaces if two pins in the group are used as R_{UP} and R_{DN} pins for OCT calibration. You can still use the ×16/×18 groups, including the ×4 groups. However, there are restrictions on using ×8/×9 groups that include these ×4 groups.

(3) All I/O pin counts include eight dedicated clock inputs (`CLK1p`, `CLK1n`, `CLK3p`, `CLK3n`, `CLK8p`, `CLK8n`, `CLK10p`, and `CLK10n`).

Figure 7–5. Number of DQS/DQ Groups per Bank in HC335L and HC335F Devices in a 1152-pin FineLine BGA Package *(Note 1)*



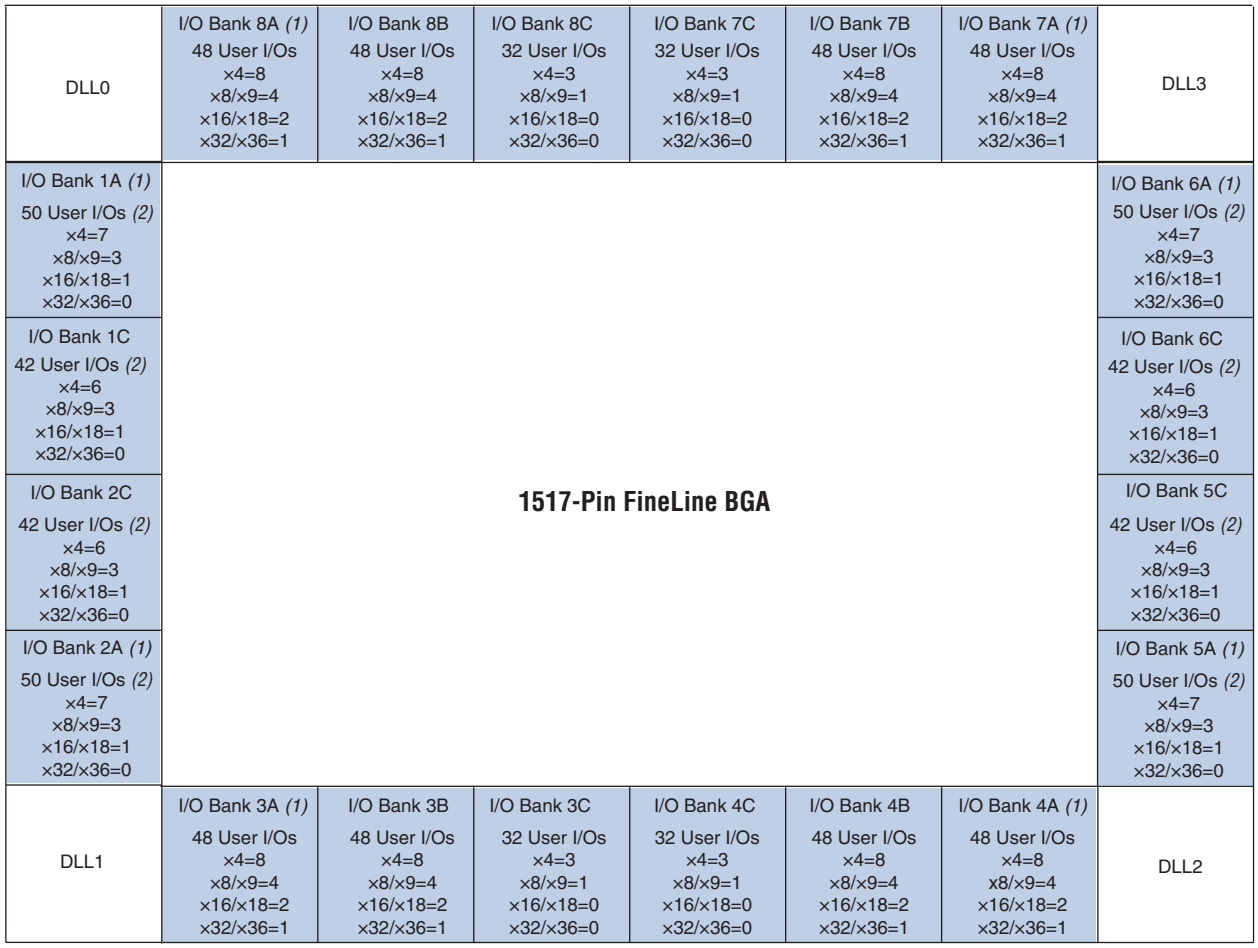
Notes to Figure 7–5:

(1) These devices do not support ×32/×36 mode.

(2) You can use DQS/DQSn pins in some of the ×4 groups as R_{UP}/R_{DN} pins. You cannot use a ×4 group for memory interfaces if two pins in the group are used as R_{UP} and R_{DN} pins for OCT calibration. You can still use the ×16/×18 groups including the ×4 groups. However, there are restrictions on using ×8/×9 groups that include these ×4 groups.

(3) All I/O pin counts include eight dedicated clock inputs (`CLK1p`, `CLK1n`, `CLK3p`, `CLK3n`, `CLK8p`, `CLK8n`, `CLK10p`, and `CLK10n`).

Figure 7–6. Number of DQS/DQ Groups per Bank in HC335L and HC335F Devices in a 1517-pin FineLine BGA Package



Notes to Figure 7–6:

(1) You can use DQS/DQSn pins in some of the ×4 groups as R_{UP}/R_{DN} pins. You cannot use a ×4 group for memory interfaces if two pins in the group are used as R_{UP} and R_{DN} pins for OCT calibration. You can still use the ×16/×18 or ×32/×36 groups including the ×4 groups. However, there are restrictions on using ×8/×9 groups that include these ×4 groups.

(2) All I/O pin counts include eight dedicated clock inputs (`CLK1p`, `CLK1n`, `CLK3p`, `CLK3n`, `CLK8p`, `CLK8n`, `CLK10p`, and `CLK10n`) and eight dedicated corner PLL clock inputs (`PLL_L1_CLKp`, `PLL_L1_CLKn`, `PLL_L4_CLKp`, `PLL_L4_CLKn`, `PLL_R4_CLKp`, `PLL_R4_CLKn`, `PLL_R1_CLKp`, and `PLL_R1_CLKn`) that can be used for data inputs.

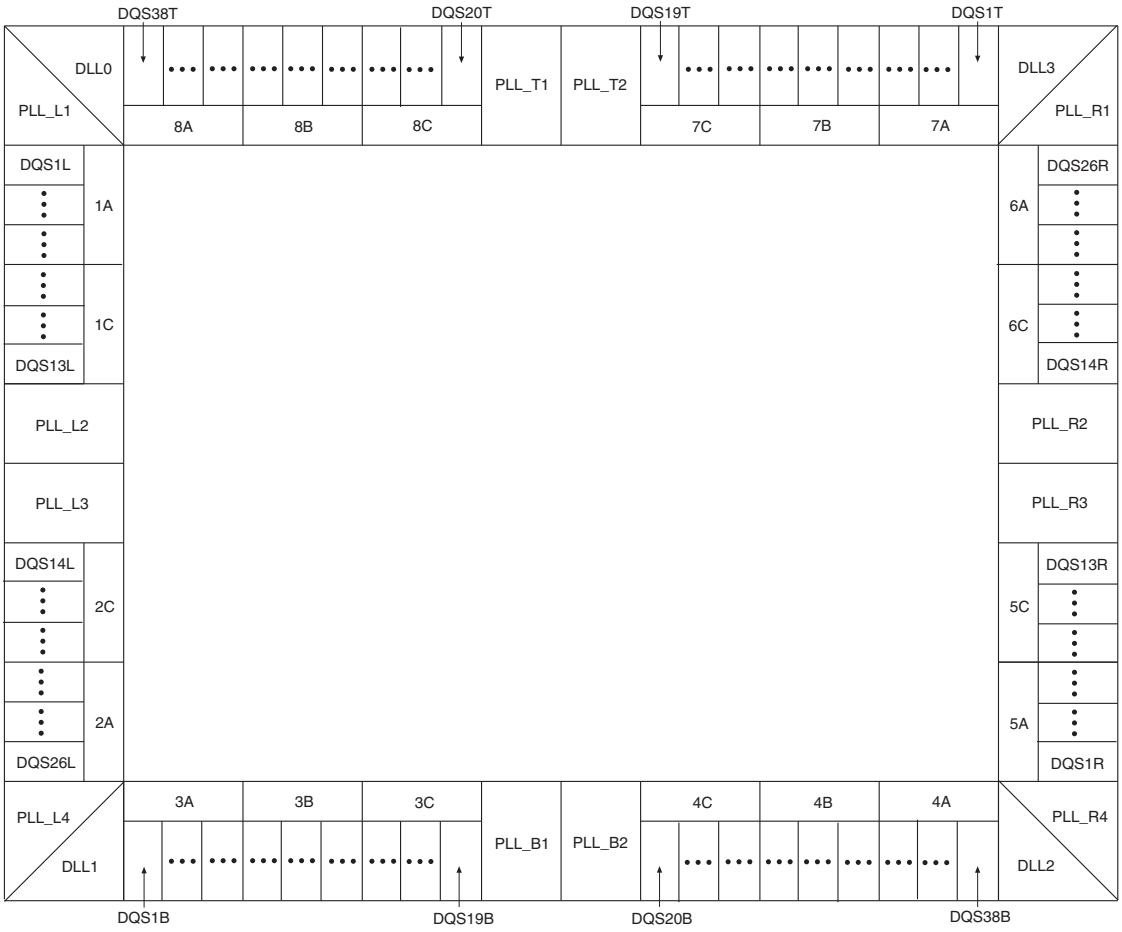
The DQS and DQSn pins are listed in the HardCopy III pin tables as DQSXY and DQSnXY, respectively, where X denotes the DQS/DQ grouping number, and Y denotes whether the group is located on the top (T), bottom (B), left (L), or right (R) side of the device.

The corresponding DQ pins are marked as DQXY, where X indicates which DQS group the pins belong to and Y indicates whether the group is located on the top (T), bottom (B), left (L), or right (R) side of the device. For example, `DQS1L` indicates a DQS pin, located on the left side of the device, as shown in Figure 7–7. The DQ pins belonging to that group are shown as `DQ1L` in the pin table.

Figure 7–7 show how the DQS/DQ groups are numbered in a package-bottom view of the device. The numbering scheme starts from the top left side of the device going counter-clockwise. The top and bottom sides of the HardCopy III device can contain up to 38 x4 DQS/DQ groups; the left and right sides of the device can contain up to 26 x4 DQS/DQ groups.

The parity, DM, BWSn, ECC, and QVLD pins are shown as DQ pins in the pin table. When not used as memory interface pins, these pins are available as regular I/O pins.

Figure 7–7. DQS Pins in HardCopy III E I/O Banks



The DQ pin numbering is based on ×4 mode. In ×4 mode, there are up to eight DQS/DQ groups per I/O bank. Each ×4 mode DQS/DQ group consists of a DQS pin, a DQSn pin, and four DQ pins. In ×8/×9 mode, the I/O bank combines two adjacent ×4 DQS/DQ groups; one pair of DQS and DQSn/CQn pins can drive all the DQ and parity pins in the new combined group that consists of up to 10 DQ pins (including parity or DM and QVLD pins) and a pair of DQS and DQSn/CQn pins. Similarly, in ×16/×18 mode, the I/O bank combines four adjacent ×4 DQS/DQ groups to create a group with a maximum of 19 DQ pins (including parity or DM and QVLD pins) and a pair of DQS and DQSn/CQn pins. In ×32/×36 mode, the I/O bank combines eight adjacent ×4 DQS/DQ groups together to create a group with a maximum of 37 DQ pins (including parity or DM and QVLD pins) and a pair of DQS and DQSn/CQn pins.

HardCopy III modular I/O banks allow easy formation of the DQS/DQ groups. If all the pins in the I/O banks are user I/O pins and are not used for R_{UP}/R_{DN} OCT calibration or PLL clock output pins, you can divide the number of I/O pins in the bank by six to get the maximum possible number of x4 groups. You can then divide that number by two, four, or eight to get the maximum possible number of x8/x9, x16/x18, or x32/x36, respectively, as listed in Table 7–4. However, some of the pins in the I/O bank may be used for other functions.

Table 7–4. DQ/DQS Group in HardCopy III Modular I/O Banks

Modular I/O Bank Size *(1)*	Maximum Possible Number of x4 Groups	Maximum Possible Number of x8/x9 Groups	Maximum Possible Number of x16/x18 Groups	Maximum Possible Number of x32/x36 Groups
24 pins	4 *(2)*	2	1	0
32 pins	5 *(3)*	2	1	0
40 pins	6	3	1	0
48 pins	8	4	2	1

Notes to Table 7–4:

(1) This I/O pin count does not include dedicated clock inputs or the dedicated corner PLL clock inputs.

(2) Some of the x4 groups may use the R_{UP} and R_{DN} pins. You cannot use these groups if you use the HardCopy III calibrated OCT feature.

(3) The actual maximum number of x4 groups for an I/O bank with 32 pins is four in the HardCopy III devices.

Optional Parity, DM, BWSn, ECC, and QVLD Pins

You can use any DQ pin from the same DQS/DQ group for data as parity pins in HardCopy III devices. The HardCopy III device family supports parity in the x8/x9, x16/x18, and x32/x36 modes. There is one parity bit available per eight bits of data pins. Use any of the DQ (or D) pins in the same DQS/DQ group as data for parity because parity bits are treated, set, and generated similar to a DQ pin.

DM pins are only required when writing to DDR3, DDR2, DDR SDRAM, and RLDRAM II devices. QDRII+ and QDRII SRAM devices use the `BWSn` signal to select which byte to write into the memory. A low on the `DM` or `BWSn` signals indicates the write is valid. If the `DM` or `BWSn` signal is high, the memory masks the DQ signals. If the system does not require write data masking, connect the memory DM pins low to indicate every write data is valid. You can use any of the DQ pins in the same DQS/DQ group as write data for the `DM` or `BWSn` signals.

Each group of DQS and DQ signals in DDR3, DDR2, and DDR SDRAM devices requires a DM pin. There is one DM pin per RLDRAM II device and one BWSn pin per nine bits of data in x9, x18, and x36 QDRII+/QDRII SRAM. The ×8 QDRII SRAM device has two BWSn pins per eight data bits, which are referred to as the NWSn pins. Generate the DM or `BWSn` signals using DQ pins and configure the signals similarly to the DQ (or D) output signals. HardCopy III devices do not support the `DM` signal in x4 DDR3 SDRAM or in x4 DDR2 SDRAM interfaces with differential DQS signaling.

Some DDR3, DDR2, and DDR SDRAM devices or modules support error correction coding (ECC), which is a method of detecting and automatically correcting errors in data transmission. In 72-bit DDR3, DDR2, or DDR SDRAM interfaces, the typical eight ECC pins are used in addition to the 64 data pins. Connect the DDR3, DDR2, and DDR SDRAM ECC pins to a HardCopy III device DQS/DQ group. These signals are also generated similar to DQ pins. The memory controller requires encoding and decoding logic for the ECC data. You can also use the extra byte of data for other error checking methods.

QVLD pins are used in RLDRAM II and QDRII+ SRAM interfaces to indicate the read data availability. There is one QVLD pin per memory device. A high on the QVLD pin indicates that the memory is outputting the data requested. Similar to DQ inputs, this signal is edge-aligned with the read clock signals (CQ/CQn in QDRII+/QDRII SRAM and QK/QK# in RLDRAM II) and is sent half-a-clock cycle before data starts from the memory. The QVLD pin is not used in the ALTMEMPHY solution for QDRII+ SRAM.

For more information about the parity, ECC, and QVLD pins, and when these pins are treated as DQ pins, refer to "Data and Data Clock/Strobe Pins" on page 7–4.

Address and Control/Command Pins

Address and control/command signals are typically sent at single data rate. The only exception is in QDRII SRAM burst-of-two devices, in which case the read address must be captured on the rising edge of the clock and the write address must be captured on the falling edge of the clock by the memory. There is no special circuitry required for the address and control/command pins. You can use any of the user I/O pins in the same I/O bank as the data pins.

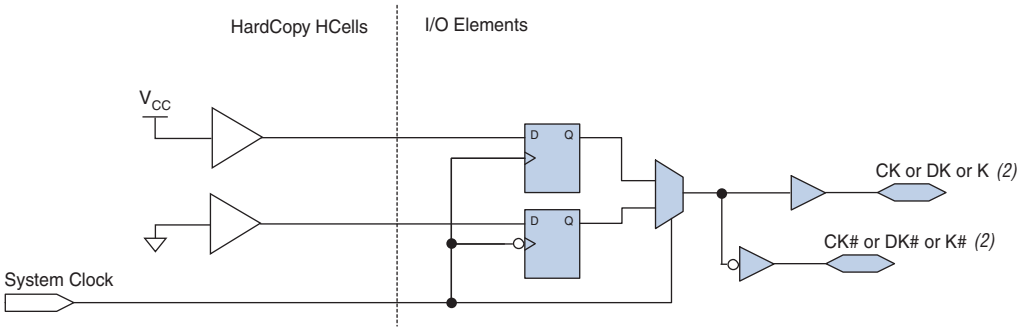
Memory Clock Pins

In addition to DQS (and CQn) signals to capture data, DDR3, DDR2, DDR SDRAM, and RLDRAM II use an extra pair of clocks, called CK and CK# signals, to capture the address and control/command signals. The CK and CK# signals must be generated to mimic the write data-strobe using HardCopy III DDR I/O registers (DDIOs) to ensure that the timing relationships between the CK, CK#, and DQS signals (tDQSS in DDR3, DDR2, and DDR SDRAM or tCKDK in RLDRAM II) are met. QDRII+ and QDRII SRAM devices use the same clock (K/K#) to capture the data, address, and control/command signals.

Memory clock pins in HardCopy III devices are generated using a DDIO register going to differential output pins, marked in the pin table with DIFFOUT, DIFFIO_TX, and DIFFIO_RX prefixes. For more information about which pins to use for memory clock pins, refer to Table 7–2 on page 7–6.

Figure 7–8 shows memory clock generation for HardCopy III devices.

Figure 7–8. Memory Clock Generation Block Diagram ***(Note 1)***



Notes to Figure 7–8:

(1) For the pin location requirements for these pins, refer to Table 7–1 on page 7–4.

(2) The `mem_clk[0]` and `mem_clk_n[0]` pins for DDR3, DDR2, and DDR SDRAM interfaces use the I/O input buffer for feedback. For memory interfaces using a differential DQS input, the input feedback buffer is configured as differential input; for memory interfaces using a single-ended DQS input, the input buffer is configured as a single-ended input. Using a single-ended input feedback buffer requires that V_{REF} is provided to that I/O bank's `VREF` pins.

HardCopy III External Memory Interface Features

HardCopy III devices are rich with features that allow robust high-performance external memory interfacing. The ALTMEMPHY megafunction allows you to set these external memory interface features and helps set up the physical interface (PHY) best suited for your system.

This section describes each HardCopy III device feature that is used in external memory interfaces from the DQS phase-shift circuitry, DQS logic block, leveling multiplexers, dynamic OCT control block, IOE registers, IOE features, and the PLL.

When using the Altera® memory controller MegaCore® functions, the PHY is instantiated for you.

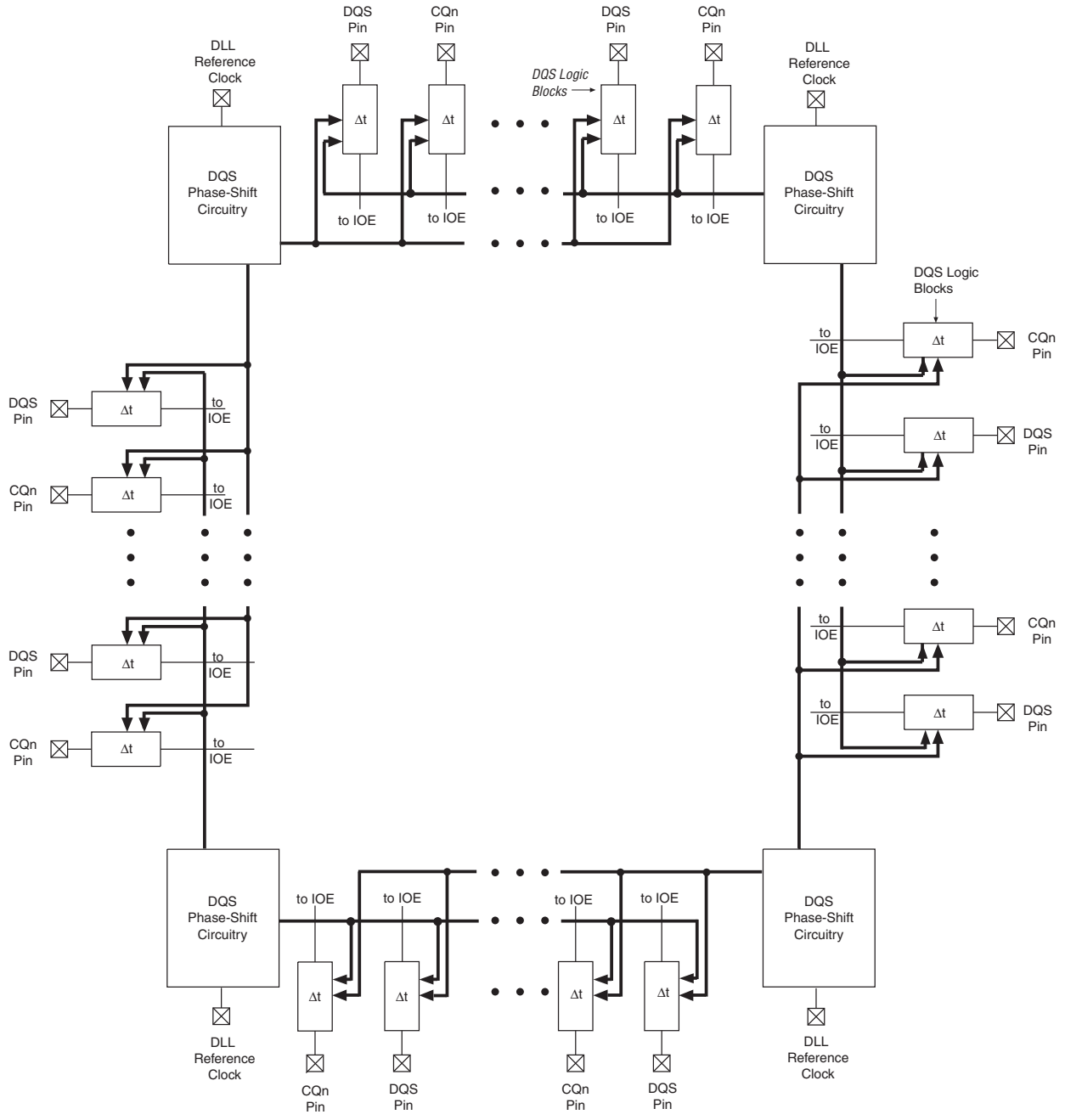
The ALTMEMPHY megafunction and the Altera memory controller MegaCore functions can run at half the frequency of the I/O interface of the memory devices to allow better timing management in high-speed memory interfaces. HardCopy III devices have built-in registers to convert data from full-rate (I/O frequency) to half-rate (controller frequency) and vice versa. You can bypass these registers if your memory controller is not running at half the rate of the I/O frequency.

For more information about the ALTMEMPHY megafunction, refer to the *External Memory Interface Handbook*.

DQS Phase-Shift Circuitry

The HardCopy III phase-shift circuitry provides phase shift to the DQS and CQn pins on read transactions when the DQS and CQn pins are acting as input clocks or strobes to the HardCopy III device. The DQS phase-shift circuitry consists of DLLs that are shared between multiple DQS pins and the phase-offset module to further fine-tune the DQS phase shift for different sides of the device. Figure 7–9 shows how the DQS phase-shift circuitry is connected to the DQS and CQn pins in the device.

Figure 7–9. DQS and CQn Pins and DQS Phase-Shift Circuitry



The DQS phase-shift circuitry is connected to the DQS logic blocks that control each DQS or CQn pin. The DQS logic blocks allow the DQS delay settings to be updated concurrently at every DQS or CQn pin.

DLL

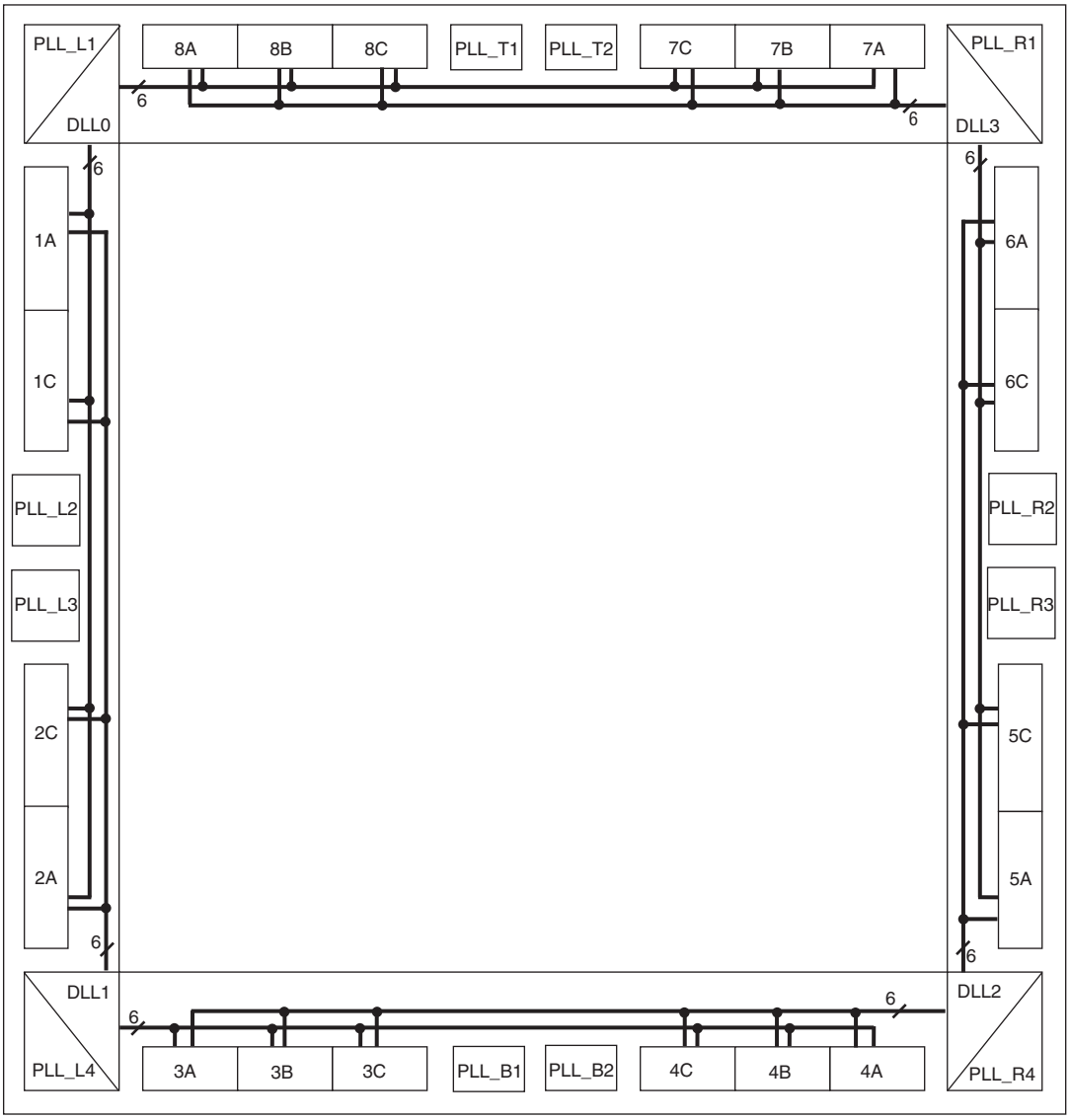
DQS phase-shift circuitry uses a DLL to dynamically measure the clock period required by the DQS/CQn pin. The DLL, in turn, uses a frequency reference to generate dynamically controlled signals for the delay chains in each of the DQS and CQn pins, allowing it to compensate for PVT variations. The DQS delay settings are Gray-coded to reduce jitter when the DLL updates the settings. The phase-shift circuitry requires a maximum of 1,280 clock cycles to calculate the correct input clock period. Do not send data during these clock cycles because there is no guarantee that it will be captured properly. Because the settings from the DLL may not be stable until this lock period has elapsed, anything using these settings (including the leveling delay system) may be unstable during this period.

You can still use the DQS phase-shift circuitry for any memory interfaces that are less than 100 MHz. The DQS signal is shifted by 2.5 ns. Even if the DQS signal is not shifted exactly to the middle of the DQ valid window, the IOE must be able to capture the data in low frequency applications where a large amount of timing margin is available.

There are four DLLs in a HardCopy III device, located in each corner of the device. These four DLLs can support a maximum of four unique frequencies, with each DLL running at one frequency. Each DLL can have two outputs with different phase offsets, allowing one HardCopy III device to have eight different DLL phase shift settings. Figure 7–10 shows the DLL and I/O bank locations in HardCopy III devices, from a package-bottom view.

Altera recommends enabling the PLL reconfiguration feature and the DLL phase offset feature (DLL reconfiguration) for HardCopy III devices. Because HardCopy III devices are mask programmed, they cannot be changed after the silicon is fabricated. By implementing these two features, you can perform timing adjustments to improve or resolve timing issues after the silicon is fabricated.

Figure 7–10. HardCopy III DLL and I/O Bank Locations (Package-Bottom View)



The DLL can access the two adjacent sides from its location within the device. For example, DLL0 on the top left of the device can access the top side (I/O banks 7A, 7B, 7C, 8A, 8B, and 8C) and the left side of the device (I/O banks 1A, 1C, 2A, and 2C). This means that each I/O bank is accessible by two DLLs, giving more flexibility to create multiple frequencies and multiple-types interfaces. For example, you can design an interface spanning one side of the device or two sides adjacent to the DLL. The DLL outputs the same DQS delay settings for both sides of the device adjacent to the DLL.

Interfaces that span across two sides of the device are not recommended for high-performance memory interface applications.

Each bank can use settings from either or both DLLs of the adjacent bank. For example, DQS1L can use phase-shift settings from DLL0, and DQS2L can use phase-shift settings from DLL1. Table 7–5 lists the DLL location and supported I/O banks for HardCopy III devices.

You can only have one memory interface in I/O banks with the same I/O bank number (such as I/O banks 1A and 1C) when you use the leveling delay chains because there is only one leveling delay chain shared by these I/O banks.

Table 7–5. DLL Location and Supported I/O Banks

DLL	Location	Accessible I/O Banks
DLL0	Top left corner	1A, 1C, 2A, 2C, 7A, 7B, 7C, 8A, 8B, 8C
DLL1	Bottom left corner	1A, 1C, 2A, 2C, 3A, 3B, 3C, 4A, 4B, 4C
DLL2	Bottom right corner	3A, 3B, 3C, 4A, 4B, 4C, 5A, 5C, 6A, 6C
DLL3	Top right corner	5A, 5C, 6A, 6C, 7A, 7B, 7C, 8A, 8B, 8C

The reference clock for each DLL may come from the PLL output clocks or any of the two dedicated clock input pins located in either side of the DLL. Table 7–6 through Table 7–8 show the available DLL reference clock input resources for HardCopy III devices.

Table 7–6. DLL Reference Clock Input for HC325W, and HC325F Devices

DLL	CLKIN (Top/Bottom)	CLKIN (Left/Right)	PLL (Top/Bottom)	PLL (Left/Right)
DLL0	CLK12P, CLK13P, CLK14P, CLK15P	CLK0P, CLK1P, CLK2P, CLK3P	PLL_T1	PLL_L2
DLL1	CLK4P, CLK5P, CLK6P, CLK7P	CLK0P, CLK1P, CLK2P, CLK3P	PLL_B1	PLL_L2
DLL2	CLK4P, CLK5P, CLK6P, CLK7P	CLK8P, CLK9P, CLK10P, CLK11P	PLL_B1	PLL_R2
DLL3	CLK12P, CLK13P, CLK14P, CLK15P	CLK8P, CLK9P, CLK10P, CLK11P	PLL_T1	PLL_R2

Table 7–7. DLL Reference Clock Input for HC335L and HC335F with F1152-Pin Package Devices

DLL	CLKIN (Top/Bottom)	CLKIN (Left/Right)	PLL (Top/Bottom)	PLL (Left/Right)
DLL0	CLK12P, CLK13P, CLK14P, CLK15P	CLK0P, CLK1P, CLK2P, CLK3P	PLL_T1	PLL_L2
DLL1	CLK4P, CLK5P, CLK6P, CLK7P	CLK0P, CLK1P, CLK2P, CLK3P	PLL_B1	PLL_L3
DLL2	CLK4P, CLK5P, CLK6P, CLK7P	CLK8P, CLK9P, CLK10P, CLK11P	PLL_B2	PLL_R3
DLL3	CLK12P, CLK13P, CLK14P, CLK15P	CLK8P, CLK9P, CLK10P, CLK11P	PLL_T2	PLL_R2

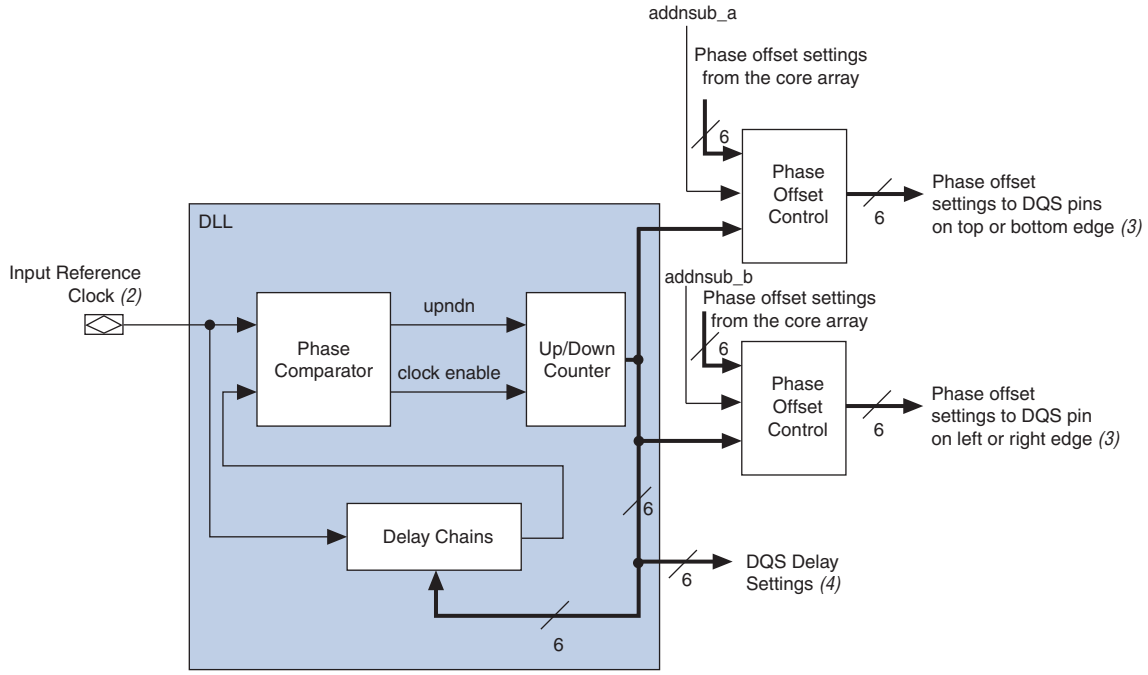
Table 7–8. DLL Reference Clock Input for HC335L and HC335F with F1517-Pin Package Devices

DLL	CLKIN (Top/Bottom)	CLKIN (Left/Right)	PLL (Top/Bottom)	PLL (Left/Right)
DLL0	CLK12P, CLK13P, CLK14P, CLK15P	CLK0P, CLK1P, CLK2P, CLK3P	PLL_T1	PLL_L1, PLL_L2
DLL1	CLK4P, CLK5P, CLK6P, CLK7P	CLK0P, CLK1P, CLK2P, CLK3P	PLL_B1	PLL_L3, PLL_L4
DLL2	CLK4P, CLK5P, CLK6P, CLK7P	CLK8P, CLK9P, CLK10P, CLK11P	PLL_B2	PLL_R3, PLL_R4
DLL3	CLK12P, CLK13P, CLK14P, CLK15P	CLK8P, CLK9P, CLK10P, CLK11P	PLL_T2	PLL_R1, PLL_R2

When you have a dedicated PLL that only generates the DLL input reference clock, set the PLL mode to **No Compensation**; otherwise, the Quartus II software changes it automatically. Because the PLL does not use any other outputs, it does not have to compensate for any clock paths.

Figure 7–11 shows a block diagram of the DLL. The input reference clock goes into the DLL to a chain of up to 16 delay elements. The phase comparator compares the signal coming out of the end of the delay chain block to the input reference clock. The phase comparator then issues the `upndn` signal to the Gray-code counter. This signal increments or decrements a six-bit delay setting (DQS delay settings) that increases or decreases the delay through the delay element chain to bring the input reference clock and the signals coming out of the delay element chain in phase.

Figure 7–11. Simplified Diagram of the DQS Phase Shift Circuitry ***(Note 1)***



Notes to Figure 7–11:

(1) All features of the DQS phase-shift circuitry are accessible from the ALTMEMPHY MegaWizard Plug-In Manager in the Quartus II software.

(2) For exact PLL and input clock pin information, the input reference clock for the DQS phase-shift circuitry can come from a PLL output clock or an input clock pin. For more information, refer to Table 7–6 through Table 7–8.

(3) Phase offset settings can go only to the DQS logic blocks.

(4) DQS delay settings can go to the core array, the DQS logic block, and the leveling circuitry.

The DLL can be reset from either the core array or a user I/O pin. Each time the DLL is reset, you must wait for 1,280 clock cycles before you can capture the data properly.

Depending on the DLL frequency mode, the DLL can shift the incoming DQS signals by 0°, 22.5°, 30°, 36°, 45°, 60°, 67.5°, 72°, 90°, 108°, 120°, 135°, 144°, or 180°. The shifted DQS signal is then used as the clock for the DQ IOE input registers.

All DQS and CQn pins referenced to the same DLL can have their input signal phase shifted by a different degree amount, but all must be referenced at one particular frequency. For example, you can have a 90° phase shift on DQS1T and a 60° phase shift on DQS2T referenced from a 200-MHz clock. However, not all phase-shift combinations are supported. The phase shifts on the DQS pins referenced by the same DLL must all be a multiple of 22.5° (up to 90°), a multiple of 30° (up to 120°), a multiple of 36° (up to 144°), or a multiple of 45° (up to 180°).

There are seven different frequency modes for the HardCopy III DLL, as shown in Table 7–9. Each frequency mode provides different phase shift selections. In frequency modes 0, 1, 2, and 3, the 6-bit DQS delay settings vary with PVT to implement the phase-shift delay. In frequency modes 4, 5, and 6, only 5 bits of the DQS delay settings vary to implement the phase-shift delay; the MSB of the DQS delay setting is set to 0.

For the frequency range of each mode, refer to the *DC and Switching Characteristics of HardCopy III Devices* chapter.

Table 7–9. DLL Frequency Modes in HardCopy III Devices

Frequency Mode	DQS Delay Setting Bus Width	Available Phase Shift	Number of Delay Chains
0	6 bits	22.5°, 45°, 67.5°, 90°	16
1	6 bits	30°, 60°, 90°, 120°	12
2	6 bits	36°, 72°, 108°, 144°	10
3	6 bits	45°, 90°, 135°, 180°	8
4	5 bits	30°, 60°, 90°, 120°	12
5	5 bits	36° 72°, 108°, 144°	10
6	5 bits	45°, 90°, 135°, 180°	8

For the 0° shift, the DQS signal bypasses both the DLL and the DQS logic blocks. The Quartus II software automatically sets the DQ input delay chains so that the skew between the DQ and DQS pin at the DQ IOE registers is negligible when the 0° shift is implemented. You can feed the DQS delay settings to the DQS logic block and the core array.

The shifted DQS signal goes to the DQS bus to clock the IOE input registers of the DQ pins. The signal can also go into the core array for resynchronization if you are not using the IOE resynchronization registers. The shifted CQn signal can only go to the negative-edge input register in the DQ IOE and is only used for QDRII+ and QDRII SRAM interfaces.

Phase Offset Control

Each DLL has two phase-offset modules and can provide two separate DQS delay settings with independent offset, one for the top and bottom I/O banks and one for the left and right I/O banks, so you can fine-tune the DQS phase shift settings between two different sides of the device. Even though you have an independent phase offset control, the frequency of the interface using the same DLL must be the same. Use the phase offset control module for making small shifts to the input signal

and use the DQS phase-shift circuitry for larger signal shifts. For example, if the DLL only offers a multiple of a 30° phase shift, but your interface requires a 67.5° phase shift on the DQS signal, you can use two delay chains in the DQS logic blocks to give you a 60° phase shift and use the phase offset control feature to implement the extra 7.5° phase shift.

You can use either a static phase offset or a dynamic phase offset to implement the additional phase shift. The available additional phase shift is implemented in 2's-complement in Gray-code between settings –64 to +63 for frequency modes 0, 1, 2, and 3, and between settings –32 to +31 for frequency modes 4, 5, and 6. The DQS phase shift is the sum of the DLL delay settings and the user selected phase offset settings, which reaches a maximum at setting 64 for mode frequency modes 0, 1, 2 and 3, and a maximum at setting 32 for frequency modes 4, 5, and 6. The actual physical offset setting range is 64 or 32 subtracted by the DQS delay settings from the DLL.

You must monitor the DQS delay settings to determine how many offsets you can add and subtract in the system.

The DQS delay settings output by the DLL are also Gray-coded.

For example, if the DLL determines that a DQS delay setting of 28 is required to achieve a 30° phase shift in DLL frequency mode 1, you can subtract up to 28 phase offset settings and add up to 35 phase offset settings to achieve the optimal delay that you need. However, if the same DQS delay setting of 28 is required to achieve a 30° phase shift in DLL frequency mode 4, you can still subtract up to 28 phase offset settings, but you can only add up to 3 phase offset settings before the DQS delay settings reach their maximum settings. This is because DLL frequency mode 4 only uses 5-bit DLL delay settings.

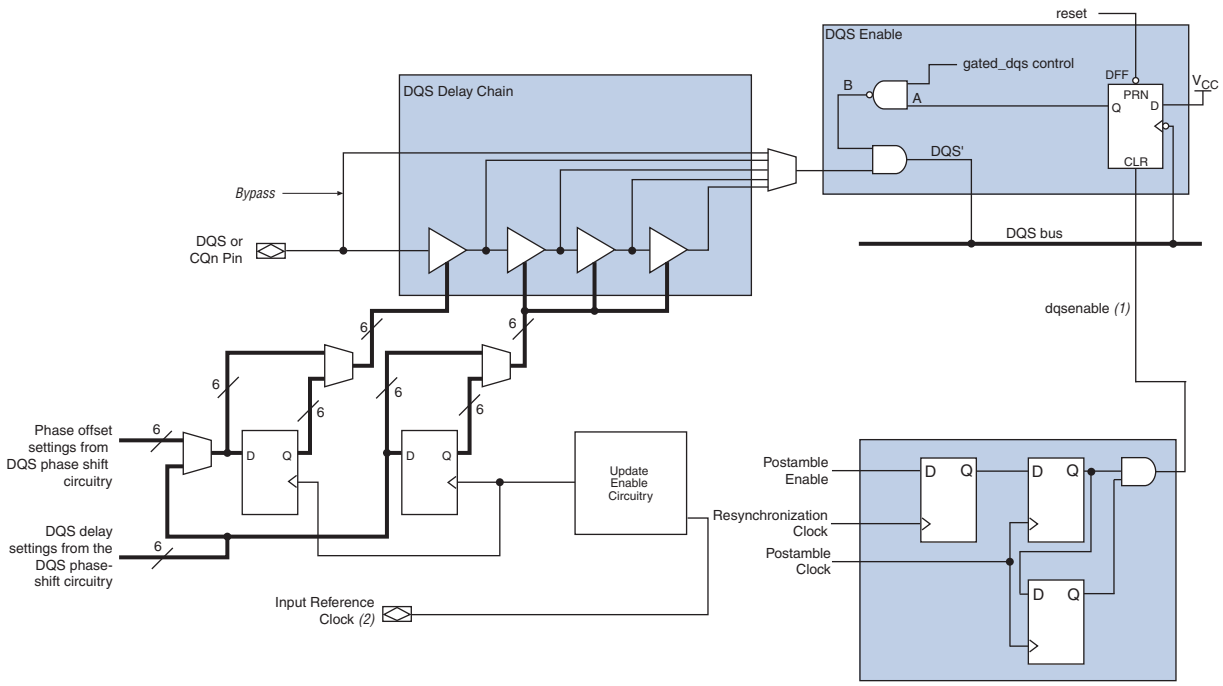
For information about the value for each step, refer to the *DC and Switching Characteristics of HardCopy III Devices* chapter.

If you use the static phase offset, specify the phase-offset amount in the ALTMEMPHY megafunction as a positive number for addition or a negative number for subtraction. You can also have a dynamic phase offset that is always added to, subtracted from, or both added to and subtracted from the DLL phase shift. When you always add or subtract, you can dynamically input the phase offset amount into the `dll_offset[5..0]` port. When you want to both add and subtract dynamically, you control the `addnsub` signal in addition to the `dll_offset[5..0]` signals.

DQS Logic Block

Each DQS and CQn pin is connected to a separate DQS logic block, which consists of the DQS delay chains, the update enable circuitry, and the DQS postamble circuitry as shown in Figure 7–12.

Figure 7–12. DQS Logic Block in HardCopy III Devices



Notes to Figure 7–12:

(1) The `dqsenable` signal can also come from the HardCopy III core fabric.

(2) The input reference clock for the DQS phase-shift circuitry can come from a PLL output clock or an input clock pin. For the exact PLL and input clock pin, refer to Table 7–6 through Table 7–8.

DQS Delay Chain

The DQS delay chains consist of a set of variable delay elements to allow the input DQS and CQn signals to be shifted by the amount specified by the DQS phase-shift circuitry or the core array. There are four delay elements in the DQS delay chain; the first delay chain closest to the DQS pin can be shifted either by the DQS delay settings or by the sum of the DQS delay setting and the phase-offset setting. The number of delay chains required is transparent to you because the ALTMEMPHY megafunction automatically sets it when you choose the operating frequency. The DQS delay settings can come from the DQS phase-shift circuitry on either end of the I/O banks or from the core array.

The delay elements in the DQS logic block have the same characteristics as the delay elements in the DLL. When the DLL does not control the DQS delay chains, you can input your own Gray-coded 6-bit or 5-bit settings using the `dqs_delayctrlin[5..0]` signals available in the ALTMEMPHY megafunction. These settings control 1, 2, 3, or all 4 delay elements in the DQS delay chains. The ALTMEMPHY megafunction can also dynamically choose the number of DQS delay chains required for the system. The amount of delay is equal to the sum of the delay element's intrinsic delay and the product of the number of delay steps and the value of the delay steps.

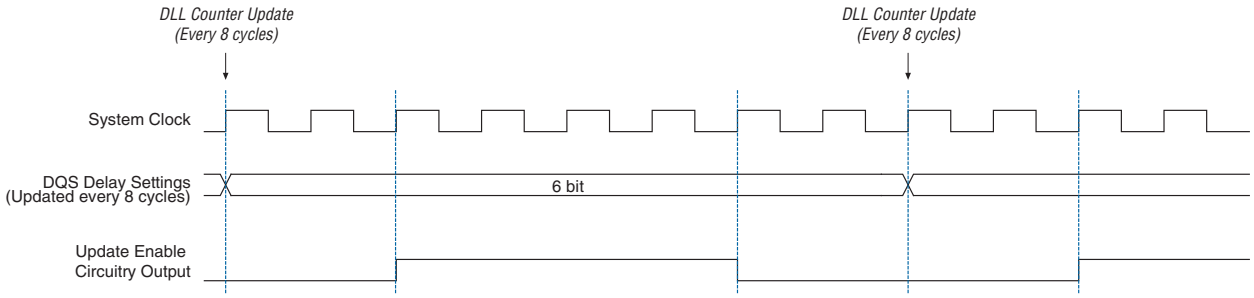
You can also bypass the DQS delay chain to achieve a 0° phase shift.

For more information about the ALTMEMPHY megafunction, refer to the *External Memory Interface Handbook*.

Update Enable Circuitry

Both the DQS delay settings and the phase-offset settings pass through a register before entering the DQS delay chains. The registers are controlled by the update enable circuitry to allow enough time for changes in the DQS delay setting bits to arrive at all the delay elements. This allows them to be adjusted at the same time. The update enable circuitry enables the registers to allow enough time for the DQS delay settings to travel from the DQS phase-shift circuitry or core logic to all the DQS logic blocks before the next change. It uses the input reference clock or a user clock from the core to generate the update enable output. The ALTMEMPHY megafunction uses this circuit by default. Figure 7–13 shows an example waveform of the update enable circuitry output.

Figure 7–13. DQS Update Enable Waveform

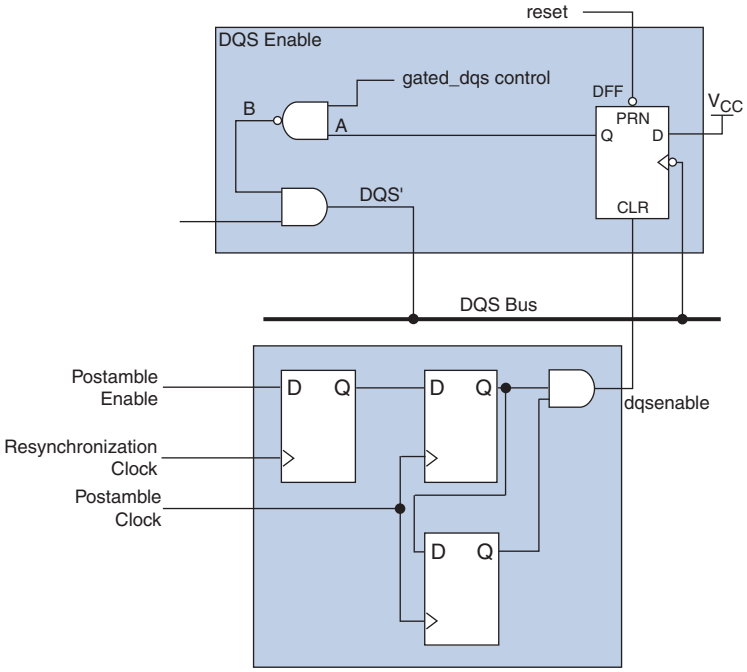


DQS Postamble Circuitry

For external memory interfaces that use a bidirectional read strobe such as DDR3, DDR2, and DDR SDRAM, the DQS signal is low before going to or coming from a high-impedance state. The state where DQS is low, just after a high-impedance state, is called the preamble state; the state where DQS is low, just before it returns to a high-impedance state, is called the postamble state. There are preamble and postamble specifications for both read and write operations in DDR3, DDR2, and DDR SDRAM.

The DQS postamble circuitry, shown in Figure 7–14, ensures that data is not lost when there is noise on the DQS line at the end of a read postamble time. HardCopy III devices have a dedicated postamble register that can be controlled to ground the shifted DQS signal used to clock the DQ input registers at the end of a read operation. This ensures that any glitches on the DQS input signals at the end of the read postamble time do not affect the DQ IOE registers.

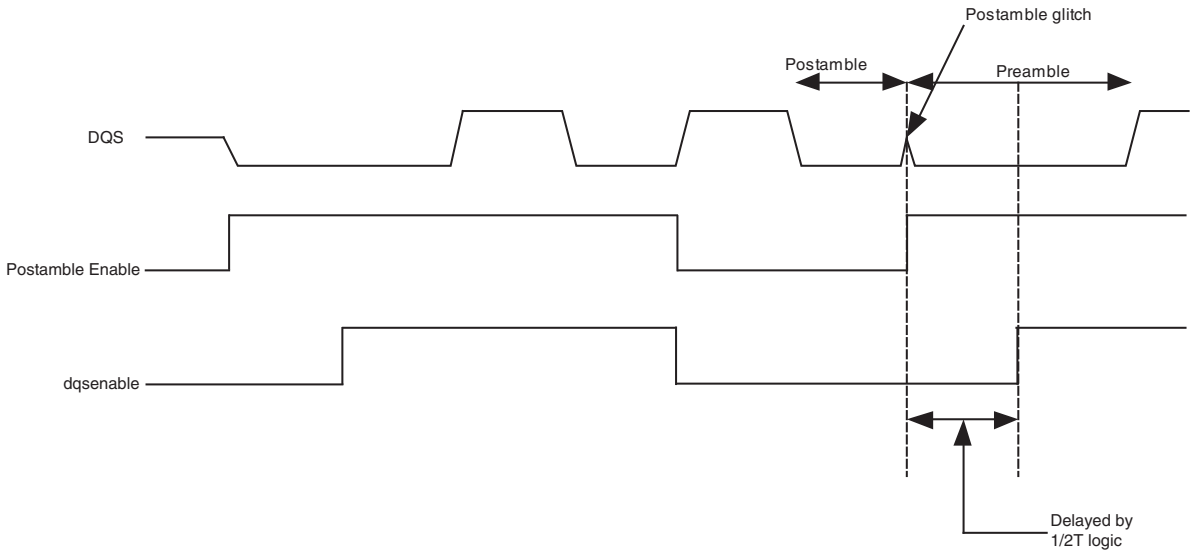
Figure 7–14. DQS Postamble Circuitry in HardCopy III Devices



In addition to the dedicated postamble register, HardCopy III devices also have an HDR block inside the postamble enable circuitry. These registers are used if the controller is running at half the frequency of the I/Os.

Using the HDR block as the first stage capture register in the postamble enable circuitry block in Figure 7–14 is optional. The HDR block is clocked by the half-rate resynchronization clock, which is the output of the I/O clock divider circuit (shown in Figure 7–20). The AND gate after the postamble register outputs is used to avoid postamble glitches from a previous read burst on a non-consecutive read burst. This scheme allows a half-a-clock cycle latency for `dqsenable` assertion and zero latency for `dqsenable` deassertion, as shown in Figure 7–15.

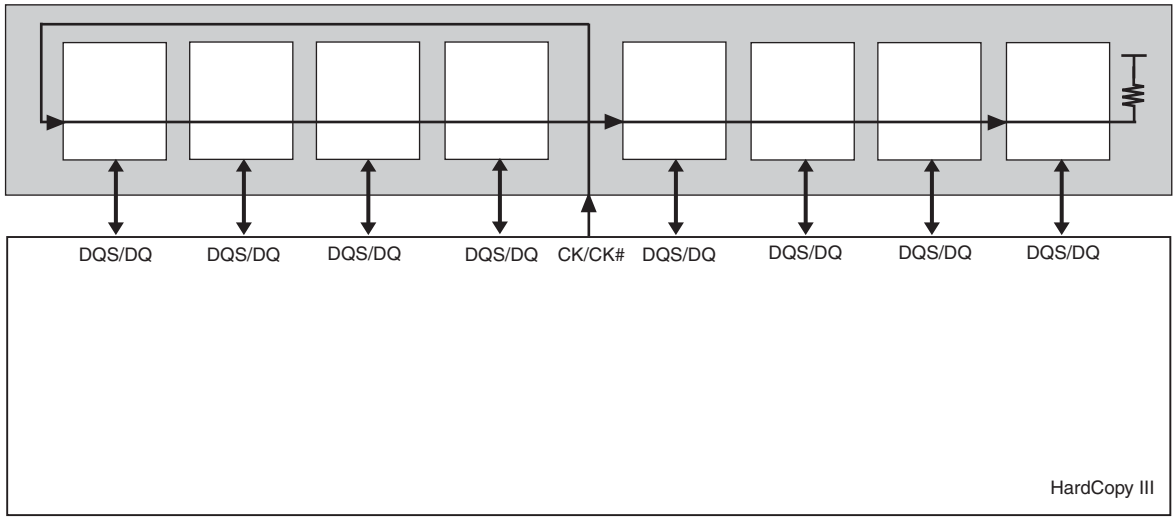
Figure 7–15. Avoiding Glitch on a Non-Consecutive Read Burst Waveform



Leveling Circuitry

DDR3 SDRAM unbuffered modules use a fly-by clock distribution topology for better signal integrity. This means that the CK/CK# signals arrive at each DDR3 SDRAM device in the module at different times. The difference in arrival time between the first DDR3 SDRAM device and the last device on the module can be as long as 1.6 ns. Figure 7–16 shows the clock topology in DDR3 SDRAM unbuffered modules.

Figure 7–16. DDR3 SDRAM Unbuffered Module Clock Topology

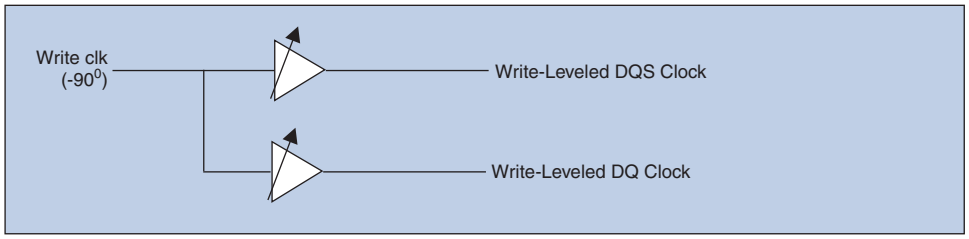


Because the data and read strobe signals are still point-to-point, special consideration must be taken to ensure that the timing relationship between the CK/CK# and DQS signals (tDQSS) during a write is met at every device on the modules. Furthermore, read data returning to the HardCopy III ASIC from the memory is also staggered in a similar way. HardCopy III ASICs have leveling circuitry to compensate for the different CK/CK# arrival time at each device in the memory module.

There is one group of leveling circuitry per I/O bank, with the same I/O number (for example, there is one leveling circuitry shared between I/O bank 1A and 1C) located in the middle of the I/O bank. These delay chains are PVT-compensated by the same DQS delay settings as the DLL and DQS delay chains. The generated clock phases are distributed to every DQS logic block that is available in the I/O bank. The delay chain taps, then feeds a multiplexer controlled by the ALTMEMPHY megafunction to select which clock phases are to be used for that ×4 or ×8 DQS group. Each group can use a different tap output from the read-leveling and write-leveling delay chains to compensate for the different CK/CK# delay going into each device on the module.

Figure 7–17 and Figure 7–18 show the HardCopy III read-and-write leveling circuitry.

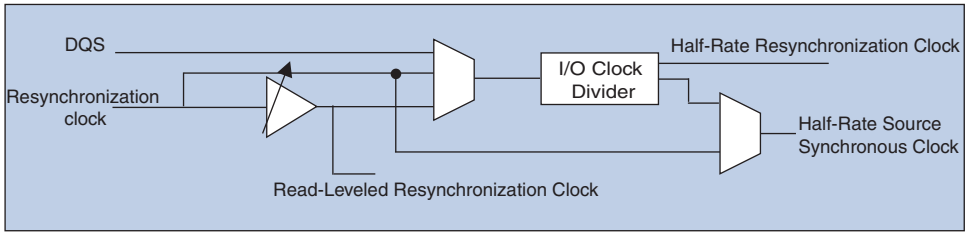
Figure 7–17. Write-Leveling Delay Chains for HardCopy III Devices *(Note 1)*



Note to Figure 7–17:

(1) There is only one leveling delay chain per I/O bank with the same I/O number (for example, I/O banks 1A and 1C). You can only have one memory controller in these I/O banks when you use the leveling delay chains.

Figure 7–18. Read-Leveling Delay Chains and Multiplexers for HardCopy III Devices *(Note 1)*



Note to Figure 7–18:

(1) There is only one leveling delay chain per I/O bank with the same I/O number (for example, I/O banks 1A and 1C). You can only have one memory controller in these I/O banks when you use the leveling delay chains.

The –90° write clock of the ALTMEMPHY megafunction feeds the write-leveling circuitry to produce the clock to generate the DQS and DQ signals. During initialization, the ALTMEMPHY megafunction picks the correct write-leveled clock for the DQS and DQ clocks for each DQS/DQ group after sweeping all the available clocks in the write calibration process. The DQ clock output is –90° phase-shifted compared to the DQS clock output.

Similarly, the resynchronization clock feeds the read-leveling circuitry to produce the optimal resynchronization and postamble clock for each DQS/DQ group in the calibration process. The resynchronization and postamble clocks can use different clock outputs from the leveling circuitry. The output from the read-leveling circuitry can also generate the half-rate resynchronization clock that goes to the core fabric.

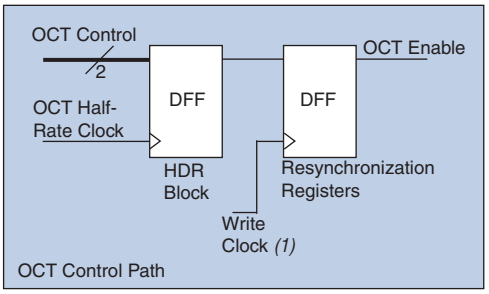
The ALTMEMPHY megafunction calibrates the alignment for read and write leveling dynamically during the initialization process. For more information about the ALTMEMPHY megafunction, refer to the *External Memory Interface Handbook*.

Dynamic On-Chip Termination Control

Figure 7–19 shows the dynamic OCT control block. The block includes all the registers required to dynamically turn OCT on during a read and turn OCT off during a write.

For more information about OCT, refer to "OCT" on page 7–31, or to the *HardCopy III Device I/O Features* chapter.

Figure 7–19. Dynamic OCT Control Block in HardCopy III Devices



Note to Figure 7–19:

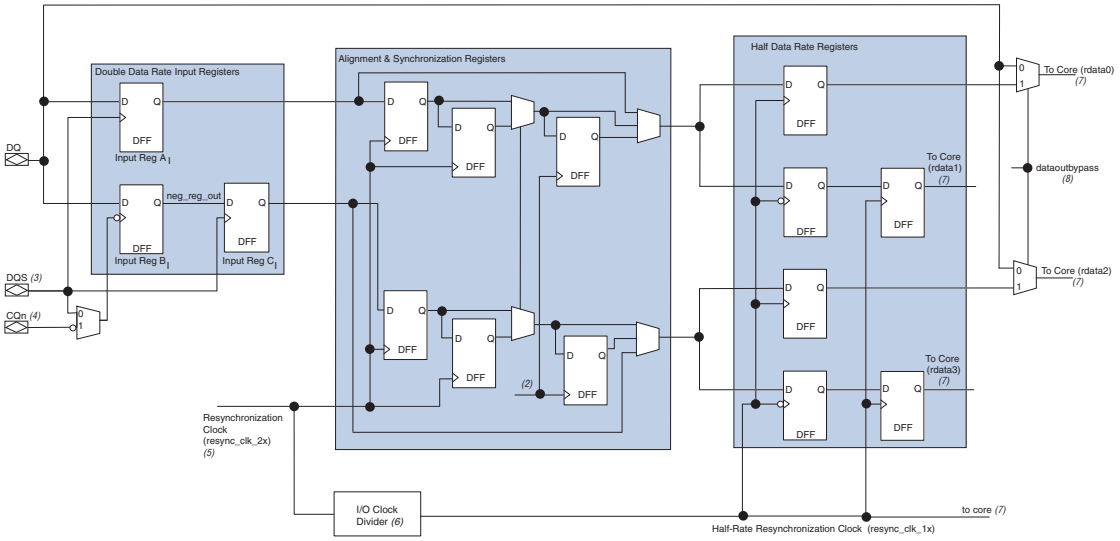
(1) The write clock comes from either the PLL or the write-leveling delay chain.

I/O Element Registers

The IOE registers have been expanded to allow source-synchronous systems to have faster register-to-register transfers and resynchronization. Both top, bottom, left, and right IOEs have the same capability, although left and right IOEs have extra features to support LVDS data transfer.

Figure 7–20 shows the registers available in the HardCopy III input path. The input path consists of the DDR input registers, resynchronization registers, and HDR block. You can bypass each block of the input path.

Figure 7–20. IOE Input Registers in HardCopy III Devices *(Note 1)*



Notes to Figure 7–20:

(1) You can bypass each register block in this path.
(2) This is the 0-phase resynchronization clock from the read-leveling delay chain.
(3) The input clock can be from the DQS logic block (whether the postamble circuitry is bypassed or not) or from a global clock line.
(4) This input clock comes from the CQn logic block.
(5) This resynchronization clock can come either from the PLL or from the read-leveling delay chain.
(6) The I/O clock divider resides adjacent to the DQS logic block. In addition to the PLL and read levelled resync clock, the I/O clock divider can also be fed by the DQS bus or CQn bus.
(7) The half-rate data and clock signals feed into a FIFO in the core.
(8) You can change the `dataoutbypass` signal dynamically after the device enters user mode.

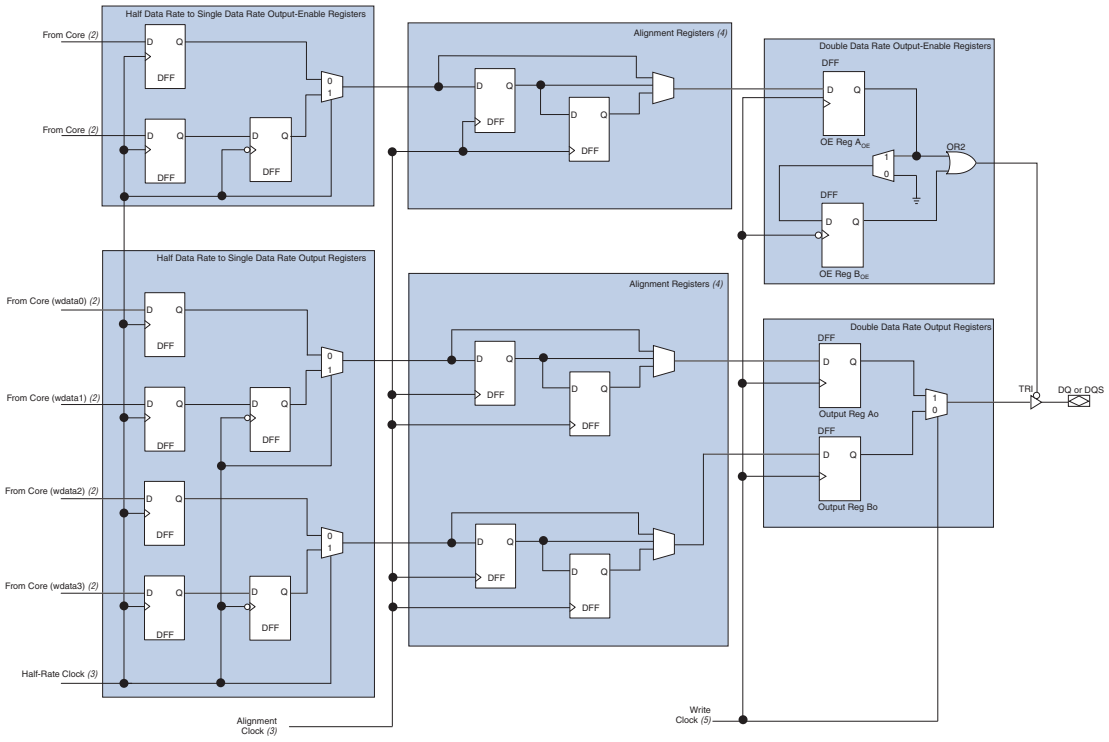
There are three registers in the DDR input registers block. Two registers capture data on the positive and negative edges of the clock, while the third register aligns the captured data. You can choose to have the same clock for the positive edge and negative edge registers, or two different clocks (DQS for positive-edge register and CQn for negative-edge register). The third register that aligns the captured data uses the same clock as the positive-edge register.

The resynchronization registers consist of up to three levels of registers to resynchronize the data to the system clock domain. These registers are clocked by the resynchronization clock that is either generated by the PLL or the read-leveling delay chain. The outputs of the resynchronization registers can go straight to the core or to the HDR blocks, which are clocked by the divided-down resynchronization clock.

For more information about the read-leveling delay chain, refer to "Leveling Circuitry" on page 7–26.

Figure 7–21 shows the registers available in the HardCopy III output and output-enable paths. The path is divided into the HDR block, resynchronization registers, and output/output-enable registers. The device can bypass each block of the output and output-enable path.

Figure 7–21. IOE Output and Output-Enable Path Registers in HardCopy III Devices *(Note 1)*



Notes to Figure 7–21:

(1) You can bypass each register block of the output and output-enable paths.
(2) Data coming from the ASIC core are at half the frequency of the memory interface.
(3) Half-rate and alignment clocks come from the PLL.
(4) These registers are only used in DDR3 SDRAM interfaces.
(5) The write clock can come from either the PLL or from the write-leveling delay chain. The DQ write clock and DQS write clock have a 90° offset between them.

The output path is designed to route combinational or registered SDR outputs and full-rate or half-rate DDR outputs from the core. Half-rate data is converted to full-rate data using the HDR block, clocked by the half-rate clock from the PLL. The resynchronization registers are also clocked by the same 0° system clock, except in the DDR3 SDRAM interface. In DDR3 SDRAM interfaces, the leveling registers are clocked by the write-leveling clock.

For more information about the write leveling delay chain, refer to "Leveling Circuitry" on page 7–26.

The output-enable path has a structure similar to the output path. You can have a combinational or registered output in SDR applications and you can use half-rate or full-rate operation in DDR applications. You also have the resynchronization registers similar to the output path registers' structure, ensuring that the output enable path goes through the same delay and latency as the output path.

IOE Features

This section describes how OCT, delay chains, output delay, slew rate control, and drive strength setting are useful in memory interfaces.

These IOE features are mask programmed and cannot be changed after the silicon is fabricated.

For more information about the features listed below, refer to the *HardCopy III Device I/O Features* chapter.

OCT

HardCopy III devices feature dynamic calibrated OCT, in which the series termination (OCT R_S) is turned on when driving signals and turned off when receiving signals, and the parallel termination (OCT R_T) is turned off when driving signals and turned on when receiving signals. This feature complements the DDR3/DDR2 SDRAM on-die termination (ODT), in which the memory termination is turned off when the memory is sending data and turned on when receiving data. You can use OCT for other memory interfaces to improve signal integrity.

You cannot use the drive strength and slew rate features when using OCT R_S.

To use the dynamic calibrated OCT feature, you must use the R_{UP} and R_{DN} pins to calibrate the OCT calibration block. You can use one OCT calibration block to calibrate one type of termination with the same V_{CCIO} on the entire device. There are up to eight OCT calibration blocks to allow for different types of terminations throughout the device. For more information, refer to "Dynamic On-Chip Termination Control" on page 7–28.

You have the option to use the OCT R_S feature with or without calibration. However, the OCT R_T feature is only available with calibration.

You can also use the R_{UP} and R_{DN} pins as DQ pins, so you cannot use the DQS/DQ groups where the R_{UP} and R_{DN} pins are located if you are planning to use dynamic calibrated OCT. The R_{UP} and R_{DN} pins are located in the first and last ×4 DQS/DQ group on each side of the device.

Use the OCT R_T or R_S setting for unidirectional read-and-write data and a dynamic OCT setting for bidirectional data signals.

IOE Delay Chains

You can use the delay chains in the HardCopy III I/O registers as deskewing circuitry. Each pin can have a different input delay from the pin to the input register or a delay from the output register to the output pin to ensure that the bus has the same delay going into or out of the device. This feature helps read and write time margins because it minimizes the uncertainties between signals in the bus.

Output Buffer Delay

In addition to allowing for output buffer duty-cycle adjustment, the output buffer delay chain allows you to adjust the delays between the data bits in your output bus to introduce or compensate channel-to-channel skew. Incorporating skew to the output bus can help minimize simultaneous switching events by enabling smaller parts of the bus to switch simultaneously instead of the whole bus. This feature is useful in DDR3 SDRAM interfaces where the memory system clock delay can be much larger than the data and data clock/strobe delay. You can use this delay chain to add delay to the data and data clock/strobe to better match the memory system clock delay.

Slew Rate Control

HardCopy III devices provide four levels of static output slew rate control—0, 1, 2, and 3; Level 0 is the slowest slew rate setting and level 3 is the fastest slew rate setting. The default setting for the HSTL and SSTL I/O standards is **3**. A fast slew rate setting allows you to achieve higher I/O performance; a slow slew-rate setting reduces system noise and signal overshoot. This feature is disabled if you use the OCT R_S features.

Drive Strength

You can choose the optimal drive strength required for your interface after performing board simulation. Higher drive strength helps provide a larger voltage swing, which in turn provides bigger eye diagrams with greater timing margin. However, higher drive strengths typically require more power, result in faster slew rates, and add to simultaneous switching noise (SSN). You can use the slew rate control with this feature to minimize SSN with higher drive strengths. This feature is also disabled if you use the OCT R_S feature, which is the default drive strength in HardCopy III devices. Use the OCT R_T/R_S setting for unidirectional read-and-write data and the dynamic OCT setting for bidirectional data signals. You must simulate the system to determine the drive strength required for command, address, and clock signals.

PLL

You can use PLLs to generate the memory interface controller clocks, such as the 0° system clock, the –90° or 270° phase-shifted write clock, the half-rate PHY clock, and the resynchronization clock. You can also use the PLL reconfiguration feature to calibrate the resynchronization phase shift to balance the setup and hold margin. The VCO and counter setting combinations may be limited for high-performance memory interfaces.

Altera recommends enabling the PLL reconfiguration feature and the DLL phase offset feature (DLL reconfiguration) for HardCopy III devices. Because HardCopy III devices are mask programmed, they cannot be changed after the silicon is fabricated. By implementing these two features, you can perform timing adjustments to improve or resolve timing issues after the silicon is fabricated.

PLL reconfiguration is not required for the ALTMEMPHY AFI because it uses auto-calibration. Adding PLL reconfiguration adds very little value and the ALTMEMPHY IP which is generated is not PLL-reconfiguration friendly. Altera strongly recommends implementing PLL reconfiguration for the UniPHY IP.

For more information about HardCopy III PLLs, refer to the *Clock Networks and PLLs in HardCopy III Devices* chapter.

Document Revision History

Table 7–10 lists the revision history for this chapter.

Table 7–10. Document Revision History

Date	Version	Changes
March 2012	3.2	■ Updated DLLx numbering in Figure 7–1, Figure 7–3, Figure 7–4, Figure 7–5, Figure 7–6, Figure 7–7, and Figure 7–8. ■ Updated DLLx numbering in Table 7–5, Table 7–6, Table 7–7, and Table 7–8.
January 2011	3.1	■ Updated Figure 7–1. ■ Updated Table 7–2 and Table 7–6. ■ Updated to include UniPhy IP information. ■ Changed the *External DDR Memory PHY Interface Megafunction User Guide (ALTMEMPHY)* link to the *External Memory Interface Handbook* link. ■ Minor text edits.
June 2009	3.0	■ Updated Table 7–1, Table 7–2, and Table 7–5. ■ Added Figure Table 7–8. ■ Updated “DLL” on page 7–19. ■ Removed “Conclusion” and “Referenced Documents” sections.
December 2008	2.0	Format changes.
May 2008	1.0	Initial release.