Preliminary

10Gb/s SFP+ Optical Transceiver Module

SPP5200LR-GL
SPP5200LR-GL-M

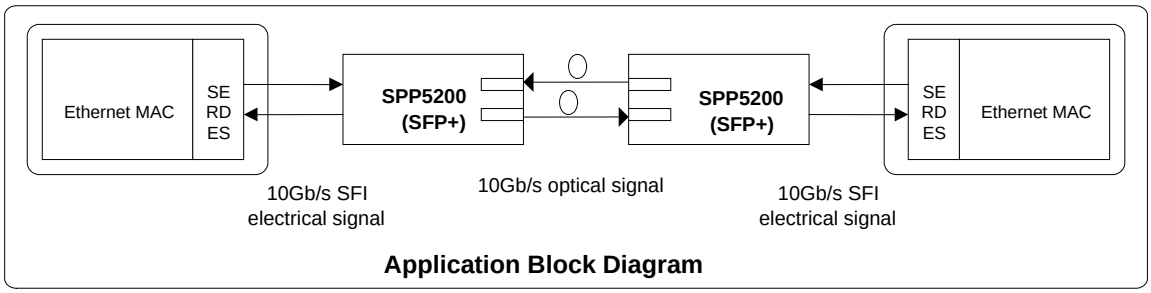
(10GBASE-LR/LW and 1200-SM-LL-L, 1310nm DFB-LD, PIN-PD)

Features

- 10Gb/s Serial Optical Interface
  - High quality and reliability optical device and sub-assemblies
  - 1310nm DFB laser for up to 10km over single mode fiber
  - High sensitivity PIN photodiode and TIA
- SFP+ MSA Compliant
  - Compliant with SFF 8431 for electrical interface
    - SFI High Speed electrical interface
    - Tx_Disable and Rx_LOS function supported
  - Compliant with SFF 8432 for mechanical interface
    - SFP Mechanical Interface for easy removal
    - Duplex LC Receptacle
  - Compliant with SFF 8742 for 2-wire interface for management and diagnostic monitor
- Support Dual Protocol (9.95Gbps to 10.52Gbps)
  - IEEE802.3ae 10GBASE-LR/LW
  - ANSI 10GFC 1200-SM-LL-L
- Low Power Consumption for Single 3.3V Power Supply Not over 1W in commercial temperature range of 0 to 70 deg.C (SPP5200LR-GL), in extended Temperature range of -5 to 85deg.C (SPP5200LR-GL-M)
- RoHS6 compliant

Applications

- 10G Ethernet switches and routers
- 10GE Storage
- 10GFC Storage
- Inter Rack Connection
- Other high speed data connections



Application Block Diagram

1. General Description

SPP5200LR-GL is a very compact 10Gb/s optical transceiver module for serial optical communication applications at 10Gb/s. SPP5200LR-GL converts a 10Gb/s serial electrical data stream to 10Gb/s optical output signal and a 10Gb/s optical input signal to 10Gb/s serial electrical data streams. The high speed 10Gb/s electrical interface is fully compliant with SFI specification of SFF 8431.

SPP5200LR-GL is designed for Ethernet LAN (10.3Gb/s)/WAN(9.95Gb/s) and 10G FC (10.5Gb/s) applications. The high performance 1310nm DFB-LD transmitter and high sensitivity PIN receiver provide superior performance for Ethernet and Fiber Channel applications at up to 10km links.

The fully SFP compliant form factor provides hot pluggability, easy optical port upgrades and low EMI emission.

Table 1. Fiber compliance

SFP+ type	Wavelength [nm]	Cable Type	Core Size	Cable distance
10GBASE-LR/LW 1200-SM-LL-L	1310	SMF	Compliant with G.652	10km

2. Functional Description

SPP5200LR-GL contains a duplex LC connector for the optical interface and a 20-pin connector for the electrical interface. Figure 2 shows the functional block diagram of SPP5200LR-GL SFP+ Transceiver.

Transmitter Operation

The transceiver module receives 10Gb/s electrical data and transmits the data as an optical signal. The transmitter output can be turned off by Tx disable signal via TX_DIS pin. When TX_DIS is asserted High, Transmitter is turned off.

Receiver Operation

The received optical signal is converted to serial electrical data signal. The RX_LOS signal indicates insufficient optical power for reliable signal reception at the receiver.

Management Interface

A 2-wire interface (SCL, SDA) is used for serial ID, digital diagnostics and other control /monitor functions.

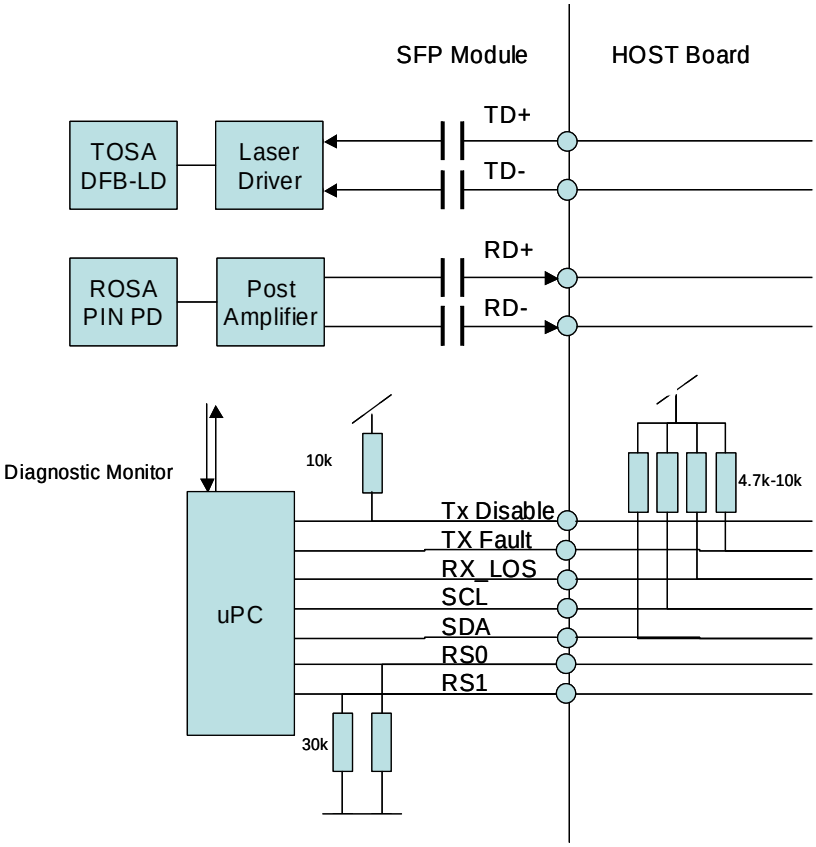


Figure 2. Functional Block Diagram

3. Package Dimensions

Figure 3. shows the package dimensions of SPP5200LR-GL. SPP5200LR-GL is designed to be complaint with SFP MSA specification. Package dimensions are specified in SFF-8432.

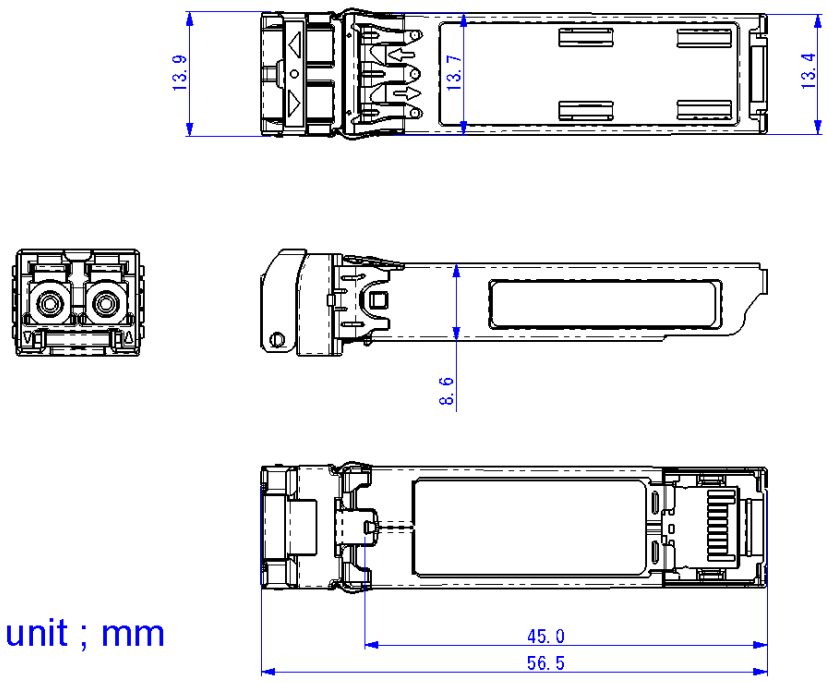


Figure 3. Package dimensions

4. Pin Assignment and Pin Description

4.1. SFP Transceiver Electrical Pad Layout

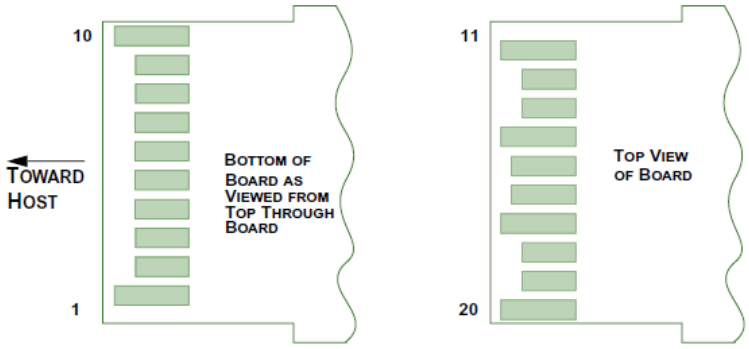


Figure 4.1. SFP Transceiver Electrical Pad Layout

4.2. Host PCB SFP Pinout

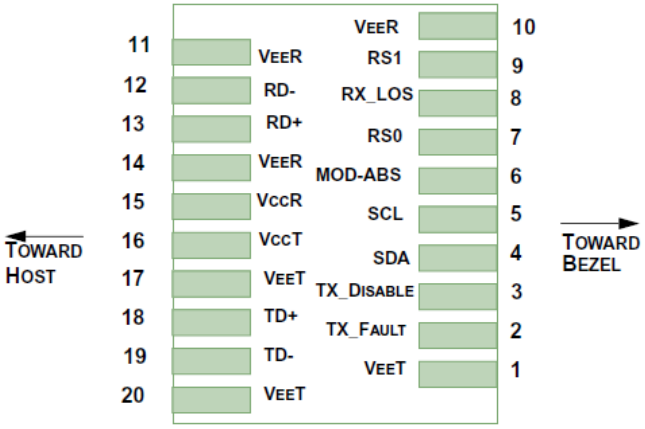


Figure 4.2. Host PCB SFP Pinout

4.3. Pin Descriptions

Table 4.3. Pin Description

Pin#	Name	Logic	Description	Power Sequence Order	Note
1	VeeT		Module Transmitter Ground	1st	1
2	Tx_Fault	LVTTL-O	Module Transmitter Fault	3rd	2
3	Tx_Disable	LVTTL-I	Transmitter Disable,Turns off transmitter laser output	3rd	3
4	SDA	LVTTL-I/O	2 Wire Serial Interface Data Line	3rd	
5	SCL	LVTTL-I/O	2 Wire Serial Interface Clock Line	3rd	
6	MOD_ABS		Module Absent, connected to VeeT or VeeR in the module	3rd	2
7	RS0	LVTTL-I	Rate Select 0 (not functional for this product)	3rd	
8	RX_LOS	LVTTL-O	Receiver Loss of Signal Indication	3rd	2
9	RS1	LVTTL-I	Rate Select 1 (not functional for this product)	3rd	
10	VeeR		Module Receiver Ground	1st	1
11	VeeR		Module Receiver Ground	1st	1
12	RD-	CML-O	Receiver Inverted Data Output	3rd	
13	RD+	CML-O	Receiver Non-Inverted Data Output	3rd	
14	VeeR		Module Receiver Ground	1st	1
15	VccR		Module Receiver 3.3V Supply	2nd	
16	VccT		Module Transmitter 3.3V Supply	2nd	
17	VeeT		Module Transmitter Ground	1st	1
18	TD+	CML-I	Transmitter Non-Inverted Data Input	3rd	
19	TD-	CML-I	Transmitter Inverted Data Input	3rd	
20	VeeT		Module Transmitter Ground	1st	1

Note

1: Module ground pins are isolated from the module case and chassis ground within the module.

2: Shall be pulled up with 4.7k to 10k ohm to a voltage between 3.15V and 3.45V on the host board.

3: Pulled up with 4.7k to 10k ohm to VccT inside the module.

5. Absolute Maximum Ratings and Recommended Operating Conditions

Table 5.1. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Note
Storage Temperature	Tst	-40	85	degC	
Relative Humidity (non-condensation)	RH	-	85	%	
Supply Voltage	VccR/VccT	-0.5	4	V	
Voltage on LVTTL Input	Vilvttl	-0.5	VCC3+0.5	V	
LVTTL Output Current	Iolvttl	-	15	mA	
Voltage on Open Collector Output	Voco	0	6	V	
Receiver Input Optical Power(Average)	Mip	-	1.5	dBm	

Table 5.2. Recommended Operating Conditions and Supply Requirements

Parameter	Symbol	Min	Max	Unit	Note
Operating Case Temperature	Topc	-5	70	degC	1
		-5	85		2
Relative Humidity(non-condensing)	Rhop	-	85	%	
Power Supply Voltage	VccR/VccT	3.135	3.465	V	
Total Power Consumption	Pc	-	1	W	

Note 1. SPP5200LR-GL

2. SPP5200LR-GL-M

6. Electrical Interface

6.1. High Speed Electrical Interface

SFI Application Reference model

Figure 6.1.1. shows the high speed electrical interface (SFI) compliance points.

SFI electrical interface is specified for each compliance point in the SFP MSA specification.

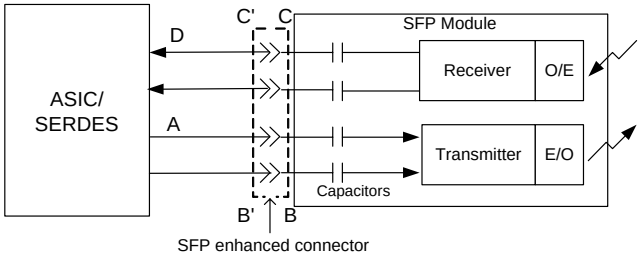


Figure 6.1.1. SFI Application Reference Model

SFI Module Transmitter Input Electrical Interface Specification at B' and Calibrated B"

Table 6.1.1. SFI Transmitter Input Electrical Specifications at B'

Parameter-B'	Symbol	Condition	Min	Typ	Max.	Unit
Single Ended Input Voltage Tolerance		Referenced to VeeT	-0.3		4.0	V
AC Common Mode Voltage Tolerance		Note 1	15			mV
Differential Input S-parameter	SDD11	0.01 to 4.1GHz			Note 2	dB
		4.1 to 11.1GHz			Note 3	dB
Reflected Differential to Common Mode Conversion	SCD11	0.01 to 11.1GHz			-10	dB

Note 1. Measured at B" with Host Compliance Board and Module Compliance Board pair specified in SFF-8431

2. Reflection Coefficient given by equation SDD11(dB)< -12+2*SQRT(f), with f in GHz

3. Reflection Coefficient given by equation SDD11(dB)< -6.3+13*log10(f/5.5), with f in GHz

Table 6.1.2. Transmitter Input Tolerance Signal Calibrated at B"

Parameter- B"	Symbol	Condition	Min	Target.	Max.	Unit
Crosstalk Source Rise/Fall time (20% to 80%)	Tr, Tf	Note 1, 2		34		ps
Crosstalk Source Amplitude (p-p differential)		Note 1, 2		1000		mV
AC Common Mode Voltage		Note 3			15	mV (RMS)
Total Jitter	TJ				0.28	UI (p-p)
Data Dependent Jitter	DDJ			0.10		UI (p-p)
Pulse Width Shrinkage Jitter	DDPWS			0.055		UI (p-p)
Uncorrelated Jitter	UJ	Note 4		0.023		UI (RMS)
Eye Mask Figure 6.1.2	X1	Mask hit ratio of $5x10^{-5}$		0.12		UI
	X2			0.33		UI
	Y1			95		mV
	Y2			350		mV

Note 1. Measured at C" with Host Compliance Board and Module Compliance Board pair specified in SFF-8431.

2. Since the minimum module output transition time is faster than the crosstalk transition time the amplitude of crosstalk source is increased to achieve the same slew rate.

3. The tester is not expected to generate this common mode voltage however its output must not exceed this value.

4. It is not possible to have the maximum UJ and meet the TJ specifications if the UJ is all Gaussian.

SFI Module Receiver Output Electrical Interface Specifications at C'

Table 6.1.3. SFI Receiver Output Electrical Specifications at C'

Parameter -C'	Symbol	Condition	Min	Target	Max	Unit
Crosstalk source Rise/Fall Time (20% to 80%)	Tr, Tf	Note 1		34		ps
Crosstalk Source Amplitude (p-p differential)		Note 1		700		mV
Termination Mismatch at 1 MHz	dZ_M				5	%
Single Ended Output Voltage Tolerance			-0.3		4.0	V
Output AC Common Mode Voltage					7.5	mV (RMS)
Differential Output S-parameter	SDD22	0.01 to 4.1GHz			Note 2	dB
		4.1 to 11.1GHz			Note 3	dB
Common Mode Output Reflection Coefficient	SCC22	0.01 to 2.5GHz			Note 4	dB
		2.5 to 11.1GHz			-3	dB

Note 1. Measured at B'' with Host Compliance Board and Module Compliance Board pair specified in SFF-8431.

2. Reflection Coefficient given by equation SDD11(dB)< -12+2*SQRT(f), with f in GHz

3. Reflection Coefficient given by equation SDD11(dB)< -6.3+13*log10(f/5.5), with f in GHz

4. Reflection Coefficient given by equation SCC22(dB)< -7+1.6*f, with f in GHz

Table 6.1.4. SFP+ Limiting Output Jitter and Eye Mask Specifications at C'

Parameter- C'	Symbol	Condition	Min	Target	Max	Unit
Output Rise/Fall time (20% to 80%)	Tr, Tf		28			ps
Total Jitter	TJ				0.70	UI (p-p)
99% Jitter	J2				0.42	UI (p-p)
Eye Mask Figure 6.1.3	X1	Mask hit ratio of $1x10^{-12}$		0.35		UI
	Y1			150		mV
	Y2			425		mV

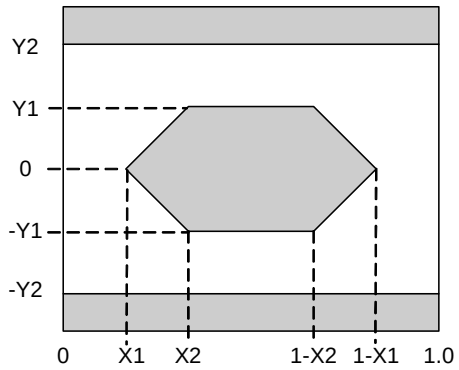


Figure 6.1.2.
Transmitter Input Eye Mask

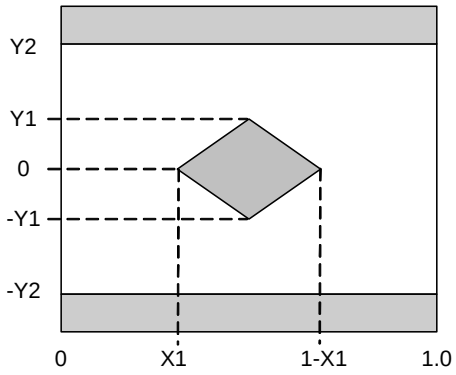


Figure 6.1.3.
Receiver Output Eye Mask

6.2. 2-Wire Interface

SPP5200LR-GL management interface is based on 2-wire interface. Management memory map is based on SFF-8472.

Table 6.2.1. 2-wire Electrical Specifications

Parameter	Symbol	Min	Max	Unit	Condition
Host 2-wire Vcc	Vcc_Host_2w	3.14	3.46	V	Note1
SCL and SDA	V_{OL}	0.0	0.40	V	Rp2w(Note2) pulled to Vcc_Host_2w, Note 3
	V_{OH}	Vcc_Host_2w-0.5	Vcc_Host_2w+0.3	V	
SCL and SDA	V_{IL}	-0.3	VccT*0.3	V	Note3
	V_{IH}	VccT*0.7	VccT+0.5	V	
Input current on the SCL and SDA contacts	I_I	-10	10	uA	
Capacitance on SCL and SDA I/O contact	C_i (Note4)		14	pF	
Total bus capacitance for SCL and for SDA	C_b (Note5)		100	pF	At 400kHz, 3.0kOhm Rp2w, max At 100kHz, 8.0kOhm Rp2w, max
			290	pF	At 400kHz, 1.1kOhm Rp2w, max At 100kHz, 2.75kOhm Rp2w, max

Note 1. The Host 2-wire Vcc is the voltage used for resistive pull ups for the 2 wire interface..

2. Rp2w is the pull up resistor. Active bus termination may be used by the host in place of a pullup resistor. Pull ups can be connected to any one of several power supplies, however the host board design shall ensure that no module contact has voltage exceeding module VccT/R +0.5V nor requires the module to sink more htan 3.0mA current.

3. These voltages are measured on the other side of the connector to the device under test.

4. Ci is the capacitance looking into the module SCL and SDA contacts.

5. Cb is the total bus capacitance on the SCL or SDA bus.

Table 6.2.2 2-wire Timing Specifications

Parameter	Symbol	Min	Max	Unit	Condition
Clock Frequency	f_{SCL}	0	400	kHz	Note1
Clock Pulse Width Low	t_{LOW}	1.3		us	
Clock Pulse Width High	t_{HIGH}	0.6		us	
Time bus free before new transmission can start	t_{BUF}	20		us	Note2
START Hold Time	$t_{HD, STA}$	0.6		us	
START Set-up Time	$t_{SU, STA}$	0.6		us	
Data In Hold Time	$t_{HD, DAT}$	0		us	
Data In Set-up Time	$t_{SU, DAT}$	0.1		us	
Input Rise Time (100kHz)	$t_{R, 100}$		1000	ns	Note3
Input Rise Time (400kHz)	$t_{R, 400}$		300	ns	Note3
Input Fall Time (100kHz)	$t_{F, 100}$		300	ns	Note4
Input Fall Time (400kHz)	$t_{F, 400}$		300	ns	Note4
STOP Set-up Time	$t_{SU, STO}$	0.6		us	

Note 1. .Module shall operate with f_{SCL} up to 100kHz without requiring clock stretching. The module may clock stretch with f_{SCL} greater than 100kHz and up to 400kHz.

2. Between STOP and START and between ACK and ReSTART.

3. From ($V_{IL,MAX}$-0.15) to ($V_{IH,MIN}$+0.15)

4. From ($V_{IH,MIN}$+0.15) to ($V_{IL,MAX}$-0.15)

Table 6.2.3. Memory Specifications

Parameter	Symbol	Min	Max	Unit	Conditions
Serial Interface Clock Holdoff "Clock Stretching"	T_clock_hold		500	us	Note1
Complete Single or Sequential Write up to 4 Byte	t_{WR}		40	ms	
Complete Sequential Write of 5-8 Byte	t_{WR}		80	ms	
Endurance (Write Cycles)		10k		cycles	

Note 1. Maximum time the SFP+ module may hold the SCL line low before continuing with a read or write operation.

6.3. Recommended Filter for Voltage Supply

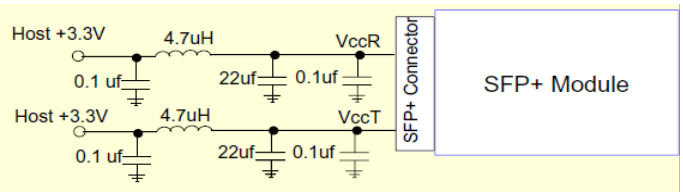


Figure 6.3. Recommended Voltage Supply Fileter

7. Optical Interface

Optical Interfaces of SPP5200LR-GL are defined in the IEEE802.3ae (10GBASE-LR).

7.1. Optical Transmitter

Table 7.1. Transmitter Optical Interface

Parameter	Symbol	Min	Typ	Max	Unit
Signaling Speed 10GBASE-LR 10GBASE-LW 1200-SM-LL-L		 -	10.3125 9.95328 10.51875		Gb/s
Signaling speed variation from nominal (max)		-100 (LR) -20 (LW)		+100 (LR) +20 (LW)	ppm
Center wavelength		1260		1355	nm
Side Mode Suppression Ratio	SMSR	30			dB
Average launch power	Pave	-8.2		+0.5	dBm
OMA	Poma	-5.2			dBm
OMA-TDP		-6.2			dBm
Transmitter and dispersion penalty	DP			3.2	dB
Average launch power of Tx OFF	Pave_off			-30	dBm
Extinction ratio	ER	3.5			dB
RIN OMA	RIN			-128	dB/Hz
Optical Return Loss Tolerance	ORLT			12	dB
Transmitter Reflectance				-12	dB
Eye mask(X1,X2,X3,Y1,Y2,Y3)		(0.25, 0.40, 0.45, 0.25, 0.28, 0.40) Note 1			

Note 1 Refer to Figure 7.1.

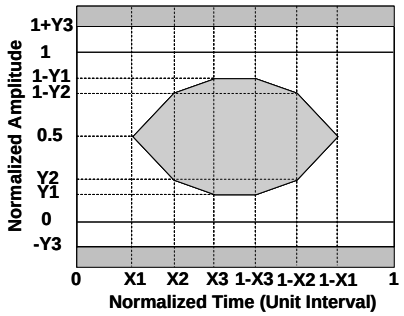


Figure.7.1. Transmission eye mask definition

7.2. Optical Receiver

Table 7.2. Receiver Optical Interface

Parameter	Symbol	Min	Typ	Max	Unit
Center Wavelength		1260		1355	nm
Signaling Speed 10GBASE-LR 10GBASE-LW 1200-SM-LL-L			10.3125 9.95328 10.51875		Gb/s
Signaling speed variation from nomimal (max)		-100		+100	ppm
Average receive power		-14.4		+0.5	dBm
Receiver sensitivity in OMA				-12.6	dBm
Receiver Reflectance				-12	dB
Stressed receiver sensitivity in OMA (Note 1, 2)				-10.3	dBm
Vertical eye closure penalty (Note3)		2.2			dB
Stressed eye jitter (Note3)		0.3			UIpp
Receive electrical 3dB upper cutoff frequency				12.3	GHz

Note 1. Receiver sensitivity is informative. Stressed receiver sensitivity shall be measured with conformance test signal for BER=10^-12.

2. The stressed sensitivity values in the table are for system level BER measurements which include the effects of CDR circuit.

3. Test condition for measuring stressed receiver sensitivity.

8. Electrical and Optical I/O Signal Relationship

Table.8. TX_DIS vs. Optical Output Power

TX_DIS	Optical Output Power
Low (V_{IL}=-0.3 to 0.8V)	Enabled
High (V_{IH} =2.0 to VCC3+0.3V)	Disabled (<-30dBm)

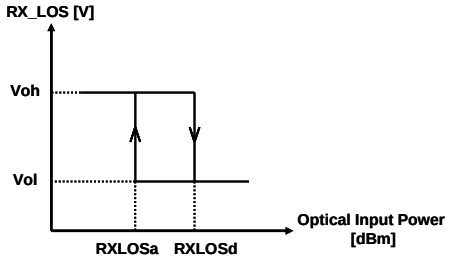


Figure.8. Optical Input Power vs. RX_LOS

9. User Interface

9.1. SFP Mechanical Interface

SFP Mechanical Interface is specified in the SFF-8432. Also, bail latch system is adequate for the particular specification.

9.2. Management Interface

SFP 2-Wire Serial Interface Protocol

SFP 2-wire serial interface is specified in the SFF-8472.

The SFP 2-wire serial interface is used for serial ID, digital diagnostics, and certain control functions. The 2-wire serial interface is mandatory for all SFP modules.

The 2-wire serial interface address of the SFP module is A0h and A2h. In order to access to a specific module on the 2-wire serial bus, the SFP has a MOD_ABS (module absent pin). This pin, which is pulled down in the module, must be held low to notify a module installation and to allow communication over 2-wire serial interface.

SFP Management Interface

SFP Managed interface is specified in the SFF-8472.

The Figure 9.2. shows the structure of the memory map. The normal 256 Byte address space is divided into lower and upper blocks of 128 Bytes. The lower block of 128 Byte is

always directly available and is used for the diagnostics and control functions that must be accessed repeatedly. Multiple blocks of memories are available in the upper 128 Bytes of the address space. These are individually addressed through a table select Byte which the user enters into a location in the lower address space. The upper address space tables are used for less frequently accessed functions and control space for future standards definition.

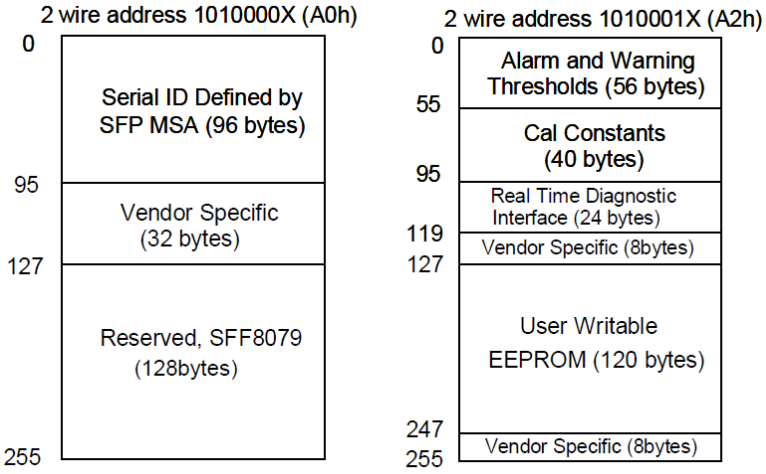


Figure 9.2. 2-wire Serial Interface Memory Map

9.3. Serial ID Memory Map (Data Field – Address A0h)

Address	Size (Bytes)	Name	Hex	ASC	Description
0	1	Identifier	03		SFP Plus
1	1	Ext.Identifier	04		Serial ID module
2	1	Connector	07		LC Connector
3	8	Transceiver	20		10GBASE-LR
4			00		
5			00		
6			00		
7			12		Long distance (10GFC)
8			0		1.3um Laser (10GFC)
9			1		Single Mode (10GFC)
10			80		1200MBytes/sec(10GFC)
11	1	Encoding	06		64B66B
12	1	BR, Nominal	67		10.3Gbps
13	1	Rate Identifer	00		unspecified
14	1	Length(SMF, km)	0A		10km
15	1	Length(SMF)	64		10km
16	1	Length(50um)	00		not support MMF
17	1	Length(62.5um)	00		not support MMF
18	1	Length(Copper)	00		not support copper
19	1	Length(OM3)	00		not support MMF
20	16	Vendor name	53	S	
21			75	u	
22			6D	m	
23			69	i	
24			74	t	
25			6F	o	
26			6D	m	
27			6F	o	
28			45	E	
29			6C	l	
30			65	e	
31			63	c	
32			74	t	
33			72	r	
34			69	i	
35			63	c	
36	1	Transceiver	00		
37	3	Vendor OUI	00		
38			00		
39			5F		
40	16	Vendor PN	53	S	
41			50	P	
42			50	P	
43			35	5	
44			32	2	
45			30	0	
46			30	0	
47			4C	L	
48			52	R	
49			2D	-	
50			47	G	
51			4C	L	
52			2D	-	*1
53			4D	M	*1
54			20		
55			20		
56	4	Vendor rev	41	A	*2
57			20		
58			20		
59			20		
60	2	Wavelength	05		1310nm Laser
61			1E		
62	1		00		
63	1	CC_BASE	19		Check Code *3

Address	Size (Bytes)	Name	Hex	ASC	Description
64	2	Options	00		Uncoold LD, Power Level 1, Limiting Receiver Output
65			1A		TxDisable, TxFault , LOS implemented
66	1	BR,max	00		
67	1	BR,min	00		
68	16	Verdor SN	xx		
69			xx		
70			xx		
71			xx		
72			xx		
73			xx		
74			xx		
75			xx		
76			xx		
77			xx		
78			xx		
79			xx		
80			xx		
81			xx		
82			xx		
83			xx		
84	8	Date Code	xx		Year code
85			xx		
86			xx		Month code
87			xx		
88			xx		Day code
89			xx		
90			xx		LOT code
91			xx		
92	1	Diagnostis Monitoring Type	68		Internal cal , Average Power
93	1	Enhanced Options	F0		Alarm/Warning flags, Soft TxDisable, Soft TxFault, Soft RxLOS implemented
94	1	SFF-8472 Compliance	04		Rev.10.4
95	1	CC_EXT	xx		Check Code *4
96-127	32	Vender Specific	00		
128-255	128	Reserved	00		

*1: "20"(space) for SPP5100LR-GL
*2: Revision level for part number provided by vendor (ASCII). Variable
*3: Checksum of Add.0 to 62
*4: Checksum of Add.64 to 94

9.4. Alarm/Warming threshold

A2h address	Meaning	Unit	SPP5200LR-GL	SPP5200LR-GL-M
0-1	Temperature High Alarm	deg	75	90
2-3	Temperature Low Alarm	deg	-5	-10
4-5	Temperature High Warning	deg	70	85
6-7	Temperature Low Warning	deg	0	-5
8-9	Voltage High Alarm	V	3.63	3.63
10-11	Voltage Low Alarm	V	2.97	2.97
12-13	Voltage High Warning	V	3.465	3.465
14-15	Voltage Low Warning	V	3.135	3.135
16-17	Tx Bias High Alarm	mA	*TBD*	*TBD*
18-19	Tx Bias Low Alarm	mA	*TBD*	*TBD*
20-21	Tx Bias High Warning	mA	*TBD*	*TBD*
22-23	Tx Bias Low Warning	mA	*TBD*	*TBD*
24-25	Tx Power High Alarm	dBm	3.5	3.5
26-27	Tx Power Low Alarm	dBm	-12.2	-12.2
28-29	Tx Power High Warning	dBm	0.5	0.5
30-31	Tx Power Low Warning	dBm	-8.2	-8.2
32-33	Rx Power High Alarm	dBm	3.5	3.5
34-35	Rx Power Low Alarm	dBm	-18.4	-18.4
36-37	Rx Power High Warning	dBm	0.5	0.5
38-39	Rx Power Low Warning	dBm	-14.4	-14.4

Note. Alarm /Warming flag is linked to TxFault by default setting.

9.5. Digital Diagnostic Monitor Accuracy

The following characteristics are defined over recommended operating conditions.

Parameter	Accuracy	Unit
Internally measured transceiver temperature	±3	deg.C
Internally measured transceiver supply voltage	±3	%
Measured Tx bias current	±10	%
Measured Tx output power	±3	dB
Measured Rx received average optical power	±3	dB

10. RoHS COMPLIANCY

Compliancy versus requirements contained inside the following reference document is guaranteed:"Directive 2002/95/EC of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment" from official journal of European Union (European Parliament and of the Council). This product is Compliant at RoHS-6/6 level and contains no leaded solders.

11. Qualification Testing

SPP5200LR-GL 10Gb/s transceiver is qualified to Sumitomo Electric Industries internal design and manufacturing standards. Telecordia GR-468-CORE reliability test standards, using methods per MIL-STD-883 for mechanical integrity, endurance, moisture, flammability and ESD thresholds, are followed.

12. Laser Safety Information

SPP5200LR-GL transceiver uses a semiconductor laser system that is classified as Class 1 laser products per the Laser Safety requirements of FDA/CDRH, 21 CFR1040.10 and 1040.11. These products have also been tested and certified as Class 1 laser products per IEC 60825-1:2001 International standards.

Caution

If this product is used under conditions not recommended in the specification or is used with unauthorized revision, the classification for laser product safety is invalid. Reclassify the product at your responsibility and take appropriate safety measures.

---

13. Electromagnetic Compatibility

EMI (Emission)

SPP5200LR-GL is designed to meet FCC Class B limits for emissions and noise immunity per CENELEC EN50 081 and 082 specifications.

RF Immunity

SPP5200LR-GL has an immunity to operate when tested in accordance with IEC 61000-4-3 (80- 1000MHz, Test Level 3) and GR-1089.

Electrostatic Discharge (ESD) Immunity

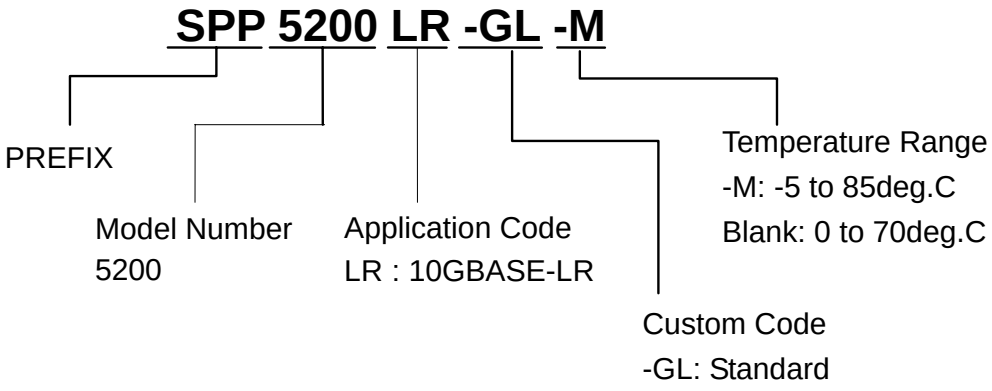
SPP5200LR-GL has an immunity against direct and indirect ESD when tested accordance with IEC 61000-4-2.

14. Firmware version

This product contains the firmware inside. Sumitomo Electric may upgrade the firmware version without advance notice as far as such would be upper compatible. When customer should prefer to have the current firmware version, Sumitomo Electric will accommodate such request and will assign customized part number for this purpose.

15. Ordering Information

15.1. Part Numbering System



15.2. Ordering Number Code

Table 15.2. SPP5200LR Application Code

Part Number	Temperature Range	Distance	Fiber	E/O	O/E	IEEE 802.3ae	ANSI 10GFC
SPP5200LR-GL	0 to 70deg.C	10km	SMF	DFB 1310nm	PIN	10GBASE -LR	1200-SM -LL-L
SPP5200LR-GL-M	-5 to 85deg.C						

16. Label information

17. Contact Information

U.S.A.
Sumitomo Electric Device Innovations, U.S.A., Inc.
<West Coast (USA Headquarters)>
2355 Zanker Rd. San Jose, CA 95131-1138, USA
Tel: +1-408-232-9500
Fax: +1-408-428-9111
<East Coast>
4021 Stirrup Creek Drive, Suite 200, Durham, NC 27703, USA
Tel: +1-919-361-1600
Fax: +1-919-361-1619
Email: information@sei-device.com
http://www.sei-device.com/

Europe
Sumitomo Electric Europe Ltd.
220 Centennial Park, Elstree, Herts, WD6 3SL UK
Tel: +44-208-953-8681
Fax: +44-208-207-5950
E-mail: photonics@sumielectric.com
http://www.sumielectric.com

Asia
Sumitomo Electrics Asia Ltd.
Photonics Department
Room 2624 - 2637, 26F., Sun Hung Kai Center, 30 Harbour Road, Wanchai, Hongkong.
Tel: +852-2576-0080
Fax: +852-2576-6412

Japan
Sumitomo Electric Industries, Ltd.
Device Sales Department
<Tokyo>
3-9-1, Shibaura, Minato-ku, Tokyo 108-8539, Japan
TEL +81-3-6722-3286
FAX +81-3-6722-3284
<Osaka>
4-5-33, Kitahama, Chuo-ku, Osaka 541-0041, Japan
Tel: +81-6-6220-4245
Fax: +81-6-6222-6231
E-mail: optoele-sales-pro-sml@list.sei.jp
http://www.sei.co.jp/products/index.html