Blackfin® EZ-Extender® Manual

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Regulatory Compliance

The Blackfin EZ-Extender has been certified to comply with the essential requirements of the European EMC directive 89/336/EEC (inclusive 93/68/EEC) and, therefore, carries the "CE" mark.

The Blackfin EZ-Extender has been appended to Analog Devices Development Tools Technical Construction File referenced "DSPTOOLS1" dated December 21, 1997 and was awarded CE Certification by an appointed European Competent Body and is on file.



The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.



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PREFACE

Thank you for purchasing the Blackfin EZ-Extender[®], Analog Devices (ADI) extender board to the EZ-KIT Lite[®] evaluation system for ADSP-BF533 and ADSP-BF561 Blackfin[®] processors.

The Blackfin processors are embedded processors that support a Media Instruction Set Computing (MISC) architecture. This architecture is the natural merging of RISC, media functions, and digital signal processing (DSP) characteristics towards delivering signal processing performance in a microprocessor-like environment.

The Blackfin EZ-Extender is designed to be used in conjunction with the ADSP-BF533 or ADSP-BF561 EZ-KIT Lite evaluation system. The EZ-KIT Lite includes an evaluation suite of VisualDSP++[®] software, which is limited in program memory size for use solely with the EZ-KIT Lite product. VisualDSP++ is a powerful programming tool with flexibility that significantly decreases the time required to port software code to a processor, reducing time-to-market.

To learn more about Analog Devices development software, go to http://www.analog.com/dsp/tools/.

Example programs are available to demonstrate the capabilities of the Blackfin EZ-Extender board.

The Blackfin EZ-Extender is a separately sold assembly that plugs onto the expansion interface of the ADSP-BF533 and ADSP-BF561 EZ-KIT Lite evaluation system. The board extends the capabilities of the evaluation system by providing a connection between the parallel peripheral interface (PPI) of the ADSP-BF533 processor (the PPI0 and PPI1 interfaces of the ADSP-BF561 processor), an Analog Devices high-speed converter (HSC) evaluation board, a camera evaluation board, and an LCD display device. Moreover, the extender broadens the range of the EZ-KIT Lite applications by providing surface mounted (SMT) footprints for breadboard capabilities and access to all of the pins on the EZ-KIT Lite's expansion interface.

The extender features:

- High-speed converter (HSC) evaluation board interface
 - 40-pin, right angle, 0.1 in. spacing, female socket to connect to analog-to-digital converter (ADC) boards
 - 40-pin straight, 0.1 in. spacing header to connect to digital-to-analog converter (DAC) boards
 - Switches for routing and direction selection
 - RJ-45 with serial peripheral interconnect (SPI) to configure converter registers
- Camera interface
 - ✓ Connection to OmniVision OV6630AA evaluation boards
 - 32-pin, right angle, 0.1 in. spacing, female socket
- LCD interface
 - 32-pin, right angle FLZ-type connector to connect to LCD displays
- SMT footprint area
 - 1206 and 805 footprints
 - SOIC24 and SOIC20 footprints

- Dimensions
 - ✓ 5 in (H) x 5 in (W)

Purpose of This Manual

The *Blackfin EZ-Extender Manual* describes the operation and configuration of the components on the board. A schematic and a bill of materials are provided as a reference for future ADSP-BF533 and ADSP-BF561 Blackfin processor board designs.

Intended Audience

This manual is a user's guide and reference to the Blackfin EZ-Extender. Programmers who are familiar with the Analog Devices Blackfin processor architecture, operation, and development tools are the primary audience for this manual.

Programmers who are unfamiliar with VisualDSP++ or EZ-KIT Lite evaluation software should refer to the *ADSP-BF533 EZ-KIT Lite Evaluation System Manual* or *ADSP-BF561 EZ-KIT Lite Evaluation System Manual*, VisualDSP++ online Help, and user's or getting started guides. For the locations of these documents, refer to "Related Documents".

Manual Contents

The manual consists of:

- Chapter 1, "EZ-Extender Interfaces" on page 1-1 Provides basic board information.
- Chapter 2, "EZ-Extender Hardware Reference" on page 2-1 Provides information on the hardware aspects of the board.

- Appendix A, "EZ-Extender Bill Of Materials" on page A-1 Provides a list of components used to manufacture the Blackfin EZ-Extender board.
- Appendix B, "EZ-Extender Schematic" on page B-1 Provides the resources to allow extender board-level debugging or to use as a reference design.

Appendix B now is part of the online Help. The PDF version of the *Blackfin EZ-Extender Manual* is located in the Docs\EZ-KIT Lite Manuals folder on the installation CD. Alternatively, the book can be found at the Analog Devices Web site, www.analog.com/processors.

What's New in This Manual

This edition of the *Blackfin EZ-Extender Manual* has been updated for the latest revision of VisualDSP++.

Technical or Customer Support

You can reach Analog Devices, Inc. Customer Support in the following ways:

- Visit the Embedded Processing and DSP products Web site at http://www.analog.com/processors/technicalSupport
- E-mail tools questions to processor.tools.support@analog.com
- E-mail processor questions to processor.support@analog.com (World wide support) processor.europe@analog.com (Europe support) processor.china@analog.com (China support)

- Phone questions to 1-800-ANALOGD
- Contact your Analog Devices, Inc. local sales office or authorized distributor

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    Send questions by mail to:
Analog Devices, Inc.
    One Technology Way
    P.O. Box 9106
    Norwood, MA 02062-9106
    USA
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Supported Products

The Blackfin EZ-Extender is an extender board to the ADSP-BF533 and ADSP-BF561 EZ-KIT Lite evaluation systems.

Product Information

You can obtain product information from the Analog Devices Web site, from the product CD-ROM, or from the printed publications (manuals).

Analog Devices is online at www.analog.com. Our Web site provides information about a broad range of products—analog integrated circuits, amplifiers, converters, and digital signal processors.

MyAnalog.com

MyAnalog.com is a free feature of the Analog Devices Web site that allows customization of a Web page to display only the latest information on products you are interested in. You can also choose to receive weekly e-mail notifications containing updates to the Web pages that meet your interests. MyAnalog.com provides access to books, application notes, data sheets, code examples, and more.

Registration:

Visit www.myanalog.com to sign up. Click **Register** to use MyAnalog.com. Registration takes about five minutes and serves as means for you to select the information you want to receive.

If you are already a registered user, just log on. Your user name is your e-mail address.

Processor Product Information

For information on embedded processors and DSPs, visit our Web site at www.analog.com/processors, which provides access to technical publications, data sheets, application notes, product overviews, and product announcements.

You may also obtain additional information about Analog Devices and its products in any of the following ways.

- E-mail questions or requests for information to processor.support@analog.com (World wide support) processor.europe@analog.com (Europe support) processor.china@analog.com (China support)
- Fax questions or requests for information to 1-781-461-3010 (North America) +49-89-76903-157 (Europe)

Related Documents

For information on product-related development software, see the following publications.

Title	Description
ADSP-BF533 Blackfin Embedded Processor Datasheet ADSP-BF561 Blackfin Embedded Symmetric Multi-Processor Data sheet	General functional description, pinout, and timing.
Blackfin Processor Hardware Reference	Description of internal processor architecture and all register functions.
Blackfin Processor Instruction Set Reference	Description of all allowed processor assembly instructions.

Table 1. Related Processor Publications

Table 2. Related VisualDSP++ Publications

Title	Description
ADSP-BF533 EZ-KIT Lite Evaluation System Manual ADSP-BF561 EZ-KIT Lite Evaluation System Manual	Detailed description of the EZ-KIT Lite features and usage.
VisualDSP++ User's Guide	Detailed description of VisualDSP++ features and usage.
VisualDSP++ Assembler and Preprocessor Manual for Blackfin Processors	Description of the assembler function and commands for Blackfin processors.
VisualDSP++ C/C++ Complier and Library Manual for Blackfin Processors	Description of the complier function and commands for Blackfin processors.
VisualDSP++ Linker and Utilities Manual	Description of the linker function and commands for the processors.
VisualDSP++ Loader and Utilities Manual	Description of the loader/splitter function and commands for the processors.

If you plan to use the EZ-KIT Lite board in conjunction with a JTAG emulator, also refer to the documentation that accompanies the emulator.

All documentation is available online. Most documentation is available in printed form.

Visit the Technical Library Web site to access all processor and tools manuals and data sheets:

http://www.analog.com/processors/resources/technicalLibrary.

Online Technical Documentation

Online documentation comprises the VisualDSP++ Help system, software tools manuals, hardware tools manuals, processor manuals, the Dinkum Abridged C++ library, and Flexible License Manager (FlexLM) network license manager software documentation. You can easily search across the entire VisualDSP++ documentation set for any topic of interest. For easy printing, supplementary .PDF files of most manuals are provided in the Docs folder on the VisualDSP++ installation CD.

Each documentation file type is described as follows.

File	Description
.CHM	Help system files and manuals in Help format
.HTM or .HTML	Dinkum Abridged C++ library and FlexLM network license manager software doc- umentation. Viewing and printing the .html files requires a browser, such as Internet Explorer 5.01 (or higher).
.PDF	VisualDSP++ and processor manuals in Portable Documentation Format (PDF). Viewing and printing the .PDF files requires a PDF reader, such as Adobe Acrobat Reader (4.0 or higher).

If documentation is not installed on your system as part of the software installation, you can add it from the VisualDSP++ CD at any time by running the Tools installation. Access the online documentation from the VisualDSP++ environment, Windows[®] Explorer, or the Analog Devices Web site.

Notation Conventions

Text conventions used in this manual are identified and described as follows.

Example	Description	
Close command (File menu)	Titles in reference sections indicate the location of an item within the VisualDSP++ environment's menu system (for example, the Close command appears on the File menu).	
{this that}	Alternative required items in syntax descriptions appear within curly brackets and separated by vertical bars; read the example as this or that. One or the other is required.	
[this that]	Optional items in syntax descriptions appear within brackets and sepa- rated by vertical bars; read the example as an optional this or that.	
[this,]	Optional item lists in syntax descriptions appear within brackets delimited by commas and terminated with an ellipse; read the example as an optional comma-separated list of this.	
.SECTION	Commands, directives, keywords, and feature names are in text with letter gothic font.	
filename	Non-keyword placeholders appear in text with italic style format.	
í	Note: For correct operation, A Note provides supplementary information on a related topic. In the online version of this book, the word Note appears instead of this symbol.	
×	Caution: Incorrect device operation may result if Caution: Device damage may result if A Caution identifies conditions or inappropriate usage of the product that could lead to undesirable results or product damage. In the online version of this book, the word Caution appears instead of this symbol.	
\bigcirc	Warning: Injury to device users may result if A Warning identifies conditions or inappropriate usage of the product that could lead to conditions that are potentially hazardous for the devices users. In the online version of this book, the word Warning appears instead of this symbol.	



Additional conventions, which apply only to specific chapters, may appear throughout this document.

Notation Conventions

1 EZ-EXTENDER INTERFACES

The Blackfin EZ-Extender board offers the following interfaces.

- "ADC and Mixed-Signal HSC Interface"
- "DAC HSC Interface"
- "Camera Interface"
- "LCD Interface"

The following sections describe each extender interface.

ADC and Mixed-Signal HSC Interface

The Blackfin EZ-Extender can connect to an analog-to-digital converter (ADCs) and a mixed-signal HSC evaluation board via the ADC/mixed-signal HSC interface. The ADC/mixed-signal HSC interface consists of a 40-pin female header, which contains all of the control and data signals necessary to transfer data between the processor's parallel peripheral interface (PPI) and the HSC evaluation board. Additionally, the extender provides a RJ-45 connector, which contains all of the serial peripheral interconnect (SPI) signals necessary to configure the control registers of capable HSC converters. For a block diagram of this interface, see Figure 2-1 on page 2-2.

Before using the Blackfin EZ-Extender, familiarize yourself with the documentation and schematics of the target board and the EZ-KIT Lite. For example, on the EZ-KIT Lite, it may be necessary to disable other devices on the PPI, route the PPI clocks, and disable the push buttons. To configure the Blackfin EZ-Extender to connect to an ADC or mixed-signal HSC evaluation board, first determine the source of the PPI clock. To learn about possible clock settings, refer to "Clock Routing Switch (SW2)" on page 2-5. It is also necessary to determine the direction of the data and frame synchronization signals. The direction is dependent upon the type of the board to which you connect. With ADC boards, it is necessary to set up the data driver on the extender as a receiver. With mixed-signal boards, the data direction can change and a programmable flag is used to change the direction in real time. The frame sync signals are dependent on the external user interface; thus, the functionality of the interface must be taken into consideration. For more information, refer to "System Architecture" on page 2-1 and "DIP Switches and Jumpers" on page 2-4.

Refer to the Analog Devices Web site at http://www.analog.com/en/prod/0%2C2877%2CBF%25252DEXTENDER%2C00.html for more information about the daughter card.

A list of ADC and mixed-signal evaluation boards compatible with the extender can be found at http://www.analog.com/processors/processors/blackfin/technicalLibrary/manuals/pdf/EZ-Extender_to_DSP_Su pported.pdf. Example programs can be found at ftp:// ftp.analog.com/pub/tools/patches/bf_extender_card.zip, when available. To learn more about Analog Devices data converters, go to http://www.analog.com.

DAC HSC Interface

The Blackfin EZ-Extender can connect to digital-to-analog converter HSC evaluation boards via the DAC HSC interface. The DAC HSC interface consists of a 40-pin male header, which contains all of the control and data signals necessary to transfer data from the processor's PPI to the DAC evaluation board. Your extender kit includes the cable used to make a connection. For more information about this interface, see Figure 2-1 on page 2-2.

Before using the Blackfin EZ-Extender, familiarize yourself with the documentation and schematics of the target board and the EZ-KIT Lite. For example, on the EZ-KIT Lite, it may be necessary to disable other devices on the PPI, route the PPI clocks, and disable the push buttons.

To configure the Blackfin EZ-Extender to connect to a DAC evaluation board, first determine the source of the PPI clock. To learn about possible clock settings, refer to "Clock Routing Switch (SW2)" on page 2-5. It is also necessary to determine the direction and source of the data and frame synchronization signals. If your processor holds more than one PPI, the DAC interface allows you to communicate with either PPI0 or PPI1 of the processor. The direction of the frame sync signals is dependent on the target; thus, the functionality of the interface must be taken into consideration. For more information, refer to "System Architecture" on page 2-1 and "DIP Switches and Jumpers" on page 2-4.

A list of DAC HSC evaluation boards compatible with the Blackfin EZ-Extender can be found at http://www.analog.com/processors/processors/blackfin/technicalLibrary/manuals/pdf/EZ-Extender_to_DSP _Supported.pdf. Example programs can be found at ftp:// ftp.analog.com/pub/tools/patches/bf_extender_card.zip, when available. To learn more about Analog Devices data converters, go to http://www.analog.com.

Camera Interface

The Blackfin EZ-Extender camera interface is a right-angle 32-pin connector with control signals compatible to the ITU-R BT.656 camera interface specification. Specifically, the extender's camera interface is directly compatible with camera interface boards, such as the Omnivision

LCD Interface

OV6630AA evaluation module. To learn more about the OV6630AA evaluation module, go to http://www.ovt.com. For a block diagram of the camera interface, see Figure 2-1 on page 2-2.

Before using the Blackfin EZ-Extender, familiarize yourself with the documentation and schematics of the target board and the EZ-KIT Lite. For example, on the EZ-KIT Lite, it may be necessary to disable other devices on the PPI, route the PPI clocks, and disable the push buttons.

To configure the Blackfin EZ-Extender to connect to a camera, first determine the source of the PPI clock. To learn about possible clock settings, refer to "Clock Routing Switch (SW2)" on page 2-5. It is also necessary to set the direction of the data and the frame sync signals. The direction of frame synchronization signals depends on the camera's configuration. The data must be set as an input to the PPI port. For more information, refer to "System Architecture" on page 2-1 and "DIP Switches and Jumpers" on page 2-4.

LCD Interface

The LCD interface is intended to drive an LCD display device. A 32-pin, right-angle FLZ-type connector is provided to connect the data and control lines of commercially available LCD panels. For a block diagram of this interface, see Figure 2-1 on page 2-2.

A timing and functional analysis is required to determine if a specific LCD can connect to the Blackfin EZ-Extender. An example of a display which does connect to the extender is the Sharp LQ058T5DRQ1 display. For more information about the Sharp LCD panel (part number LQ058T5DRQ1), go to

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http://www.sharpsma.com/fastfocus/nidetail.asp?t=DIS-
PLAY&ck=f&p=PCPVTSBY3&n=2.
```

Please note that the power for the backlight feature of the LCD must be provided by the customer. Information on the backlight inverter module (part number LXM1614-14-11) needed to connect to the LCD panel is available at http://www.chipdocs.com/pnde-

coder/datasheets/MSEMI/LXM1614-14-11.html?ReR=IN. The part number of the connector on the EZ-Extender is JST32FLZ-SM1-R-TB. The cable connecting the JST part to the data port on the LCD is available from Parlex Corporation (part number 050-32-76B).

Before using the Blackfin EZ-Extender, familiarize yourself with the documentation and schematics of the target board and the EZ-KIT Lite. For example, on the EZ-KIT Lite, it may be necessary to disable other devices on the PPI, route the PPI clocks, and disable the push buttons.

To configure the EZ-Extender to connect to the LCD interface, first determine the source of the PPI clock and the source and direction of the data and frame sync signals. If your target processor holds more than one PPI, the LCD interface allows you to communicate with either PPI0 or PPI1 of the processor. For more information, refer to "System Architecture" on page 2-1 and "DIP Switches and Jumpers" on page 2-4.

Example programs can be found at ftp://ftp.ana-

log.com/pub/tools/patches/bf_extender_card.zip, when available. To learn more about Analog Devices LCD drivers, go to http://www.analog.com.

LCD Interface

2 EZ-EXTENDER HARDWARE REFERENCE

This chapter describes the hardware design of the Blackfin EZ-Extender. The following topics are covered.

- "System Architecture" on page 2-1 Describes the configuration of the extender and explains how the board components interface with the processor and EZ-KIT Lite.
- "DIP Switches and Jumpers" on page 2-4 Describes the function of the configuration DIP switches.

System Architecture

A detailed block diagram of the Blackfin EZ-Extender is shown in Figure 2-1. Note that the arrow in the bidirectional driver symbols denotes the direction of the driver when in transmit mode. The bidirectional driver is in transmit mode when the direction pin is pulled high. Use the diagram in conjunction with information in "DIP Switches and Jumpers" section of this manual to configure your Blackfin EZ-Extender.

Before using the EZ-Extender, familiarize yourself with the documentation and schematics of the target board and the EZ-KIT Lite. For example, on the EZ-KIT Lite, it may be necessary to disable other devices on the PPI, route the PPI clocks, and disable the push buttons.

The block diagram in Figure 2-1 shows that all of the interfaces have clock signals, frame sync signals, data signals and, possibly, general-purpose signals. Each signal's configuration depends on how your interface operates.



Figure 2-1. Blackfin EZ-Extender Block Diagram

The EZ-Extender holds two clock signals, TX_CLK and RX_CLK. The TX_CLK signal is used as an output to the interface you are using. The TX_CLK signal can be generated in three ways: applying a signal via an SMA connector, populating a socket with an oscillator, or using a 27 MHz signal provided by the EZ-KIT Lite. Only one of these sources can be used at a time, the other sources must be disabled. For how to disable the TX_CLK sources, see "SMA Connector Clock Disconnect Jumper (P10)" on page 2-9 and "External Clock Disable Jumper (P37)" on page 2-10. The RX_CLK signal is generated by the target board. Both the TX_CLK and RX_CLK can connect to the PPI_CLK signal as an input to the processor. See "Clock Routing Switch (SW2)" on page 2-5 for more information.

The ADC/mixed-signal HSC interface and camera interface have two frame sync signals, FSYNC1 and FSYNC2. For information on how to set the direction and the source of these signals, refer to "Direction Control Switch (SW1)" on page 2-4 and "General Frame Sync Routing Switch (SW3)" on page 2-7.

The LCD interface has two frame sync signals, FSYNC1_LCD and FSYNC2_LCD. These signals are always outputs, but it is possible set the source of the signals. For more information see, "LCD Frame Sync Routing Switch (SW4)" on page 2-8.

The ADC/mixed-signal HSC interface and camera interface connect to the DATA_A[15:0] parallel bus. The DAC HSC interface and the LCD interface connect to the DATA_B[15:0] parallel bus. The DATA_A bus is attached to only the PPI0 bus, while DATA_B[15:0] can connect to either PPI0 or PPI1 busses. This allows access to all of the interfaces with a single PPI port or access to two separate interfaces with two PPI ports. For more information about the routing of the PPI data signals see, "PPI Data Routing Jumper (P36)" on page 2-9. To configure the direction of the DATA_A signals, see "Direction Control Switch (SW1)" on page 2-4.

DIP Switches and Jumpers

The following section describes the function of all of the jumpers and switches on the EZ-Extender. Before connecting the extender, make sure you understand each possible settings effect on your application.

Direction Control Switch (SW1)

The PPI interface is bidirectional and half-duplex. A designated DIP switch, SW1, provides an independent direction control for the DATA_A bus and the sync signals (FSYNC1 and FSYNC2) going to the camera interface and ADC/mixed-signal HSC interface, as illustrated in Figure 2-1 on page 2-2. Each of the signals can be hardwired to be either transmit or receive, or can be changed in real time using the PF0 processor programmable flag pin.

If the PFO programmable flag is intended for direction control, ensure the flag is not used for other purposes on the EZ-KIT Lite board (the motherboard).

When the switch connects a direction control signal to ground (GND), the corresponding signal (or signals) being controlled is an input.

The SW1 DIP switch settings are summarized in Table 2-1 through Table 2-3.

SW1 Position 1	SW1 Position 2	Function
OFF	OFF	EZ-KIT Lite is transmitter
ON	OFF	PF0 sets the direction: 0 = EZ-KIT Lite is receiver 1 = EZ-KIT Lite is transmitter
OFF	ON	EZ-KIT Lite is receiver
ON	ON	Do not use

Table 2-1. SW1 Data Direction Control Positions 1 and 2

SW1 Position 3	SW1 Position 4	Function
OFF	OFF	EZ-KIT Lite is transmitter
ON	OFF	PF0 sets the direction: 0 = EZ-KIT Lite is receiver 1 = EZ-KIT Lite is transmitter
OFF	ON	EZ-KIT Lite is receiver
ON	ON	Do not use

Table 2-2. SW1 FSYNC1 Direction Control Positions 3 and 4

Table 2-3. SW1 FSYNC2 Direction Control Positions 5 and 6

SW1 Position 5	SW1 Position 6	Function
OFF	OFF	EZ-KIT Lite is transmitter
ON	OFF	PF0 sets the direction: 0 = EZ-KIT Lite is receiver 1 = EZ-KIT Lite is transmitter
OFF	ON	EZ-KIT Lite is receiver
ON	ON	Do not use

Clock Routing Switch (SW2)

The source of the clock input signals PPI0_CLK and PPI1_CLK are configured through the SW2 DIP switch settings, as illustrated in Figure 2-1 on page 2-2. The SW2 settings are summarized in Table 2-4 and Table 2-5.

Table 2-4. PPI0_CLK Source Settings

SW2 Position 1 RX_CLK	SW2 Position 2 TX_CLK	PPI0_CLK Source
OFF	OFF	The PPIO_CLK signal is not generated by the EZ-Extender
OFF	ON	TX_CLK; this signal must be generated by one of the user-configured PPI clock sources

SW2 Position 1 RX_CLK	SW2 Position 2 TX_CLK	PPI0_CLK Source
ON	OFF	RX_CLK
ON	ON	RX_CLK ; in this configuration, the RX_CLK signal is also routed to the TX_CLK as an output

Table 2-5. PPI1_CLK Source Settings

SW2 Position 3 RX_CLK	SW2 Position 4 TX_CLK	PPI1_CLK Source
OFF	OFF	The PPI1_CLK signal is not generated by the EZ-Extender
OFF	0 N	TX_CLK; this signal must be generated by one of the user-configured PPI clock sources
ON	OFF	RX_CLK
ON	0 N	RX_CLK; in this configuration, the RX_CLK signal is also routed to the TX_CLK as an output

Possible user-configured PPI clock sources are:

- 27 MHz clock signal from the EZ-KIT Lite (not available on ADSP-BF533 EZ-KIT Lite). See "External Clock Disable Jumper (P37)" on page 2-10.
- A local oscillator, by populating the oscillator socket (U10).
- An external clock source using the SMA connector (J5). See "SMA Connector Clock Disconnect Jumper (P10)" on page 2-9.



Only one of these sources can be used at a time —ensure that all of the other sources are disabled.

General Frame Sync Routing Switch (SW3)

Frame synchronization signals FSYNC1 and FSYNC2 get configured through the SW3 DIP switch settings, as illustrated in Figure 2-1 on page 2-2.

The FSYNC1 signal can be set by either the PF2 programmable flag or the processor's PPI0_SYNC1 signal. The FSYNC2 signal can be set by either the PF3 programmable flag or the PPI0_SYNC2 signal. Table 2-6 and Table 2-7 depict the available options. Note that the source of the PPI0_SYNC1 and PPI0_SYNC2 signals is dependent on the EZ-KIT Lite to which you connect.



If the PF2 or PF3 programmable flags are used, ensure the flags are not used for other purposes on the EZ-KIT Lite board (the mother board).

SW3 Position 1 RX_CLK	SW3 Position 2 TX_CLK	FSYNC1 Source	
OFF	OFF	FSYNC1 signal is used	
OFF	ON	FSYNC1 signal is not used	
ON	OFF	FSYNC1 = PF2	
-	-	All others, do not use	

Table 2-6	. FSYNC1	Source	Settings
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Table 2-7.	FSYNC2	Source	Settings
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SW3 Position 3 RX_CLK	SW3 Position 4 TX_CLK	FSYNC2 Source	
OFF	OFF	FSYNC2 signal is used	
OFF	ON	FSYNC2 signal is not used	
ON	OFF	FSYNC2 = PF3	
-	-	All others, do not use	

LCD Frame Sync Routing Switch (SW4)

Frame synchronization signals FSYNC1_LCD and FSYNC2_LCD get configured through the SW4 DIP switch settings, as illustrated in Figure 2-1 on page 2-2.

The FSYNC1_LCD signal can be set by the PF2 programmable flag, PPI0_SYNC1, or PPI1_SYNC1 signal. The FSYNC2_LCD signal can be set by the PF3 programmable flag, PPI0_SYNC2, or PPI1_SYNC2 signal. Figure 2-8 and Figure 2-9 depict the available options.



If the PF2 or PF3 programmable flag is used, ensure the flag is not used for other purposes on the EZ-KIT Lite board (the mother board).

SW4 Position 1 PF2	SW4 Position 2 PPI0_SYNC1	SW4 Position 3 PPI1_SYNC1	FSYNC1_LCD Source
OFF	OFF	OFF	FSYNC1_LCD signal is used
OFF	ON	OFF	FSYNC1_LCD = PPI0_SYNC1
OFF	OFF	OFF	FSYNC1_LCD = PPI1_SYNC1
ON	OFF	ON	FSYNC1_LCD = PF2
_	_	_	All other configurations should not be used

Table 2-8. FSYNC1_LCD Source Settings

Table 2-9. FSYNC2_LCD Source Settings

SW4 Position 4 PF2	SW4 Position 5 PPI0_SYNC2	SW4 Position 6 PPI1_SYNC2	FSYNC2_LCD Source
OFF	OFF	OFF	FSYNC2_LCD signal is used
OFF	ON	OFF	FSYNC2_LCD = PPI0_SYNC2
OFF	OFF	OFF	FSYNC2_LCD = PPI1_SYNC2

SW4 Position 4 PF2	SW4 Position 5 PPI0_SYNC2	SW4 Position 6 PPI1_SYNC2	FSYNC2_LCD Source
ON	OFF	ON	FSYNC2_LCD = PF3
_	_	_	All other configurations should not be used

Table 2-9. FSYNC2_LCD Source Settings (Cont'd)

MISO Disconnect Jumper (P7)

The SO signal of the SPI connector (J1) is driven by a buffer to the processor's MISO signal, as illustrated in Figure 2-1 on page 2-2. When the SPI connector is not in use, remove the jumper to prevent any interfering with other devices on the SPI bus.

SMA Connector Clock Disconnect Jumper (P10)

The SMA connector (J5) provides the ability to input a clock from a signal generator or other clock source. This signal is first put though a buffer, as illustrated in Figure 2-1 on page 2-2. When the SMA connector is not in use, remove the jumper to prevent any interfering with other devices on the net.

PPI Data Routing Jumper (P36)

The flexibility of the EZ-Extender used with the Blackfin processor's single and double PPI requires the PPI data signals to be routed accordingly. Figure 2-2 and Figure 2-3 show the data flow when P36 is installed and when it is not installed.



When connecting to the OV6630AA evaluation module, ensure that the P36 jumper is not installed. The signals attached to PPI1 are used as input by the camera.



Figure 2-2. P36 Not Installed Data Flow



Figure 2-3. P36 Installed Data Flow

External Clock Disable Jumper (P37)

The EZ-KIT Lite provides a 27 MHz clock, which can be used as a transmit clock for all of the interfaces as illustrated in Figure 2-1 on page 2-2. When the 27 MHz clock is not being used, remove the jumper to prevent the TX_CLK signal from being driven. For information about other transmit clock sources, see "Clock Routing Switch (SW2)" on page 2-5.

A EZ-EXTENDER BILL OF MATERIALS

The bill of materials corresponds to "EZ-Extender Schematic" on page B-1. Please check the latest schematic on the Analog Devices Web site:

http://www.analog.com/Processors/Processors/DevelopmentTools/tec hnicalLibrary/manuals/DevToolsIndex.html#Evaluation%20Kit%20Manuals.

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
1	1	74LVX244MSOIC20	U8	FAIRCHILD	74LVX244M
2	1	SN74AHC1G00 SOT23-5	U13	TI	SN74AHC1G00DBVR
3	6	SN74LVC1G125 SOT23-5	U4-6,U9,U12, U14	TI	74LVC1G125DBVRE4
4	4	74LVTH16245MEA SSOP48	U1-2,U10-11	FAIRCHILD	74LVTH16245MEA
5	1	SN74LVC1G14DBV R SOT23-5	U3	DIGI-KEY	296-11607-1-ND
6	1	DIP 8 DIP8SOC	U7	MILL-MAX	614-43-308-31-007000
7	3	0.0545x2CON018	P1-3	SAMTEC	TFC-145-32-F-D
8	2	DIP6 SWT017	SW1,SW4	C&K	TDA06H0SB1
9	1	IDC 16X2 IDC16X2RASOC	J2	SAMTEC	SSW-116-02-F-D-RA
10	1	IDC 20X2 IDC20X2RASOC	J3	SAMTEC	SSW-120-02-G-D-RA

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
11	1	RJ45 8PIN Con_RJ45	J1	ТҮСО	1-16609214-1
12	2	DIP4 SWT018	SW2-3	ITT	TDA04HOSB1
13	1	SMA XPINS CON043	J5	JOHNSON COMP	142-0701-201
14	1	IDC 20x2 IDC20x2_S	P8	AMP/TYCO	5499910-9
15	1	FLZ 32-PIN CON044	J6	JST	32FLZ-SM1-R-TBLF
16	5	IDC 2X1 IDC2X1	P7,P9-10,P36-37	FCI	90726-402HLF
17	1	51 1/8W 5% 1206	R9	VISHAY	CRCW120651R0JKEA
18	25	0.1UF50V10%0805	C1-10,C12-26	AVX	08055C104KAT
19	14	10K1/10W5%0805	R5-7,R11-12, R15-16,R21-25, R28,R30	VISHAY	CRCW080510K0JNEA
20	4	33 1/10W 5% 0805	R10,R13,R18, R29	VISHAY	CRCW080533R0JNEA
21	5	10UF 16V 10% B	CT1-5	AVX	TAJB106K016R
22	2	0 1/10W 5% 0805	R1,R14	VISHAY	CRCW08050000ZSEA
23	4	22 1/10W 5% 0805	R3-4,R26-27	VISHAY	CRCW080522R0JNEA
24	3	1.2K1/10W5%0805	R17,R19-20	VISHAY	CRCW08051K20JNEA
25	8	22 125MW 5% RNS001	RN1-8	CTS	744C083220JP
26	1	10K 1/2W 10% RES002	R8	COPAL ELECT	CT9EW103

BLACKFIN EZ-EXTENDER SCHEMATIC

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	ANALOG DEVICES		n Road NH 03063 0-ANALOGD				
Title	BLACKFI	N EZ-E	EXTEND)ER			
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Date	4-24-2006_9:34		S	heet	1	of	7
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$3.3V \qquad 5V \\ + CT4 \qquad C5 \qquad + CT3 \qquad C15 \\ 0.1UF \qquad 0.005 \qquad 0.005$	5V 		EXPANSION INTERFACE (TYPE B)
PP1_SYNC2	PPI1_D14 22 P3_28 28 P3_30 30 P3_32 32 P3_34 34 P3_36 36 P3_38 38 P3_34 34 P3_36 36 P3_38 38 P3_42 42 P3_42 42 P3_48 48 P3_50 50 P3_52 52 P3_54 54 P3_56 56 P3_66 60 P3_62 62 P3_64 64 P3_66 66 P3_70 70 P3_74 74 P3_78 78 P3_80 80 P3_84 84 P3_86 86 P3_84 84 P3_86 86 P3_86 86	7 $P3_7$ 9 PPI1_D3 11 PPI1_D5 13 PPI1_D7 15 PPI1_D9 17 PPI1_D11 19 PPI1_D13 21 PPI1_D15 23 PPI1_D15 24 PPI1_D15 25 P3_29 + 29 P3_33 P3_33 + 33 P3_39 P3_37 + 33 + 43 + 43 + 44 + 43 + 44 + 43 + 44 + 45 P3_47 + 49 P3_47 + 49 + 51 - + - + - + - + - + - + - + - +	P3_[1:90] PIN 18 SIGNAL (OMNI PWDN) ADSP-BF533 ADSP-BF561 PA7_A PP11_D10 (=PF34) PEXP_PP11_CLK PP11_SYNC2 PP11_SYNC2	PPI1_D0 PPI1_D4 PPI1_D6 PPI1_D10 PPI1_D12 PPI1_D14

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Camera Interface

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ADC/Mixed Signal HSC Interface



DAC HSC Interface

		DATA_B[0:15]
P8		
	+ 1 DATA_B15	
4	+ 3 DATA_B14	
	+ 5 DATA_B13	
8+	+ 7 DATA_B12	
	+ 9 DATA_B11	
	+ 11 DATA_B10	
	+ 13 DATA_B9	
	+ 15 DATA_B8	
	+ 17 DATA_B7	
20 +	+ 19 DATA_B6	
	+ 21 DATA_B5	
	+ 23 DATA_B4	
26 +	+ 25 DATA_B3	
	+ 27 DATA_B2	
30 +	+ 29 DATA_B1	
32 +	+ 31 DATA_B0	
34 +	+ 33	TX_CLK
36 +	+ 35	
38 +	+ 37	
40 +	+ 39	
	20X2_S	
\checkmark		



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TP52	P12 1	2	TP59
TP50	3	4	TP60
TP51	5	6	TP61
TP54	7	8	
TP56	9	10	
TP55	11	12	
TP58	13	14	
TP57	15	16	
\smile	so	IC16	0



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TP89 TP91 TP90	$ \begin{array}{r} P34 \\ \hline $	2 TP92 4 TP93 6 TP95	
	PRT_NUM=DI	NE	

TP46	P35	TP49
TP44 TP45	$\frac{3}{+} + \frac{4}{-}$	TP48
0	-5 + + $-5SOT23-6$	O

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TP33	P15		TP22
TP34		+	
TP36	+ 5	+ _ 6	TP24
TP35	7	8	TP25
TP38	9	10	TP26
TP37	11	12	TP27
TP40	13	14	TP28
TP39	15 +	16	TP29
TP41	17 +	18	TP30
TP42	19	20	TP31
Ŭ	SOIC	20	0

TP68	P14 1	2	TP76
TP86	3	4	TP75
TP84	5	6	TP67
TP85	7	8	TP74
TP82	9	10	TP73
TP83	11	12	TP72
TP79	13	14	TP71
TP81	15	16	TP70
TP88	17 +	18	TP77
TP87	19	20	TP78
Ŭ	SOIC	20	0



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