

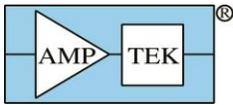
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AMETEK[®]
MATERIALS ANALYSIS DIVISION

DP5G User Manual

Rev A1, Mar 2016

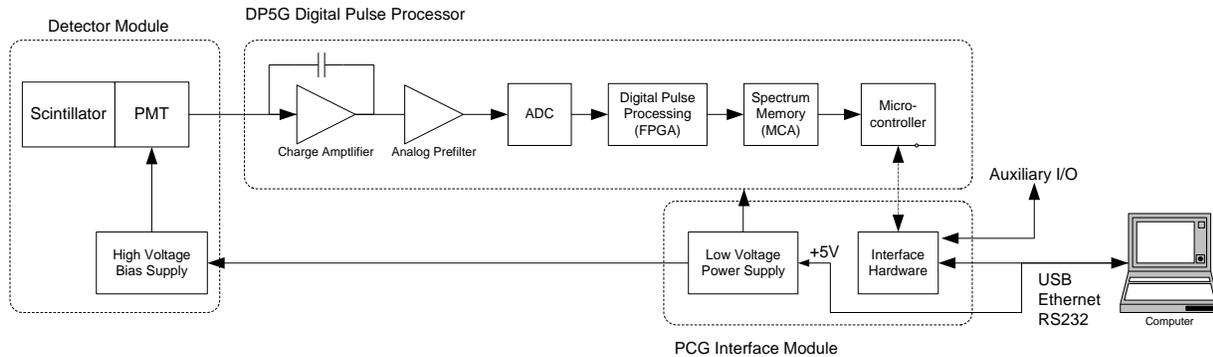
1	Introduction	2
1.1	DP5G Description	2
1.2	DP5 Family	2
1.3	Options and Variations	3
2	Specifications	3
2.1	Spectroscopic Performance	3
2.2	Processing, physical, and power	3
3	Mechanical Interface	5
3.1	DP5G Dimensions.....	5
3.2	Connectors	5
4	Electrical Interface	6
4.1	Input signal interface	6
4.2	Power Interface.....	6
5	DP5G Design.....	6
5.1	Analog prefilter	6
5.2	DP5G to PCG Connector.....	9
6	Application Advice	11
6.1	Configuring the DP5G for a particular scintillator.....	11
7	PCG Auxiliary Board	17
7.1	PCG-901 Connectors	17
7.2	PCG-902 Connectors	18
7.3	PCG Electrical Interface.....	21
7.4	PCG HV Bias Control.....	21
7.5	PCG Mechanical Dimensions and Configuration	22



1 Introduction

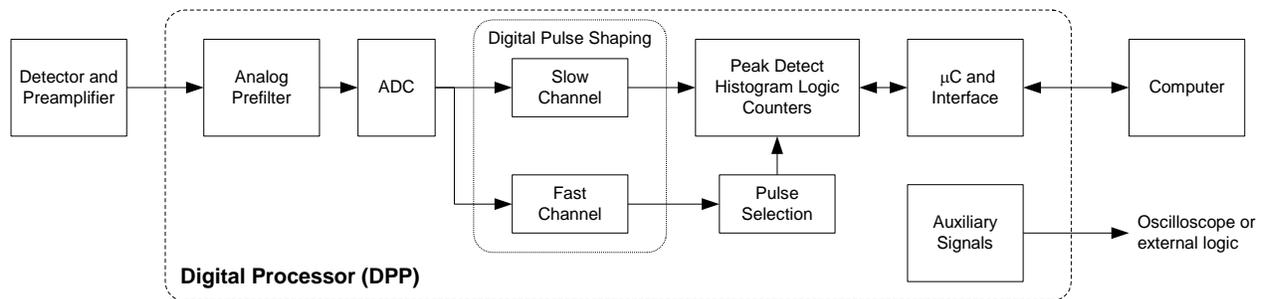
1.1 DP5G Description

The DP5G is a member of Amptek's DP5 signal processing family. It is a component in a complete γ -ray spectrometer, sketched below. The DP5G includes only the core signal processing functions and is optimized for scintillation spectroscopy. A complete system must also include a detector module (scintillator, PMT, HV supply, tube base) and interface circuitry with power supplies and connectors for the serial connections. Amptek can provide an OEM user with the DP5G alone, or can provide it with a PCG interface module, or can provide a complete system, including the detector module. The complete system is a separate Amptek product, the Gamma-Rad5.



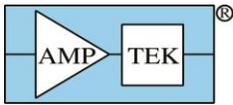
1.2 DP5 Family

Amptek has a family of products built around its core DP5 digital pulse processing technology, designed for pulse height spectroscopy. It was originally designed for the detection of ionizing radiation, principally X-ray and gamma-ray spectroscopy. A generic system, illustrated below, includes (a) a sensor, a.k.a. detector, (b) a charge sensitive preamplifier, (c) analog prefilter circuitry, (d) an ADC, (e) an FPGA which implements pulse shaping and multichannel analysis, (f) a communications interface, (g) power supplies, (h) data acquisition and control software, and (i) analysis software.



The core DP5 technology shared by all the systems includes the ADC, the FPGA, the communication interface, and the data acquisition and control software. All products in the DP5 product family include nearly the same digital signal processing algorithms, the same communication interfaces (both the primary serial interfaces and the auxiliary I/O), and use the same data acquisition and control software. The DPPMCA software package is a complete, compiled data acquisition and control software package used across the family; Amptek also offers an SDK for custom software solutions.

The products in the DP5 family differ in the sensor for which they are designed, which leads to changes in the analog prefilter, power supplies, and form factor. They also differ in their completeness:



some of Amptek's products are "complete", with elements (a) through (i), while others offer only a portion of the functionality for the user to integrate into a complete system.

1.3 Options and Variations

- The DP5G is available using either a 20 MHz or 80 MHz ADC. The 20 MHz ADC is sufficient for NaI(Tl), where the count rate and timing are limited by the decay time constant of the scintillator, and it draws less power than the 80 MHz option. The 80 MHz ADC can be operated at 20 MHz but still draws more power. It is recommended for use with faster scintillators.
- The preamplifier time constant is available at either 1.6 or 3.2 μ s. The slower, 3.2 μ s tail is suitable for slower scintillators such as NaI(Tl). The 1.6 μ s tail supports higher count rates. Note that the pulse peaking time is not limited by the preamplifier time constant; the digital shaping is unlike that of traditional analog systems.
- The DP5G is a very small board with minimal components. It was designed to be integrated inside a complete instrument. The DP5G does not contain low voltage power supplies or standard USB and Ethernet interface connectors. The user can build their own system board with these or can procure from Amptek the PCG boards which contains these. The typical application uses two PCG boards: the PCG-901 has low voltage supplies, USB connector, and Ethernet connector while the PCG-902 has the RS232 transceiver and an auxiliary connector.

The DP5G/PCG stack is a more complete signal processing solution than the DP5G alone. The TB5 includes these two along with an HVPS and enclosure, making it a complete electronic system, while the Gamma-Rad5 also includes the scintillator and PMT. These standard building blocks permit a user to build up scintillation spectroscopy systems which are ideal for their specific applications.

2 Specifications

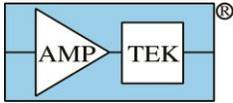
2.1 Spectroscopic Performance

The spectroscopic performance is determined by the scintillator material and the PMT. The performance obtained with a NaI(Tl) scintillator and the TB-5 is equivalent to that shown in the Gamma-Rad5 manual. For a 76x76 mm NaI(Tl), Amptek typically measures <7% FWHM at the 662 keV line of ¹³⁷Cs.

2.2 Processing, physical, and power

Several of the Gamma-Rad5 specifications differ from those in the standard, family-wide manual. Specifications not listed here are unchanged from the standard in the family.

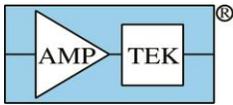
Pulse Processing Performance	
Gain Settings	Four software selectable coarse gain settings are available: 3 MeV full scale to 750 keV full scale. Fine gain is adjustable between 0.75 and 1.25. System gain can also be changed by changing the HV on the PMT.
Pulse Shape	Trapezoidal, software selectable from 0.8 to 102.4 μ s. The flat top has 63 software selectable values for each peaking time. For NaI(Tl), T_{peak} is usually set to 2.4 μ s and T_{flat} to 1.0 μ s, with a pulse shape similar to an analog 1 μ s shaping time. The fast channel, used for pile-up rejection and pulse shape discrimination, has



	a pulse pair resolving time of 0.25 or 0.5 μ s.
Pile up interval	This is approximately equal to the sum of T_{peak} , and T_{flat} , and the scintillator time constant.
Gain Stabilization	The gain from the NaI(Tl) and PMT is well known to vary with temperature. A software gain stabilization algorithm is available.
Maximum Count Rate, Dead Time, and Throughput	With the typical configuration, $T_{peak}=2.4 \mu$ s, the maximum input count rate is 1.5×10^5 cps with a throughput of >50% and good baseline stability and pile-up rejection. At $T_{peak}=0.8 \mu$ s, the maximum input count rate is 2×10^5 cps.
Custom Configuration	The DP5G is set at the factory for either a 20 MHz or 80 MHz clock. For NaI(Tl), the 20 MHz is standard, yielding the specifications listed above. The 80 MHz setting allows for peaking times down to 0.1 μ s in the slow channel and 0.05 μ s in the fast channel but draws more power. The 80 MHz setting is recommended for custom scintillation materials with faster decay times, fast pulse shape discrimination, or other unique requirements.

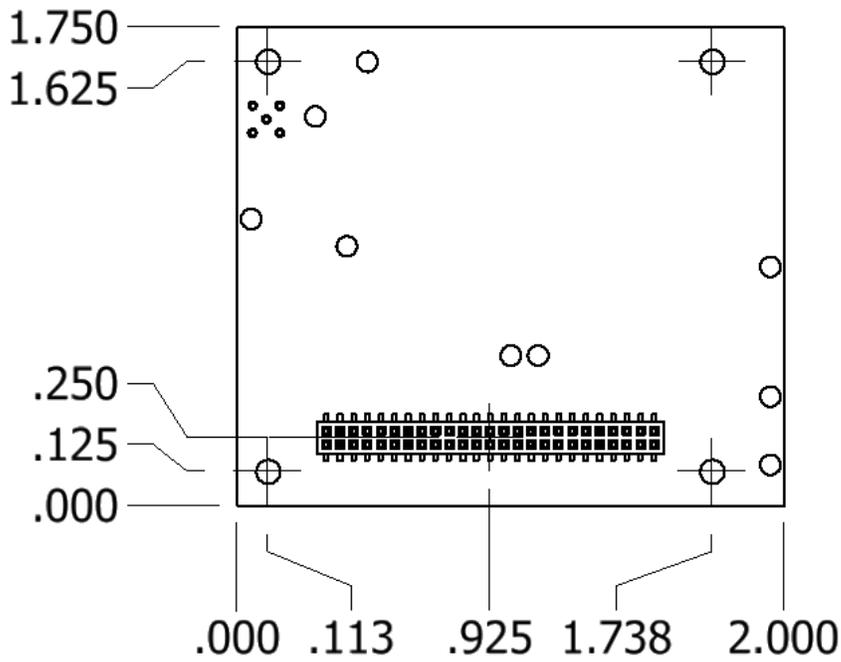
Physical	
Dimensions	2.0" x 1.75"
Weight	13 g

Power	
Nominal Input:	@ +3.3 VDC: 165 mA (0.85 W) typical , 20 MHz ADC, USB interface 190 mA (1.0 W) typical , 20 MHz ADC, Ethernet 80 MHz ADC adds 30 mA (typical)
Input Range:	+3 V to +6.4 V
Power Source:	USB bus for USB interface External DC PoE for Ethernet interface



3 Mechanical Interface

3.1 DP5G Dimensions



Note: the PCG mechanical interface can be found in section 7.

3.2 Connectors

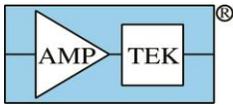
Signal Input

MMCX Connector: FCT Electronics PN A22J2PC-000-10G

An example mate I sa MMCX to BNC cable, Samtec RF174-Q3SP1-Q4SP3-0300. (Amptek PN ACH-466).

Main Interconnect

Samtec PN CLP-125-02-L-D-A



4 Electrical Interface

4.1 Input signal interface

The input to the DP5G is the AC coupled anode output of a PMT, a current pulse, not a voltage pulse. The current into U11 is integrated on the 6800 pF feedback capacitor.

4.2 Power Interface

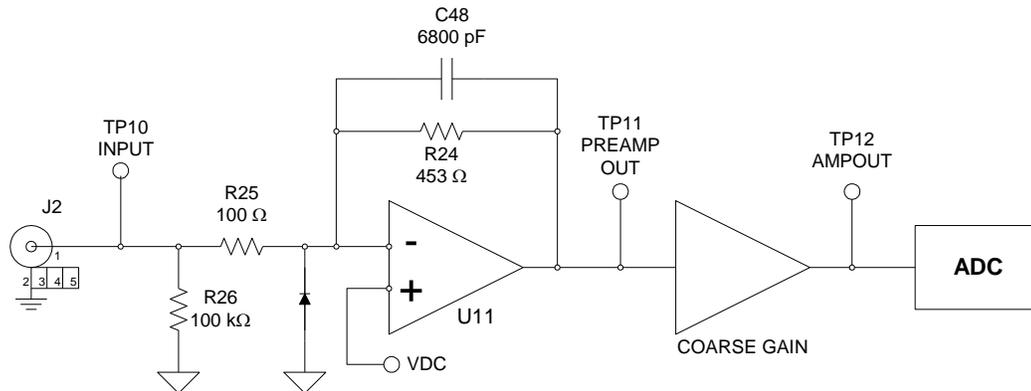
The DP5G requires a regulated +3.3VDC supply, from which digital and analog circuitry is operated. It has a switching regulator which produces 2.5V and 1.2V to operate digital circuitry.

Amptek provides the PCG board, as an option, which has additional power supplies and also standard USB, Ethernet, and AUX connectors. The DP5G is a very small board with minimal components, ideal for integrating within instruments which provide their own power and interface components. The PCG is documented in section 7 of this document

5 DP5G Design

5.1 Analog prefilter

The analog input of the DP5G is significantly different from that of the DP5. Some key changes include (1) the fact that the first stage is a charge amplifier, optimized for signals from a scintillator/combination, (2) the coarse gain range is smaller, from 1.6 to 6.5, because one can adjust the PMT bias for a larger range, and (3) the input connector is a coaxial connector, more suitable for a PMT output.

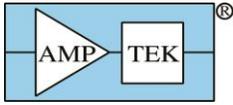


Charge Amplifier

Schematic of charge amplifier at DP5G input

- **Input signal:** The input to the DP5G is the AC coupled anode output of a PMT, a current pulse, not a voltage pulse. The current into U11 is integrated on the 6800 pF feedback capacitor.

NOTE: This has been a source of confusion for many customers. The current pulse from the PMT must be connected directly to the DP5G. If the PMT is first connected to an external preamplifier or transimpedance amplifier, and the preamp output connected to the DP5G, it will not work. These preamplifiers produce a voltage pulse while the DP5G requires a current input. The circuitry around U11 must be modified if the DP5G is preceded by any amplifier. Contact Amptek, Inc. for details.



The DP5G can be used with either a positive or negative bias on the PMT. In either case, the signal is a pulse of electrons into the DP5G, as illustrated in **Error! Reference source not found.**

- **Charge amplifier conversion gain:** The input to the charge amplifier is a current pulse with total charge Q_{IN} . The charge amplifier has $C_F=6800$ pF, with a conversion gain of $1/C_F$, meaning that at TP11 one measures a voltage pulse with magnitude

$$\Delta V_{TP11} = \frac{Q_{IN}}{C_F}$$

In a typical application, $Q_{IN} = 10^{-9}$ C, so $\Delta V=150$ mV. For example, if one measures a gamma ray spectrum with a scintillator and a photomultiplier, the charge can be written

$$Q_{IN} = E_\gamma N_{phot} \varepsilon G_{PMT}$$

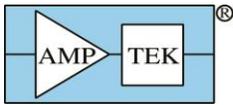
where E_γ is the energy of the gamma-ray (in MeV), N_{phot} is the light yield of the scintillator, in photons/MeV, ε is the quantum efficiency (the product of the light collection efficiency of the system and the quantum efficiency of the photocathode), and G_{PMT} is the gain of the photomultiplier tube. For a 662 keV gamma-ray measured by a NaI(Tl) scintillator (3.8×10^4 photons/MeV) with a bialkali photocathode ($\varepsilon=0.3$) and 900V bias on a typical 9 stage PMT ($G=10^5$), $Q_{IN}=1.2 \times 10^{-10}$ C and $\Delta V=18$ mV.

- **Coarse gain:** There are four coarse gain settings: 1.6, 2.6, 4.1, and 6.5. This permits the system gain to be changed by a factor of four, with overlapping fine gains. One can adjust the HV bias on the PMT to obtain a larger gain range.
- **Pulse Shape:** The input signal, the current pulse into J2 from the preamplifier, typically has a very fast rising edge and then an exponential decay determined by the properties of the scintillator. The amplifier integrates this current to measure the charge but with a 3.2 μ s time constant. The figure below shows the pulse shapes measured for a specific example, ^{60}Co gamma-rays measured using a NaI(Tl) scintillator with a PMT. For more information, refer to page **Error! Bookmark not defined.**

The light blue trace represents the AC coupled anode output of the PMT. It was measured at TP10. The current pulse across the 100 k Ω resistor produces a voltage pulse which can be measured. The 0.23 μ s decay time of the NaI(Tl) can clearly be seen.

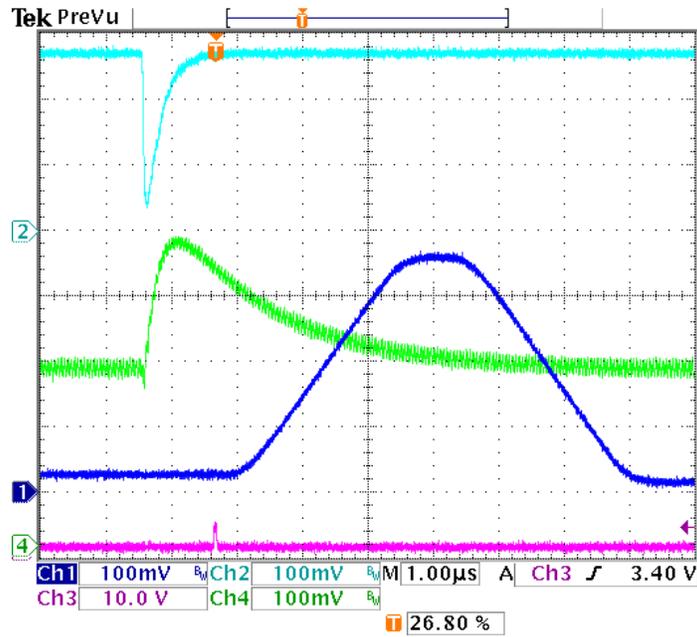
The green trace was measured at TP12, the input to the ADC. There is a DC offset of about 300 mV, determined by VDC. The risetime of this pulse is determined by the time constant of the scintillator. The decay time of this pulse is due to the 3.2 μ s time constant of the U11 feedback components.

The dark blue trace is the shaped pulse, measured at the DAC output. The peaking time was 2.4 μ s, the flat top 1 μ s. The scintillator time constant shifts the pulse shape from the true trapezoidal shape, which is the impulse response of the pulse shaping.

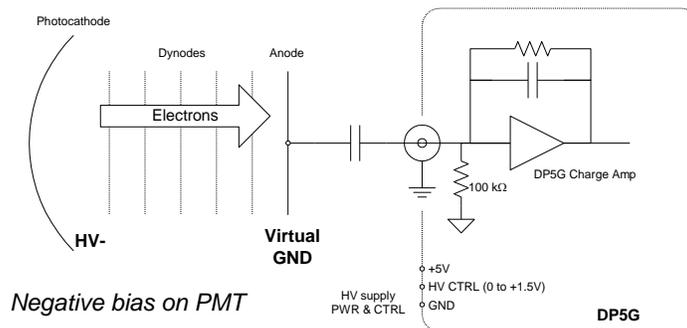
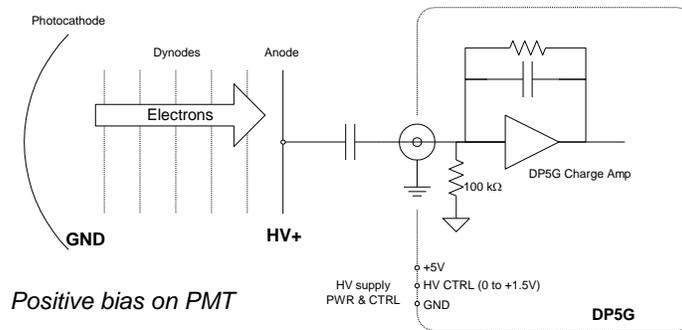


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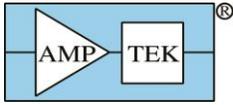
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Oscilloscope traces measured using a NaI(Tl) scintillator and a PMT. Light blue: PMT output measured at TP10. Green: TP12 (ADC INPUT) Dark blue: Shaped pulse



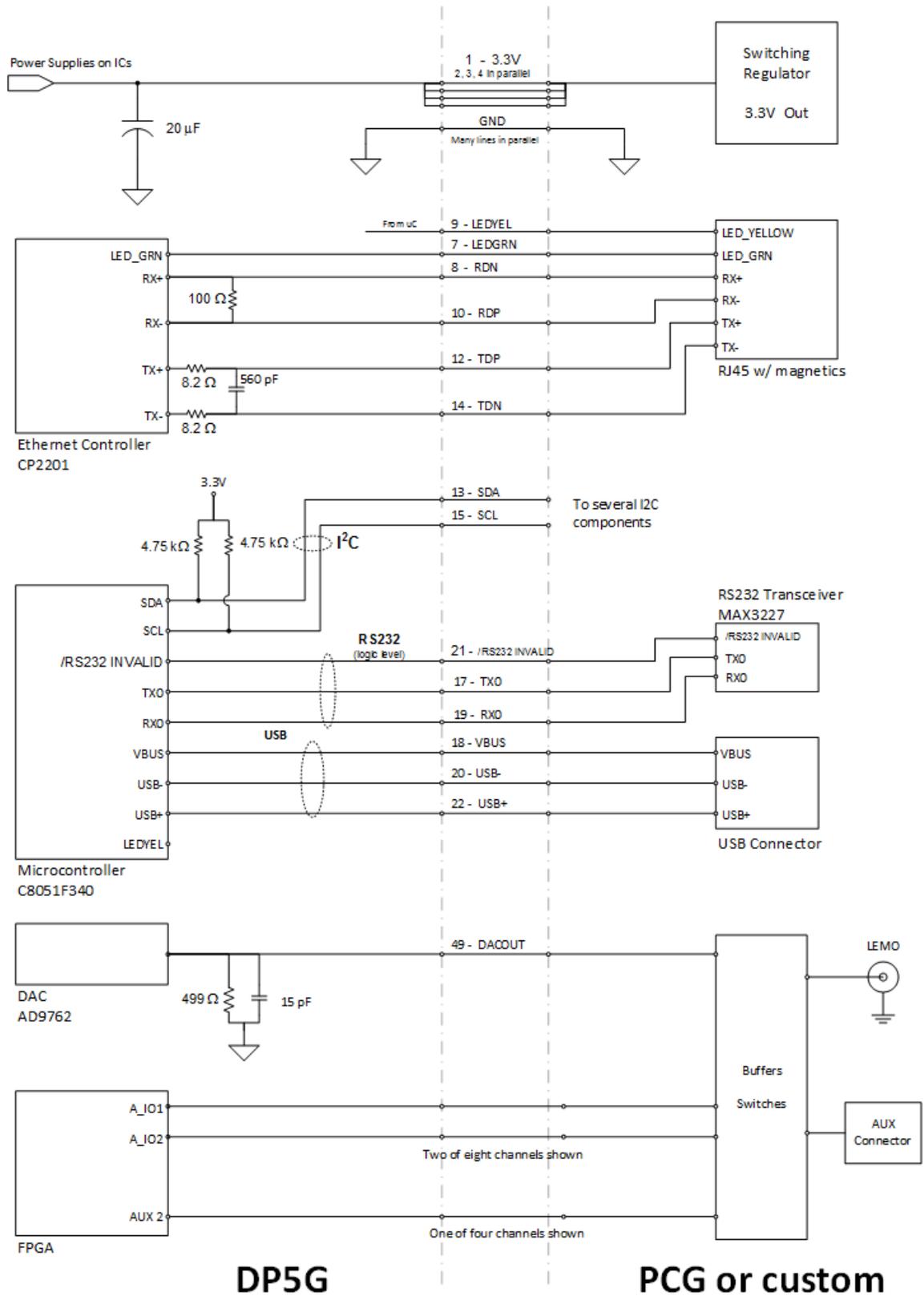
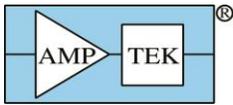
Figures showing operation with both positive and negative PMT bias voltages. In both cases, the signal is a pulse of electrons across the coupling capacitor and into the DP5G charge amp. Note: the “negative bias” option may be implemented with DC coupling.



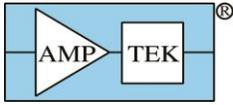
5.2 DP5G to PCG Connector

J1 on the DP5G is the main connector to the PCG (J4 on the PCG). This is the 50 pin connector which separates the microcontroller, FPGA, and similar circuits on the DP5G from the Ethernet connector, USB connector, power regulators, and similar circuits on the PCG. The user may develop a custom interface board but will utilize the 50 pin connector. The DP5G interface is defined by the table, schematic, and discussion below.

Pin	Name	Description	Pin	Name	Description
1	3.3V	Pins 1-4 are connected in parallel and are the input power for the DP5G. This must be regulated 3.3VDC.	26	Reserved	Do Not Connect
2	3.3V		27	GND	
3	3.3V		28	GND	
4	3.3V		29	A_IO1	SCA 1 (or streaming mode bus)
5	GND		30	A_IO2	SCA 2 (or streaming mode bus)
6	GND		31	A_IO3	SCA 3 (or streaming mode bus)
7	LED_GRN	Ethernet LED	32	A_IO4	SCA 4 (or streaming mode bus)
8	RDN	Ethernet RX-	33	GND	
9	LED_YEL	Ethernet LED	34	GND	
10	RDP	Ethernet RX+	35	A_IO5	SCA 5 (or streaming mode bus)
11	GND		36	A_IO6	SCA 6 (or streaming mode bus)
12	TDP	Ethernet TX+	37	A_IO7	SCA 7 (or streaming mode bus)
13	SDA	I2C SDA	38	A_IO8	SCA 8 (or streaming mode bus)
14	TDN	Ethernet TX+	39	GND	
15	SCL	I2C SCL	40	GND	
16	GND		41	AUX1	Digital auxiliary I/O
17	TX0	Logic level RS232 TX0	42	AUX2	Digital auxiliary I/O
18	VBUS	USB VBUS	43	AUX3	Digital auxiliary I/O
19	RX0	Logic level RS232 RX0	44	AUX4	Digital auxiliary I/O
20	USB-	USB D-	45	GND	
21	/RS232_INV	Input to DP5G from external RS232 transeiver on PCG: logic high = valid RS232 level detected	46	GND	
22	USB+	USB D+	47	Reserved	Do Not Connect
23	GND		48	Reserved	Do Not Connect
24	Reserved	Do Not Connect	49	DACOUT	Used to display processed pulses
25	Reserved	Do Not Connect	50	Reserved	Do Not Connect



Schematic of power and communication interface between DP5G and the PCG or custom board.



Interface Discussion

- **Power input:** The DP5G requires a regulated 3.3V input. The DP5G does not regulate this input and has no protection circuitry. It directly powers the digital circuits, and through a filter powers the analog circuitry. Input current is typically 160 mA. Pins 1-4 are in parallel for redundancy and reduced voltage drop.
- **Ethernet:** The CP2201 Ethernet controller connects via J1 to an Ethernet connector with magnetics on the PCG (P/N Tyco 660572-1). Refer to the CP2201 data sheet for details. Note that the "Ethernet Yellow" LED line is driven by the μ C on the DP5G.
- **I²C:** There are several I²C devices used on the PCG, including a DAC used to control the HV supply in the Gamma-Rad5 (discussed below). A customer may use additional I²C devices and command them through the DP5G. See the DP5 programmer's guide for details.
- **RS232:** The DP5G μ C produces logic level RS232 signals, which are sent via J1 to the PCG. An RS232 transceiver is located on the PCG.
- **USB:** The DP5G μ C produces the USB signals, which go to a standard USB connector on the PCG. The VBUS line is only used by the DP5G as an indicator to the μ C. On the PCG, the USB VBUS line can be used to power the system (discussed below).
- **Auxiliary:** There are several auxiliary outputs available on the DP5G. These same lines are available on the DP5 and their use is documented in the DP5 User Manual. The analog output (used to display shaped pulses for diagnostic purposes) is generated by a DAC on the DP5G. The remaining auxiliary signals are digital inputs and outputs which connect directly to the FPGA on the DP5G. The PCG contains buffer and protection circuitry.

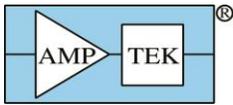
The AUX1 and AUX2 lines on the DP5G correspond to the AUX_IN_1 and AUX_IN_2 lines on the DP5. The AUX3 and AUX4 lines on the DP5G correspond to the AUX_OUT_1 and AUX_OUT_2 lines on the DP5.
- **Reserved:** There are several lines on J1 which are reserved. No connection should be made to these.

6 Application Advice

6.1 Configuring the DP5G for a particular scintillator

The default configuration loaded in the DP5G was based on NaI(Tl) and a particular PMT. You will need to change some of the parameters to obtain good performance with your scintillator/PMT module. The following parameters often require adjustments:

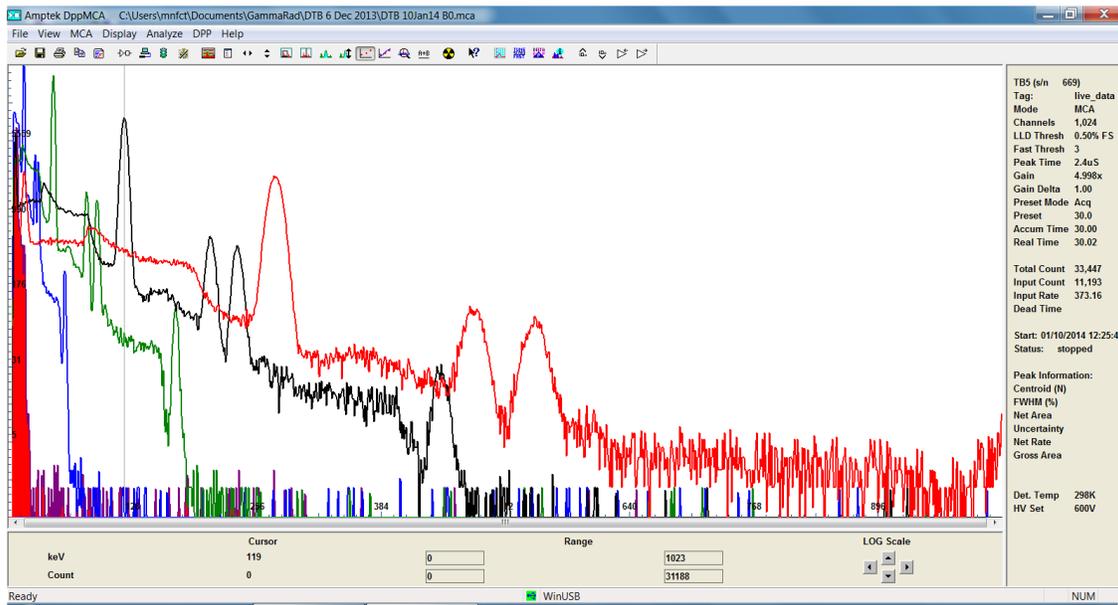
- **High voltage bias:** Every PMT has a slightly different gain versus bias curve. Even among "identical" PMT/scintillator modules, the HV bias will generally need to be changed to obtain consistent spectra. There is also a "gain" parameter in the signal processor. We recommend adjusting the HV bias for large changes in gain, then using processor's gain parameter for fine tuning.
- **Pulse shaping parameters:** There are several different parameters which control the pulse shaping: T_{peak} , T_{flat} , T_{fast} , T_{scint} , T_{PUR} . The optimum settings will vary with the scintillator material. Adjusting these will primarily affect pile-up so they are most important at high count rates. In many cases, they will not need adjusting.



- **Thresholds:** There are two "thresholds" in the logic: a slow threshold (used in pulse height analysis for the main spectrum) and a fast threshold (used in the fast channel, for pile-up rejection and for measuring input count rate). The ideal setting can be a function of the system gain (including HV bias) and of the pulse shaping so they should be adjusted after the other parameters are set.

High Voltage

The figure below shows spectra taken from a single NaI(Tl)/PMT/TB-5 units, using DPPMCA, at HV bias settings of 600V, 700V, 800V, 900V, and 1000V. The source consisted of 1 μ Ci ¹³⁷Cs and 1 μ Ci ⁶⁰Co. When the TB-5 was first turned on, at 600V, only a few counts were seen in the lowest channels. The system gain increased by about a factor of 2.5 for every 100V bias.

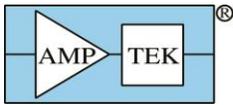


Procedure: We recommend beginning at a HV setting around 600V, with an analog gain around 5. Put a source in front and increase HV in 100V steps until the photopeaks are within a factor of two of the correct channels. The HV and/or analog gain can be further refined to get the desired range. The DPPMCA "Calibrate" button can be used to calibrate the energy scale. Its use is documented in the DPPMCA HELP.

Thresholds

The TB-5, like Amptek's other digital processors, has both a "fast" and a "slow" channel. The slow channel is optimized for good resolution; it is the input to the pulse height analysis. The fast channel is optimized for separating counts; it is input to the fast counter (to determine true input count rate) and to the pile-up rejection circuitry. Both channels have thresholds. The slow threshold functions as both a low level discriminator (pulses below it are rejected) and is used in the peak detect circuit. The fast threshold is purely a low level discriminator in the fast channel. For best performance, these should be set just above the electronic noise.

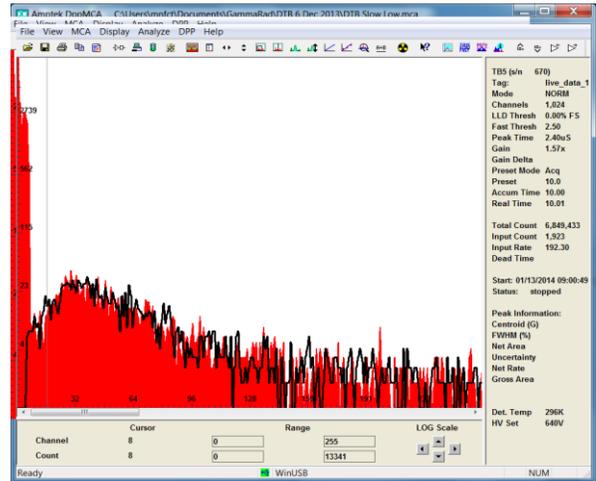
The DPPMCA software includes an "autotune threshold" function to set these above the noise but the current algorithm does not work well for scintillators so manual adjustment is recommended. The current algorithm raises the thresholds until the total rates above threshold is only 1 cps, assumed to be noise. The background radiation in a scintillator is generally above this, causing the algorithm to fail.



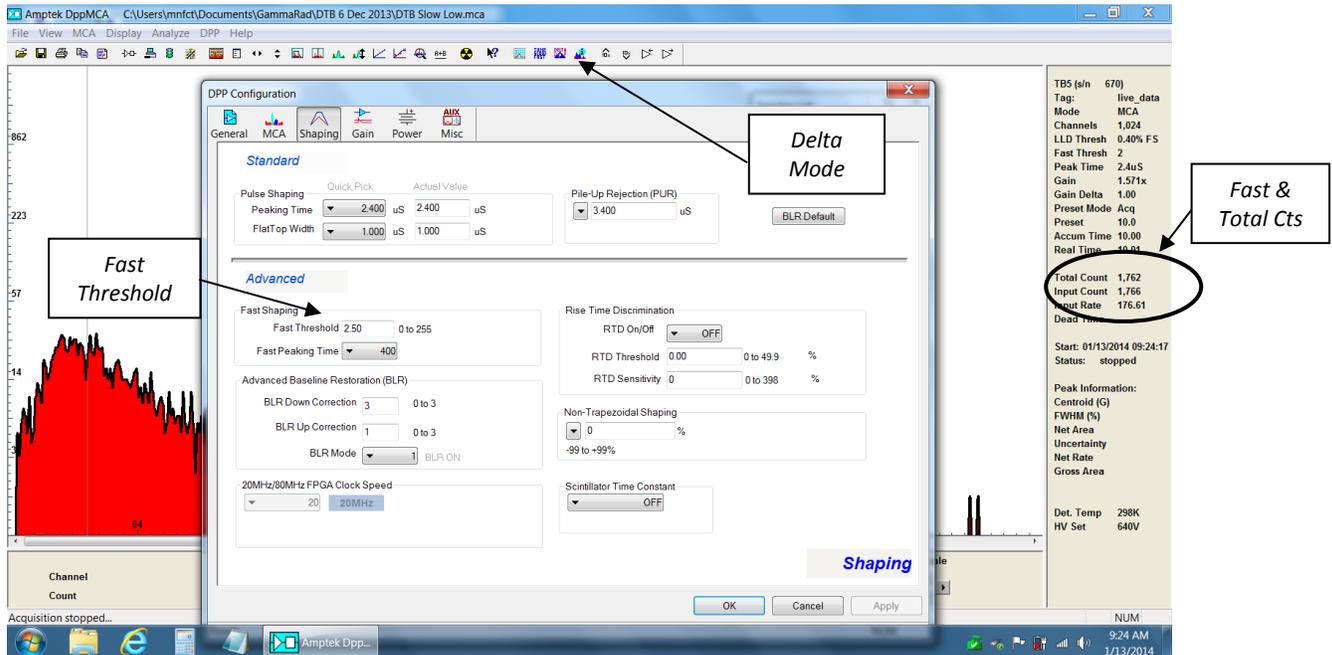
Therefore, we do not recommend use of "auto-tune" with the TB-5. An improved version will be released in the future.

Procedure: First, set the slow threshold. To do this turn off "pile up rejection" (if the fast threshold is incorrect, it will affect pile-up rejection and thus the observed spectrum). Remove all sources and observe the spectrum. Manually place the threshold just high enough to avoid noise counts, as illustrated in the spectrum to the right. The filled red spectrum has the slow threshold too low, so noise fluctuations are recorded as real pulses. The black trace shows natural background in our lab.

You can manually set the threshold either by placing the cursor in the correct channel and pressing the "F8" key or by opening the "Acquisition Setup" dialog to the "MCA" tab and entering a value.

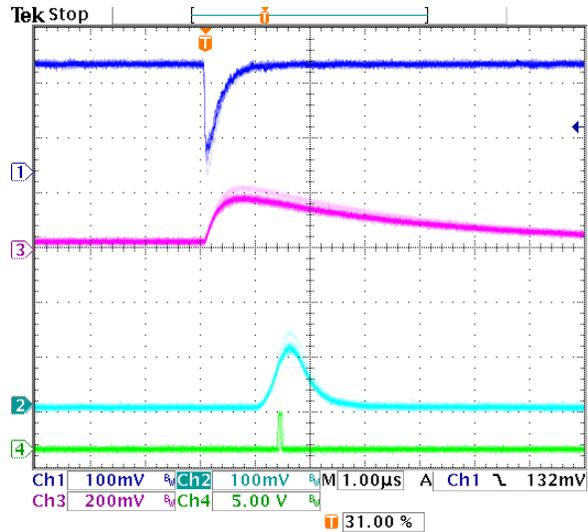
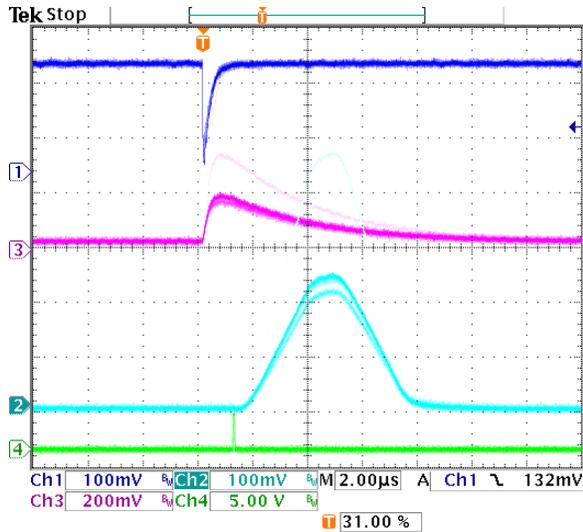
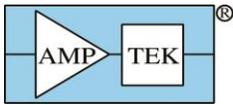


Second, set the fast threshold. To do this, put the system into "delta mode", where the data are updated without integrating, making it easy to see changes. Compare the "Total counts" and "Fast counts", in the Info Pane. If only background radiation is present, the two should be very similar. If the "Fast counts" are much higher (lower) than the "Total counts", then adjust the Fast threshold higher (lower). After tuning, place a stronger source to get a few kcps rate and verify that the "Fast counts" are higher than the "Total counts".



Pulse Shaping

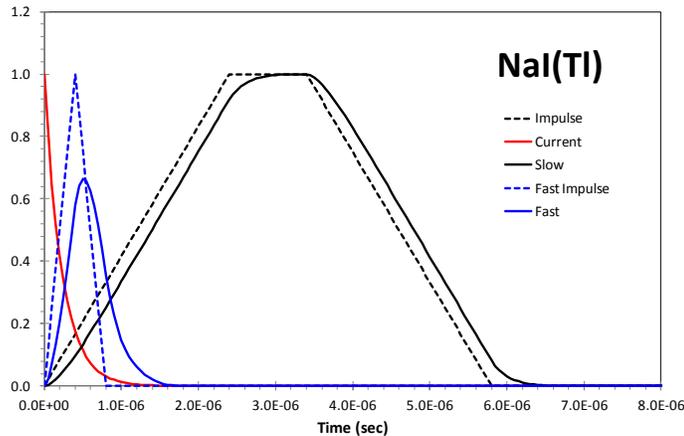
The figure below shows oscilloscope traces taken with a TB-5. The dark blue trace is the current output from the PMT while the magenta traces show the output from the charge amplifier. The light blue trace shows the shaped output (left) and fast output (right), for $T_{peak}=2.4 \mu s$, $T_{flat}=1.0 \mu s$, and $T_{fast}=0.4 \mu s$. The green trace shows the ICR output, a fast channel trigger. The light blue traces can be seen on the AUX1 output and the green trace on the AUX2 output. The others are internal to the TB-5.

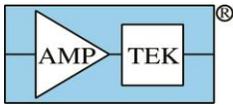


Peaking time, flat top, and fast channel shaping

A shorter peaking and flat top duration will lead to a shorter duration pulse but one cannot shorten them arbitrarily without loss of performance. The scintillator has a characteristic time constant or time constants; the shaped pulse will be nonzero for several times these time constants. For the best, overall performance, we recommend a peak time and flat top several times longer than the scintillator time constant. The user may shorten these and the spectrometer will still function and indeed will give good energy resolution. But pulses will occur on the tails of preceding pulses, and this can affect resolution, stability, and even triggering (if a small pulse occurs on the tail of a large one, it may not be detected).

The basic trapezoidal shaping used by most digital pulse processors, including Amptek's TB-5, was originally designed for use with semiconductor or solid state detectors (SSDs). There is an important difference in the signals produced by a scintillator versus an SSD: in an SSD, the current flows for a finite time, the time required for the carriers to cross the detector. This is a finite impulse. In a scintillator, the optical current decreases exponentially with time (or as the sum of exponentials). This is an infinite impulse and it lengthens the shaped pulse. The plot below shows the computed response for a finite current (dashed) and for a NaI(Tl) time constant (solid curve). The difference can be important, if a low energy photon is on the tail of a much larger event.

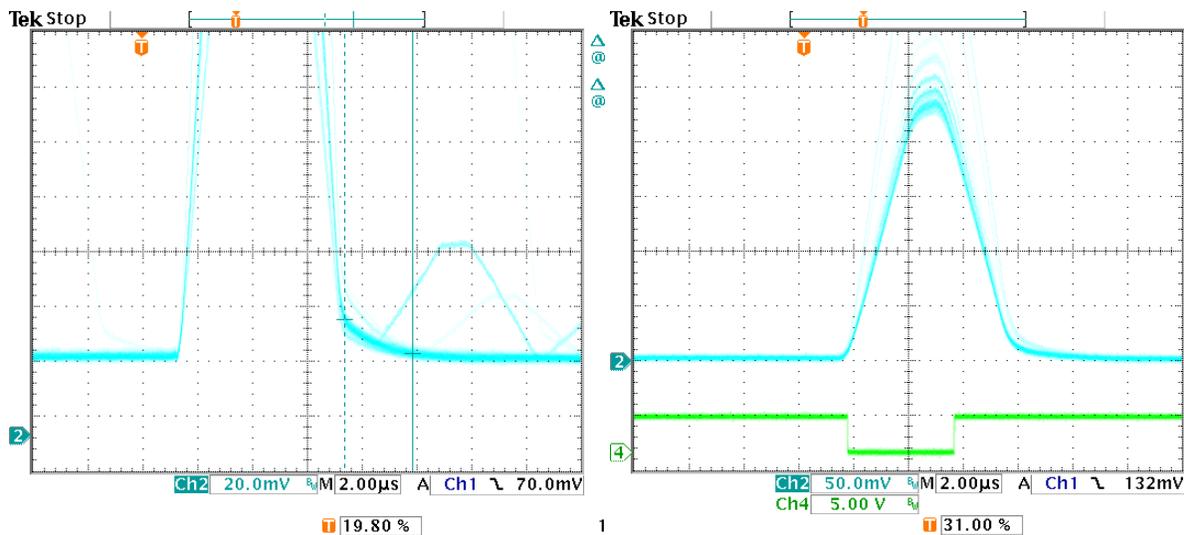




Pile-up inspection interval

By default, the digital processor in the TB-5 uses a pile-up inspection interval which is the sum of T_{peak} and T_{flat} . This is the appropriate interval for a detector with a finite impulse but does not entirely account for the tail arising from the infinite impulse of the scintillator. The oscilloscope trace on the left below illustrates the difference. The dashed vertical line marks where the end would be for a finite response; the slow component in the NaI(Tl) leads to a tail of about 2 μ s longer. To accommodate this, a non-standard pile-up inspection interval can be commanded in Amptek's firmware. Using an interval longer than the default will reduce the throughput somewhat while also reducing pile-up. The user must determine the optimum for any given application.

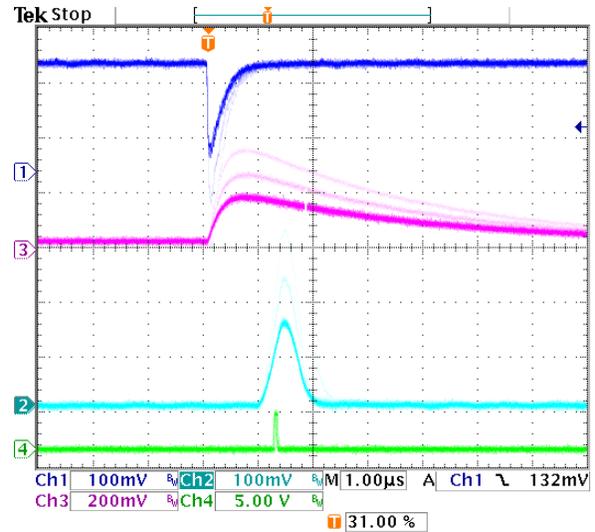
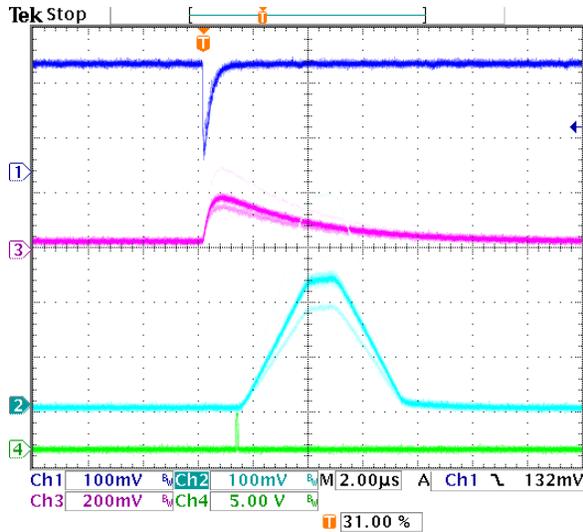
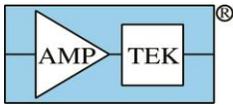
Procedure: In the DPPMCA software, go to "Acquisition setup", the "Shaping" tab. Use the PUR box to set a particular value, in microseconds. This should be the complete PUR interval: T_{peak} , plus T_{fast} , plus the "tail" interval. Then click "Apply". Note that, there is a maximum allowable value; this varies with peaking time.



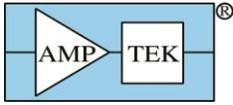
Oscilloscope traces showing pile-up with shaped pulses. Left: Illustration of extended interval due to scintillator time constant. The dashed cursor shows where the shaped pulse would terminate with a finite impulse; the solid cursor shows where the pulse tail is negligible with the scintillator. Right: The green trace shows the output of "ONE SHOT", an AUX output signal used in the pile-up rejection logic, indicating the end of the pile-up inspection interval.

Scintillator time constant

Amptek has introduced a new processing parameter which reduces the effect of this tail. Termed the "scintillator time constant", it can correct the shape for an exponential decay. Most real scintillators have two or more time constants and this algorithm only corrects for one time constant. The plots below show the shaped and fast outputs after correction (for NaI(Tl)); note that the shape is closer to a trapezoid, the tail is reduced, and the fast channel pulse is narrower. Note also that the fast channel pulse is larger; this correction effectively increases the gain of the fast channel.



Procedure: To use the scintillator time constant, go "Acquisition setup", to the "pulse shaping" tab. Set the "scintillator time constant" to the nominal value of the primary time constant of the scintillator, in nanoseconds. For NaI(Tl), for example, set this to 230. Then click "apply". Note: Because the gain of the fast channel has increased, the fast threshold will need to be increased as well. When the scintillator time constant is first applied, the fast rate usually increases dramatically due to (false) noise triggering. To view the effect of this change, connect an oscilloscope to AUX1 and set the DAC output to the shaped or fast signals. You can observe the light blue and green traces above (the dark blue and magenta are observed at nodes inside the TB-5 package).



7 PCG Auxiliary Board

The DP5G contains the core signal processing functions but does not contain signal connectors or any power supplies. Amptek can provide an optional additional module, the PCG, which provides these functions. There are actually up to three circuit boards in the PCG module:

- The PCG-901 is the “core” auxiliary board. It connects to the DP5G and includes low voltage power supplies along with the USB, Ethernet, external power, and AUX 1 LEMO connector.
- The PCG-902 can plug into the PCG-901. The PCG-902 provides the RS-232 interface and also has the AUX 2 LEMO connector and the AUX 3 connector.
- The PoE-901 can plug into the PCG-901 and provides the PoE capability.

Section 7.3 shows the architecture of the low voltage power supply, which takes a loosely regulated 5V input and produces the voltage used on the DP5G. It also shows the circuit used to control a HVPS. Note that the PCG does not include the PMT HVPS.

Note: the PCG-901 Rev Dx replaced the PCG-901 Rev Cx in 2014. While functionally the same, the Rev Dx includes the ability to accept a PoE (Power over Ethernet) daughter board, and the interconnect to the PCG-902 AUX board is different (as documented below). Otherwise, the connectors are the same.

Each board has a sticker which includes the part number, revision, and serial number.

The PCG-901 Rev Dx (and later) is designed to mate with the PCG902 Rev Cx (and later) AUX board. One of the differences between these boards and the earlier ones is that the RS232 and SCA transceivers were relocated from the PCG-901 to the PCG-902 AUX board. Hence, on the J7 interconnect on the PCG-901 Rev Dx, RS232 signals are logic level, and the SCAs are unbuffered.

The documentation included here is for the PCG-901 Rev Dx and PCG-902 Rev Cx, unless otherwise noted. If mechanical drawings, etc. are needed for the obsolete PCG-901 Rev Cx (or PCG-902 Rev Bx), please contact Amptek.

7.1 PCG-901 Connectors

Power (J1)

Provides power to the PCG. Switching regulators on the PCG (discussed below) provide power to PCG circuitry as well as to the DP5G and to the HV supply.

Power Jack on PCG: P/N Molex 39-30-1020.

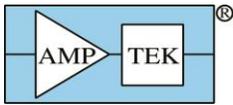
Mating Plug: Housing P/N Molex 39-01-2020. Terminal P/N could be Molex 44476-1112 (18-24 ga) or Molex 44476-3112 (16 ga).

Pin #	Name
1	VIN (+5 V DC)
2	GND

PMT (J2)

Provides power and a DC reference voltage which can control a PMT high voltage power supply. Note that the DP5G does not include a HV power supply, but these signals can interface to and control many suitable HVPS modules. The control circuit is discussed below.

Receptacle on PCG: Molex 53014-0310



Mating Plug: Housing Molex 51004-0300, Terminal Molex 50011-8100

Pin #	Name
1	HV CONTROL
2	PWR (5VDC)
3	GND

Ethernet (J12) **[PCG901 Rev Dx and later]**

Ethernet (J3) **[PCG901 Rev Cx and earlier]**

Standard Ethernet connector (RJ-45)

USB (J5)

Standard USB Type B jack. The DP5G can be powered from the USB bus (see discussion below). The orange jack indicates that it features higher mating/demating force than a standard USB jack.

Auxiliary LEMO (J6)

P/N Lemo EPK 00.250.NTN

This is the only coaxial auxiliary I/O line available on the PCG-901. For maximum flexibility, the DP5G includes an analog switch which permits one to connect either AUX1 or DACOUT to the LEMO. Since AUX1 is AUX_IN_1, one can use the LEMO with the DP5G general purpose counter, e.g. to count pulses from a ³He neutron monitor. We recommend connecting DACOUT to the LEMO for diagnostic purposes, to view the shaped pulses, as discussed in the DP5 User Manual.

Auxiliary (J7) **[PCG901 Rev Dx and later]**

Connects from the PCG-901 to the PCG-902

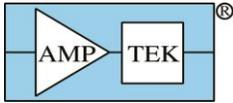
26-pin 0.050" spacing. For orientation, refer to DP5G/PCG assembly drawing.

Connector on PCG: Samtec SLM-113-01-G-D.

Mates with P/N Samtec DWM-13-58-L-D-325.

Pin #	Name	Pin #	Name
1	3.3V	2	3.3V
3	TX0 [logic-level RS232]	4	RX0 [logic-level RS232]
5	/RS232_INVALID	6	SPARE
7	SCA_DIR*	8	SCA_OE*
9	SCA 1*	10	SCA 2*
11	SCA 3*	12	GND
13	SCA 4*	14	SCA 5*
15	GND	16	SCA 6*
17	SCA 7*	18	SCA 8*
19	AUX2	20	AUX2DIR
21	AUX3	22	GND
23	AUX3DIR	24	AUX4
25	AUX4DIR	26	GND

*SCA1-SCA8 signals are unbuffered on J7. SCA_DIR and SCA_OE are control signals for a SN74LVC245 transceiver on the PCG902 AUX board.



Auxiliary (J7) [PCG901 Rev Cx and earlier]

Connects from the PCG-901 to the PCG-902

18-pin 2 mm spacing.

Connector on PCG: Samtec SMM-109-2-L-D-LC.

Mates with P/N Samtec TCMD-09-D-XX.XX-01.

Pin #	Name	Pin #	Name
1	GND	2	SCA 1
3	SCA 2	4	SCA 3
5	SCA 4	6	GND
7	SCA 5	8	SCA 6
9	SCA 7	10	SCA 8
11	GND	12	AUX 2
13	AUX 3	14	AUX 4
15	SPARE	16	GND
17	RS232-RX	18	RS232-TX

External Temperature (J8)

Connection for an external AD592 temperature sensor (for scintillator temperature, etc.)

Receptacle on PCG: Molex 53014-0210

Mating Plug: Housing Molex 51004-0200, Terminal Molex 50011-8100

Pin #	Name
1	+AD592
2	-AD592

I²C (J9)

Unpopulated header position, used for connecting external I²C slave devices. The DP5G is an I²C master only; see the DP5 Programmer’s Guide for information on communicating with external I²C slave devices.

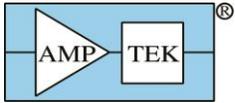
4-pin 0.100” through-hole header.

Pin #	Name
1	3.3V
2	SCL
3	SDA
4	GND

7.2 PCG-902 Connectors

AUX-3

15 socket D connector which includes (a) the lines for a serial RS232 interface, (b) the AUX_OUT_1 and AUX_OUT_2 digital input/output lines, and (c) the 8 SCA outputs.

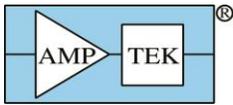


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The RS232 lines connect to a MAX3227, located on the PCG-902. If the PCG-902 is not installed, then logic-level RS232 is available. Note that the RS232 signal names are relative to the DP5G – it transmits on TX, and receives on RX.

Pin #	Name	Pin #	Name
1	GND	9	SCA8
2	RS232-TX	10	SPARE
3	RS232-RX	11	SCA7
4	SCA6	12	SCA1
5	SCA5	13	SCA2
6	GND	14	SCA3
7	AUX_OUT_1	15	SCA4
8	AUX_OUT_2		



7.3 PCG Electrical Interface

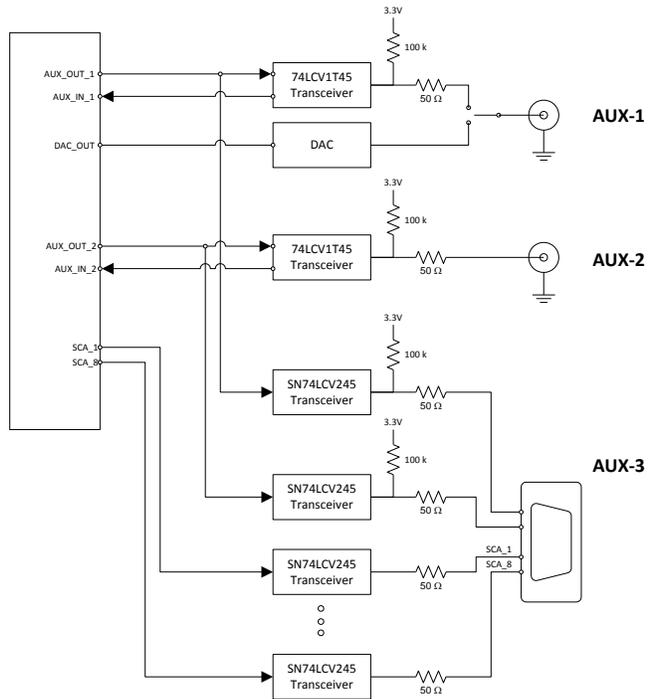
Communications

The USB and Ethernet interfaces, on the PCG, consist only of connections to the drivers located on the DP5G.

For RS232, the transceivers are located on the PCG-902 board. Only logic-level RS232 is available without this board.

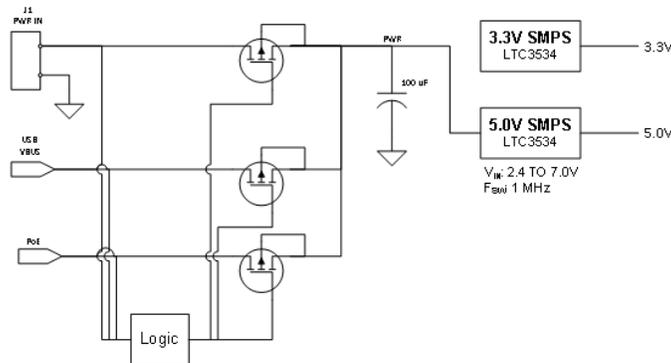
Auxiliary

The figure to the right shows the schematic of the auxiliary interfaces on the PCG assembly.



PCG Low Voltage Power Supply

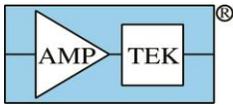
A schematic of the power supply on the PCG is shown below. It takes as input either (a) the 5V VBUS from the USB or (b) a voltage from 2.4V to 7V on the J1 connector. There are two switch mode power supplies on the PCG, one which produces 5V to power the PMT HVPS and one which produces 3.3V to power the DP5G and circuitry on the PCG. Q1 switches the power sources, drawing power from whichever source is higher (J1 or USB).



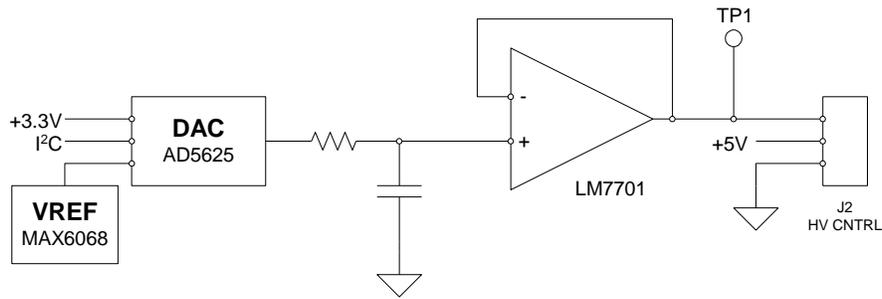
The DP5G typically draws 165 mA on the 3.3V line. The current into J1 is typically 155 mA at 5V.

7.4 PCG HV Bias Control

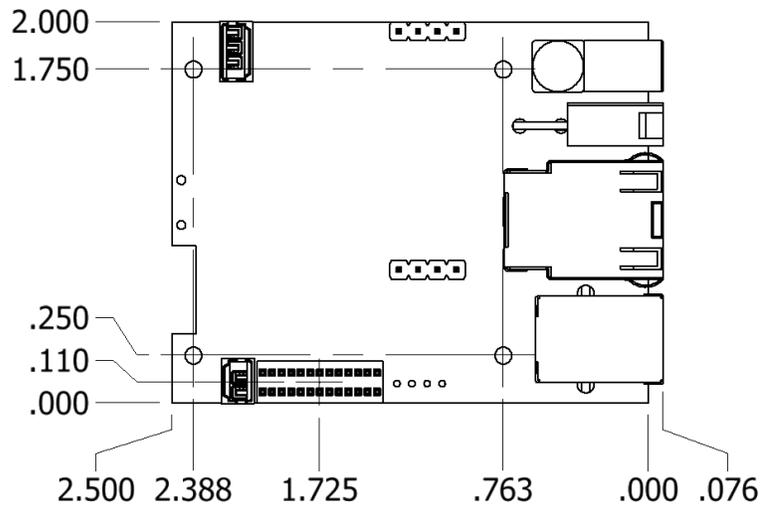
The circuit below is used to generate a control voltage to the PMT HVPS in the Gamma-Rad5 and can be used with other detector modules. Via software, a command is sent to the DP5G which sets the DAC output voltage. Using the standard DP5G configuration packets, the value is divided by 1000. That



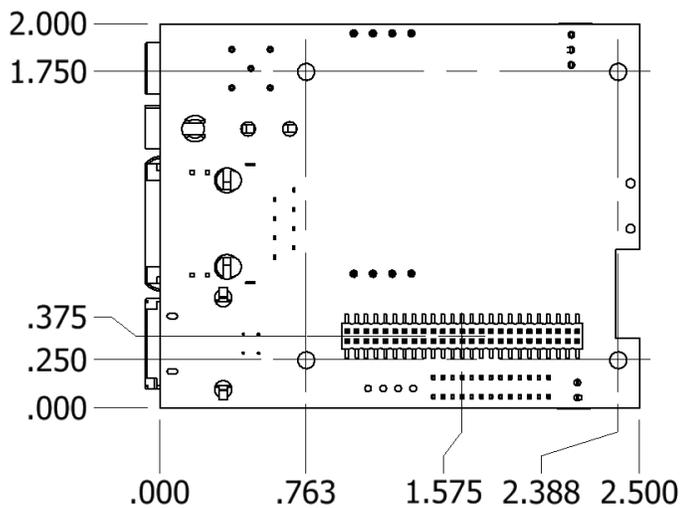
is, setting the “HV” to 900V in the DP5G software results in 900 mV at the output of the DAC and hence at pin 1 of J2. The LM7701 simply buffers this DAC output.



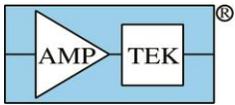
7.5 PCG Mechanical Dimensions and Configuration



Top View of PCG-901

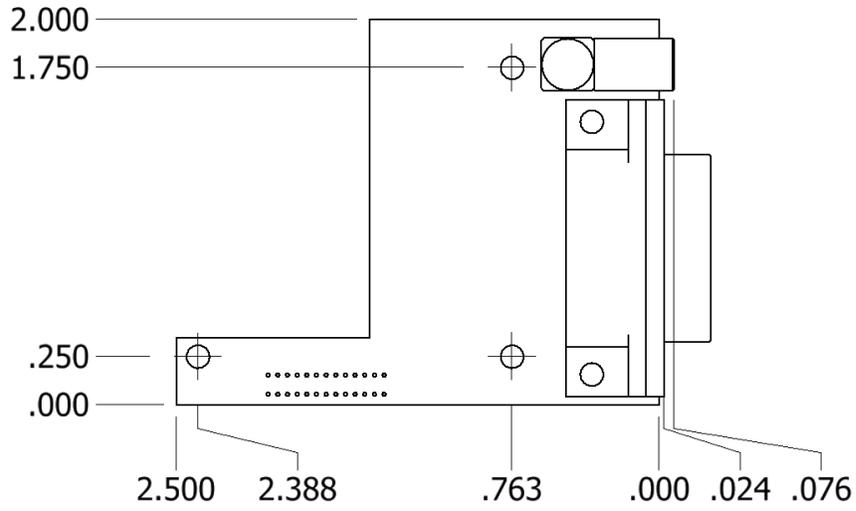


Bottom View of PCG-901

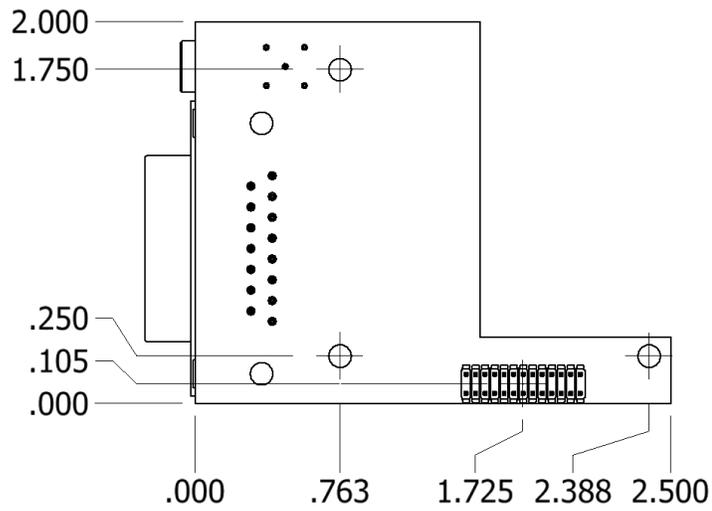


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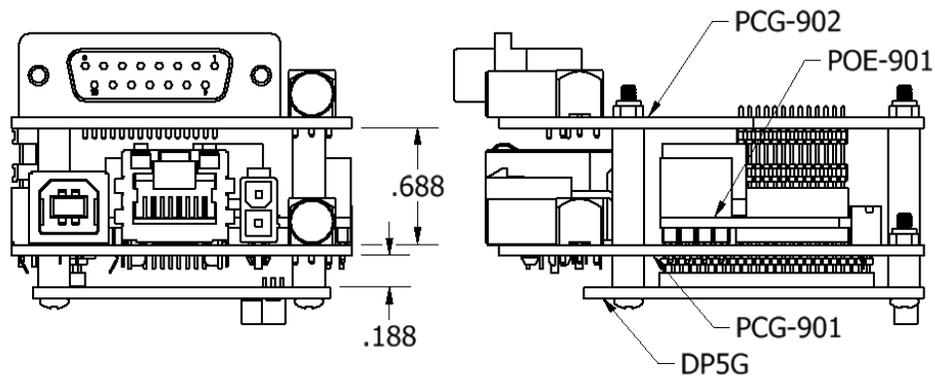
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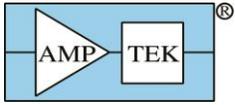
Top View of PCG-902



Bottom View of PCG-902

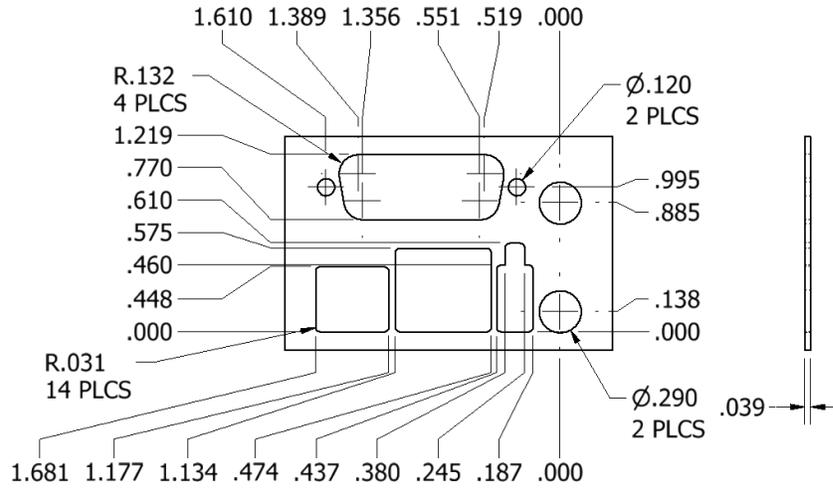


PCB Stack



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Panel Cutout