IT6263

Single Chip De-SSC LVDS to HDMI Converter

Preliminary Datasheet

ITE TECH. INC.

General Description

The IT6263 is a high-performance single-chip De-SSC LVDS to HDMI converter. Combined with LVDS receiver and HDMI Transmitter, the IT6263 supports LVDS input and HDMI1.3 output by conversion function. The build-in LVDS receiver can support single-link and dual-link LVDS inputs, and the build-in HDMI transmitter is fully compliant with HDMI 1.3, HDCP 1.2 and backward compatible with DVI 1.0 specification. With high speed LVDS RX, the IT6263 can support resolution up to 1080P and UXGA and 10-bit deep colors.

In order to reduce the EMI noise on legacy system application, the traditional LVDS source will transmit differential signals with spread spectrum, but this spread spectrum does not be allowed for HDMI protocol. The IT6263 also build-in unique De-SSC (De-Spread Spectrum) function , it can help customers easily to adopt the IT6263 on the EMI-concerned platform, with SSC has been generated from LVDS source processors.

The IT6263 also encodes and transmits up to 8 channels of I^2S digital audio, with sampling rate up to 192kHz and sample size up to 24 bits. In addition, an S/PDIF input port takes in compressed audio of up to 192kHz frame rate.

The newly supported High-Bit Rate (HBR) audio by HDMI Specifications v1.3 is provided by the IT6263 in two interfaces: with the four I^2S input ports or the S/PDIF input port. With both interfaces the highest possible HBR frame rate is supported at up to 768kHz.

Each IT6263 chip comes preprogrammed with an unique HDCP key, in compliance with the HDCP 1.2 standard so as to provide secure transmission of high-definition content. Users of the IT6263 need not purchase any HDCP keys or ROMs.

The single chip IT6263 provides high performance, cost effective, LVDS2HDMI conversion function, and it can be applied to IP TV STBs and Scaler Boxs which need small size video outputs.

Features (LVDS RX)

- Support LVDS Input modes: Single Link, Dual Link
- Support input clock rate up to 150MHz
- Support input color depth up to 10bit
- Support **De-SSC (De-Spread Spectrum)**
- Support Data Mapping: Open LDI, JEIDA, VESA

Features (HDMI TX)

- HDMI 1.3 transmitter
- Compatible with HDMI 1.3, HDCP1.2 and DVI 1.0 specifications
- Support deep color depth up to 12bit
- Support link speeds of up to 2.25Gbps (link clock rate of 225MHz)
- Support Gammat Metadata packet
- Digital audio input interface supporting
    - up to four I^2S interface supporting 8-channel audio, with sample rates of 32~192 kHz and smaple sizes of 16~24 bits
    - S/PDIF interface supporting PCM, Dolby Digital, DTS digital audio at up to 192kHz frame rate
    - Support for high-bit-rate (HBR) audio such as DTS-HD and Dolby TrueHD through the four I^2S interface or the S/PDIF interface, with frame rates as high as 768kHz
    - Compatible with IEC 60958 and IEC 61937
    - Audio down-sampling of 2X and 4X
- Software programmable, auto-calibrated TMDS source terminations provide for optimal source
- Software programmable HDMI output current level
- MCLK input is optional for audio operation. Users could opt to implement audio input interface with or without MCLK
- Integrated pre-programmed HDCP keys
- Purely hardware HDCP engine increasing the robustness and security of HDCP operation

- Monitor detection through Hot Plug Detection and Receiver Termination Detection
- Embedded full-function pattern generator
- Intelligent, programmable power management

Features (Combined)

- Support up to **Full-HD/1080P and UXGA(1600x1200)** display format
- Support deep color depth up to **10bit**
- 64-pin QFN (9mm x 9mm) package
- RoHS Compliant (100% Green available)

Ordering Information

Model	Temperature Range	Package Type	Green/Pb free Option
IT6263FN	0~70	64-pin QFN	Green

Pin Diagram

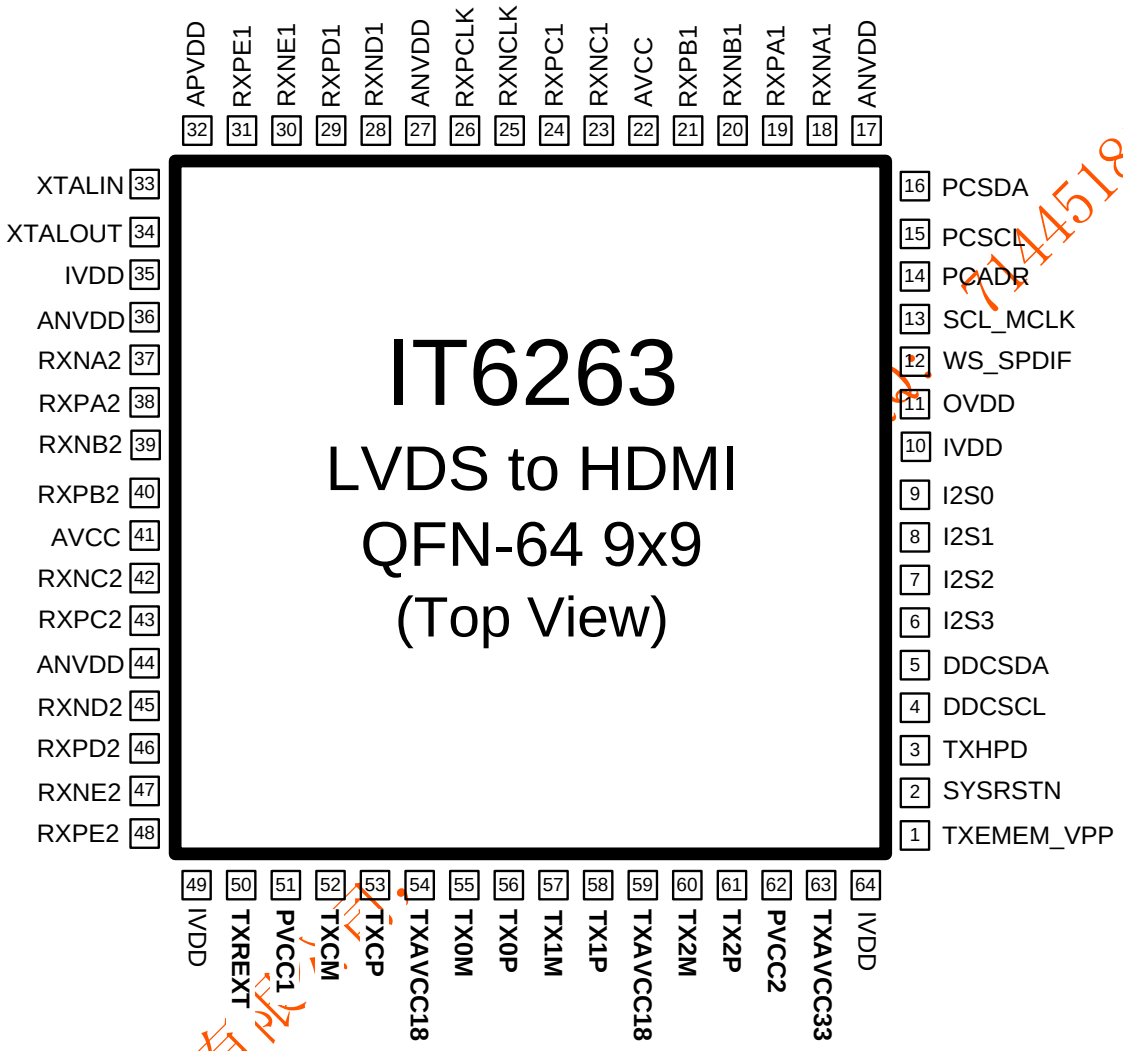


Figure 1. IT6263 pin diagram

Pin Description

LVDS front-end interface pins

Pin Name	Direction	Description	Type	Pin No.
RXNA1	Analog	LVDS first link negative input	LVDS	18
RXPA1	Analog	LVDS first link positive input	LVDS	19
RXNB1	Analog	LVDS first link negative input	LVDS	20
RXPB1	Analog	LVDS first link positive input	LVDS	21
RXNC1	Analog	LVDS first link negative input	LVDS	23
RXPC1	Analog	LVDS first link positive input	LVDS	24
RXND1	Analog	LVDS first link negative input	LVDS	28
RXPD1	Analog	LVDS first link positive input	LVDS	29
RXNE1	Analog	LVDS first link negative input	LVDS	30
RXPE1	Analog	LVDS first link positive input	LVDS	31
RXNCLK	Analog	LVDS negative clock input	LVDS	25
RXPCLK	Analog	LVDS positive clock input	LVDS	26
RXNA2	Analog	LVDS second link negative input	LVDS	37
RXPA2	Analog	LVDS second link positive input	LVDS	38
RXNB2	Analog	LVDS second link negative input	LVDS	39
RXPB2	Analog	LVDS second link positive input	LVDS	40
RXNC2	Analog	LVDS second link negative input	LVDS	42
RXPC2	Analog	LVDS second link positive input	LVDS	43
RXND2	Analog	LVDS second link negative input	LVDS	45
RXPD2	Analog	LVDS second link positive input	LVDS	46
RXNE2	Analog	LVDS second link negative input	LVDS	47
RXPE2	Analog	LVDS second link positive input	LVDS	48
XTALIN	Analog	Crystal clock input	Analog	33
XTALOUT	Analog	Crystal clock output	Analog	34

HDMI front-end interface pins

Pin Name	Direction	Description	Type	Pin No.
TX2P	Analog	HDMI Channel 2 positive output	TMDS	61
TX2M	Analog	HDMI Channel 2 negative output	TMDS	60
TX1P	Analog	HDMI Channel 1 positive output	TMDS	58
TX1M	Analog	HDMI Channel 1 negative output	TMDS	57
TX0P	Analog	HDMI Channel 0 positive output	TMDS	56
TX0M	Analog	HDMI Channel 0 negative output	TMDS	55

TXCP	Analog	HDMI Clock Channel positive output	TMDS	53
TXCM	Analog	HDMI Clock Channel negative output	TMDS	52
TREXT	Analog	External resistor for setting TMDS output level. Default tied to TXAVCC18 via a 698-Ohm SMD resistor.	Analog	50

Digital Audio Input Pins

Pin Name	Direction	Description	Type	Pin No.
SCL_MCLK	Input	I2S serial clock input /Audio master clock input	LVTTL	13
WS_SPDIF	Input	I2S word select input /S/PDIF audio input	LVTTL	12
I2S0	Input	I2S serial data input	LVTTL	9
I2S1	Input	I2S serial data input	LVTTL	8
I2S2	Input	I2S serial data input	LVTTL	7
I2S3	Input	I2S serial data input	LVTTL	6

Programming Pins

Pin Name	Direction	Description	Type	Pin No.
SYSRSTN	Input	Hardware reset pin. Active LOW (5V-tolerant)	Schmitt	2
DDCSCL	I/O	I^2C Clock for DDC (5V-tolerant)	Schmitt	4
DDCSDA	I/O	I^2C Data for DDC (5V-tolerant)	Schmitt	5
PCSCL	Input	Serial Programming Clock for chip programming (5V-tolerant)	Schmitt	15
PCSDA	I/O	Serial Programming Data for chip programming (5V-tolerant)	Schmitt	16
PCADR	Input	Serial programming device address select	LVTTL	14
TXHPD	Input	HDMI TX Hot Plug Detection (5V-tolerant)	LVTTL	3
TXEMEM_VPP	Input	Must be tied low via a resistor.	LVTTL	1

Power/Ground Pins

Pin Name	Description	Type	Pin No.
IVDD	Digital logic power (1.8V)	Power	10, 35, 49, 64
OVDD	I/O Pin power (3.3V)	Power	11
TXAVCC18	HDMI analog frontend power (1.8V)	Power	54, 59
TXAVCC33	HDMI analog frontend power (3.3V)	Power	63
PVCC1	HDMI frontend core PLL power (1.8V)	Power	51
PVCC2	HDMI frontend Filter PLL power (1.8V)	Power	62
AVCC	LVDS frontend power (3.3V)	Power	22, 41
ANVDD	LVDS frontend analog power (1.8V)	Power	17, 27, 36, 44
APVDD	LVDS frontend PLL power (1.8V)	Ground	32
GND	Exposed GND pad	Ground	65

Block Diagram

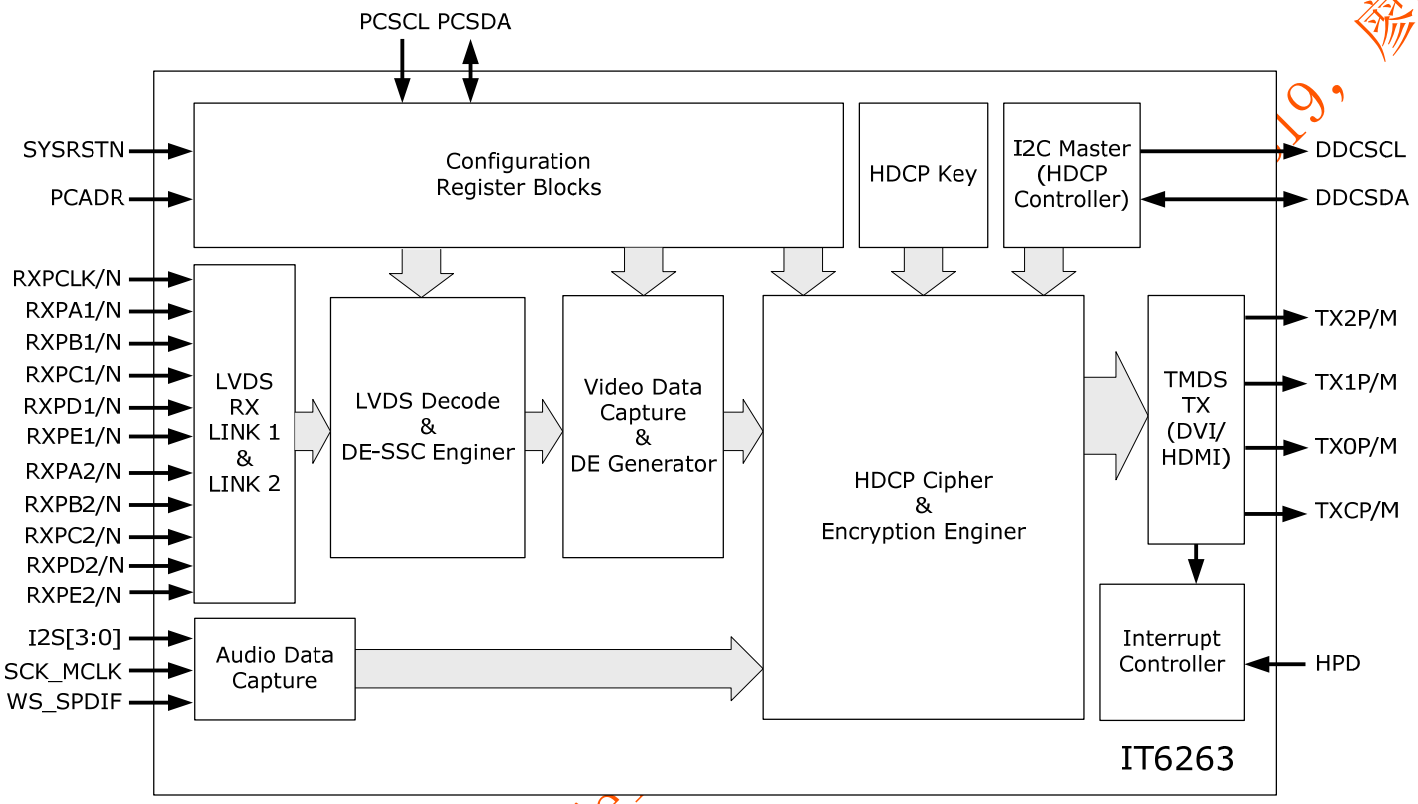


Figure 2. The IT6263 block diagram

Configuration and Function Control

The IT6263 includes two serial programming ports by default : one for interfacing with micro-controller, the other for accessing the DDC channels of HDMI link. The serial programming interface for interfacing the micro-controller is a slave interface, comprising PCSCL (Pin 15) and PCSDA (Pin 16). The micro-controller uses this interface to monitor all the statuses and control all the functions. Two device addresses are available, depending on the input logic level of PCADR (Pin 14). If PCADR is pulled high by the user, the device address is **0x9A**. If pulled low, **0x98**.

The I^2C interface for accessing the DDC channels of the HDMI link is a master interface, comprising DDCSCL (Pin 4) and DDCSDA (Pin 5). The IT6263 uses this interface to read the EDID data and perform HDCP authentication protocol with the sink device over the HDMI cable.

De-SSC Advantage and Performance

LVDS Input Conditions:
Single Channel LVDS at 1080P (Input Clk = 148.5MHz) with +/- 5000ppm SSC LVDS Input.

Output Results of HDMI Compliance Test (Measured HDMI Output Eye Diagram):

With ITE De-SSC Technology – Pass, Eye Diagram is Open. (Fig. 2)
Without De-SSC Technology – Fail, Eye Diagram is Closed and Blur. (Fig. 3)

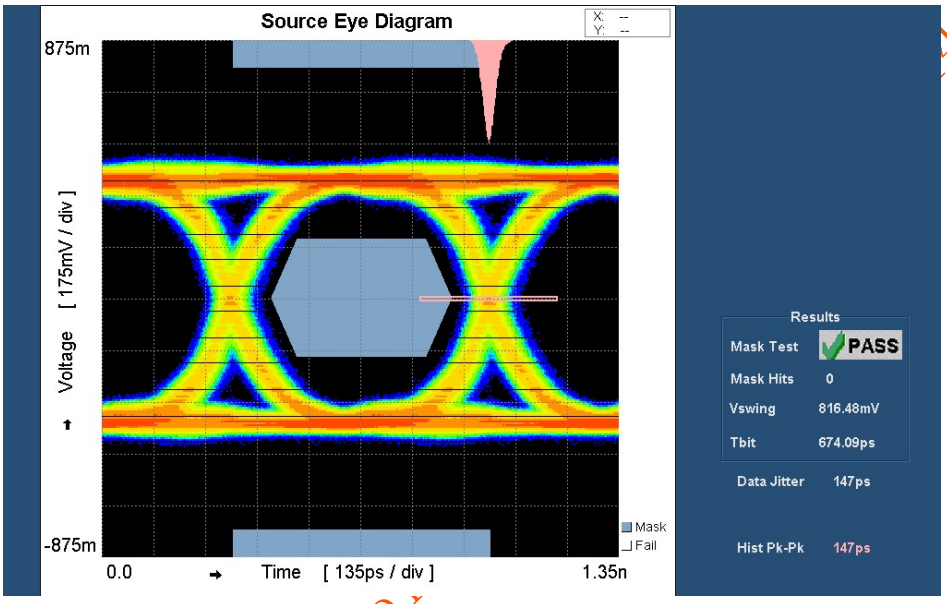


Figure 3. HDMI Output Eye Diagram with De-SSC (Pass)

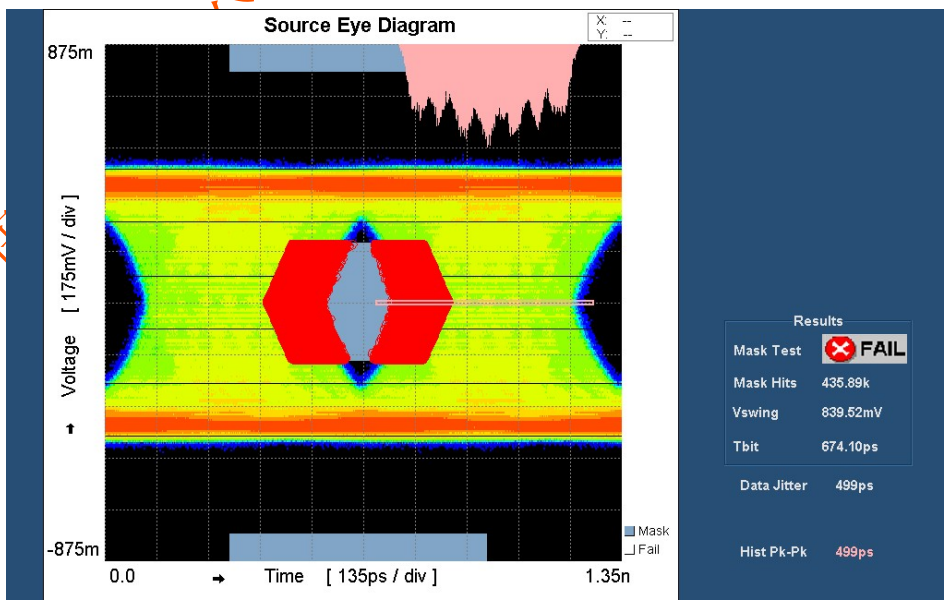


Figure 4. HDMI Output Eye Diagram without De-SSC (Fail)

Electrical Specifications

Absolute Maximum Ratings

Symbol	Parameter	Min.	Typ	Max	Unit
IVDD	Core logic supply voltage	-0.3		2.5	V
OVDD	I/O pins supply voltage	-0.3		4.0	V
TXAVCC18	HDMI analog frontend supply voltage	-0.3		2.5	V
TXAVCC33	HDMI analog frontend supply voltage	-0.3		4.0	V
PVCC1	HDMI core PLL supply voltage	-0.3		2.5	V
PVCC2	Filter PLL supply voltage	-0.3		2.5	V
AVCC	LVDS frontend power	-0.3		4.0	V
ANVDD	LVDS frontend analog power	-0.3		2.5	V
APVDD	LVDS frontend PLL power	-0.3		2.5	V
V_I	Input voltage	-0.3		OVDD+0.3	V
V_O	Output voltage	-0.3		OVDD+0.3	V
T_J	Junction Temperature			125	°C
T_{STG}	Storage Temperature	-65		150	°C
ESD_HB	Human body mode ESD sensitivity	2000			V
ESD_MM	Machine mode ESD sensitivity	200			V

Notes:
1. Stresses above those listed under Absolute Maximum Ratings might result in permanent damage to the device.
2. Refer to Functional Operation Conditions for normal operation.

Functional Operation Conditions

Symbol	Parameter	Min.	Typ	Max	Unit
IVDD	Core logic supply voltage	1.62	1.8	1.98	V
OVDD	I/O pins supply voltage	2.97	3.3	3.63	V
TXAVCC18	HDMI analog frontend supply voltage	1.71	1.8	1.89	V
TXAVCC33	HDMI analog frontend supply voltage	2.97	3.3	3.63	V
PVCC1	HDMI core PLL supply voltage	1.62	1.8	1.98	V
PVCC2	Filter PLL supply voltage	1.62	1.8	1.98	V
AVCC	LVDS frontend power	2.97	3.3	3.63	V
ANVDD	LVDS frontend analog power	1.62	1.8	1.98	V
APVDD	LVDS frontend PLL power	1.62	1.8	1.98	V
$V_{CCNOISE}$	Supply noise			100	mV_{pp}
T_A	Ambient temperature	0	25	70	°C
Θ_{ja}	Junction to ambient thermal resistance				°C/W

Notes:
1. TXAVCC18, TXAVCC33, PVCC1, PVCC2, AVCC, ANVDD and APVDD should be regulated.
2. See System Design Consideration for supply decoupling and regulation.

DC Electrical Specification

Under functional operation conditions

Symbol	Parameter	Pin Type	Conditions	Min.	Typ	Max	Unit
V_{IH}	Input high voltage[1]	LVTTL		2.0			V
V_{IL}	Input low voltage[1]	LVTTL				0.8	V
V_T	Switching threshold[1]	LVTTL			1.5		V
V_{T-}	Schmitt trigger negative going threshold voltage[1]	Schmitt		0.8	1.1		V
V_{T+}	Schmitt trigger positive going threshold voltage[1]	Schmitt			1.6	2.0	V
V_{OL}	Output low voltage[1]	LVTTL	I_{OL}=2~16mA			0.4	
V_{OH}	Output high voltage[1]	LVTTL	I_{OH}=-2~-16mA	2.4			
I_{IN}	Input leakage current[1]	all	V_{IN}=5.5V or 0		±5		μA
I_{OZ}	Tri-state output leakage current[1]	all	V_{IN}=5.5V or 0		±10		μA
I_{OL}	Serial programming output sink current[2]	Schmitt	V_{OUT}=0.2V	4		16	mA
V_{swing}	TMDS output single-ended swing[3]	TMDS	R_{LOAD}=50Ω V_{LOAD}=3.3V R_{EXT}=698Ω	400		600	mV
I_{OFF}	Single-ended standby output current[3]	TMDS	V_{OUT}=0			10	μA
V_{TH}	Differential Input high threshold	LVDS	VCM = +1.2V			100	mV
V_{TL}	Differential Input low threshold	LVDS	VCM = +1.2V	-100			mV
I_{IN}	Input current	LVDS	VCM = +2.4V/0V			±6	μA

Notes:

1. Guaranteed by I/O design.
2. The serial programming output ports are not real open-drain drivers. Sink current is guaranteed by I/O design under the condition of driving the output pin with 0.2V. In a real serial programming environment, multiple devices and pull-up resistors could be present on the same bus, rendering the effective pull-up resistance much lower than that specified by the I^2C Standard. When set at maximum current, the serial programming output ports of the IT6263 are capable of pulling down an effective pull-up resistance as low as 500Ω connected to 5V termination voltage to the standard I^2C V_{IL}. When experiencing insufficient low level problem, try setting the current level to higher than default.
3. Internal source turned off. Limits defined by HDMI Specifications v1.3a

Audio AC Timing Specification

Under functional operation conditions

Symbol	Parameter	Conditions	Min.	Typ	Max	Unit
F_{S_I2S}	I^2S sample rate	Up to 8 channels	32		192	kHz
F_{S_SPDIF}	S/PDIF sample rate	2 channels	32		192	kHz

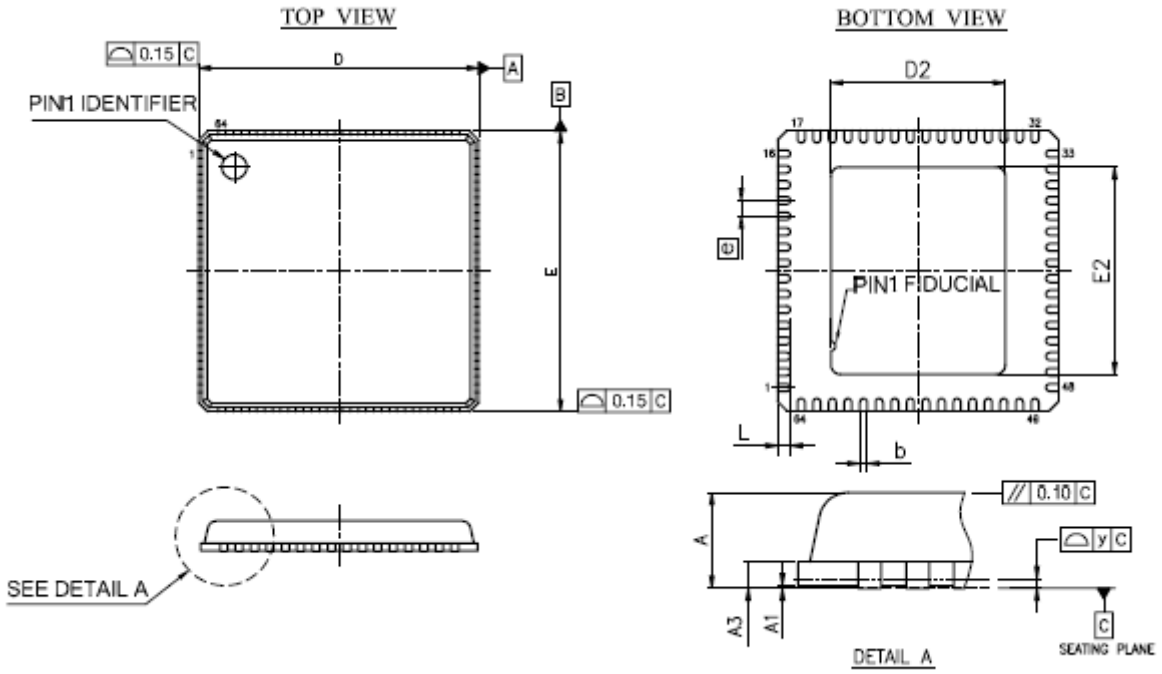
Operation Supply Current Specification

Symbol	Parameter	PIXELCLK	Typ	Max	Unit
I_{IVDD_OP}	IVDD current under normal operation	27MHz	47	48	mA
		74.25MHz	96	97	mA
		148.5MHz	166	161	mA
		148.5MHz(DI)[4]	144	157	mA
I_{IOVDD_OP}	OVDD current under normal operation	27MHz	623	623	µA
		74.25MHz	615	615	µA
		148.5MHz	595	670	µA
		148.5MHz(DI)[4]	672	672	µA
$I_{TXAVCC18\_OP}$	TXAVCC18 current under normal operation	27MHz	34	38	mA
		74.25MHz	36	40	mA
		148.5MHz	39	43	mA
		148.5MHz(DI)[4]	39	44	mA
$I_{TXAVCC33\_OP}$	TXAVCC33 current under normal operation	27MHz	58	58	µA
		74.25MHz	57	58	µA
		148.5MHz	49	59	µA
		148.5MHz(DI)[4]	50	59	µA
I_{PVCC1_OP}	PVCC1 current under normal operation	27MHz	2	2	mA
		74.25MHz	5	5	mA
		148.5MHz	7	11	mA
		148.5MHz(DI)[4]	7	11	mA
I_{PVCC2_OP}	PVCC2 current under normal operation	27MHz	2	2	mA
		74.25MHz	6	6	mA
		148.5MHz	13	13	mA
		148.5MHz(DI)[4]	13	13	mA
I_{ANVDD_OP}	ANVDD current under normal operation	27MHz	28	30	mA
		74.25MHz	36	38	mA
		148.5MHz	47	51	mA
		148.5MHz(DI)[4]	59	62	mA
I_{APVDD_OP}	APVDD current under normal operation	27MHz	4	5	mA
		74.25MHz	12	13	mA
		148.5MHz	24	27	mA
		148.5MHz(DI)[4]	13	14	mA
I_{AVCC_OP}	AVCC current under normal operation	27MHz	9	10	mA
		74.25MHz	9	10	mA
		148.5MHz	9	10	mA

		148.5MHz(DI)[4]	15	16	mA
W_{TOTAL_OP}	Total power consumption under normal operation[3]	27MHz	243	286	mW
		74.25MHz	376	432	mW
		148.5MHz	565	645	mW
		148.5MHz(DI)[4]	547	656	mW

Notes:
1. Typ: OVDD=TXAVCC33=AVCC=3.3V, IVDD=AVCC18=PVCC1=PVCC2=APVDD=ANVDD=1.8V
   Max: OVDD=TXAVCC33=AVCC=3.6V, IVDD=AVCC18=PVCC1=PVCC2=APVDD=ANVDD=1.98V
2. PIXELCLK refer to the video clock
3. PIXELCLK=27MHz: 480p with 48kHz/8-channel audio,
   PIXELCLK=74.25MHz: 1080i with 192kHz/8-channel audio,
   PIXELCLK=148.5MHz: 1080p with 192kHz/8-channel audio.
4. DI: LVDS Dual Link.
5. PW_{TOTAL_OP} are calculated by multiplying the supply currents with their corresponding supply voltage and summing up all the items.

Package Dimensions



Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.031	0.035	0.039	0.80	0.90	1.00
A1	0.000	0.001	0.002	0.00	0.02	0.05
A3	0.008 REF			0.20 REF		
b	0.007	0.010	0.012	0.18	0.25	0.30
D	0.350	0.354	0.358	8.90	9.00	9.10
D2	0.141	0.149	0.157	3.58	3.78	3.98
E	0.350	0.354	0.358	8.90	9.00	9.10
E2	0.141	0.149	0.157	3.58	3.78	3.98
e	0.020 BSC			0.50 BSC		
L	0.012	0.016	0.020	0.30	0.40	0.50
y	--	--	0.003	--	--	0.08

Figure 5. 64-pin QFN Package Dimensions