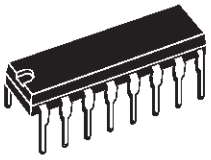
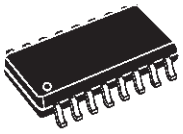
L6353

SMART DRIVER FOR POWER MOS & IGBT

- PEAK HIGH OUTPUT CURRENT CAPABILITY (±8A)
- WIDE SUPPLY VOLTAGE RANGE (12.5 TO 18V)
- 0 TO –7.5V NEGATIVE BIAS VOLTAGE SUPPLY RANGE
- OVER CURRENT AND DESATURATION PROTECTION OF THE EXTERNAL POWER DEVICE (EXTERNALLY PROGRAMMABLE)
- LATCH-UP PROTECTION (FOR IGBT)
- TWO STEPS TURN-ON (PROGRAMMABLE)
- PROTECTION AGAINST POSITIVE SUPPLY UNDER-VOLTAGE
- INPUT COMPATIBLE WITH OPTOCOUPLER OR PULSE TRANSFORMER
- PROGRAMMABLE TURN-ON DELAY
- THERMAL PROTECTION WITH ON-CHIP OVER-TEMPERATURE ALARM AND TURN-OFF PROCEDURE
- OPERATING FREQUENCY UP TO 100kHz



DIP16



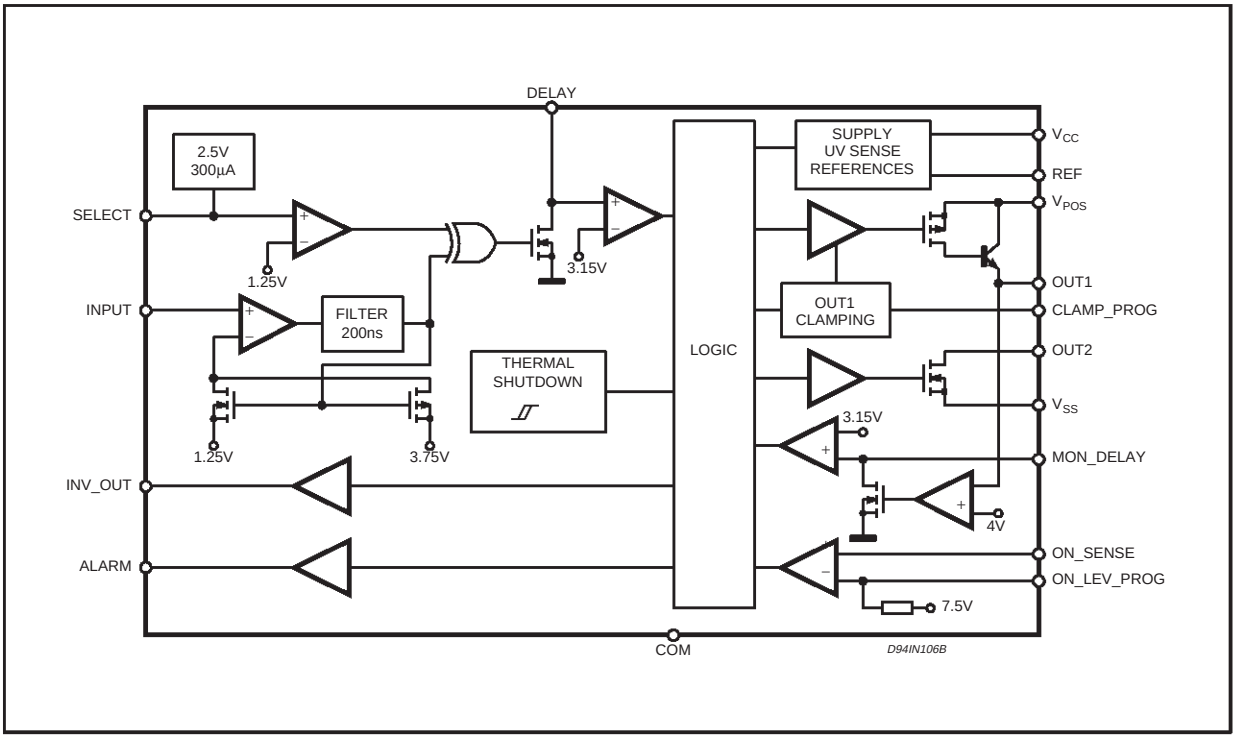
SO16

ORDERING NUMBERS: L6353 (DIP)
L6353D (SO)

DESCRIPTION

The L6353 device is a smart driver, with all the drive and protection know-how ”on board”.
Available in both DIP and SO package, it can be triggered with a logic level or with the signal from an optocoupler or a pulse transformer. It filters parasitic input signals and drives any MOS or IGBT.

BLOCK DIAGRAM



DESCRIPTION (continued)

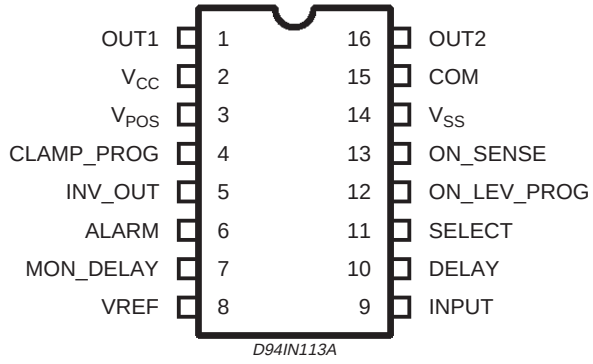
It monitors the on-state voltage drop of the driven power device and protects it against overload and short circuit.

The on-state voltage drop level is externally programmable from 5 to 15V. This function is inhibited during the turn-on of the external power device for an externally programmable period.
An internal inhibition time of 200ns avoids false triggering.

Overload or overheating are signalled on an alarm output. If temperature continues to increase the power output is switched off and maintained in the off-state until the temperature decreases below the low threshold. A programmable turn-on delay avoids cross conduction in bridge configurations.

To preserve the external power device (especially IGBT) from the risk of latch-up, the gate voltage can be risen in two different steps (of which the first is externally programmable from 7 to 11V).

PIN CONNECTION (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage referred to COM pin	20	V
V_{SS}	Negative Supply Voltage referred to COM pin	– 8 to 0	V
V_{POS} - V_{OUT1}	Collector-Emitter Voltage of High Side NPN	25	V
V_{OUT2} - V_{SS}	Drain-Source Voltage of Low Side DMOS	25	V
V_{EXT1}	Externally Forced Voltage (pin 9)	-0.3 to V_{CC}	V
V_{EXT2}	Externally Forced Voltage (pins 4,7,10, 11, 12)	-0.3 to 7	V
I_{DELAY}	Sink Current pin Delay	3	mA
I_{MON_DELAY}	Sink Current Pin Mon_Delay	3	mA
V_{ON_SENSE}	Voltage on ON_SENSE Pin	VSS-0.3 to V_{CC}	V
I_{OUT1}	Positive Output Current (tp ≤1ms) (peak)	8	A
I_{OUT2}	Negative Output Current (tp ≤1ms) (peak)	8	A
I_{INV_OUT}	Output Current in INV_OUT Pin	±20	mA
I_{ALARM}	Output Current in ALARM Pin	±20	mA
P_{tot}	Total Power Dissipation	internally limited	
T_{amb}	Operating Temperature Range	-25 to +85	°C
T_{stg}	Storage Temperature	-50 to +150	°C

THERMAL DATA

Symbol	Parameter		DIP16	SO16	Unit
$R_{thj\text{-}ambient}$	Thermal Resistance Junction-ambient	Max	80	90	°C/W

PIN FUNCTIONS

N.	Name	Function
1	OUT1	Output of high side driver (emitter of power NPN transistor).
2	V_{CC}	Positive Supply Voltage (referred to COM). See under voltage lockout functioning
3	V_{POS}	Positive Bias Voltage (collector of the NPN power transistor).
4	CLAMP_PROG	First Step of the Gate Voltage Programming. The programming is achieved setting an appropriate voltage on this pin (i.e. using a resistence voltage divider).
5	INV-OUT	Inverted Output Driver Status. The buffer output is able to drive some auxiliary circuit (i.e. a LED).
6	ALARM	Diagnostic Output Signal. A fault condition is signalled by this output buffer.
7	MON_DELAY	V_{ON} Monitor Delay. An R-C network connected between this, the COM and the V_{REF} pins, define t_{MON_DELAY} time interval (see fig 4)
8	V_{REF}	Output of the 5V/10mA internal voltage reference.
9	INPUT	Input signal. The driving signal can be a logic level either active LOW (inverted mode) or HIGH (direct mode) in the Logic Level or a pulse in the Pulse Transformer Mode (see Figure 2)
10	DELAY	On Triggering Delay. An R-C network connected between this, the COM and the V_{REF} pins, definethe t_{DELAY} time interval (see fig 4)
11	SELECT	Select the direct/inverted mode in the Logic Level Mode. It's also the reference pin in Pulse transformer mode.
12	ON_LEV_PROG	V_{ON} level programming. This pin is used to set the V_{ON} monitor level. The programming is achieved setting an appropriate voltage on this pin (i.e. using a resistive divider).
13	ON_SENSE	On State Monitor. This pin is used to monitor the turning on of the external power device.
14	V_{SS}	Negative supply voltage (referred to the COM). This pin is the source of the low side driver DMOS.
15	COM	Ground
16	OUT2	Output of the low side driver (drain of the DMOS).

DC ELECTRICAL CHARACTERISTICS (V_{POS} = V_{CC}=15V; V_{SS} = -5 to 0V; T_j = -25 to +125°C; unless otherwise specified)

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{drop}	1	V_{POS} - V_{OUT1}	I_{OUT1} = 2A		2.5		V
V_{CC}	2	Operating Supply Voltage	(referred to COM pin)	12.5		18	V
V_{CCth1}		Under Voltage Upper Threshold		10.5	11.5	12.5	V
V_{CCth2}		Under Voltage Lower Threshold		10	11	12	V
V_{CChys}		Under Voltage Hysteresis		0.3	0.5	0.7	V
I_{CCq}		Quiescent Supply Current			5		mA
V_d	4, 12	Output Voltage	pin floating		1.26		V
I_{so}		Sourced Current	pin grounding		20		µA
I_{si}		Sinked Current	pin at +5V		-20		µA
V_{drop_sig}	5, 6	High State Output Voltage Drop	I_{out} = 20mA			V_{CC}–3	V
		Low State Output Voltage Drop				3	V
V_{ref}	8	Output of Internal Voltage Reference	I_{ref} = 0A; T_j = 25°C	4.9	5	5.1	V
			$I_{ref} \leq$ 10mA; T_j = 25°C	4.8		5.2	mA
R_{in}	7, 10	Comparator Input Resistance				100	Ω
V_{dth}		Comparator Threshold			3.15		V
R_{ins}	13	Input Resistance			75		KΩ
I_{outs}		Output Current	pin grounded		200		µA
V_{SS}	14	Operating Negative Bias Voltage	(referred to COM)	– 7		0	V
R_{ON}	16	On Resistance	OUT2 to V_{SS}); I_{OUT2} = 2A		0.5		Ω
V_{il}	9	Low Level Voltage	(Logic Level Mode)	0		1	V
V_{ih}		High Level Voltage	(Logic Level Mode)	4		V_{CC}	V
I_{in}		Input Current	0<V_{in}<V_{CC} (Logic Level Mode)	– 10		10	µA
t_{inh}		Inhibited Parasitic Pulse Duration	(Logic Level Mode)		200	300	ns
V_{ton}		Turn-on Threshold Voltage	Referred to V_{sel} (Pulse Transformer Mode)			1.5	V
V_{toff}		Turn-off Threshold Voltage	Referred to Vsel (Pulse Transformer Mode)	– 1.5			V
V_{sl}	11	Low Level Voltage	(Logic Level Mode)	0		1	V
V_{sh}		High Level Voltage	(Logic Level Mode)	2		V_{REF}	V
I_{sl}		Current Output of SELECT Pin	V_{sl} = 0V (Logic Level Mode)		300		µA
V_{sel}		Output Voltage of SELECT Pin	(Pulse Transformer Mode)	2.25	2.5	2.75	V

AC ELECTRICAL CHARACTERISTICS

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_{on}	9 vs 1	Turn on Propagation Delay Time			400		ns
t_{off}	9 vs 16	Turn off propagation delay time			400		ns
t_r	1,16	Rise Time			50		ns
t_f		Fall Time			50		ns
t_{fault}		Delay Time for Fault Detection				400	ns

THERMAL PROTECTION

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
T_{th1}	Over Temperature Threshold	(Thermal Procedure)		130		°C
T_{hys1}	Over Temperature Threshold Hysteresis			20		°C
T_{th2}	Over Temperature Shutdown			160		°C
T_{hys2}	Over Temperature Shutdown Hysteresis			20		°C

Figure 1: Switching waveforms and test circuit

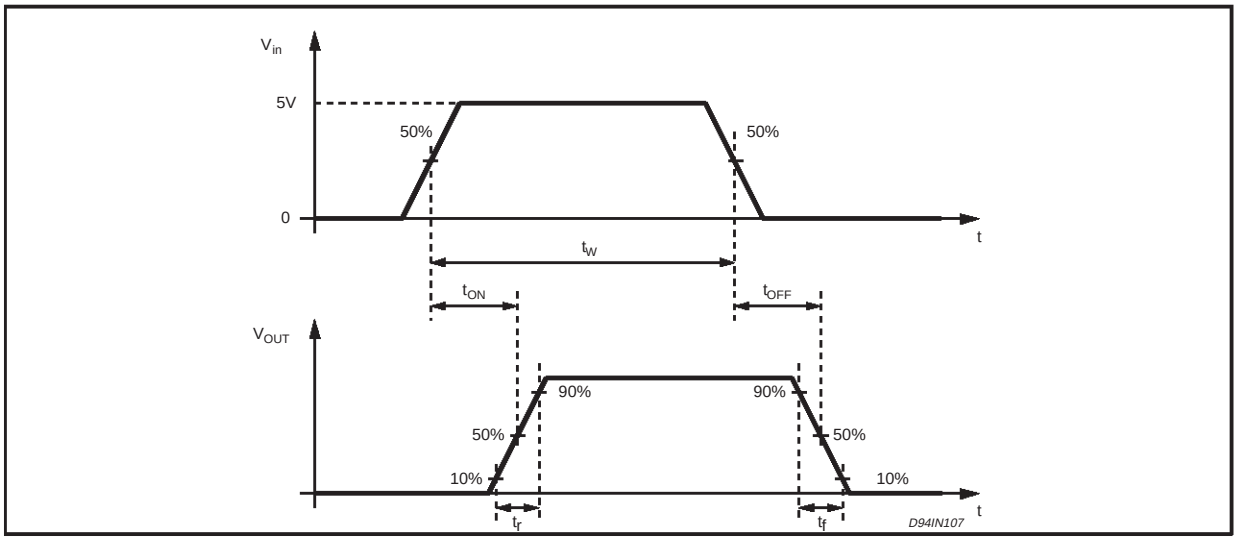


Figure 1a : Switching waveforms and test circuit

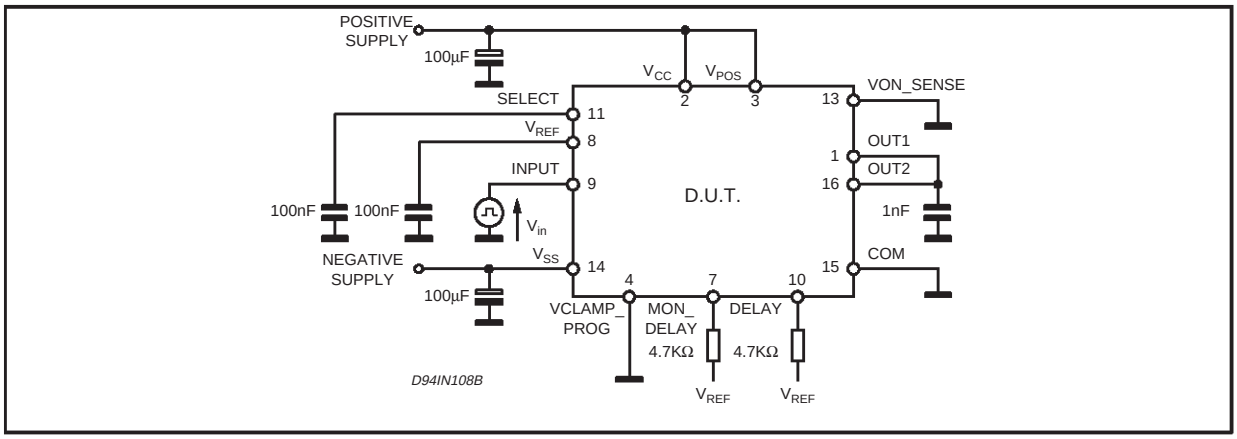


Figure 2. Pulse Transformer mode operation.

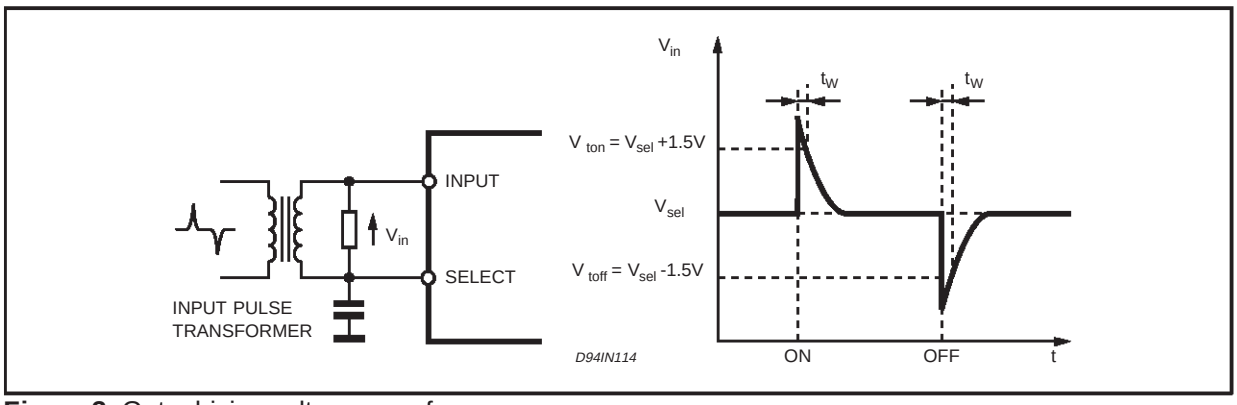


Figure 3. Gate driving voltage waveforms.

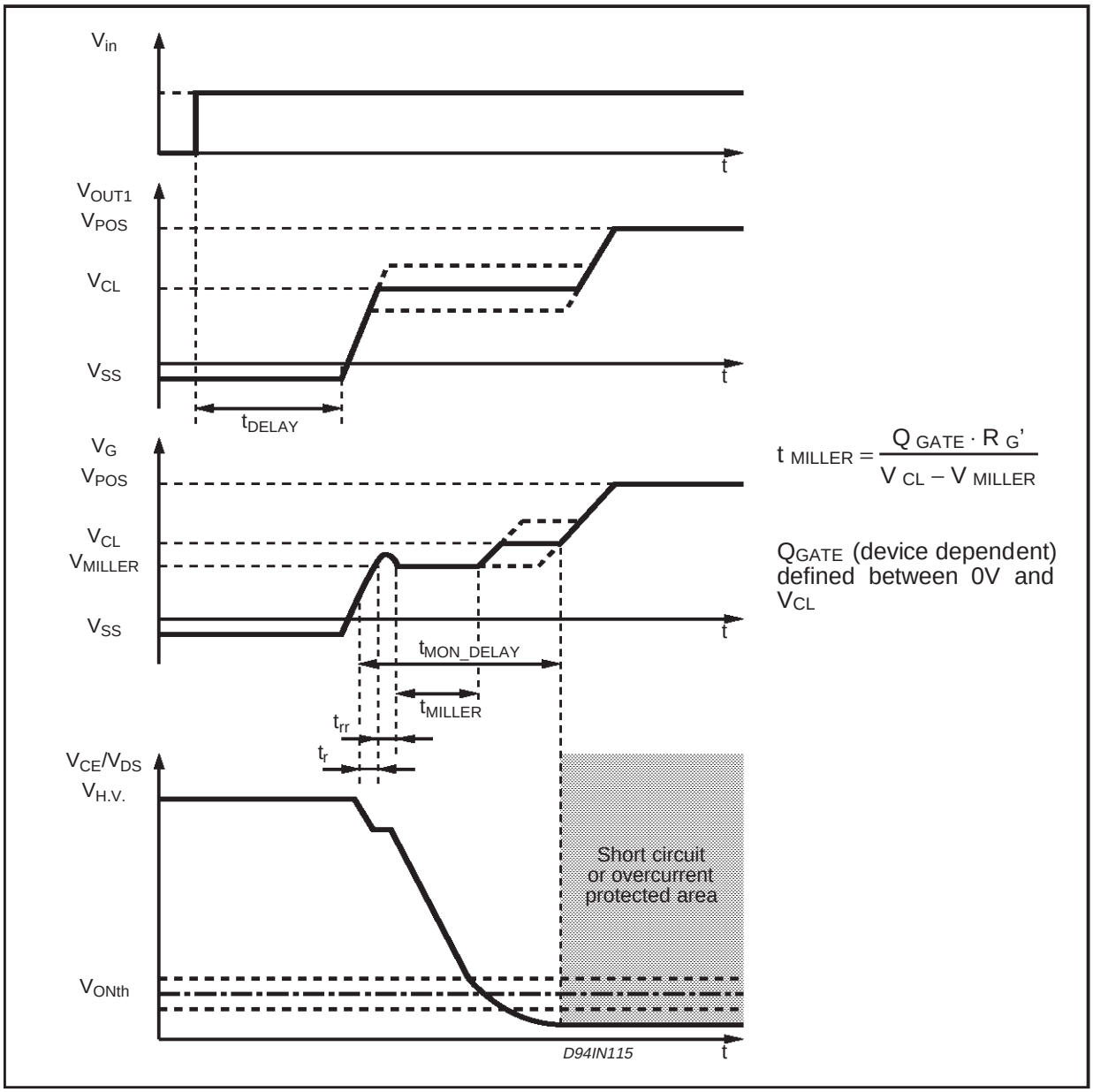
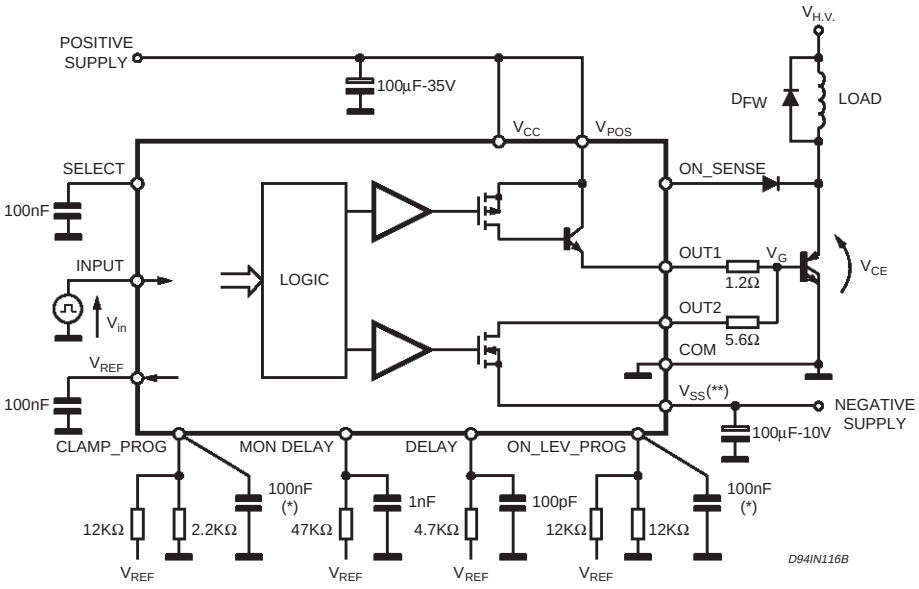


Figure 4. Gate driving waveforms test circuit.



NOTES:
(*) The capacitor is required if the pin is left floating.
(**) If the negative supply is not used, the V_{SS} pin must be connected to the COM pin as close as possible to the IC.

INPUT INTERFACE

To drive the external power device three different possibilities are allowed:

The Logic Level Mode, either direct or inverted, and the Pulse Transformer Mode

Using the Logic Level Mode (direct) an high level (referred to COM), at the INPUT pin will start the Turn on Procedure (i.e. firing an N channel external device). A low level (referred to COM) will instead close the OUT2 pin to VSS.

The functioning is reversed in the inverted mode. To select the direct mode the SELECT pin must be connected via a capacitor to COM. The inverted mode is chosen by connecting the SELECT pin to COM.

In logic Level Mode pulses lasting less than t_{inh} (200ns typ.) are filtered out.

In the Pulse Transformer Mode the SELECT pin will be the reference pin for the signal applied to the INPUTpin. The positive pulse will start the TURN ON PROCEDURE, while the negative pulse will close OUT2 to V_{SS}. The duration of this pulses (t_w, see fig.2) must be again $t_w > t_{inh}$.

TURN-ON PROCEDURE

The firing of the external power device is performed in three steps in order to avoid the most common problems that can arise.

In each of these steps there are a number of parameters that can be easily externally presetted to the requested values.

First Step

Parameter: t_{DELAY}

In order to avoid cross-conduction between the external power device in half bridge arrangement the driver output is activated after an externally programmable delay time (t_{DELAY}, see fig. 3) after the input signal. To set the t_{DELAY}interval an R-C network has to be connected between the DELAY, V_{REF} and COM pins (see fig.4) giving:

$$t_{DELAY}\ (\mu sec) = R_{EXT}\ (K\Omega)\ .\ C_{EXT}(nF) + t_{on}$$

To minimize this interval only a resistor has to be connected between the DELAY and the V_{REF} limiting thus the duration to the internal propagation delay ton.

Second step

Parameters: t_{MON_DELAY}, V_{CL}

To protect the driven device from latch-up at turn-on (IGBT) after the t_{DELAY} time interval a second externally programmable time interval t_{MON_DELAY} (presettable using the same technique used to set the t_{DELAY} interval, see fig.4)

$$t_{MON\text{-}DELAY}\ (\mu sec) = R_{EXT}\ (K\Omega)\ .\ C_{EXT}(nF)$$

during the t_{MON_DELAY} the voltage on the $V_{OUT1)}$ is limited to the V_{CL} level. To program this value an appropriate voltage drop has to be imposed, by mean of a resistive voltage divider, at the CLAMP_PROG pin according to the following formula:

$$V_{CLAMP\_PROG} = \frac{V_{CL}}{6}$$

with

$$7V \leq V_{CL} \leq 11V$$

Leaving the CLAMP_PROG pin floating the V_{CL} level is set to 9V. If the pin is grounded the function is inhibited (i.e. no intermediate step during the firing).

Third step

Parameter: V_{ONth}

At the end of the t_{MON_DELAY} the gate of the driven device is pulled toward the V_{POS} level in order to ensure an appropriate drive to minimize the power losses. The external power device is considered in overload whenever the voltage on its output, sensed via the V_{ON_SENSE} pin, is above V_{ONth}. The comparison value is programmable setting at a certain level, by means of a resistive divider, the ON_LEV_PROG pin according to the following formula:

$$V_{ON\_LEV\_PROG} = V_{ONth.}\ 0.17$$

with

$$5V \leq V_{ONth.} \leq 15V$$

and

$$V_{ONth.} < V_{CC} - 1V.$$

If the ON_LEV_PROG pin is left floating the V_{ONth} level is set to 7.5V.

The overload status is signalled via the ALARM pin, active LOW. To inhibite the V_{ON} Monitor function, the V_{SENSE} pins must be grounded.

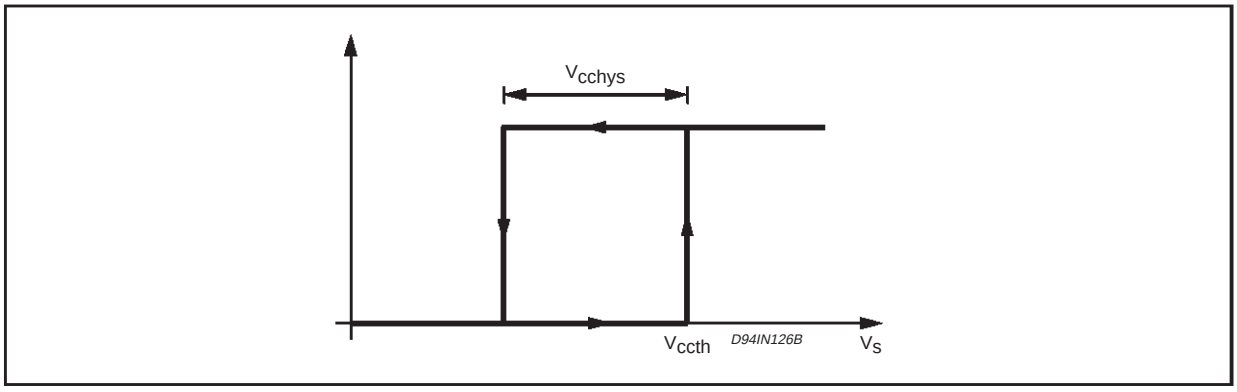
THERMAL PROCEDURE

As the junction temperature raises, two different events will take place. When the Over Temperature Threshold (T_{th1}), set at 130°C is reached, the ALARM output is activated (low level). If the temperature keeps on raising, up to the Over Temperatur Shutdown (T_{th2} = 160°C Typ) the output power device is turned off until the temperature decrease. To prevent an oscillating behaviour both the thresholds have a built-in hysteresis of 20°C.

UNDERVOLTAGE LOCK OUT

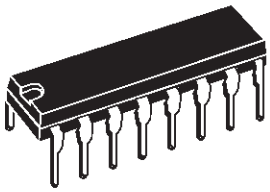
To avoid operation with non optimal drive of the external power device, an Undervoltage Lockout function is implemented. The OUT1 pin is forced close to V_{SS} until the V_{CC} supply voltage has reached the Undervoltage Upper Threshold (V_{CCth2}) value. If the supply voltage falls below the lower hysteresis value (i.e. V_{CCth1} - V_{CChys}) the OUT1 will be again forced close to V_{SS}. The built-in hysteresis will thus avoid intermittent functioning of the device at low supply voltage that may have a superimposed ripple.

Undervoltage Comparator Hysteresis

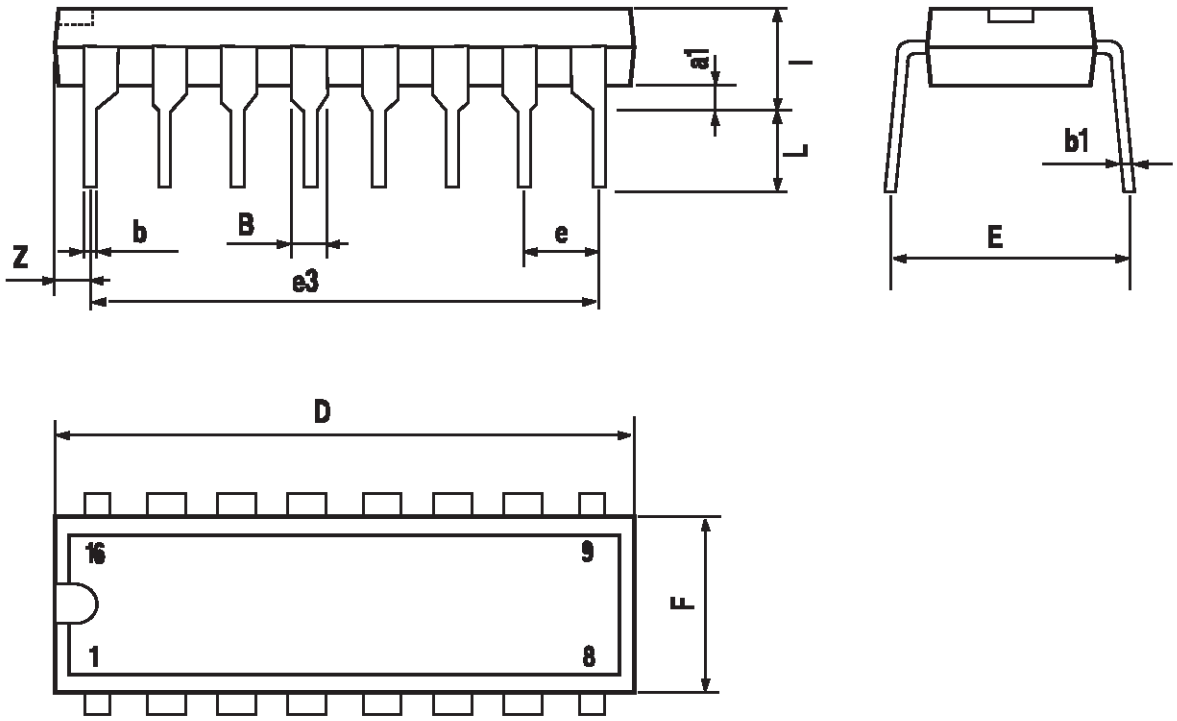


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

OUTLINE AND MECHANICAL DATA

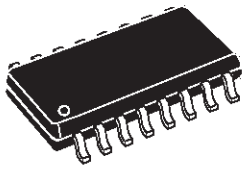


DIP16



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.009
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45° (typ.)					
D (1)	9.8		10	0.386		0.394
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F (1)	3.8		4	0.150		0.157
G	4.6		5.3	0.181		0.209
L	0.4		1.27	0.016		0.050
M			0.62			0.024
S	8°(max.)					

OUTLINE AND MECHANICAL DATA



SO16 Narrow

(1) D and F do not include mold flash or protrusions. Mold flash or potrusions shall not exceed 0.15mm (.006inch).