YM12864T-2

图形点阵式液晶显示模块
使用说明

大连佳显电子有限公司

地址: 大连市沙河口区工华街17号轩煌大厦六楼

邮编: 116021

电话: (0411)84619565

传真: (0411)84619585

E-mail: market@good-lcd.com

网址： http://www.good-lcd.com

RECORDS OF REVISION

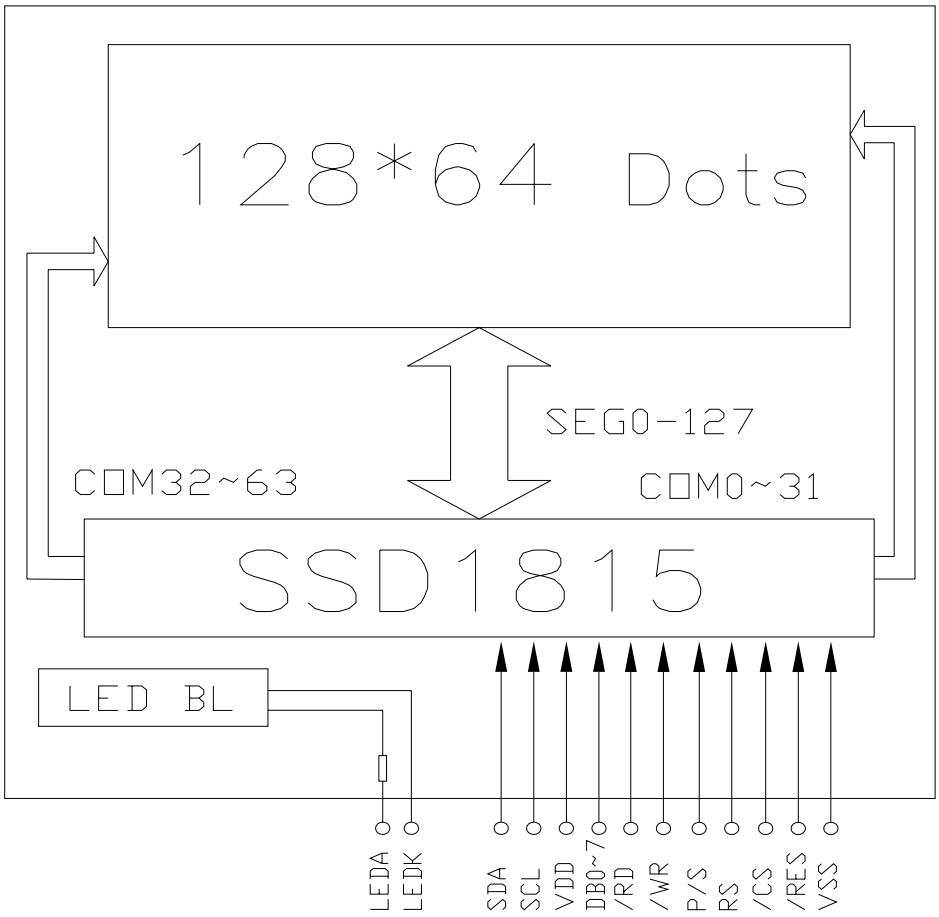
DATE	REVISED NO.	REVISED DESCRIPTIONS	PREPARED	CHECKED	APPROVED
Apr-1-2006	1.00	FIRST ISSUE	tfb		

CONTENTS

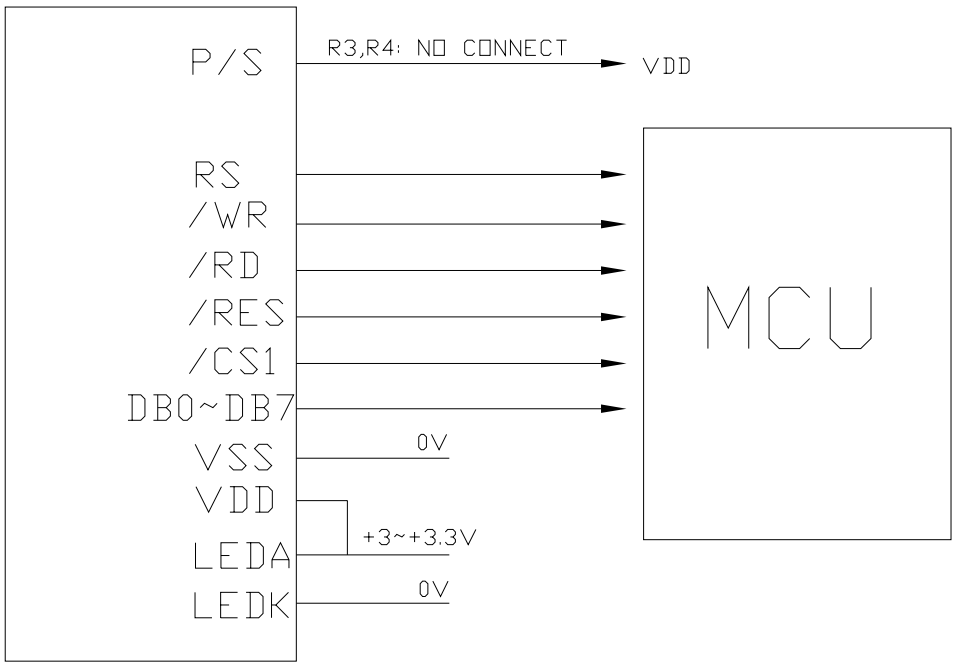
1. FEATURES：

ITEM	STANDARD VALUE	UNIT
Display Type	128 x 64 dots	-
LCD Type	■STN (Blue-white mode), Transmissive, Negative	-
LCD Duty	1/65	-
LCD Bias	1/9	-
Viewing Direction	6:00	-
Backlight Type	□BLUE(LED) □YELLOW-GREEN(LED) ■WHITE (LED)	-
Interface	8080 Series / 6800 Series / Serial Interface	-
Driver IC	SSD1815	-
Module Dimension	55.2(W) X39.8 (H) X6.0 (MAX)(T)	mm
Effective Display Area	40.92(W) X24.28 (H)	mm
Dot Size	0.28 (W) X 0.34 (H)	mm
Dot Pitch	0.32 W) X 0.38 (H)	mm

2. BLOCK DIAGRAM &APPLICATION CIRCUIT：

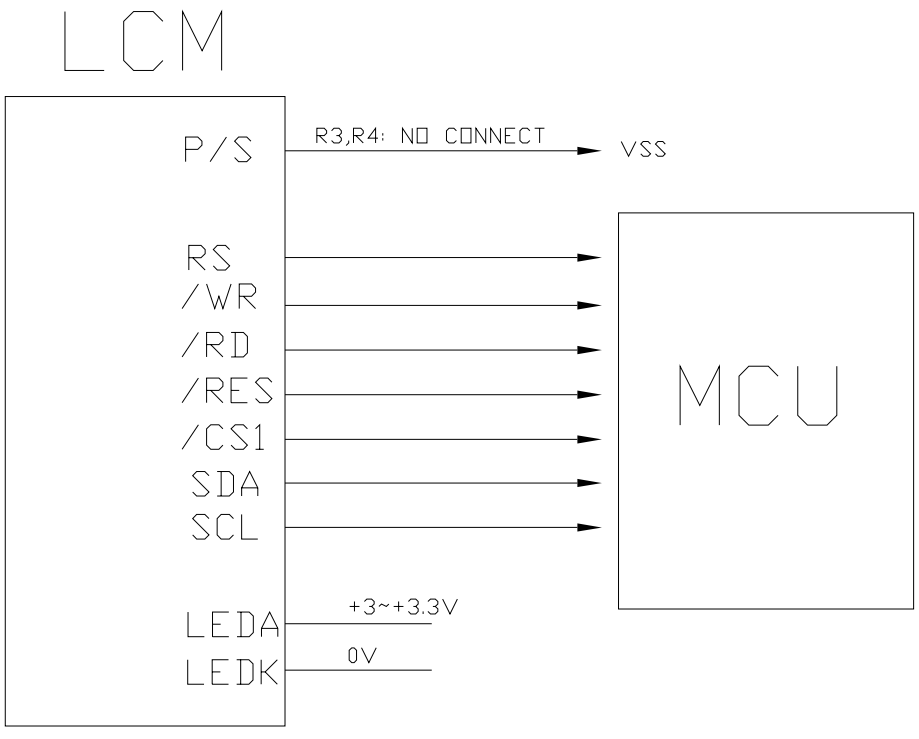


Parallel Application



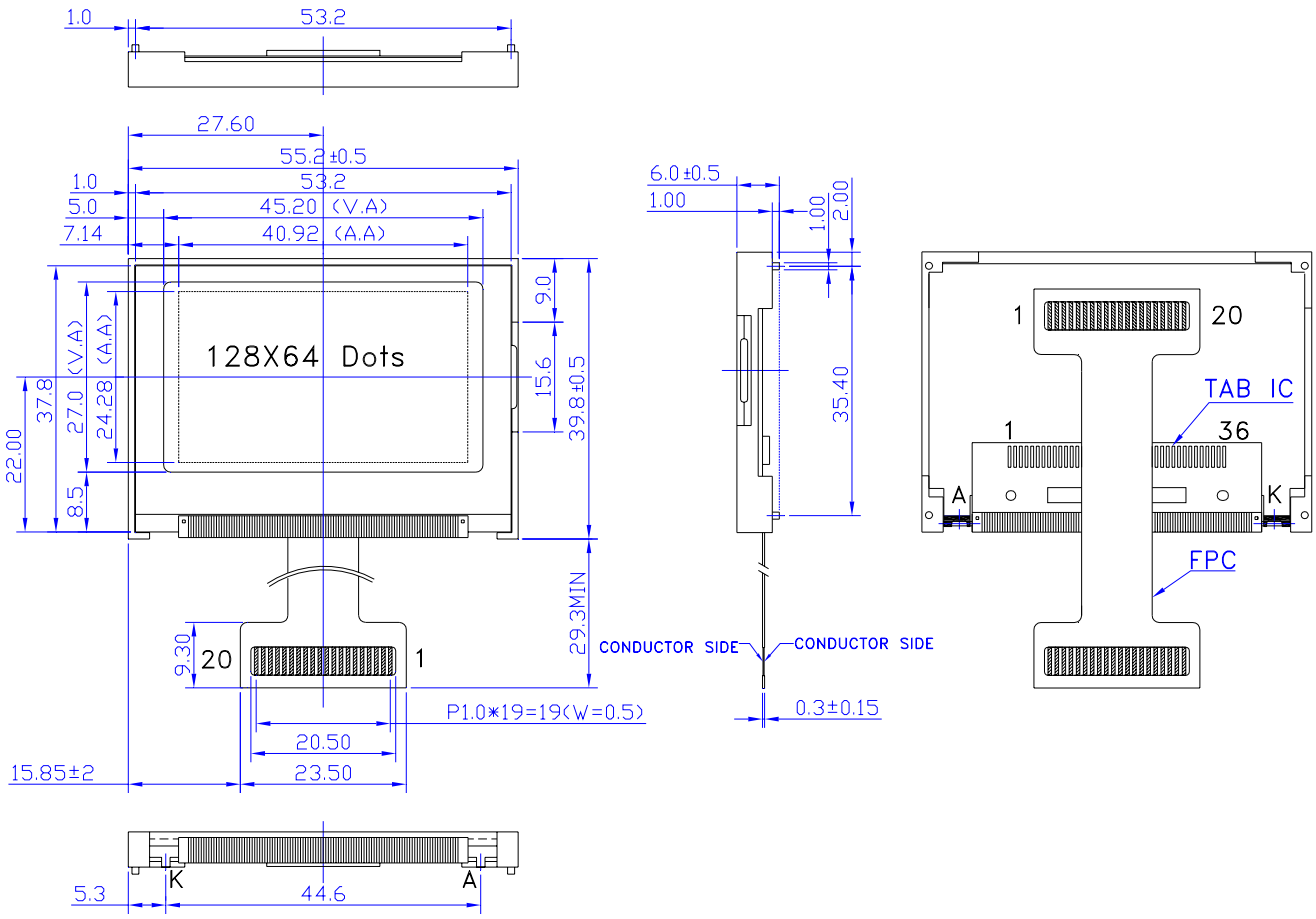
NOTE:
R1--0Ω RESISTOR: 6800-SERIES
R2--0Ω RESISTOR: 8080-SERIES
R3--0Ω RESISTOR: PARALLEL

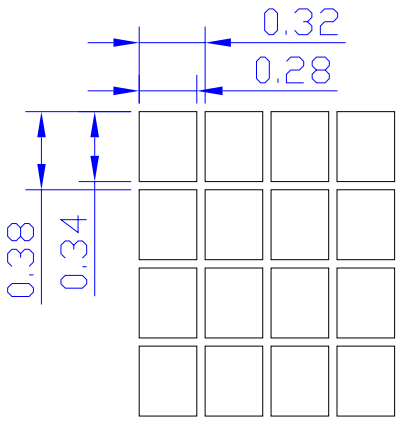
Serial Interface Application



NOTE:
R4--0Ω RESISTOR: SERIAL INTERFACE

3. OUTLINE DIMENSIONS





4. ABSOLUTE MAXIMUM RATING

ITEM	SYMBOL	CONDITION	STANDARD VALUE			UNIT
			MIN	TYP	MAX	
POWER SUPPLY FOR LOGIC	VDD	Ta=25℃	-0.3	—	+4	V
INPUT VOLTAGE	VIN	Ta=25℃	VSS-0.3	—	VDD+0.3	V
Module OPERATION TEMPERATURE	TOPR	---	-20	—	+70	℃
Module STORAGE TEMPERATURE	TSTG	---	- 30	—	+80	℃
Storage Humidity	H_D	Ta < 40 °C	-		90	%RH

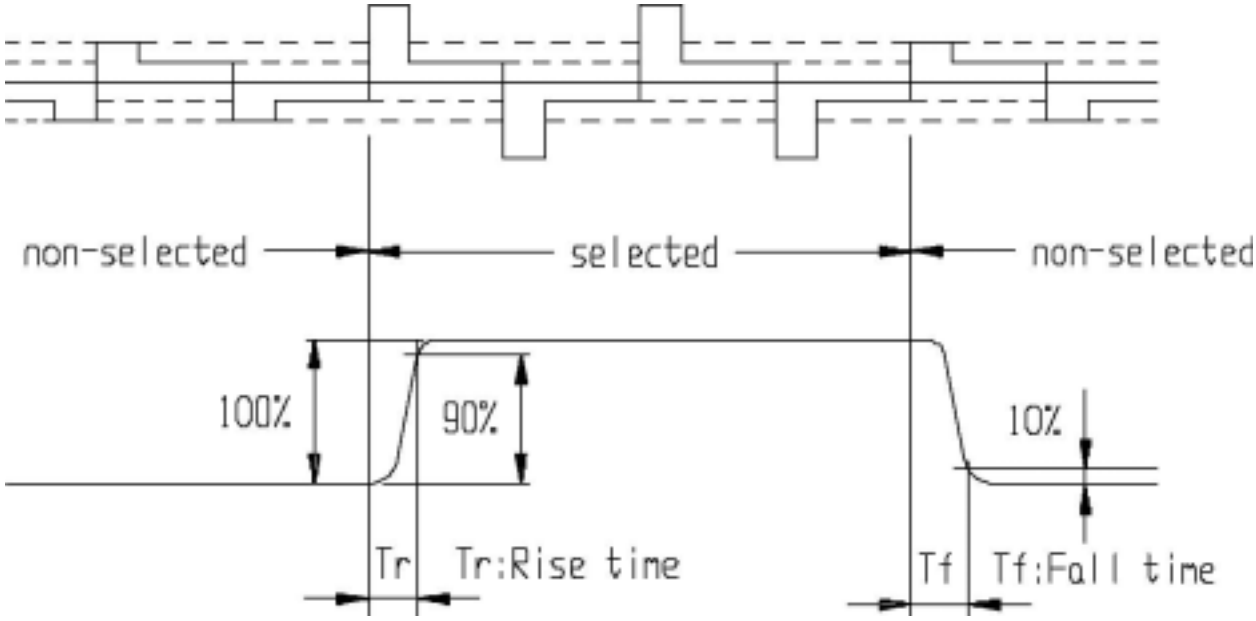
5. ELECTRICAL CHARACTERISTICS

ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Supply Voltage (logic)	VDD-VSS	-	2.4	3.3	3.5	V
Supply Voltage (LCD)	VDD-V0	Ta= +25℃	-	9.6	-	V
Input signal voltage	V-IH	"H" level	0.8VDD	-	VDD	V
	V-IL	"L" level	VSS	-	0.2VDD	V
Output signal voltage	V-OH	"H" level	0.8VDD	-	VDD	V
	VOL	"H" level	VSS	-	0.2VDD	V
Supply Current (logic)	IDD	VDD=3.0V	-	150	200	μA
Backlight Voltage	V-BL	BLUE(LED) Y-G(LED) WHITE (LED)	-	2.9 2.0 2.8	-	V
Backlight Current	I-BL	BLUE(LED) Y-G(LED) WHITE (LED)	-	20mA 60mA 40mA	-	mA
Backlight Driver Wave						kHz
Backlight Brightness						
Backlight Life Time						

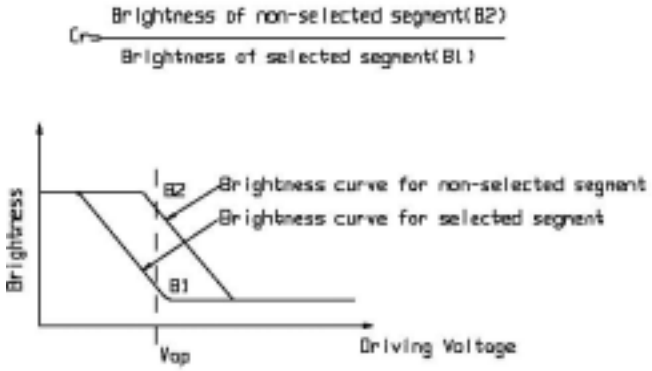
6. OPTICAL CHARACTERISTICS

Item	Symbol	Condition	Min	Typ	Max	Unit	Remarks	Note
Response Time	Tr	-	-	239	-	ms	-	1
	Tf	-	-	83	-	ms	-	1
Contrast Ratio	Cr	-	-	8.5	-	-	-	2
Viewing Angle Range	θ	Cr≥ 2	33	-	-	deg	Ø= 90	3
			32	-	-	deg	Ø = 270	3
			54	-	-	deg	Ø = 0	3
			34	-	-	deg	Ø = 180	3

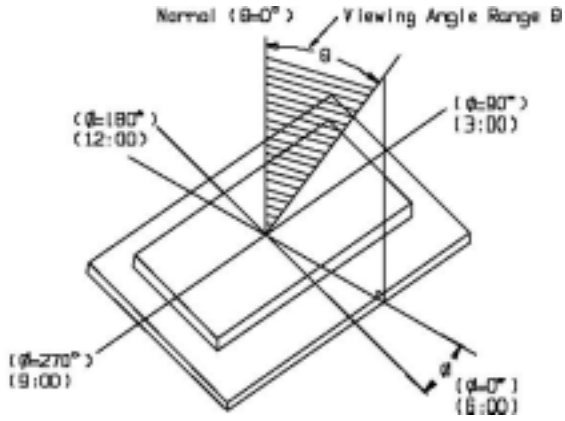
Note 1. Definition of response time



Note 2. Definition of Contrast Ratio 'Cr'



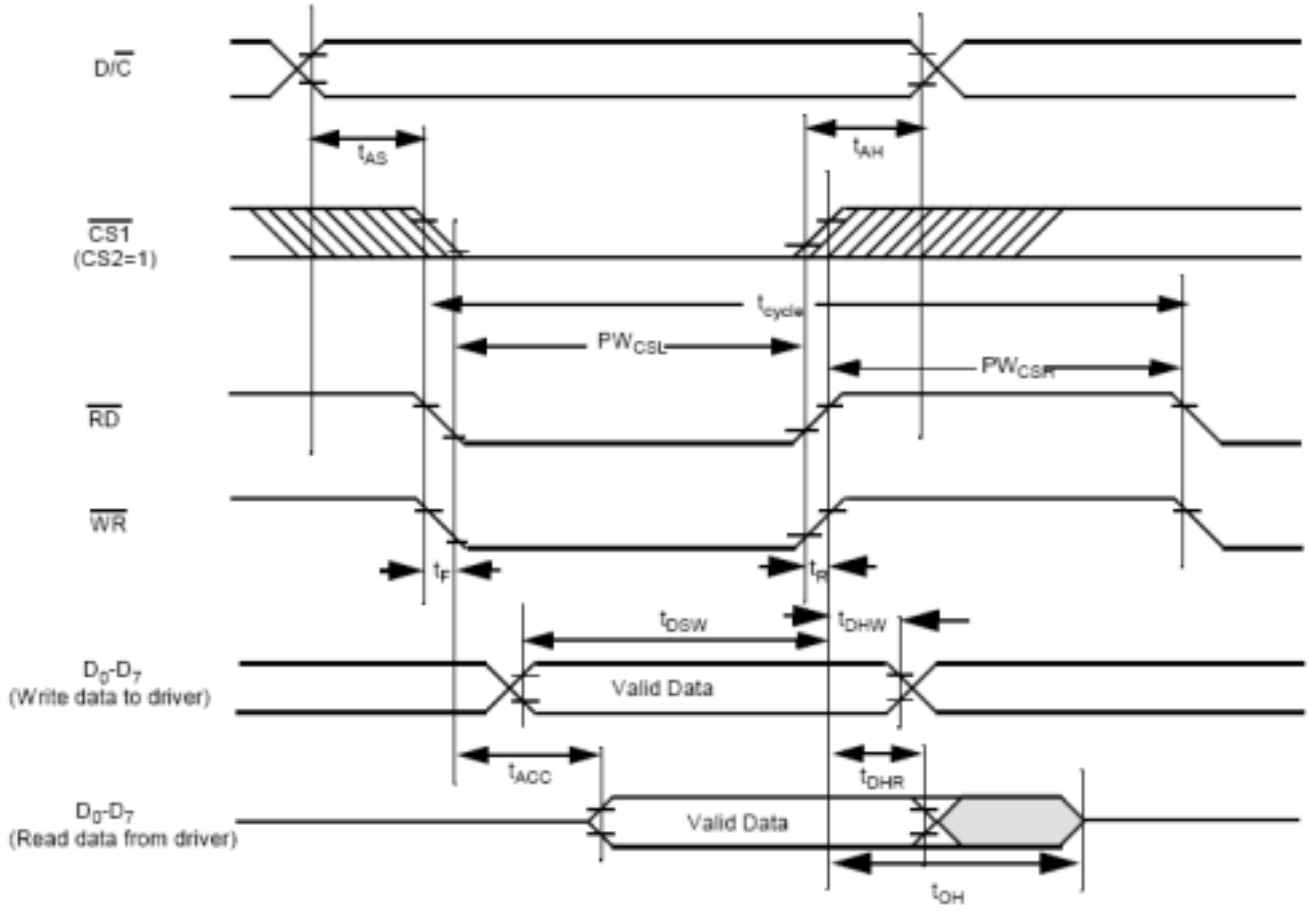
Note 3. Definition of Viewing Angle Range 'q'



7. TIMING CHARACTERISTICS

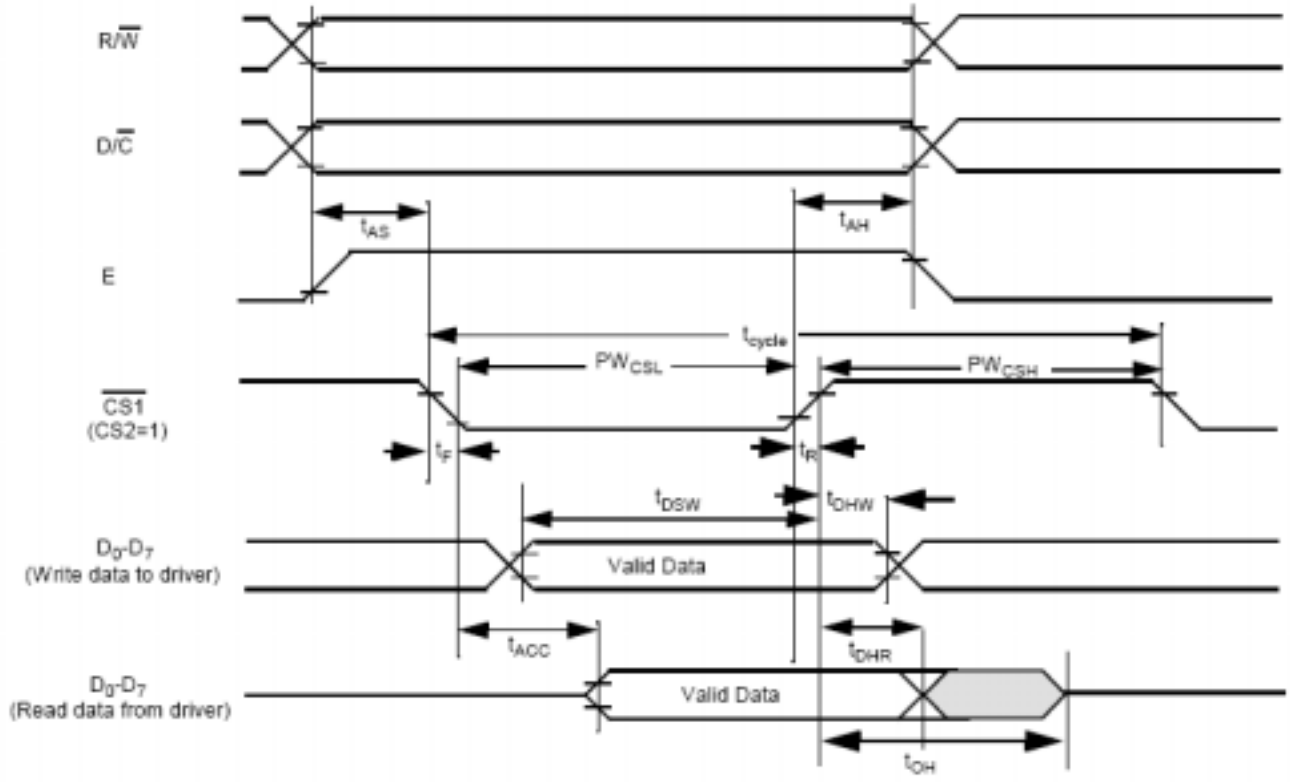
7.1 8080-Series MPU Parallel Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	- -	- -	ns ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	- -	- -	ns ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



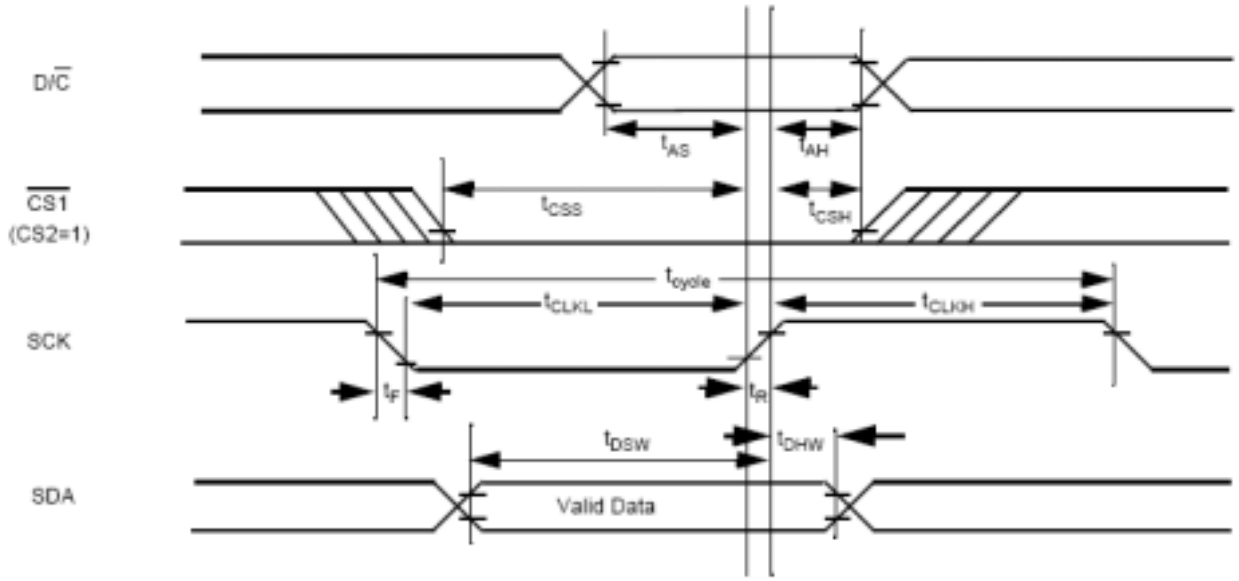
7.2 6800-Series MPU Parallel Interface Timing Characteristics

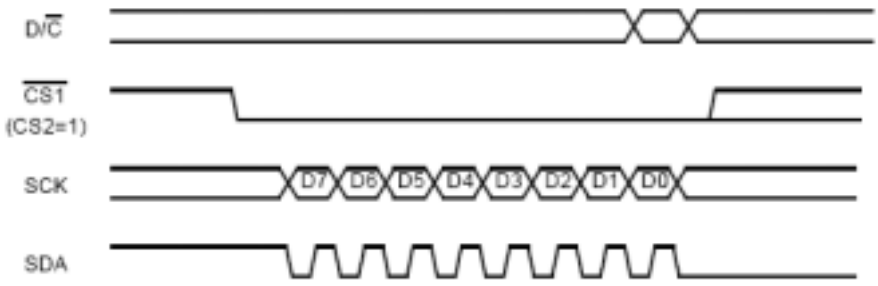
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	- -	- -	ns ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	- -	- -	ns ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



7.3 Serial Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time (for D_7 input)	120	-	-	ns
t_{CSH}	Chip Select Hold Time (for D_0 input)	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns





8. DISPLAY CONTROL INSTRUCTION

COMMAND TABLE

Bit Pattern	Write Command (D/C=0, R/W(WR)=0, E(RD)=1)	Comment
0000$X_3X_2X_1X_0$	Set Lower Column Address	Set the lower nibble of the colume address register using $X_3X_2X_1X_0$ as data bits. The initial display line register is reset to 0000b during POR.
0001$X_3X_2X_1X_0$	Set Higher Column Address	Set the higher nibble of the colume address register using $X_3X_2X_1X_0$ as data bits. The initial display line register is reset to 0000b during POR.
00100$X_2X_1X_0$	Set Internal Regulator Resistor Ratio	Internal regulator gain increases as $X_2X_1X_0$ increased from 000b to 111b. At POR, $X_2X_1X_0$ = 100b.
00101$X_2X_1X_0$	Set Power Control Register	X_0=0: turns off the output op-amp buffer (POR) X_0=1: turns on the output op-amp buffer X_1=0: turns off the internal regulator (POR) X_1=1: turns on the internal regulator X_2=0: turns off the internal voltage booster (POR) X_2=1: turns on the internal voltage booster
01$X_5X_4X_3X_2X_1X_0$	Set Display Start Line	Set display RAM display start line register from 0-63 using $X_5X_4X_3X_2X_1X_0$. Display start line register is reset to 000000 during POR.
10000001 * * $X_5X_4X_3X_2X_1X_0$	Set Contrast Control Register	Set Contrast level from 64 contrast steps. Contrast increases (V_{L0} decreases) as $X_5X_4X_3X_2X_1X_0$ is increased. $X_5X_4X_3X_2X_1X_0$ = 100000b (POR)
1010000X_0	Set Segment Re-map	X_0=0: column address 00h is mapped to SEG0 (POR) X_0=1: column address 83h is mapped to SEG0 Refer to Figure 5 for example.
1010001X_0	Set LCD Bias	X_0=0: 1/9 bias (POR) X_0=1: 1/7 bias For setting bias ratio to 1/4, 1/5, 1/6 or 1/8, see Extended Command Table.
1010010X_0	Set Entire Display On/Off	X_0=0: normal display (POR) X_0=1: entire display on
1010011X_0	Set Normal/Reverse Display	X_0=0: normal display (POR) X_0=1: reverse display
1010111X_0	Set Display On/Off	X_0=0: turns off LCD panel (POR) X_0=1: turns on LCD panel
1011$X_3X_2X_1X_0$	Set Page Address	Set GDDRAM Page Address (0-8) using $X_3X_2X_1X_0$
1100X_3 * * *	Set COM Output Scan Direction	X_3=0: normal mode (POR) X_3=1: remapped mode, COM0 to COM[N-1] becomes COM[N-1] to COM0 when Multiplex ratio is equal to N. See Figure 5 as an example for N equal to 64.
11100000	Set Read-Modify-Write Mode	Read-modify-write mode will be entered in which the column address will not be incremented during display data read. At POR, Read-modify-write mode is turned OFF.
11100010	Software Reset	Initialize the internal status register.
11101110	Set End of Read-Modify-Write Mode	Exit Read-modify-write mode. Column address before entering the mode will be restored. At POR, Read-modify-write mode is OFF.
1010110X_0 * * * * * * X_1X_0	Set Indicator On/Off Indicator Display Mode, This second byte command is required ONLY when "Set Indicator On" command is sent.	X_0 = 0: indicator off (POR, no need of second command byte) X_0 = 1: indicator on (second command byte required) X_1X_0 = 00: indicator off X_1X_0 = 01: indicator on and blinking at ~1 second interval X_1X_0 = 10: indicator on and blinking at ~1/2 second interval X_1X_0 = 11: indicator on constantly
11100011	NOP	Command for No Operation
11110000	Test Mode Reset	Reserved for IC testing. Do NOT use.
1111 * * * *	Set Test Mode	Reserved for IC testing. Do NOT use.
* * * * * * * *	Set Power Save Mode	Standby or sleep mode will be entered with compound commands

Bit Pattern	Read Command (D/C=0, R/W(WR)=1, E(RD)=0)	Comment
$D_7D_6D_5D_4D_3D_2D_1D_0$ (Data Read Back from the driver)	Status Register Read	D_7=0: indicates an internal operation is completed. D_7=1: indicates an internal operation is in progress. D_6=0: indicates reverse segment mapping with column address D_6=1: indicates normal segment mapping with column address D_5=0: indicates the display is ON D_5=1: indicates the display is OFF D_4=0: initialization is not in progress D_4=1: initialization is in progress after RES or software reset $D_3D_2D_1D_0$ = 1010, these 4-bit is fixed to 1010 which could be used to identify as Solomon Systech Device.

EXTENDED COMMAND TABLE

Bit Pattern	Command	Comment
10101000 00$X_5X_4X_3X_2X_1X_0$	$X_5X_4X_3X_2X_1X_0$: Set Multiplex Ratio	To select multiplex ratio N from 2 to 65 [Included Icon Line]. N = $X_5X_4X_3X_2X_1X_0$ + 2, eg. N = 111111b + 2 = 65 (POR)
10101001 $X_7X_6X_5X_4X_3X_2X_1X_0$	X_1X_0: Set Bias Ratio	X_1X_0 = 00: 1/8, 1/6 X_1X_0 = 01: 1/6, 1/5 X_1X_0 = 10: 1/9, 1/7 (POR) X_1X_0 = 11: Prohibited
	$X_4X_3X_2$: Set TC Value	$X_4X_3X_2$ = 000: -0.01%/C (TC0, POR) $X_4X_3X_2$ = 010: -0.10%/C (TC2) $X_4X_3X_2$ = 100: -0.18%/C (TC4) $X_4X_3X_2$ = 111: -0.25%/C (TC7) $X_4X_3X_2$ = 001, 011, 101, 110: Reserved
	$X_7X_6X_5$: Modify Osc. Freq.	Increase the value of $X_7X_6X_5$ will increase the oscillator frequency and vice versa. This command is not recommended to be used. $X_7X_6X_5$ = 011(POR)
1010101X_0	X_0: Set 1/4 Bias Ratio	X_0 = 0: use Normal Setting (POR) X_0 = 1: fixed at 1/4 Bias
11010010 0$X_6X_5$0010	X_6X_5: Set Total Frame Phases	The On/Off of the Static Icon is given by 3 phases/1 phase overlapping of the M and MSTAT signals. This command set how many phases of dividing the M/MSTAT signals for each frame. The more the phases, the less the overlapping and thus the lower the effective driving voltage. X_6X_5 = 00: 3 phases X_6X_5 = 01: 5 phases X_6X_5 = 10: 7 phases (POR) X_6X_5 = 11: 16 phases
11010011 00$X_5X_4X_3X_2X_1X_0$	$X_5X_4X_3X_2X_1X_0$: Set Display Offset (for mux ratio has been set less than 64 only)	After POR, $X_5X_4X_3X_2X_1X_0$ = 0 After setting mux ratio less than 64, data will be displayed at Center of matrix. See Table 1. To move display towards Row 0 by L, $X_5X_4X_3X_2X_1X_0$ = L To move display away from Row 0 by L, $X_5X_4X_3X_2X_1X_0$ = 64-L Note: max. value of L = (64 - display mux)/2

Note: Patterns other than that given in Command Table and Extended Command Table are prohibited to enter to the chip as a command. Otherwise, unexpected result will occurs.

Data Read / Write

To read data from the GDDRAM, input High to R/W(WR) pin and D/C pin for 6800-series parallel mode, Low to E(RD) pin and High to D/C pin for 8080-series parallel mode. No data read is provided for serial mode. In normal mode, GDDRAM column address pointer will be increased by one automatically after each data read. However, no automatic increase will be performed in read-modify-write mode. Also, a dummy read is required before the first data read. See Figure 3 in Functional Description.

To write data to the GDDRAM, input Low to R/W(WR) pin and High to D/C pin for 6800-series parallel mode. For serial interface, it will always be in write mode. GDDRAM column address pointer will be increased by one automatically after each data write.

Address Increment Table (Automatic)

D/C	R/W(WR)	Comment	Address Increment	Remarks
0	0	Write Command	No	
0	1	Read Status	No	
1	0	Write Data	Yes	
1	1	Read Data	Yes	*1

Address Increment is done automatically after data read write. The column address pointer of GDDRAM*2 is affected.

Remarks: 1. If read data is issued in read-modify-write mode, address will NOT be increased.
2. Column Address will NOT wrap round to zero when overflow.

Commands Required for R/W(WR) Actions on RAM

R/W(WR) Actions on RAMs	Commands Required	
Read/Write Data from/to GDDRAM.	Set GDDRAM Page Address Set GDDRAM Column Address Read/Write Data	$(1011X_3X_2X_1X_0)$* $(0001X_3X_2X_1X_0)$* $(0000X_3X_2X_1X_0)$ $(X_7X_6X_5X_4X_3X_2X_1X_0)$
Save/Restore GDDRAM Column Address.	Save GDDRAM Column Address by read-modify-write mode Restore GDDRAM Column Address by end of read-modify-write mode	(11100000) (11101110)

Note: 1. No need to resend the command again if it is set previously.
2. The read / write action to the Display Data RAM does not depend on the display mode. This means the user can change the RAM content whether the target RAM content is being displayed or not.

Command Description

Set Lower Column Address

This command specifies the lower nibble of the 8-bit column address of the display data RAM. The column address will be incremented by each data access after it is pre-set by the MCU.

Set Higher Column Address

This command specifies the higher nibble of the 8-bit column address of the display data RAM. The column address will be incremented by each data access after it is pre-set by the MCU.

Set Internal Regulator Resistors Ratio

This command is to enable any one of the eight internal resistor sets for different regulator gain when using internal regulator resistor network (IRS pin pulled high). Please refer to Block Diagram Description section for detail calculation of the LCD driving voltage.

Set Power Control Register

This command turns on/off the various power circuits associated with the chip.

Set Display Start Line

This command is to set Display Start Line register to determine starting address of display RAM to be displayed by selecting a value from 0 to 63. With value equals to 0, D0 of Page 0 is mapped to COM0. With value equals to 1, D1 of Page0 is mapped to COM0. The display start line values of 0 to 63 are assigned to Page 0 to 7.

Set Contrast Control Register

This commands adjusts the contrast of the LCD panel by changing V_{L6} of the LCD drive voltage provided by the On-Chip power circuits. V_{L6} is set with 64 steps (6-bit) contrast control register. It is a compound commands:

Set Segment Re-map

This commands changes the mapping between the display data column address and segment driver. It allows flexibility in layout during LCD module assembly. Refer to Figure 5 for example.

Set LCD Bias

This command selects a suitable bias ratio (1/7 or 1/9) required for driving the particular LCD panel in use. The POR default for SSD1815 is set to 1/9 bias. For setting 1/4, 1/5, 1/6 and 1/8 bias, an extended compound command should be used.

Set Entire Display On/Off

This command forces the entire display, including the icon row, to be "ON" regardless of the contents of the display data RAM. This command has priority over normal/reverse display. This command will be used with "Set Display Display ON/OFF" command to form a compound command for entering power save mode. See "Set Power Save Mode".

Set Normal/Reverse Display

This command sets the display to be either normal/reverse. In normal display, a RAM data of 1 indicates an "ON" pixel while in reverse display, a RAM data of 0 indicates an "ON" pixel. In icon mode, the icon line is not reversed by this command.

Set Display On/Off

This command alternatively turns the display on and off. When display off is issued with entire display on, power save mode will be entered. See "Set Power Save Mode" for details.

Set Page Address

This command positions the page address from 0 to 8 possible positions in GDDRAM. Refer to Figure 5 for mapping.

Set COM Output Scan Direction

This command sets the scan direction of the COM output allowing layout flexibility in LCD module assembly.

Set Read-Modify-Write Mode

This command puts the chip in read-modify-write mode in which:

1. the column address is saved before entering the mode
2. the column address is incremented by display data write but not by display data read

Software Reset

This command causes some of the internal status registers of the chip to be initialized:

1. Static indicator is turned OFF
2. Display start line register is set to 0
3. Column address counter is set to 0
4. Page address is set to 0
5. Normal scan direction of the COM outputs
6. Contrast control register is set to 0
7. Test mode is turned OFF

Set End of Read-Modify-Write Mode

This command relieves the chip from read-modify-write mode. The column address that is saved before entering read-modify-write mode will be restored.

Set Indicator On/Off

This command turns on and off the static drive indicators. It also controls whether standby mode or sleep mode will be

entered after the power save compound command. See "Set Power Save Mode".

When the "Set Indicator On" command is sent, the "Indicator Display Mode" must be followed in the next command. The "Set Indicator Off" command is a single byte command and no following command is required.

NOP

A command causing No Operation.

Set Test Mode

This command force the driver chip into its test mode for internal testing of the chip. Under normal operation, user should NOT use this command.

Set Power Save Mode

To enter Standby or Sleep Mode, it should be done by using a compound command composed of "Set Display ON/OFF" and "Set Entire Display ON/OFF" commands. When "Set Entire Display ON" is issued when display is OFF, either Standby Mode or Sleep Mode will be entered.

The status of the Static Indicator will determine which power save mode is entered. If static indicator is off, the Sleep Mode will be entered:

1. Internal oscillator and LCD power supply circuits are stopped
2. Segment and Common drivers output V_{DD} level
3. The display data and operation mode before sleep are held
4. Internal display RAM can still be accessed

If the static indicator is on, the chip enters Standby Mode which is similar to sleep mode except:

1. Internal oscillator is on
2. Static drive system is on

Note also that if the software reset command is issued during Standby Mode, Sleep Mode will be entered. Both power save modes can be exited by the issue of a new software command or by pulling Low at hardware pin $\overline{RES}$.

Status register Read

This command is issued by pulling D/$\overline{C}$ Low during a data read (refer to Figure 9 and 10 for parallel interface waveforms). It allows the MCU to monitor the internal status of the chip. No status read is provided for serial mode.

EXTENDED COMMANDS

These commands are used, in addition to basic commands, to trigger the enhanced features, on top of general ones, designed for the chip.

Set Multiplex Ratio

This command switches default 64 multiplex mode to any multiplex mode from 2 to 64. The chip pads ROW0-ROW63 will be switched to corresponding COM signal output, see Table 1 for examples of different multiplex settings.

Set Bias Ratio

Except the 1/4 bias, all the available bias ratios (1/5, 1/6, 1/7, 1/8 and 1/9) could be set using this command plus the Set LCD Bias. When changing the display multiplex ratio, the bias ratio also need to be adjusted to make display contrast consistent.

Set Temperature Coefficient (TC) Value

4 different temperature coefficient settings is selected by this command in order to match various liquid crystal temperature grades.

Modify Oscillator Frequency

The oscillator frequncy can be fine tuned by applying this command. Since the oscillator frequency will be affected by some other factors, this command is not recommended for general usage. Please contact our application engineer for more detail explaination on this command.

Set 1/4 Bias Ratio

This command sets the bias ratio directly to 1/4 bias. This ratio is especially for use in under 12mux display.

In order to restore to other bias ratio, this command must be executed, with LSB=0, before the "Set Multiplex ratio" or "Set LCD Bias" command is sent.

Set Total Frame Phases

The total number of phases for one display frame is set by this command.

The Static Icon is generated by the overlapping of the M and MSTAT signals. To turn on the Static Icon, 3 phases overlapping will be applied to these signals, while 1 phase overlapping will be given to the Off status.

The more the total number of phasesin one frame, the less the overlapping time and thus the lower the effective driving voltage at the Static Icon on the LCD panel.

Set Display Offset

This command should be sent ONLY when the multiplex ratio is set less than 64.

When the mulitplex ratio less than 64 is set, the display will be mapped in the middle (y-direction) of the LCD, see Table 1. Use this command could move the display vertically within the 64 commons.

To make the Reduced-Mux Com 0 (Com 0 after reducing the multiplex ratio) towards the Row 0 direction for L lines, the 6-bit data in second command should be given by L.

To move in the other direction by L lines, the 6-bit data should be given by 64-L.

Please note that the display is confined within the un-reduced 64 mux. That is maximum value of L is given by the half of 64 minus the reduced-multiplex ratio. For an odd display mux after reduction, moving away from Row 0 direction will has 1 more step.

9. DISPLAY CONTROL FUNCTIONS

Command Decoder and Command Interface

This module determines whether the input data is interpreted as data or command. Data is directed to this module based upon the input of the D/C pin. If D/C is high, data is written to Graphic Display Data RAM (GDDRAM). If D/C is low, the input at D_7-D_0 is interpreted as a Command and it will be decoded and be written to the corresponding command register.

MPU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D_7-D_0), R/W(WR), D/C, E(RD), CS1 and CS2. R/W(WR) input High indicates a read operation from the Graphic Display Data RAM (GDDRAM) or the status register. R/W(WR) input Low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of D/C input. The E(RD) input serves as data latch signal (clock) when high provided that CS1 and CS2 are low and high respectively. Refer to Figure 9 for Parallel Interface Timing Diagram of 6800-series microprocessors.

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 3 below.

MPU Parallel 8080-series interface

The parallel interface consists of 8 bi-directional data pins (D_7-D_0), E(RD), R/W(WR), D/C, CS1 and CS2. E(RD) input serves as data read latch signal (clock) when low provided that CS1 and CS2 are low and high respectively. Whether it is display data or status register read is controlled by D/C. R/W(WR) input serves as data write latch signal(clock) when high provided that CS1 and CS2 are low and high respectively. Whether it is display data or command register write is controlled by D/C. Refer to Figure 10 for Parallel Interface Timing Diagram of 8080-series microprocessor.

Similar to 6800-series interface, a dummy read is also required before the first actual display data read.

MPU Serial interface

The serial interface consists of serial clock SCK (D_6), serial data SDA (D_7), D/C, CS1 and CS2. SDA is shifted into a 8-bit shift register on every rising edge of SCL in the order of D_7, D_6,... D_0. D/C is sampled on every eighth clock to determine whether the data byte in the shift register is written to the Display Data RAM or command register at the same clock.

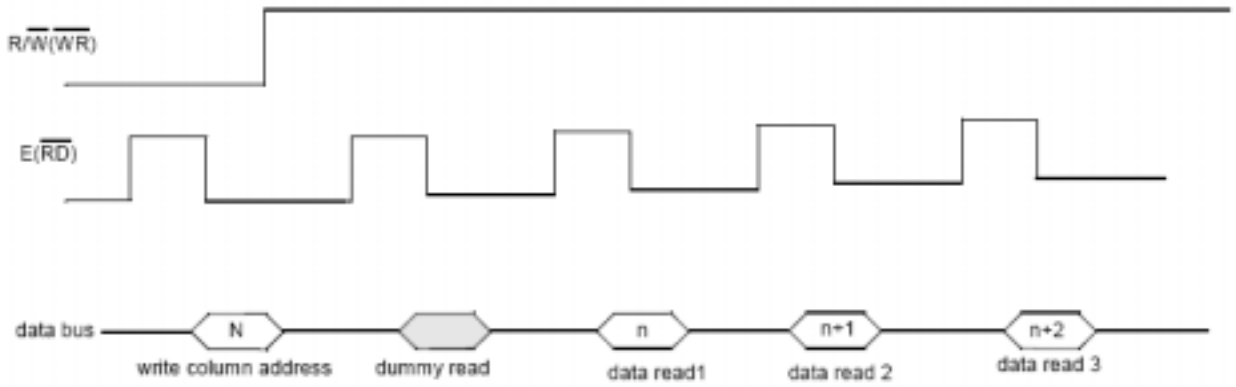


Figure 3 - Display data read with the insertion of dummy read

Oscillator Circuit

This module is an On-Chip low power RC oscillator circuitry (Figure 4). The oscillator generates the clock for the DC-DC voltage converter. This clock is also used in the Display Timing Generator.

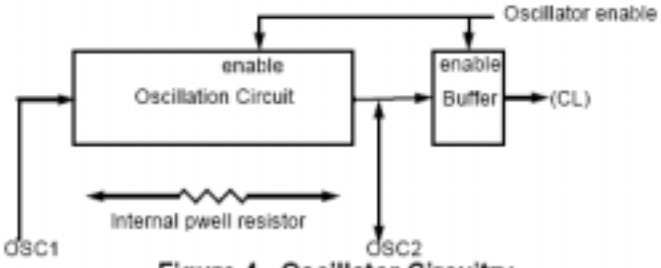
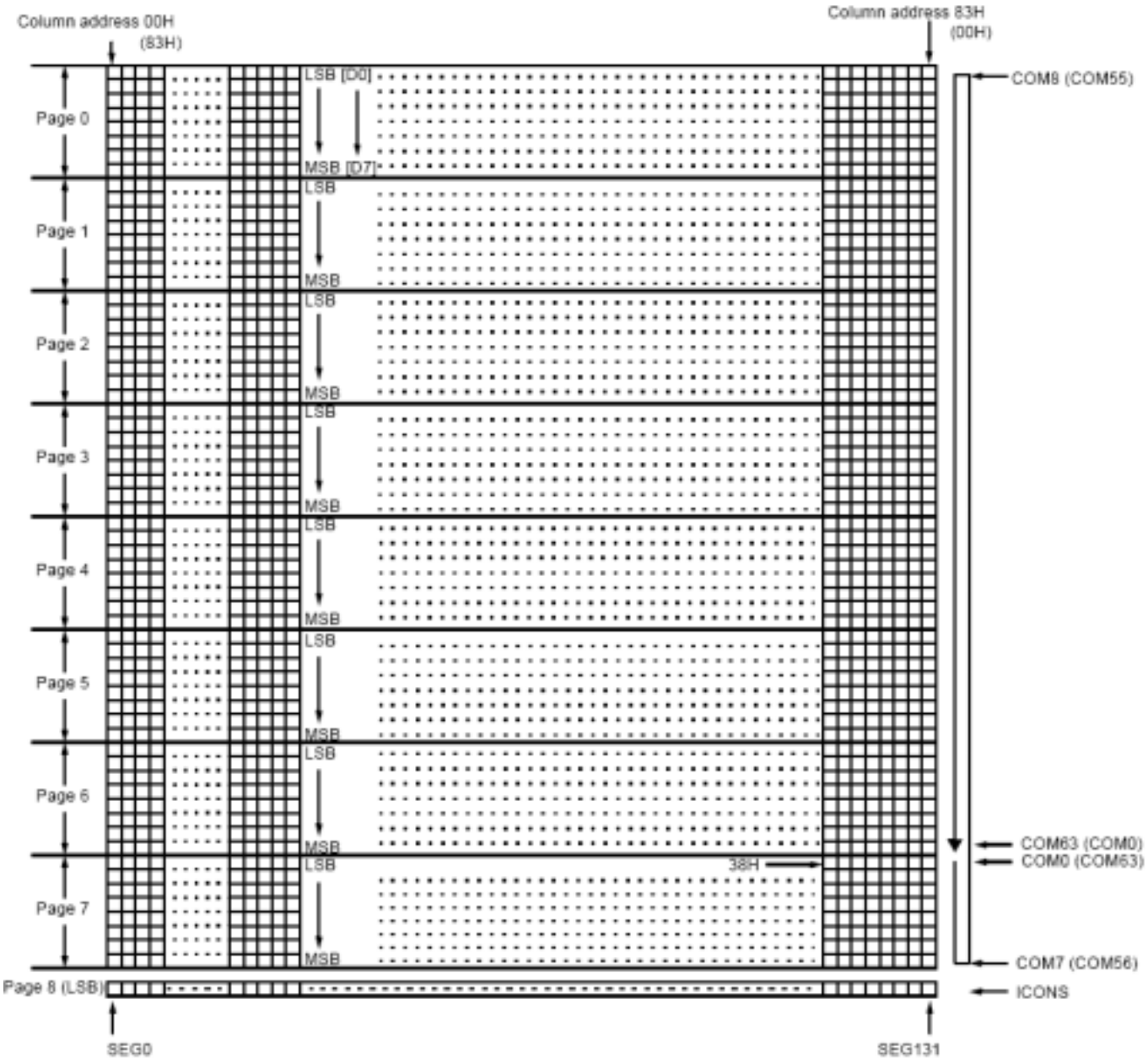


Figure 4 - Oscillator Circuitry

Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 132 X 65= 8580 bits. Figure 5 is a description of the GDDRAM address map. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. For vertical scrolling of display, an internal register storing the display start line can be set to control the portion of the RAM data to be mapped to the display. Figure 5 shows the case in which the display start line register is set to 38h.



Note: The configuration in parentheses represent the remapped values of Rows and Columns

Figure 5. Graphic Display Data RAM (GDDRAM) Address Map (with display start line at 38H)
For 132 X 64 Graphic Display Mode with separated Icon Line

LCD Driving Voltage Generator and Regulator

This module generates the LCD voltage required for display driving output. It takes a single supply input and generate necessary voltage levels. This block consists of:

1. 2X, 3X and 4X DC-DC voltage converter
   The built-in DC-DC voltage converter is use to generate large negative LCD driving voltage with reference to V_{DD} from the voltage input (V_{SS1}). For SSD1815, it is possible to produce 2X, 3X or 4X boosting from the protential different between V_{SS1} - V_{DD}.
   Detail configurations of the DC-DC converter for different boosting multiples are given in Figure 6 at the right.

2. Voltage Regulator (Voltages referenced to V_{DD})
   The feedback gain control for LCD driving contrast curves can be selected by IRS pin to either internal (IRS pin = H) or external (IRS pin = L).
   For internal resistor network is enabled, there are eight setting can be set by software.
   If external control is selected, external resistors are required to be connected between V_{DD} and V_F (R1), and between V_F and V_{L6} (R2).

3. Contrast Control (Voltages referenced to V_{DD})
   Software control of the 64 contrast voltage levels at each voltage regulator feedback gain. The equation of calculating the LCD driving voltage is given as:

$$V_{L6} - V_{DD} = Gain * (1 + \frac{Contrast}{\beta}) * V_{ref}$$

$$V_{ref} = (\frac{V_{BE} + R * (V_{DD} - V_{SS})}{1 + R})$$

where

Int. Reg. Resistor Ratio Setting	0	1	2	3	4	5	6	7	Ext. Resistor
Gain	-3.29	-3.76	-4.29	-4.82	-5.39	-5.76	-6.40	-6.95	-(1+Rb/Ra)
β	92.59	91.86	91.12	90.40	89.67	89.18	88.29	87.49	96.68

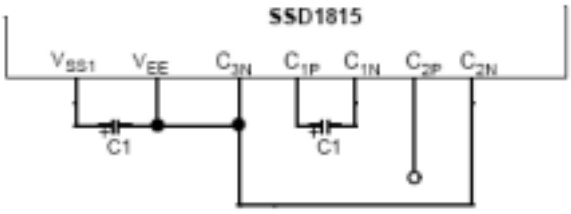
and

TC	0 (-0.01%/°C)	2 (-0.10%/°C)	4 (-0.18%/°C)	7 (-0.25%/°C)
V_{BE}	0.025	0.523	0.520	0.517
R	0.72	0.423	0.272	0.121

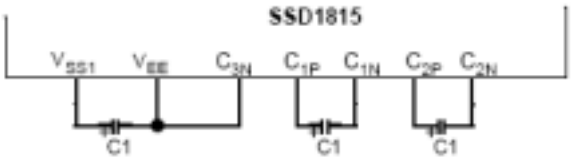
4. Bias Divider
   Divide the regulator output to give the LCD driving voltages (V_{L2} - V_{L6}). A low power consumption circuit design in this bias divider saves most of the display current comparing to traditional design.

5. Bias Ratio Selection circuitry
   Software control of 1/7 and 1/9 bias ratio to match the characteristic of LCD panel. In addition, 1/4, 1/5, 1/6 and 1/8 bias ratios are also software selectable using the extended command for any mux application.

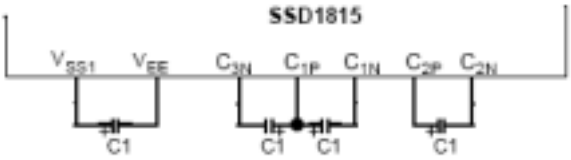
6. Self adjust temperature compensation circuitry
   This block provides 4 different compensation settings to satisfy various liquid crystal temperature gradings by software control. Default temperature coefficient (TC) setting is TC0.



2X Boosting Configuration



3X Boosting Configuration



4X Boosting Configuration

Remarks:
1. C1 = 0.47 - 1.0uF
2. Boosting input from V_{SS1}.
3. V_{SS1} should be lower potential than or equal to V_{SS}
4. All voltages are referenced to V_{DD}

Figure 6 - Configurations for DC-DC Converter

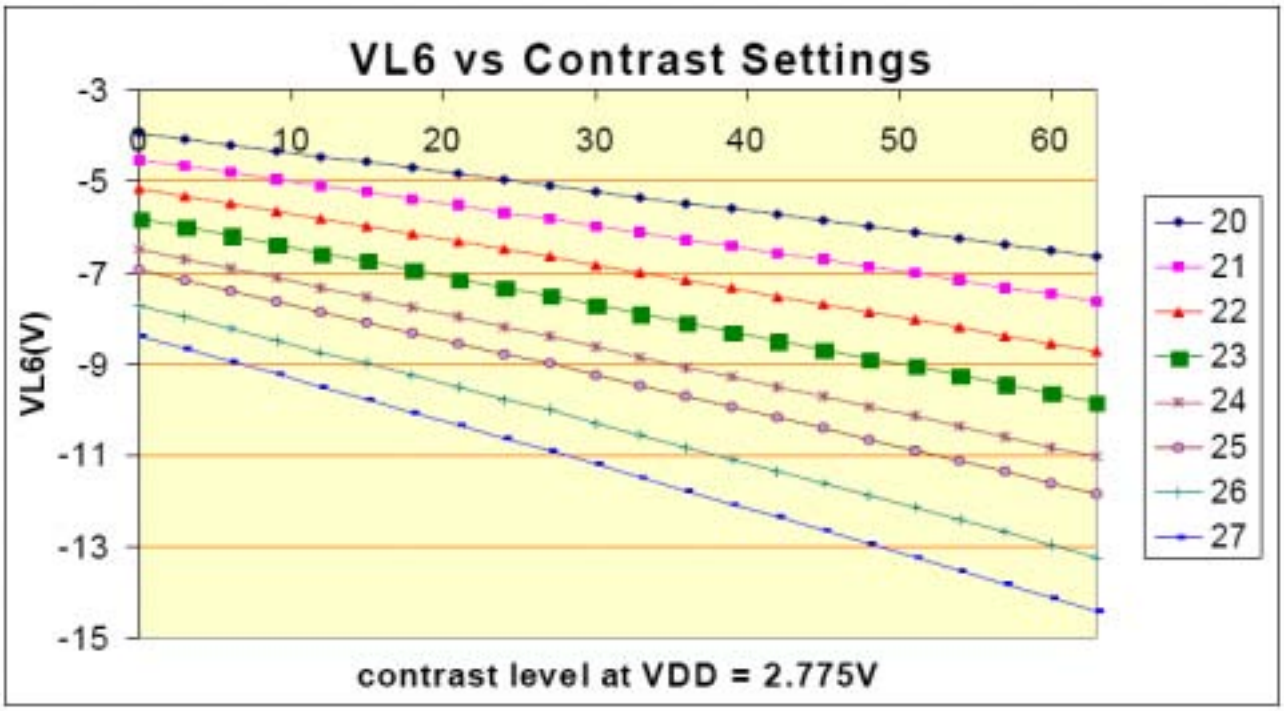


Figure 7 - Contrast Curves at Different Interneal Feedback Resistor Ratio Settings

Reset Circuit

This block includes Power On Reset circuitry and the Reset pin, RES. Both of these having the same reset function. Once RES receives a negative reset pulse, all internal circuitry will start to initialize. Minimum pulse width for completing the reset sequence is 1us. The status of the chip after reset is given by:

1. Display is turned OFF
2. 132X64 Display Display Mode with seperated Icon Line
3. Normal segment and display data column address mapping (SEG0 mapped to address 00h)
4. Read-modify-write mode is OFF
5. Power control register is set to 000b
6. Shift register data clear in serial interface
7. Bias ratio is set to 1/9
8. Static indicator is turned OFF
9. Display start line is set to display RAM column address 0
10. Column address counter is set to 0
11. Page address is set to 0
12. Normal scan direction of the COM outputs
13. Contrast control register is set to 20h
14. Test mode is turned OFF

Display Data Latch

A series of registers carrying the display signal information. For SSD1815, there are 197 latches (132 + 65) for holding the data, which will be fed to the HV Buffer Cell and Level Selector to output the required voltage level.

Level Selector

Level Selector is a control of the display synchronization. Display voltage can be separated into two sets and used with different cycles. Synchronization is important since it selects the required LCD voltage level to the HV Buffer Cell, which in turn outputs the COM or SEG LCD waveform.

HV Buffer Cell (Level Shifter)

HV Buffer Cell work as a level shifter which translates the low voltage output signal to the required driving voltage. The output is shifted out with an internal FRM clock which comes from the Display Timing Generator. The voltage levels are given by the level selector which is synchronized with the internal M signal.

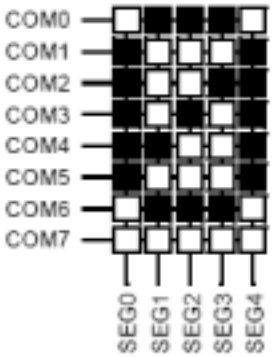
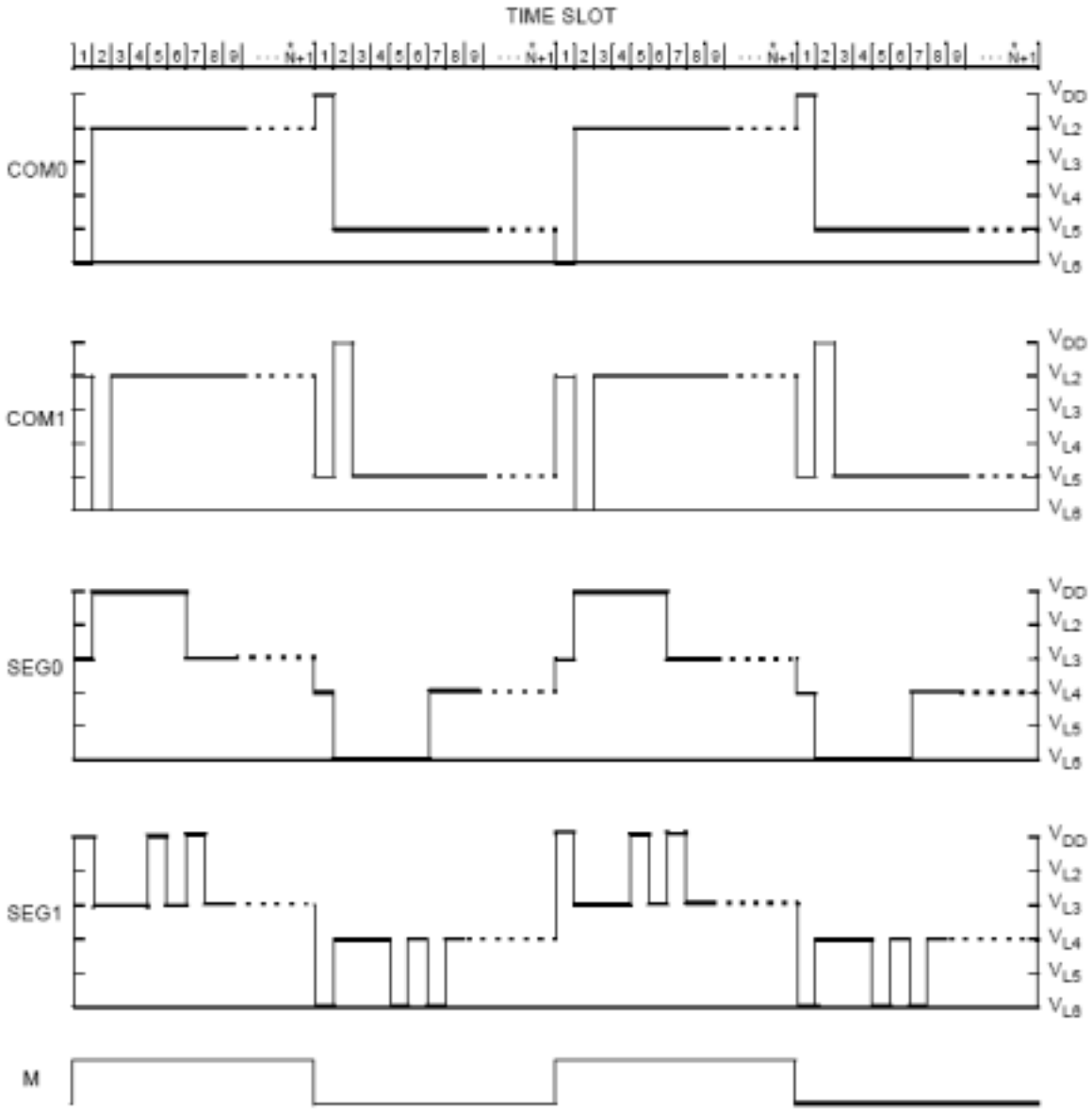


Figure 8a. LCD Display Example "0"



* Note : N is the number of multiplex ratio not included Icon, N is equal to 64 on POR.

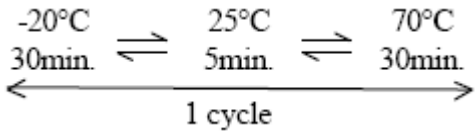
Figure 8b - LCD Driving Waveform

10. INTERFACE PIN CONNECTIONS

PIN	SYMBOL	I/O	FUNCTION
1	VSS		Ground pin, connected to 0V
2	/RES		Reset signal input: Initialization of the chip is started once this pin is pulled low. Minimum pulse width for completing the reset procedure is 5us.
3	/CS	I	Chip select input: The chip is enabled for MCU communication only when /CS is pulled low.
4	RS	I	Data/Command control pin: When the pin is pulled high, the data at DB0~DB7 is treated as display data. When the pin is pulled low, the data at DB0~DB7 wll be transferred to the command register
5	P/S	I	Parallel/Serial interface select: When the pin is pulled high, parallel interface mode is selected. When the pin is pulled low, serial interface will be selected. It is valid only when internal pull high resistor(R3) and pull low resistor(R4) are not used.
6	/WR	I	When interfacing to an 6800-series microprocessor, this pin will be used as Read/Write select input. Read mode will be carried out when this pin is pulled high and write mode when low. When interfacing to an 8080-series microprocessor, this pin will be the Write input. Data write operation is initiated when this pin is pulled low when the chip is selected.
7	/RD	I	When interfacing to an 6800-series microprocessor, this pin will be used as the Enable signal. Read/Write operation is initiated when this pin is pulled high when the chip is selected. When interfacing to an 8080-series microprocessor, this pin receives the Read signal. Data read operation is initiated when this pin is pulled low when the chip is selected.
8	DB0		8-bit bi-directional data bus
9	DB1		8-bit bi-directional data bus
10	DB2	O	8-bit bi-directional data bus
11	DB3	O	8-bit bi-directional data bus
12	DB4	O	8-bit bi-directional data bus
13	DB5	O	8-bit bi-directional data bus
14	DB6	O	8-bit bi-directional data bus
15	DB7	O	8-bit bi-directional data bus
16	VDD	I/O	Power for supply(3.0V)
17	SCL	I/O	Serial clock input
18	SDA	I/O	Serial data input
19	LEDA	I/O	LCD driver supplies voltage.
20	LEDK	I/O	LCD driver supplies voltage.

11.RELIABILITY

Content of Reliability Test

		Environmental Test		
No.	**Test Item**	**Content of Test**	**Test Condition**	**Applicable Standard**
1	High temperature storage	Endurance test applying the high storage temperature for a long time.	80 °C 200 hrs	
2	Low temperature storage	Endurance test applying the low storage temperature for a long time.	-30 °C 200 hrs	
3	High temperature operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70 °C 200 hrs	
4	Low temperature operation	Endurance test applying the electric stress under low temperature for a long time.	-20 °C 200 hrs	
5	High temperature Humidity storage	Endurance test applying the high temperature and high humidity storage for a long time.	50 °C , 90 RH 96 hrs	MIL-202E-103B JIS-C5023
6	High temperature Humidity operation	Endurance test applying the electric stress (Voltage & Current) and temperature humidity stress to the element for a long time.	50 °C , 90 RH 96 hrs	MIL-202E-103B JIS-C5023
7	Temperature cycle	Endurance test applying the low and high temperature cycle. 	-20°C - 70°C 10 cycles	
Mechanical Test				
8	Vibration test	Endurance test applying the vibration during transportation and using.	10-22Hz→1.5mmp-p 22-500Hz →1.5G Total 0.5hrs	MIL-202E-201A JIS-C5025 JIS-C7022-A-10
9	Shock test	Constructional and mechanical endurance test applying the shock during transportation.	50G half sign wave 1l msedc 3 times of each direction	MIL-202E-213B
10	Atmospheric pressure test	Endurance test applying the atmospheric pressure during transportation by air.	115 mbar 40 hrs	MIL-202E-105C
Others				
11	Static electricity test	Endurance test applying the electric stress to the terminal.	VS=800V, RS=1.5 k CS=100 pF 1 time	MIL-883B-3015.1

*** Supply voltage for logic system = 3V. Supply voltage for LCD system = Operating voltage at 25°C.

Failure Judgement Criterion

Criterion Item	Test Item No.											Failure Judgment Criterion
	1	2	3	4	5	6	7	8	9	10	11	
Basic specification												Out of the Basic Specification
Electrical characteristic												Out of the DC and AC Characterstic
Mechanical characterstic												Out of the Mechanical Specification Color change : Out of Limit Apperance Specification
Optical characterstic												Out of the Apperance Standard

12. QUALITY GUARANTEE

Acceptable Quality Level

Each lot should satisfy the quality level defined as follows.

- Inspection method : MIL-STD-105E LEVEL II Normal one time sampling
- AQL

Partition	AQL	Definition
A: Major	0.4%	Functional defective as product
B: Minor	1.5%	Satisfy all functions as product but not satisfy cosmetic standard

Definition of 'LOT'

One lot means the delivery quantity to customer at one time.

Conditions of Cosmetic Inspection

Environmental condition

The inspection should be performed at the 1cm of height from the LCD module under 2 pieces of 40W white fluorescent lamps (Normal temperature 20~25℃and normal humidity 60±15%RH).

Inspection method

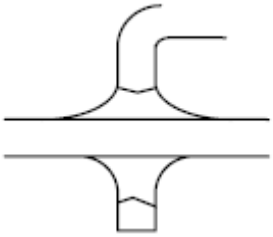
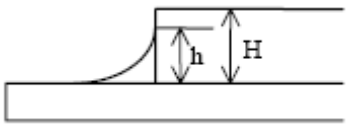
The visual check should be performed vertically at more than 30cm distance from the LCD panel.

Driving voltage

The VO value which the most optimal contrast can be obtained near the specified VO in the specification. (Within ±0.5V of typical value at 25℃.).

13. INSPECTION CRITERIA

13.1 Module Cosmetic Criteria

No.	Item	Judgement Criterion	Partition
1	Difference in Spec.	None allowed	Major
2	Pattern peeling	No substrate pattern peeling and floating	Major
3	Soldering defects	No soldering missing No soldering bridge No cold soldering	Major Major Major
4	Resist flaw on substrate	Invisible copper foil (′0.5mm or more) on substrate pattern	Minor
5	Accretion of metallic Foreign matter	No soldering dust No accretion of metallic foreign matters (Not exceed ′0.2mm)	Minor Minor
6	Stain	No stain to spoil cosmetic badly	Minor
7	Plate discoloring	No plate fading, rusting and discoloring	Minor
8	Solder amount 1. Lead parts	a. Soldering side of PCB Solder to form a ‘Filet’ all around the lead. Solder should not hide the lead form perfectly. (too much) b. Components side (In case of ‘Through Hole PCB’) Solder to reach the Components side of PCB. 	Minor
	2. Flat packages	Either ‘Toe’ (A) or ‘Seal’ (B) of the lead to be covered by ‘Filet’. Lead form to be assume over solder. A B 	Minor
	3. Chips	(3/2) H ≥h ≥(1/2) H 	Minor

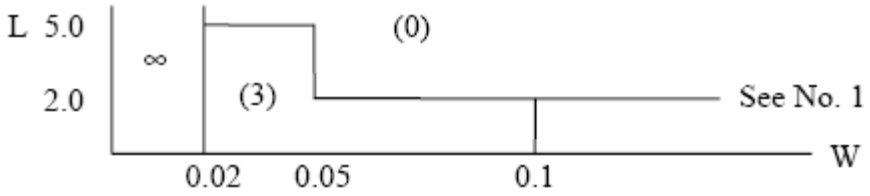
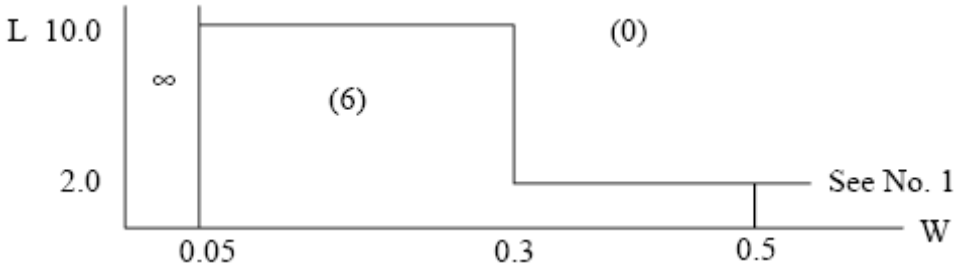
13.2 Screen Cosmetic Criteria (Non-Operating)

No.	Defect	Judgement Criterion	Partition

<table>
<tr><td>1</td><td>Spots</td><td>In accordance with Screen Cosmetic Criteria (Operating) No.1.</td><td>Minor</td></tr>
<tr><td>2</td><td>Lines</td><td>In accordance with Screen Cosmetic Criteria (Operating) No.2.</td><td>Minor</td></tr>
<tr><td>3</td><td>Bubbles in polarizer</td><td><table><tr><th>Size : d mm</th><th>Acceptable Qty in active area</th></tr><tr><td>d ≤ 0.3</td><td>Disregard</td></tr><tr><td>0.3 < d ≤ 1.0</td><td>3</td></tr><tr><td>1.0 < d ≤ 1.5</td><td>1</td></tr><tr><td>1.5 < d</td><td>0</td></tr></table></td><td>Minor</td></tr>
<tr><td>4</td><td>Scratch</td><td>In accordance with spots and lines operating cosmetic criteria. When the light reflects on the panel surface, the scratches are not to be remarkable.</td><td>Minor</td></tr>
<tr><td>5</td><td>Allowable density</td><td>Above defects should be separated more than 30mm each other.</td><td>Minor</td></tr>
<tr><td>6</td><td>Coloration</td><td>Not to be noticeable coloration in the viewing area of the LCD panels. Back-lit type should be judged with back-lit on state only.</td><td>Minor</td></tr>
<tr><td>7</td><td>Contamination</td><td>Not to be noticeable.</td><td>Minor</td></tr>
</table>

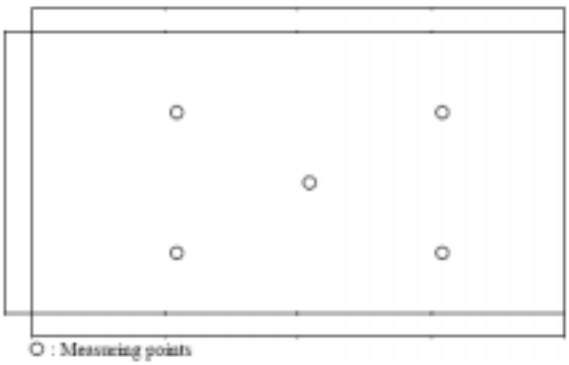
13.3. Screen Cosmetic Criteria (Operating)

<table>
<tr><th>No.</th><th>Defect</th><th>Judgement Criterion</th><th>Partition</th></tr>
<tr><td>1</td><td>Spots</td><td>A) Clear Note :
<table><tr><th>Size : d mm</th><th>Acceptable Qty in active area</th></tr><tr><td>d ≤ 0.1</td><td>Disregard</td></tr><tr><td>0.1 < d ≤ 0.2</td><td>3</td></tr><tr><td>0.2 < d ≤ 0.3</td><td>2</td></tr><tr><td>0.3 < d</td><td>0</td></tr></table>Including pin holes and defective dots which must be within one pixel size.
B) Unclear Size :
<table><tr><th>Size : d mm</th><th>Acceptable Qty in active area</th></tr><tr><td>d ≤ 0.2</td><td>Disregard</td></tr><tr><td>0.2 < d ≤ 0.5</td><td>6</td></tr><tr><td>0.5 < d ≤ 0.7</td><td>2</td></tr><tr><td>0.7 < d</td><td>0</td></tr></table></td><td>Minor</td></tr>
</table>

2	Lines	A)Clear  Note : ( ) - Acceptable Qty in active area L -Length (mm) W - Width (mm) ∞ - Disregard B) Unclear  	Minor

'Clear' = The shade and size are not changed by VO.
'Unclear' = The shade and size are changed by VO.

13.4. Screen Cosmetic Criteria (Operating) (Continued)

No.	Defect	Judgement Criterion	Partition
3	Rubbing line	Not to be noticeable.	
4	Allowable density	Above defects should be separated more than 10mm each other.	Minor
5	Rainbow	Not to be noticeable.	Minor
6	Dot size	To be 95% ~ 105% of the dot size (Typ.) in drawing. Partial defects of each dot (ex. pin-hole) should be treated as 'Spot'. (see *Screen Cosmetic Criteria (Operating) No.1*)	Minor
7	Uneven brightness (only back-lit type module)	Uneven brightness must be BMAX / BMIN ≤ 2 - BMAX : Max. value by measure in 5 points - BMIN : Min. value by measure in 5 points Divide active area into 4 vertically and horizontally. Measure 5 points shown in the following figure.  	Minor

Note :

(1) Size : d = (long length + short length) / 2

(2) The limit samples for each item have priority.

(3) Complexed defects are defined item by item, but if the number of defects are defined in above table, the total number should not exceed 10.

(4) In case of 'concentration', even the spots or the lines of 'disregarded' size should not allowed. Following three situations should be treated as 'concentration'.

- 7 or over defects in circle of ′5mm.
- 10 or over defects in circle of ′10mm.
- 20 or over defects in circle of ′20mm.

14. PRECAUTIONS FOR USING LCD MODULES

Handing Precautions

(1) The display panel is made of glass. Do not subject it to a mechanical shock by dropping it or impact.

(2) If the display panel is damaged and the liquid crystal substance leaks out, be sure not to get any in your mouth. If the substance contacts your skin or clothes, wash it off using soap and water.

(3) Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

(4) The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

(5) If the display surface becomes contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If it is heavily contaminated, moisten cloth with one of the following solvents :

- Isopropyl alcohol
- Ethyl alcohol

(6) Solvents other than those above-mentioned may damage the polarizer. Especially, do not use the following.

- Water
- Ketone
- Aromatic solvents

(7) Exercise care to minimize corrosion of the electrode. Corrosion of the electrodes is accelerated by water droplets, moisture condensation or a current flow in a high-humidity environment.

(8) Install the LCD Module by using the mounting holes. When mounting the LCD module make sure it is free of twisting, warping and distortion. In particular, do not forcibly pull or bend the I/O cable or the backlight cable.

(9) Do not attempt to disassemble or process the LCD module.

(10) NC terminal should be open. Do not connect anything.

(11) If the logic circuit power is off, do not apply the input signals.

(12) To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

- Be sure to ground the body when handling the LCD modules.
- Tools required for assembling, such as soldering irons, must be properly grounded.
- To reduce the amount of static electricity generated, do not conduct assembling and other work under dry conditions.

- The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

Storage Precautions

When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps. Keep the modules in bags (avoid high temperature˜ high humidity and low temperatures below 0□C). Whenever possible, the LCD modules should be stored in the same conditions in which they were shipped from our company.

Others

Liquid crystals solidify under low temperature (below the storage temperature range) leading to defective orientation or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subject to a low temperature.

If the LCD modules have been operating for a long time showing the same display patterns, the display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. A normal operating status can be regained by suspending use for some time. It should be noted that this phenomenon does not adversely affect performance reliability.

To minimize the performance degradation of the LCD modules resulting from destruction caused by static electricity etc., exercise care to avoid holding the following sections when handling the modules.

- Exposed area of the printed circuit board.
- Terminal electrode sections.

15. USING LCD MODULES

Liquid Crystal Display Modules

LCD is composed of glass and polarizer. Pay attention to the following items when handling.

(1) Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peel-off may occur with high temperature and high humidity.

(2) Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead (glass, tweezers, etc.).

(3) N-hexane is recommended for cleaning the adhesives used to attach front/rear polarizers and reflectors made of organic substances which will be damaged by chemicals such as acetone, toluene, ethanol and isopropylalcohol.

(4) When the display surface becomes dusty, wipe gently with absorbent cotton or other soft material like chamois soaked in petroleum benzin. Do not scrub hard to avoid damaging the display surface.

(5) Wipe off saliva or water drops immediately, contact with water over a long period of time may cause deformation or color fading.

(6) Avoid contacting oil and fats.

(7) Condensation on the surface and contact with terminals due to cold will damage, stain or dirty the polarizers. After products are tested at low temperature they must be warmed up in a container before coming is contacting with room temp erature air.

(8) Do not put or attach anything on the display area to avoid leaving marks on.

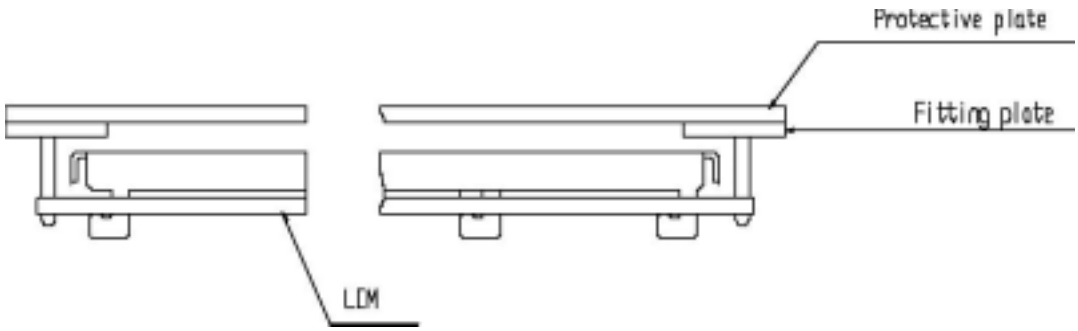
(9) Do not touch the display with bare hands. This will stain the display area and degradate insulation between terminals (some cosmetics are determinated to the polarizers).

(10) As glass is fragile. It tends to become or chipped during handling especially on the edges. Please avoid dropping or jarring.

Installing LCD Modules

The hole in the printed circuit board is used to fix LCM as shown in the picture below. Attend to the following items when installing the LCM.

(1) Cover the surface with a transparent protective plate to protect the polarizer and LC cell.



(2) When assembling the LCM into other equipment, the spacer to the bit between the LCM and the fitting plate should have enough height to avoid causing stress to the module surface, refer to the individual specifications for measurements. The measurement tolerance should be 0.1mm.

Precaution for Handing LCD Modules

Since LCM has been assembled and adjusted with a high degree of precision, avoid applying excessive shocks to the module or making any alterations or modifications to it.

(1) Do not alter, modify or change the the shape of the tab on the metal frame.

(2) Do not make extra holes on the printed circuit board, modify its shape or change the positions of components to be attached.

(3) Do not damage or modify the pattern writing on the printed circuit board.

(4) Absolutely do not modify the zebra rubber strip (conductive rubber) or heat seal connector.

(5) Except for soldering the interface, do not make any alterations or modifications with a soldering iron.

(6) Do not drop, bend or twist LCM.

Electro-Static Discharge Control

Since this module uses a CMOS LSI, the same careful attention should be paid to electrostatic discharge as for an ordinary CMOS IC.

(1) Make certain that you are grounded when handing LCM.

(2) Before remove LCM from its packing case or incorporating it into a set, be sure the module and your body have the same electric potential.

(3) When soldering the terminal of LCM, make certain the AC power source for the soldering iron does not leak.

(4) When using an electric screwdriver to attach LCM, the screwdriver should be of ground potentiality to minimize as much as possible any transmission of electromagnetic waves produced sparks coming from the commutator of the motor.

(5) As far as possible make the electric potential of your work clothes and that of the work bench the

ground potential.

(6) To reduce the generation of static electricity be careful that the air in the work is not too dried. A relative humidity of 50%60% is recommended.

Precaution for soldering to the LCM

(1) Observe the following when soldering lead wire, connector cable and etc. to the LCM.

- Soldering iron temperature : 280□C 10□C.
- Soldering time : 3-4 sec.
- Solder : eutectic solder.

If soldering flux is used, be sure to remove any remaining flux after finishing to soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended that you protect the LCD surface with a cover during soldering to prevent any damage dur to flux spatters.

(2) When soldering the electroluminescent panel and PC board, the panel and board should not be detached more than three times. This maximum number is determined by the temperature and time conditions mentioned above, though there may be some variance depending on the temperature of the soldering iron.

(3) When remove the electoluminescent panel from the PC board, be sure the solder has completely melted, the soldered pad on the PC board could be damaged.

Precautions for Operation

(1) Viewing angle varies with the change of liquid crystal driving voltage (VO). Adjust VO to show the best contrast.

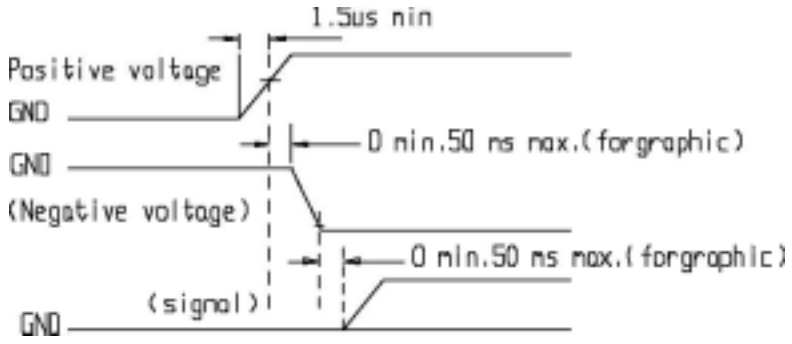
(2) Driving the LCD in the voltage above the limit shortens its life.

(3) Response time is greatly delayed at temperature below the operating temperature range. However, this does not mean the LCD will be out of the order. It will recover when it returns to the specified temperature range.

(4) If the display area is pushed hard during operation, the display will become abnormal. However, it will return to normal if it is turned off and then back on.

(5) Condensation on terminals can cause an electrochemical reaction disrupting the terminal circuit. Therefore, it must be used under the relative condition of 40□C , 50% RH.

(6) When turning the power on, input each signal after the positive/negative voltage becomes stable.



Storage

When storing LCDs as spares for some years, the following precaution are necessary.

(1) Store them in a sealed polyethylene bag. If properly sealed, there is no need for dessicant.

(2) Store them in a dark place. Do not expose to sunlight or fluorescent light, keep the temperature

between 0□C and 35□C.

(3) The polarizer surface should not come in contact with any other objects. (We advise you to store them in the container in which they were shipped.)

Safety

(1) It is recommended to crush damaged or unnecessary LCDs into pieces and wash them off with solvents such as acetone and ethanol, which should later be burned.

(2) If any liquid leakes out of a damaged glass cell and comes in contact with the hands, wash off thoroughly with soap and water.

Limited Warranty

Unless agreed between GOOD DISPLAY and customer, GOOD DISPLAY will replace or repair any of its LCD modules which are found to be functionally defective when inspected in accordance with GOOD DISPLAY LCD acceptance standards (copies available upon request) for a period of one year from date of shipments. Cosmetic/visual defects must be returned to GOOD DISPLAY within 90 days of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of GOOD DISPLAY limited to repair and/or replacement on the terms set forth above. GOOD DISPLAY will not be responsible for any subsequent or consequential events.

Return LCM under warranty

No warranty can be granted if the precautions stated above have been disregarded. The typical examples of violations are :

- Broken LCD glass.
- PCB eyelet's damaged or modified.
- PCB conductors damaged.
- Circuit modified in any way, including addition of components.
- PCB tampered with by grinding, engraving or painting varnish.
- soldering to or modifying the bezel in any manner.

Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects. Any connectors or cable installed by the customer must be removed completely without damaging the PCB eyelet's, conductors and terminals.