图形点阵液晶显示模块

LCM12864H

使用说明书

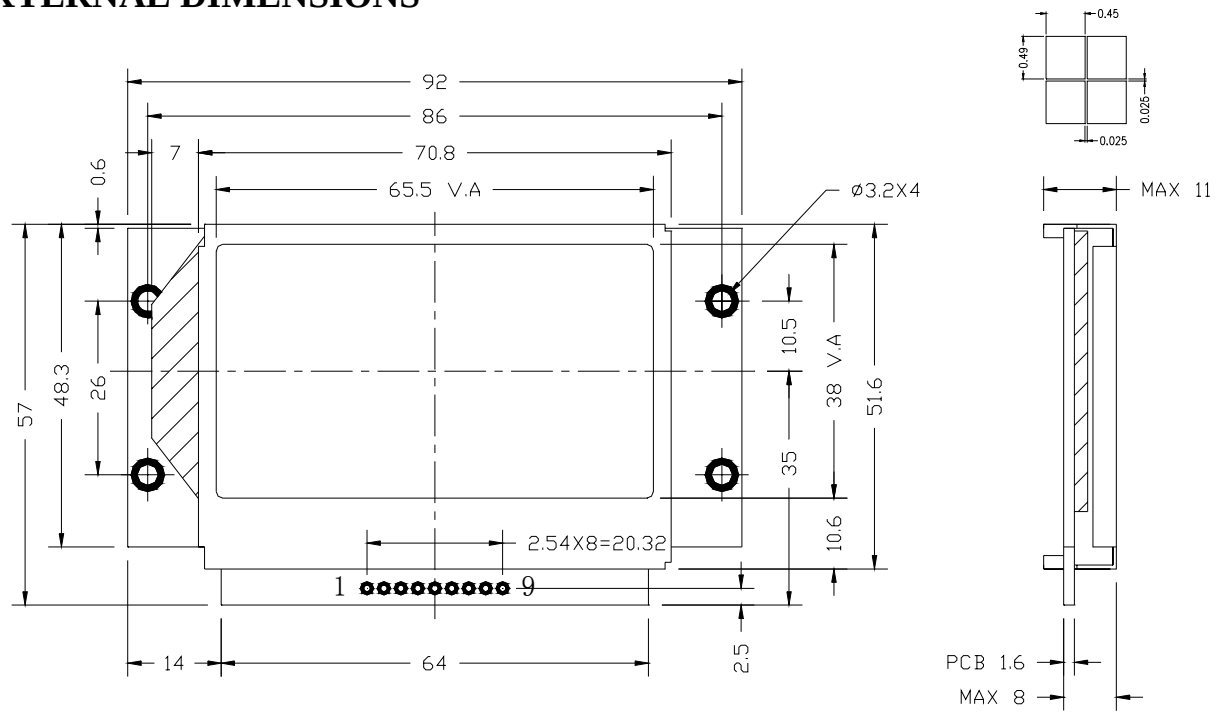
2005/11/03 Version: 1.0

北京青云创新科技发展有限公司
BEIJING QINGYUN HI-TECH DEVELOPMENT CO., LTD

■ PHYSICAL DATA

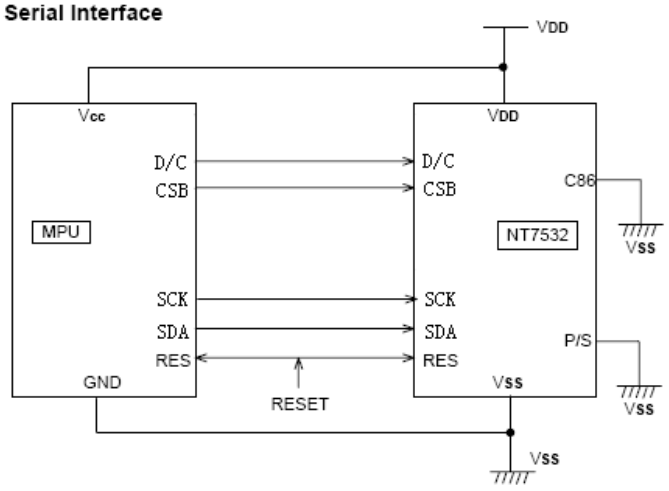
Item	Contents	Unit
显示方式	STN（黄绿）	---
LCD duty	1/64	---
LCD bias	1/9	---
视角	6:00	O'Clock
显示形式	128 X 64	dot
模块尺寸 (W×H×T)	92.0 × 57.0 × 11.0MAX	mm
视域 (W×H)	65.5 × 38	mm
显示图形域 (W×H)	60.755 × 32.935	mm
点尺寸 (W×H)	0.49 × 0.45	mm
点间距 (W×H)	0.025 × 0.025	mm
控制器	NT7532	---

■ EXTERNAL DIMENSIONS



■ BLOCK DIAGRAM

PIN NO.	1	2	3	4	5	6	7	8	9
SYMBOL	CSB	RESB	D/C	SCK	SDA	VCC	GND	LED-	LED+



■ INTERFACE PIN CONNECTIONS

Pin NO.	Symbol	I/O	Description
1	CSB	I	片选信号，低有效
2	RESB	I	复位信号，低有效
3	D/C	I	D/C为高，输入为数据；D/C为低，输入为指令
4	SCK	I/O	串行输入时脉冲信号
5	SDA	I/O	串行输入时数据信号
6	VCC		3.0V，电源正极；
7	GND		Ground，电源负极
8	LED-		背光负极
9	LED+		3.0V，15mA，背光正极

■ ABSOLUTE MAXIMUM RATINGS (Ta = 25℃)

Parameter	Symbol	Min	Max	Unit
Supply voltage for logic	VDD	2.4	3.5	V
Input voltage	VI	0	VDD	V
Operating temperature	TOP	-20	70	°C
Storage temperature	TST	-20	70	°C

■ ELECTRICAL CHARACTERISTICS (VDD = +3V±10% , VSS = 0V, Ta = 25°C)

▼ DC Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage for logic	VDD	---	2.4	3.0	3.5	V
Supply current for logic	IDD	---	---	0.2	0.4	mA
Supply voltage for side light	V_B	---	---	3.0	3.3	V
Supply current for side light	I_B	VF=3.0V	---	15	20	mA
Input voltage ' H ' level	VIH	---	0.8VDD	---	VDD	V
Input voltage ' L ' level	VIL	---	0	---	0.2VDD	V

▼ AC Characteristics

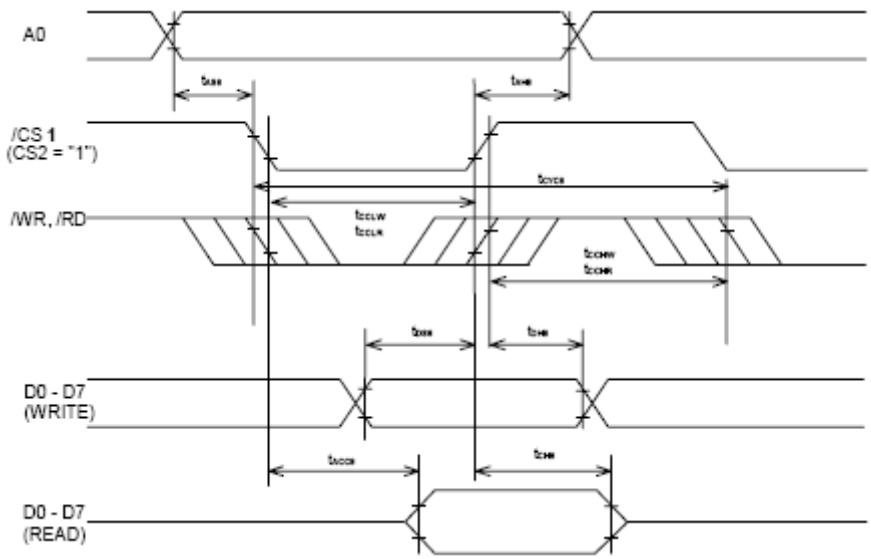
System buses Read / Write characteristics 1 (For the 8080 Series MPU)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{AH8}	Address hold time	0			ns	
t_{AS8}	Address setup time	0			ns	
t_{CYC8}	System cycle time	300			ns	
t_{CCLW}	Control L pulse width (/WR)	90			ns	
t_{CCLR}	Control L pulse width (/RD)	120			ns	
t_{CCHW}	Control H pulse width (/WR)	120			ns	
t_{CCHR}	Control H pulse width (/RD)	60			ns	
t_{DS8}	Data setup time	40			ns	
t_{DH8}	Data hold time	15			ns	
t_{ACC8}	/RD access time			140	ns	C_L = 100pF
t_{CH8}	Output disable time	10		100	ns	C_L = 100pF

*1. The input signal rise time and fall time (tr, tf) is specified at 15ns or less. When the system cycle time is extremely fast, $(t_r+t_f) \le (t_{CYC8}-t_{CCLW}-t_{CCHW})$ for $(t_r+t_f) \le (t_{CYC8}-t_{CCLR}-t_{CCHR})$ are specified.

*2. All timing is specified using 20% and 80% of V_{DD} as the reference.

*3. t_{CCLW} and t_{CCLR} are specified as the overlap between CS1 being "L" (CS2 = "H") and /WR and /RD being at the "L" level.



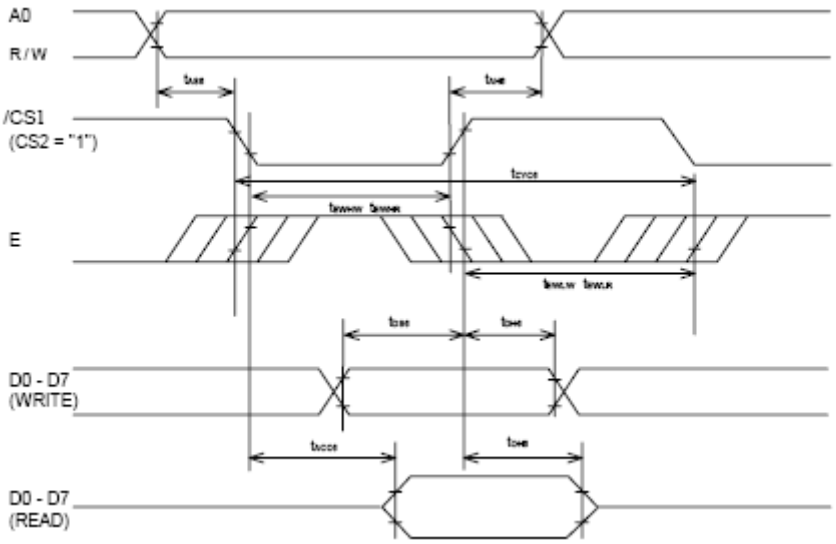
System buses Read/Write Characteristics 2 (6800 Series MPU)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tCYC6	System cycle time	300			ns	
tAS6	Address setup time	0			ns	
tAH6	Address hold time	0			ns	
tDS6	Data setup time	40			ns	
tDH6	Data hold time	15			ns	
tOH6	Output disable time	10		100	ns	C_L = 100pF
tACC6	Access time			140	ns	C_L = 100pF
tEWHR	Enable H pulse width (Read)	120			ns	
tEWHW	Enable H pulse width (Write)	90			ns	
tEWLR	Enable L pulse width (Read)	60			ns	
tEWLW	Enable L pulse width (Write)	120			ns	

*1. The input signal rise time and fall time (tr, tf) is specified at 15ns or less. When the system cycle time is extremely fast, $(t_r+t_f) \le (t_{CYC6}-t_{EWLW}-t_{EWHW})$ for $(t_r+t_f) \le (t_{CYC6}-t_{EWLR}-t_{EWHR})$ are specified.

*2. All timing is specified using 20% and 80% of V_{DD} as the reference.

*3. t_{EWLW} and t_{EWLR} are specified as the overlap between /CS1 being "L" (CS2 = "H") and E.



■ FUNCTION DESCRIPTION

Microprocessor Interface

Interface type selection

The NT7532 can transfer data via 8-bit bi-directional data bus (D7 to D0) or via serial data input (SI). When high or low is selected for the parity of P/S pad either 8-bit parallel data input or serial data input can be selected as shown in Table 1. When serial data input is selected, the RAM data cannot be read out.

Table. 1

P/S	Type	/CS1	CS2	A0	/RD	/WR	C86	D7	D6	D0 to D5
H	Parallel Input	/CS1	CS2	A0	/RD	/WR	C86	D7	D6	D0 to D5
L	Serial Input	/CS1	CS2	A0	-	-	-	SI	SCL	(HZ)

"-" Must always be high or low

Parallel Input

When the NT7532 selects parallel input (P/S = high), the 8080 series microprocessor or 6800 series microprocessor can be selected by causing the C86 pad to go high or low as shown in Table 2.

Table. 2

C86	Type	/CS1	CS2	A0	/RD	/WR	D0 to D7
H	6800 microprocessor bus	/CS1	CS2	A0	E	R//W	D0 to D7
L	8080 microprocessor bus	/CS1	CS2	A0	/RD	/WR	D0 to D7

Data Bus Signals

The NT7532 identifies the data bus signal according to A0, E, R/W(/RD, /WR) signals.

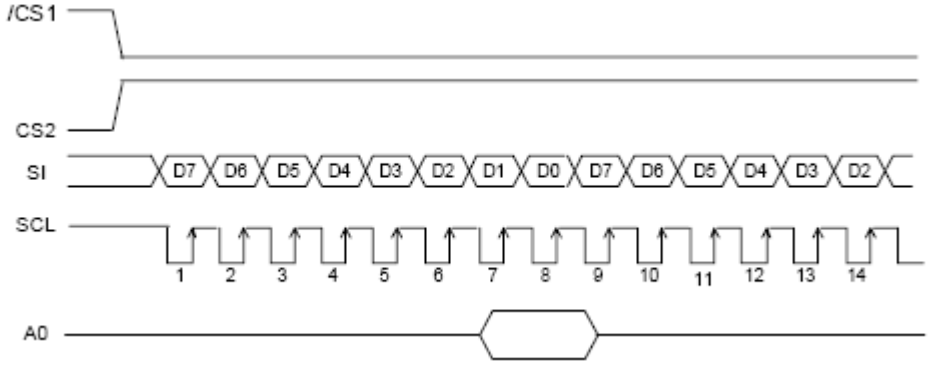
Table. 3

Common	6800 processor	8080 processor		Function
A0	(R/W)	/RD	/WR	
1	1	0	1	Reads display data
1	0	1	0	Writes display data
0	1	0	1	Reads status
0	0	1	0	Writes control data in the internal register. (Command)

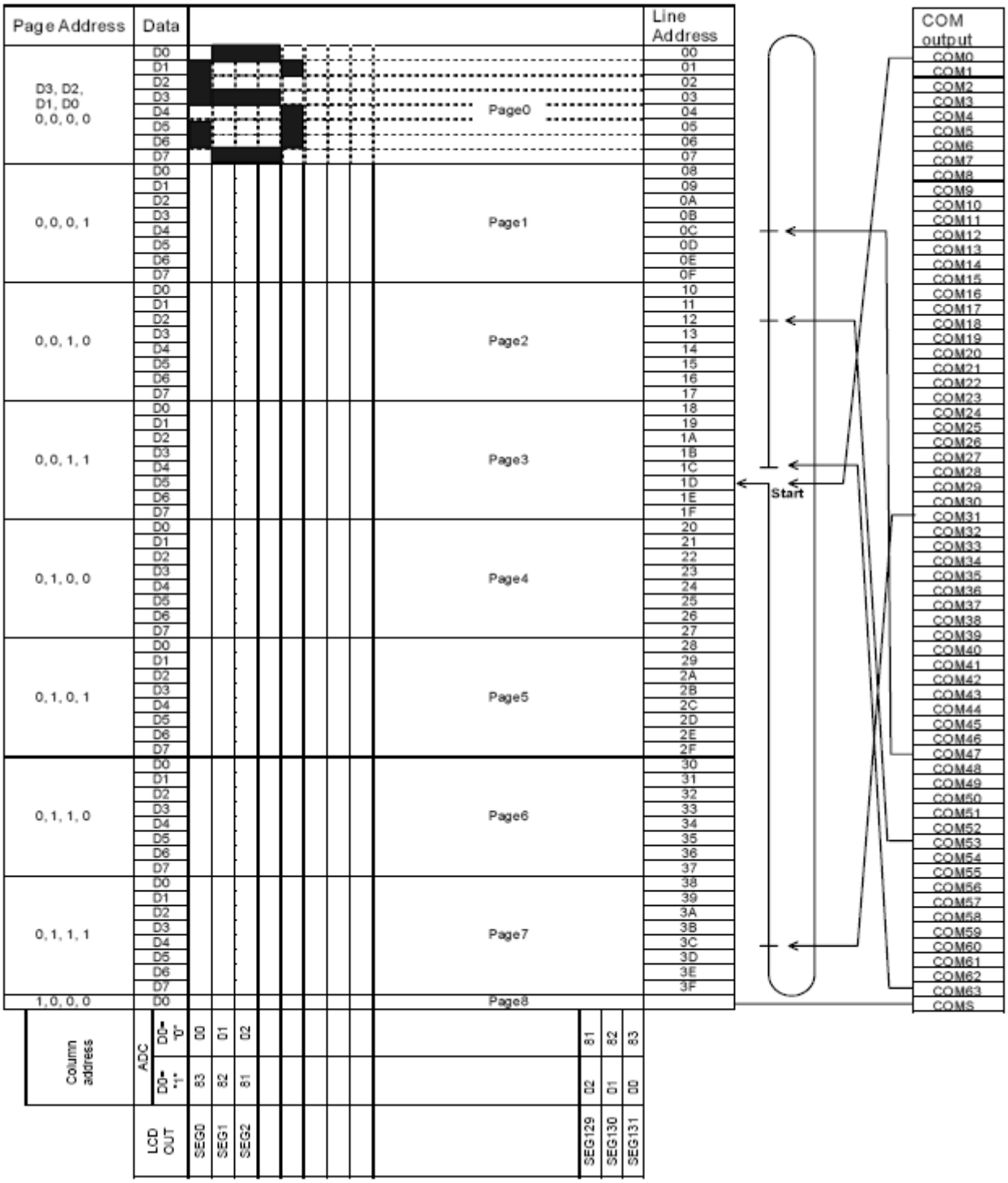
Serial Interface (P/S is low)

When the serial interface has been selected (P/S = "L"), then when the chip is in an active state (/CS1= "L" and CS2 = "H"), the serial data input (SI) and the serial clock input (SCL) can be received. The serial data is read from the serial data input pin in the rising edge of the serial clocks D7, D6 through D0, in this order. This data is converted to 8 bits of parallel data in the rising edge of the eighth serial clock for processing.

The A0 input is used to determine whether or not the serial data input is displaying data, and when A0 = "L" then the data is command data. The A0 input is read and used for detection every 8th rising edge of the serial clock after the chip becomes active.



■ DISPLAY DATA RAM ADDRESS MAP



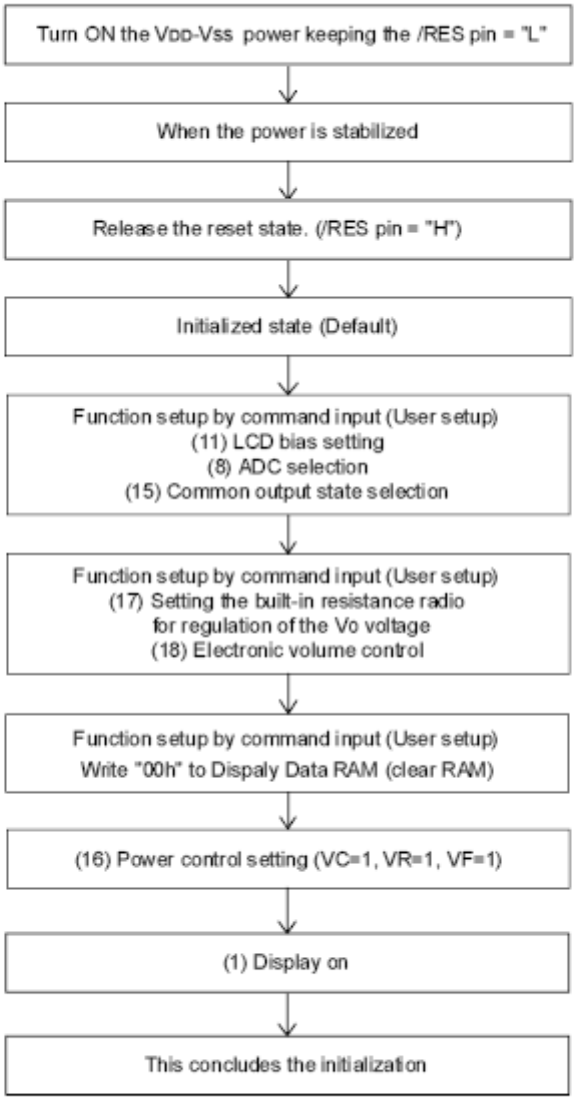
■ OPERATING PRINCIPLES & METHODS

▼ Control and Display Command

Command	Code											Function
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display on/off	0	1	0	1	0	1	0	1	1	1	D	Turns on the LCD panel when high, and turns it off when low
(2) Set display start line	0	1	0	0	1	Display start address						Specifies RAM display line for COM0
(3) Set page address	0	1	0	1	0	1	1	Page address				Sets the display RAM page in Page Address register
(4-1) Set column address 4 higher bits	0	1	0	0	0	0	1	Higher column address				Sets 4 higher bits of column address of display RAM in register
(4-2) Set column address 4 lower bits	0	1	0	0	0	0	0	Lower column address				Sets 4 lower bits of column address of display RAM in register
(5) Read status	0	0	1	Status				0	0	0	0	Reads the status information
(6) Write display data	1	1	0	Write data								Writes data in display RAM
(7) Read display data	1	0	1	Read data								Reads data from display RAM
(8) ADC select	0	1	0	1	0	1	0	0	0	0	D	Sets the display RAM address SEG output correspondence
(9) Normal/Reverse display	0	1	0	1	0	1	0	0	1	1	D	Normal indication when low, but full indication when high
(10) Entire display on/off	0	1	0	1	0	1	0	0	1	0	0 1	Selects normal display (0) or Entire Display ON (1)
(11) Set LCD bias	0	1	0	1	0	1	0	0	0	1	D	Sets LCD drive voltage bias ratio
(12) Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Increments Column Address counter during each write
(13) End	0	1	0	1	1	1	0	1	1	1	0	Releases the Read-Modify-Write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Resets internal functions
(15) Common output mode select	0	1	0	1	1	0	0	D	*	*	*	Selects COM output scan direction. * Invalid data
(16) Set power control	0	1	0	0	0	1	0	1	Operation status			Selects the power circuit operation mode
(17) V0 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio (Rb / Ra) mode
(18) Electronic volume mode set	0	1	0	1	0	0	0	0	0	0	1	Sets the V0 output voltage electronic volume register
Electronic Volume Register set	0	1	0	*	*	Electronic control value						
(19) Set static indicator On/Off	0	1	0	1	0	1	0	1	1	0	D	Sets static indicator On/Off 0: OFF 1: ON
Set Static indicator register	0	1	0	*	*	*	*	*	*	Mode		Sets the flashing mode
(20) Power save	-	-	-	-	-	-	-	-	-	-	-	Compound command of display OFF and entire display ON
(21) NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(22) Test Command	0	1	0	1	1	1	1	*	*	*	*	IC Test command. Do not use!
(23)Test Mode Reset	0	1	0	1	1	1	1	0	0	0	0	Command of test mode reset

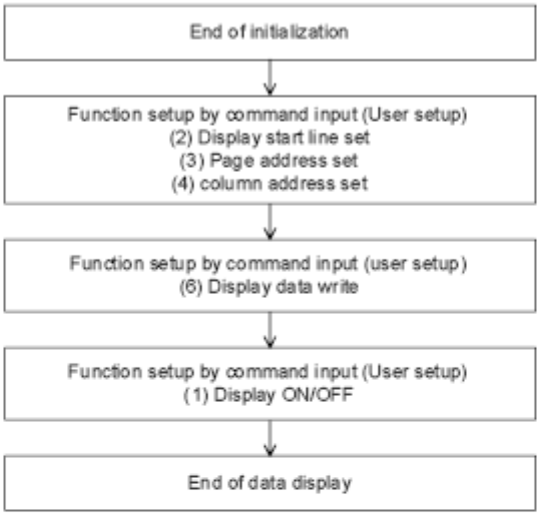
Initialization

Initialization

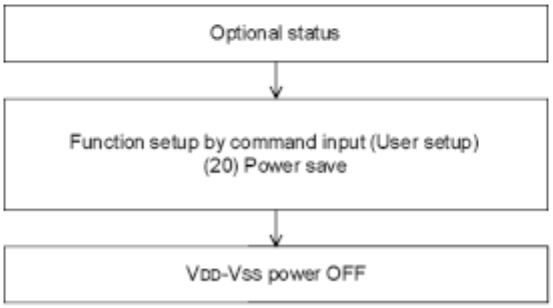


The time of initialization will vary depending on the panel characteristics and capacitance of the smoothing capacitor. Therefore, we suggest you to conduct an operation check using the actual equipment.

Data Display



Power OFF



The target time will vary depending on the panel characteristics and capacitance of the smoothing capacitor. Therefore, we suggest you conduct an operation check using the actual equipment.

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