



July 1996  
 Revised May 2005

# 74ABT16541 16-Bit Buffer/Line Driver with 3-STATE Outputs

## General Description

The ABT16541 contains sixteen non-inverting buffers with 3-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is byte controlled. Individual 3-STATE control inputs can be shorted together for 8-bit or 16-bit operation.

## Features

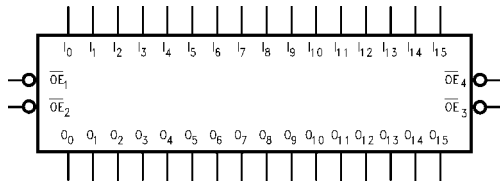
- Separate control logic for each nibble
- 16-bit version of the ABT541
- Outputs sink capability of 64 mA, source capability of 32 mA
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability

## Ordering Code:

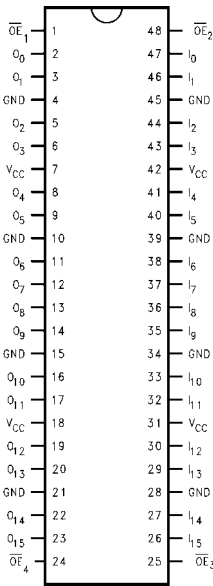
| Order Number   | Package Number | Package Description                                                         |
|----------------|----------------|-----------------------------------------------------------------------------|
| 74ABT16541CSSC | MS48A          | 48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide      |
| 74ABT16541CMTD | MTD48          | 48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide |

Device also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## Logic Symbol



## Connection Diagram



## Pin Descriptions

| Pin Names         | Description                       |
|-------------------|-----------------------------------|
| $\overline{OE}_n$ | Output Enable Inputs (Active Low) |
| $I_0$ – $I_{15}$  | Inputs                            |
| $O_0$ – $O_{15}$  | Outputs                           |

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## Truth Tables

| Inputs            |                   |           | Outputs   |
|-------------------|-------------------|-----------|-----------|
| $\overline{OE}_1$ | $\overline{OE}_2$ | $I_0-I_7$ | $O_0-O_7$ |
| L                 | L                 | L         | L         |
| L                 | L                 | H         | H         |
| H                 | X                 | X         | Z         |
| X                 | H                 | X         | Z         |

| Inputs            |                   |              | Outputs      |
|-------------------|-------------------|--------------|--------------|
| $\overline{OE}_4$ | $\overline{OE}_3$ | $I_8-I_{15}$ | $O_8-O_{15}$ |
| L                 | L                 | L            | L            |
| L                 | L                 | H            | H            |
| H                 | X                 | X            | Z            |
| X                 | H                 | X            | Z            |

H = HIGH Voltage Level

L = LOW Voltage Level

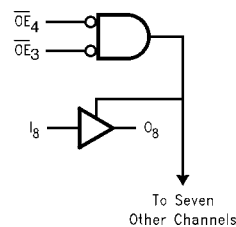
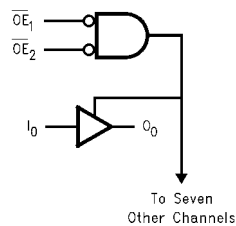
X = Immaterial

Z = High Impedance

## Functional Description

The ABT16541 contains sixteen non-inverting buffers with 3-STATE outputs. The device is byte (8 bits) controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation.

## Logic Diagrams



**Absolute Maximum Ratings**(Note 1)

|                                                                        |                                      |
|------------------------------------------------------------------------|--------------------------------------|
| Storage Temperature                                                    | –65°C to +150°C                      |
| Ambient Temperature under Bias                                         | –55°C to +125°C                      |
| Junction Temperature under Bias                                        | –55°C to +150°C                      |
| V <sub>CC</sub> Pin Potential to Ground Pin                            | –0.5V to +7.0V                       |
| Input Voltage (Note 2)                                                 | –0.5V to +7.0V                       |
| Input Current (Note 2)                                                 | –30 mA to +5.0 mA                    |
| Voltage Applied to Any Output<br>in the Disabled or<br>Power-Off State | –0.5V to 5.5V                        |
| in the HIGH State                                                      | –0.5V to V <sub>CC</sub>             |
| Current Applied to Output<br>in LOW State (Max)                        | twice the rated I <sub>OL</sub> (mA) |
| DC Latchup Source Current                                              | –500 mA                              |
| Over Voltage Latchup (I/O)                                             | 10V                                  |

**Recommended Operating Conditions**

|                                                 |                |
|-------------------------------------------------|----------------|
| Free Air Ambient Temperature                    | –40°C to +85°C |
| Supply Voltage                                  | +4.5V to +5.5V |
| Minimum Input Edge Rate ( $\Delta V/\Delta t$ ) |                |
| Data Input                                      | 50 mV/ns       |
| Enable Input                                    | 20 mV/ns       |

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

| Symbol           | Parameter                                    | Min  | Typ  | Max  | Units      | V <sub>CC</sub> | Conditions                                                                   |
|------------------|----------------------------------------------|------|------|------|------------|-----------------|------------------------------------------------------------------------------|
| V <sub>IH</sub>  | Input HIGH Voltage                           | 2.0  |      |      | V          |                 | Recognized HIGH Signal                                                       |
| V <sub>IL</sub>  | Input LOW Voltage                            |      |      | 0.8  | V          |                 | Recognized LOW Signal                                                        |
| V <sub>CD</sub>  | Input Clamp Diode Voltage                    |      |      | –1.2 | V          | Min             | I <sub>IN</sub> = –18 mA                                                     |
| V <sub>OH</sub>  | Output HIGH Voltage                          | 2.5  |      |      | V          | Min             | I <sub>OH</sub> = –3 mA                                                      |
|                  |                                              | 2.0  |      |      | V          | Min             | I <sub>OH</sub> = –32 mA                                                     |
| V <sub>OL</sub>  | Output LOW Voltage                           |      |      | 0.55 | V          | Min             | I <sub>OL</sub> = 64 mA                                                      |
| I <sub>IH</sub>  | Input HIGH Current                           |      |      | 1    | μA         | Max             | V <sub>IN</sub> = 2.7V (Note 3)                                              |
|                  |                                              |      |      | 1    | μA         | Max             | V <sub>IN</sub> = V <sub>CC</sub>                                            |
| I <sub>BVI</sub> | Input HIGH Current Breakdown Test            |      |      | 7    | μA         | Max             | V <sub>IN</sub> = 7.0V                                                       |
| I <sub>IL</sub>  | Input LOW Current                            |      |      | –1   | μA         | Max             | V <sub>IN</sub> = 0.5V (Note 3)                                              |
|                  |                                              |      |      | –1   | μA         | Max             | V <sub>IN</sub> = 0.0V                                                       |
| V <sub>ID</sub>  | Input Leakage Test                           | 4.75 |      |      | V          | 0.0             | I <sub>ID</sub> = 1.9 μA<br>All Other Pins Grounded                          |
| I <sub>OZH</sub> | Output Leakage Current                       |      |      | 10   | μA         | 0–5.5V          | V <sub>OUT</sub> = 2.7V; $\overline{OE}_n$ = 2.0V                            |
| I <sub>OZL</sub> | Output Leakage Current                       |      |      | –10  | μA         | 0–5.5V          | V <sub>OUT</sub> = 0.5V; $\overline{OE}_n$ = 2.0V                            |
| I <sub>OS</sub>  | Output Short-Circuit Current                 | –100 |      | –275 | mA         | Max             | V <sub>OUT</sub> = 0.0V                                                      |
| I <sub>CEX</sub> | Output HIGH Leakage Current                  |      |      | 50   | μA         | Max             | V <sub>OUT</sub> = V <sub>CC</sub>                                           |
| I <sub>ZZ</sub>  | Bus Drainage Test                            |      |      | 100  | μA         | 0.0             | V <sub>OUT</sub> = 5.5V<br>All Other Pins GND                                |
| I <sub>CCH</sub> | Power Supply Current                         |      |      | 100  | μA         | Max             | All Outputs HIGH                                                             |
| I <sub>CCL</sub> | Power Supply Current                         |      |      | 60   | mA         | Max             | All Outputs LOW                                                              |
| I <sub>CCZ</sub> | Power Supply Current                         |      |      | 100  | μA         | Max             | $\overline{OE}_n$ = V <sub>CC</sub><br>All Others at V <sub>CC</sub> or GND  |
| I <sub>CCT</sub> | Additional I <sub>CC</sub> /Input            |      |      | 2.5  | mA         |                 | V <sub>I</sub> = V <sub>CC</sub> – 2.1V                                      |
|                  | Outputs Enabled                              |      |      | 2.5  | mA         | Max             | Enable Input V <sub>I</sub> = V <sub>CC</sub> – 2.1V                         |
|                  | Outputs 3-STATE                              |      |      | 50   | μA         |                 | Data Input V <sub>I</sub> = V <sub>CC</sub> – 2.1V                           |
|                  | Outputs 3-STATE                              |      |      |      |            |                 | All Others at V <sub>CC</sub> or GND                                         |
| I <sub>CCD</sub> | Dynamic I <sub>CC</sub> (Note 3)             |      |      | 0.1  | mA/<br>MHz | Max             | Outputs Open, $\overline{OE}_n$ = GND<br>One Bit Toggling,<br>50% Duty Cycle |
| V <sub>OLP</sub> | Quiet Output Maximum Dynamic V <sub>OL</sub> |      | 0.4  | 0.7  | V          | 5.0             | T <sub>A</sub> = 25°C (Note 4)                                               |
| V <sub>OLV</sub> | Quiet Output Minimum Dynamic V <sub>OL</sub> | –1.3 | –1.0 |      | V          | 5.0             | T <sub>A</sub> = 25°C (Note 4)                                               |
| V <sub>OHV</sub> | Minimum HIGH Level Dynamic Output Voltage    | 2.7  | 3.0  |      | V          | 5.0             | T <sub>A</sub> = 25°C (Note 6)                                               |
| V <sub>IHD</sub> | Minimum HIGH Level Dynamic Input Voltage     | 2.0  | 1.4  |      | V          | 5.0             | T <sub>A</sub> = 25°C (Note 5)                                               |

## DC Electrical Characteristics (Continued)

| Symbol           | Parameter                               | Min | Typ | Max | Units | V <sub>CC</sub> | Conditions                     |
|------------------|-----------------------------------------|-----|-----|-----|-------|-----------------|--------------------------------|
| V <sub>ILD</sub> | Maximum LOW Level Dynamic Input Voltage |     | 1.2 | 0.8 | V     | 5.0             | T <sub>A</sub> = 25°C (Note 5) |

**Note 3:** Guaranteed but not tested.

**Note 4:** Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

**Note 5:** Max number of data inputs (n) switching. n-1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>). Guaranteed, but not tested.

**Note 6:** Max number of outputs defined as (n). n - 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

## AC Electrical Characteristics

| Symbol           | Parameter             | T <sub>A</sub> = +25°C<br>V <sub>CC</sub> = +5V<br>C <sub>L</sub> = 50 pF |     |     | T <sub>A</sub> = -40°C to +85°C<br>V <sub>CC</sub> = 4.5V–5.5V<br>C <sub>L</sub> = 50 pF |     | Units |
|------------------|-----------------------|---------------------------------------------------------------------------|-----|-----|------------------------------------------------------------------------------------------|-----|-------|
|                  |                       | Min                                                                       | Typ | Max | Min                                                                                      | Max |       |
| t <sub>PLH</sub> | Propagation           | 1.0                                                                       | 2.3 | 3.4 | 1.0                                                                                      | 3.4 | ns    |
| t <sub>PHL</sub> | Delay Data to Outputs | 1.0                                                                       | 2.7 | 3.9 | 1.0                                                                                      | 3.9 |       |
| t <sub>PZH</sub> | Output Enable         | 1.5                                                                       | 3.5 | 5.2 | 1.5                                                                                      | 5.2 | ns    |
| t <sub>PZL</sub> | Time                  | 1.5                                                                       | 3.5 | 6.0 | 1.5                                                                                      | 6.0 |       |
| t <sub>PHZ</sub> | Output Disable        | 1.0                                                                       | 4.2 | 5.1 | 1.0                                                                                      | 5.1 | ns    |
| t <sub>PLZ</sub> | Time                  | 1.0                                                                       | 3.2 | 5.1 | 1.0                                                                                      | 5.1 |       |

## Extended AC Electrical Characteristics

| Symbol              | Parameter                | -40°C to +85°C<br>V <sub>CC</sub> = 4.5V–5.5V<br>C <sub>L</sub> = 50 pF<br>16 Outputs Switching<br>(Note 7) |     |     | T <sub>A</sub> = -40°C to +85°C<br>V <sub>CC</sub> = 4.5V–5.5V<br>C <sub>L</sub> = 250 pF<br>1 Output Switching<br>(Note 8) |     | T <sub>A</sub> = -40°C to +85°C<br>V <sub>CC</sub> = 4.5V–5.5V<br>C <sub>L</sub> = 250 pF<br>16 Outputs Switching<br>(Note 9) |     | Units |
|---------------------|--------------------------|-------------------------------------------------------------------------------------------------------------|-----|-----|-----------------------------------------------------------------------------------------------------------------------------|-----|-------------------------------------------------------------------------------------------------------------------------------|-----|-------|
|                     |                          | Min                                                                                                         | Typ | Max | Min                                                                                                                         | Max | Min                                                                                                                           | Max |       |
|                     |                          |                                                                                                             |     |     |                                                                                                                             |     |                                                                                                                               |     |       |
| f <sub>TOGGLE</sub> | Maximum Toggle Frequency | 100                                                                                                         |     |     |                                                                                                                             |     |                                                                                                                               |     | MHz   |
| t <sub>PLH</sub>    | Propagation Delay        | 1.5                                                                                                         |     | 5.0 | 1.5                                                                                                                         | 6.0 | 2.5                                                                                                                           | 8.0 | ns    |
| t <sub>PHL</sub>    | Data to Outputs          | 1.5                                                                                                         |     | 5.3 | 1.5                                                                                                                         | 6.0 | 2.5                                                                                                                           | 8.0 |       |
| t <sub>PZH</sub>    | Output Enable            | 1.5                                                                                                         |     | 6.5 | 2.5                                                                                                                         | 7.8 | 2.5                                                                                                                           | 9.5 | ns    |
| t <sub>PZL</sub>    | Time                     | 1.5                                                                                                         |     | 6.5 | 2.5                                                                                                                         | 7.8 | 2.5                                                                                                                           | 8.5 |       |
| t <sub>PHZ</sub>    | Output Disable           | 1.0                                                                                                         |     | 6.7 | (Note 10)                                                                                                                   |     | (Note 10)                                                                                                                     |     | ns    |
| t <sub>PLZ</sub>    | Time                     | 1.0                                                                                                         |     | 6.7 |                                                                                                                             |     |                                                                                                                               |     |       |

**Note 7:** This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

**Note 8:** This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

**Note 9:** This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

**Note 10:** The 3-STATE delay times are dominated by the RC network (500Ω, 250 pF) on the output and have been excluded from the datasheet.

## Skew

| Symbol                  | Parameter                                  | $T_A = -40^\circ\text{C to }+85^\circ\text{C}$<br>$V_{CC} = 4.5\text{V} - 5.5\text{V}$<br>$C_L = 50\text{ pF}$<br>16 Outputs Switching<br>(Note 11) | $T_A = -40^\circ\text{C to }+85^\circ\text{C}$<br>$V_{CC} = 4.5\text{V} - 5.5\text{V}$<br>$C_L = 250\text{ pF}$<br>16 Outputs Switching<br>(Note 12) | Units |
|-------------------------|--------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
|                         |                                            | Max                                                                                                                                                 | Max                                                                                                                                                  |       |
| $t_{OSHL}$<br>(Note 13) | Pin to Pin Skew<br>HL Transitions          | 1.0                                                                                                                                                 | 1.5                                                                                                                                                  | ns    |
| $t_{OSLH}$<br>(Note 13) | Pin to Pin Skew<br>LH Transitions          | 1.0                                                                                                                                                 | 1.5                                                                                                                                                  | ns    |
| $t_{PS}$<br>(Note 14)   | Duty Cycle<br>LH-HL Skew                   | 1.5                                                                                                                                                 | 1.5                                                                                                                                                  | ns    |
| $t_{OST}$<br>(Note 13)  | Pin to Pin Skew<br>LH/HL Transitions       | 1.7                                                                                                                                                 | 2.0                                                                                                                                                  | ns    |
| $t_{PV}$<br>(Note 15)   | Device to Device Skew<br>LH/HL Transitions | 2.0                                                                                                                                                 | 2.5                                                                                                                                                  | ns    |

**Note 11:** This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.)

**Note 12:** These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

**Note 13:** Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW ( $t_{OSHL}$ ), LOW-to-HIGH ( $t_{OSLH}$ ), or any combination switching LOW-to-HIGH and/or HIGH-to-LOW ( $t_{OST}$ ). The specification is guaranteed but not tested.

**Note 14:** This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

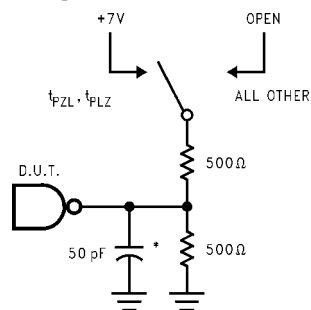
**Note 15:** Propagation delay variation for a given set of conditions (i.e., temperature and  $V_{CC}$ ) from device to device. This specification is guaranteed but not tested.

## Capacitance

| Symbol              | Parameter          | Typ | Units | Conditions<br>$T_A = 25^\circ\text{C}$ |
|---------------------|--------------------|-----|-------|----------------------------------------|
| $C_{IN}$            | Input Capacitance  | 5.0 | pF    | $V_{CC} = 5.0\text{V}$                 |
| $C_{OUT}$ (Note 16) | Output Capacitance | 9.0 | pF    | $V_{CC} = 5.0\text{V}$                 |

**Note 16:**  $C_{OUT}$  is measured at frequency  $f = 1\text{ MHz}$ ; per MIL STD-883, Method 3012.

## AC Loading



\* Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

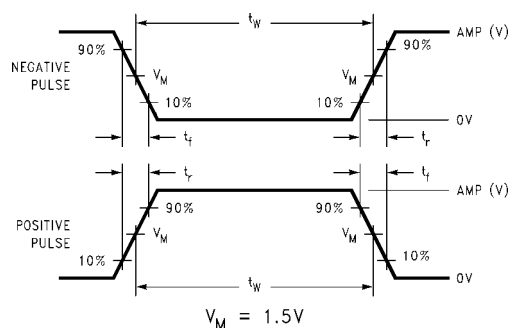


FIGURE 2. Test Input Pulse Requirements

| Amplitude | Rep Rate | $t_W$  | $t_r$  | $t_f$  |
|-----------|----------|--------|--------|--------|
| 3.0V      | 1 MHz    | 500 ns | 2.5 ns | 2.5 ns |

FIGURE 3. Test Input Signal Requirements

## AC Waveforms

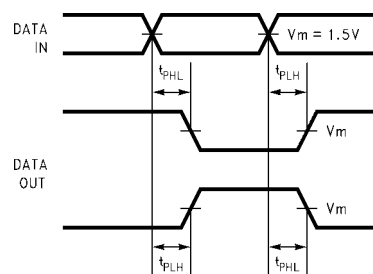


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

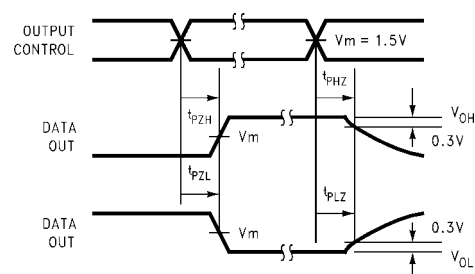


FIGURE 6. 3-STATE Output HIGH and LOW Enable and Disable Times

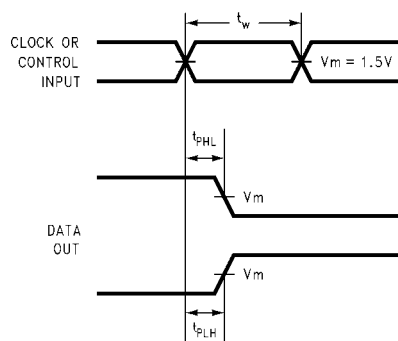


FIGURE 5. Propagation Delay, Pulse Width Waveforms

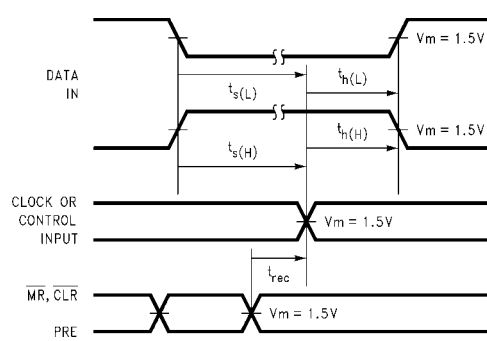
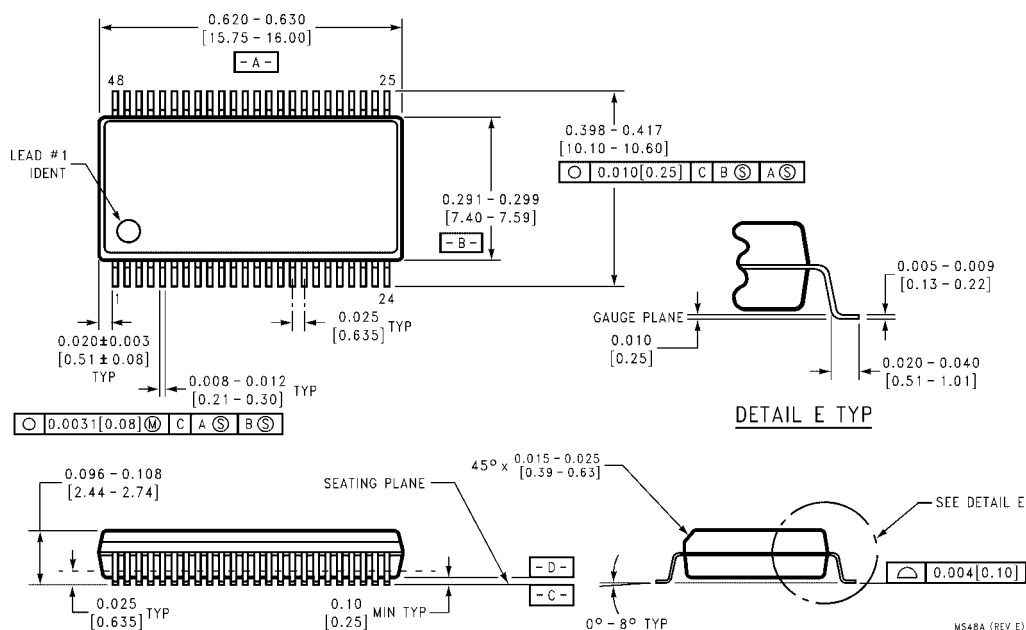


FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

**Physical Dimensions** inches (millimeters) unless otherwise noted



**48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide  
Package Number MS48A**



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