

ADS1259-Q1 汽车用, 14.4kSPS, 24 位模数转换器 具有集成低漂移基准

1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 的下列结果:
 - 温度等级: -40°C 至 125°C
 - 人体模型 (HBM) 静电放电 (ESD) 分类等级 2
 - 充电器件模型 (CDM) ESD 分类等级 C4B
- 可编程数据速率: 10SPS 至 14.4kSPS
- 单周期稳定数字滤波器
- 高性能:
 - 1.2kSPS 时的有效位数 (ENOB) 为 21.3
 - 积分非线性 (INL): 3ppm
 - 偏移漂移: $0.05\mu\text{V}/^{\circ}\text{C}$
 - 增益漂移: $0.5\text{ppm}/^{\circ}\text{C}$
- 内部基准: 2.5V, 漂移 $10\text{ppm}/^{\circ}\text{C}$
- 内部 2% 精准振荡器
- 输入信号超范围检测
- 可选校验和与冗余数据读取功能以增加数据完整性
- SPI™- 兼容接口, 模式 1
- 模拟电源: 5V 或者 $\pm 2.5\text{V}$
- 数字电源: 2.7V 至 5V

2 应用范围

- 汽车传动
- 电动汽车

3 说明

ADS1259-Q1 是一款精密, 低漂移, 24 位模数转换器 (ADC)。此器件可在数据速率高达 14.4kSPS 时执行高分辨率转换, 并因此非常适合于测量宽动态范围内快速变化的信号。一个集成的低噪声, 低漂移 2.5V 基准免除了对于外部电压基准的需要, 从而减少了系统成本和组件数量。

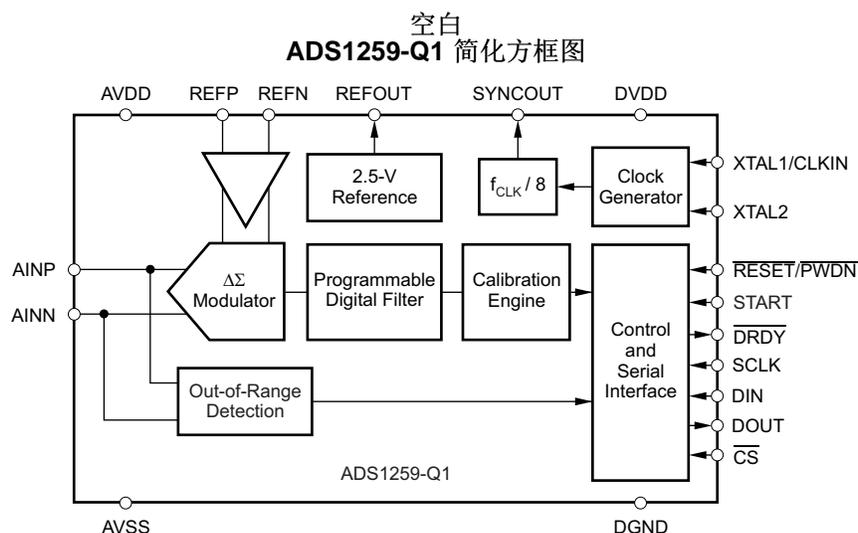
此转换器使用一个四阶、固有稳定、三角积分 ($\Delta\Sigma$) 调制器, 此调制器提供出色的噪声性能和线性。此器件可将集成振荡器、外部晶振或外部时钟用作 ADC 时钟源。

一个快速响应输入超范围检测器标志是否出现一个输入超范围事件。为了增加嘈杂汽车应用环境中的数据完整性, ADS1259-Q1 提供一个可选校验和字节与一个冗余转换数据读取功能。

ADS1259-Q1 运行时的功率为 13mW, 而在节电模式下的功耗少于 $25\mu\text{W}$ 。TI 提供的 ADS1259-Q1 器件采用薄型小外形尺寸 (TSSOP)-20 封装, 可在 -40°C 至 125° 的温度范围内完全额定运行。

器件信息

| 订货编号 | 封装 | 封装尺寸 |
|---------------|------------|---------------|
| ADS1259QPWRQ1 | TSSOP (20) | 6.5mm x 4.4mm |



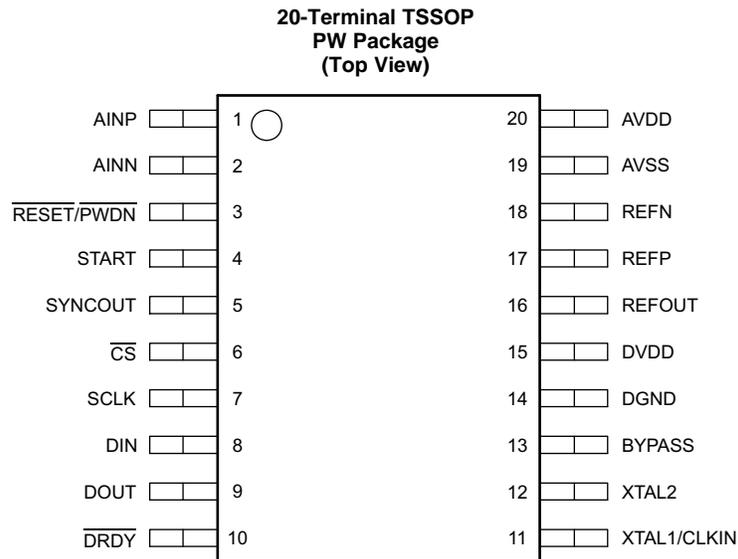
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4 修订历史记录

| 日期 | 修订版本 | 注释 |
|------------|------|--------|
| 2014 年 3 月 | * | 最初发布版本 |

5 Terminal Configuration and Functions



Terminal Functions

| TERMINAL | | TYPE | DESCRIPTION |
|----------|--------------------------------|----------------|--|
| NO. | NAME | | |
| 1 | AINP | Analog input | Positive analog input |
| 2 | AINN | Analog input | Negative analog input |
| 3 | $\overline{\text{RESET/PWDN}}$ | Digital input | Reset or power down; reset is active-low; hold low for power down. |
| 4 | START | Digital input | Start conversions, active-high |
| 5 | SYNCOUT | Digital output | Sync clock output ($f_{(\text{CLK})} / 8$) |
| 6 | $\overline{\text{CS}}$ | Digital input | SPI chip-select, active-low |
| 7 | SCLK | Digital input | SPI clock input |
| 8 | DIN | Digital input | SPI data input |
| 9 | DOUT | Digital output | SPI data output |
| 10 | $\overline{\text{DRDY}}$ | Digital output | Data-ready output, active-low |
| 11 | XTAL1/CLKIN | Digital input | Internal oscillator: DGND External clock: clock input Crystal oscillator: external crystal1 |
| 12 | XTAL2 | Digital | External crystal2, otherwise no connection |
| 13 | BYPASS | Analog | Core voltage bypass. Connect a 1- μF capacitor to DGND. |
| 14 | DGND | Digital | Digital ground |
| 15 | DVDD | Digital | Digital power supply |
| 16 | REFOUT | Analog output | Positive internal reference output. Connect a 1- μF capacitor, C_{REFOUT} , to AVSS. |
| 17 | REFP | Analog input | Positive reference input. Connect a 1- μF capacitor, C_{REFIN} , to REFN. ⁽¹⁾ |
| 18 | REFN | Analog input | Negative reference input ⁽¹⁾ |
| 19 | AVSS | Analog | Negative analog power supply and negative internal reference output |
| 20 | AVDD | Analog | Positive analog power supply |

(1) Leave unused reference inputs unconnected or tie to AVDD.

6 Specifications

6.1 Absolute Maximum Ratings⁽¹⁾

over operating ambient temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|--|---|------------|------------|------|
| AVDD to AVSS | | -0.3 | 7 | V |
| AVSS to DGND | | -2.8 | 0.3 | V |
| DVDD to DGND | | -0.3 | 7 | V |
| Analog input voltage | AINN, AINP, REFN, REFP | AVSS - 0.3 | AVDD + 0.3 | V |
| Digital input voltage | \overline{CS} , DIN, RESET/PDWN, SCLK, START, XTAL1/CLKIN | DGND - 0.3 | DVDD + 0.3 | V |
| Input current, continuous | Any terminal except supply terminals | -10 | 10 | mA |
| Operating junction temperature, T _J | | -40 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Handling Ratings

| | | MIN | MAX | UNIT |
|-----------------------------------|--|-----|-----|------|
| T _{stg} | Storage temperature range | -60 | 150 | °C |
| V _(ESD) ⁽¹⁾ | Human-body model (HBM) ESD stress voltage ⁽²⁾ | -2 | 2 | kV |
| | Charged-device model (CDM) ESD stress voltage ⁽²⁾ | -1 | 1 | kV |

- (1) Electrostatic discharge (ESD) to measure device sensitivity or immunity to damage caused by assembly-line electrostatic discharges into the device.
- (2) Meets or exceeds the passing level per AEC-Q100.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|--|-------------------|------------|-------------------|------|
| POWER SUPPLY | | | | | |
| Analog power supply | AVDD to AVSS | 4.75 | 5.0 | 5.25 | V |
| | AVSS to DGND | -2.6 | -2.5 | 0 | V |
| Digital power supply | DVDD to DGND | 2.7 | 3.3 | 5.25 | V |
| ANALOG INPUTS | | | | | |
| Absolute input voltage | AINP or AINN | AVSS - 0.1 | | AVDD + 0.1 | V |
| Differential input voltage ⁽¹⁾ | $V_{(IN)} = (V_{(AINP)} - V_{(AINN)})$ | -V _{ref} | | V _{ref} | V |
| VOLTAGE REFERENCE INPUTS | | | | | |
| Reference input voltage | $V_{ref} = (V_{(REFP)} - V_{(REFN)})$ | 0.5 | 2.5 | AVDD - AVSS + 0.2 | V |
| Absolute negative reference voltage | REFN | AVSS - 0.1 | AVSS | REFP - 0.5 | V |
| Absolute positive reference voltage | REFP | REFN + 0.5 | AVSS + 2.5 | AVDD + 0.1 | V |
| EXTERNAL CLOCK SOURCES (f_(CLK)) | | | | | |
| Crystal oscillator | Frequency | 2 | 7.3728 | 8 | MHz |
| External clock | Frequency | 0.1 | 7.3728 | 8 | MHz |
| | Duty cycle | 40% | | 60% | |
| DIGITAL INPUTS | | | | | |
| High-level input voltage, V _{IH} | | 0.8 DVDD | | DVDD | V |
| Low-level input voltage, V _{IL} | | DGND | | 0.2 DVDD | V |
| TEMPERATURE RANGE | | | | | |
| Operating ambient temperature, T _A | | -40 | | 125 | °C |

(1) Excluding the effects of offset and gain error.

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | PW (20 TERMINALS) | UNIT |
|-------------------------------|--|----------------------|------|
| R _{θJA} | Junction-to-ambient thermal resistance | 86.9 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 21 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 39.1 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 0.8 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 38.4 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

Minimum and maximum specifications are at $T_A = -40^\circ\text{C}$ to 125°C . Typical specifications are at $T_A = 25^\circ\text{C}$, $AVDD = 2.5\text{ V}$, $AVSS = -2.5\text{ V}$, $DVDD = 3.3\text{ V}$, external $f_{\text{CLK}} = 7.3728\text{ MHz}$, external $V_{\text{ref}} = 2.5\text{ V}$, and $f_{\text{DATA}} = 60\text{ SPS}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|-----------|----------------|----------|------------------------------|
| ANALOG INPUTS | | | | | |
| Differential input impedance | | | 120 | | k Ω |
| Common-mode input impedance | | | 500 | | k Ω |
| SYSTEM PERFORMANCE | | | | | |
| Resolution (no missing codes) | | 24 | | | Bits |
| Data rate, f_{DATA} | | 10 | | 14,400 | SPS |
| Noise (input referred) | Shorted inputs, See SBAS424 for more information. | | 0.7 | | μV_{RMS} |
| Integral nonlinearity, INL | Best-fit method | -10 | ± 3 | 10 | ppm |
| Offset voltage (input referred) | | -250 | ± 40 | 250 | μV |
| Offset voltage after calibration ⁽¹⁾ | | | ± 1 | | μV |
| Offset drift | $T_A = -40^\circ\text{C}$ to 125°C | | 0.05 | 0.25 | $\mu\text{V}/^\circ\text{C}$ |
| Gain error ⁽²⁾ | | -0.5% | $\pm 0.05\%$ | 0.5% | |
| Gain error after calibration ⁽¹⁾ | | | $\pm 0.0002\%$ | | |
| Gain drift | $T_A = -40^\circ\text{C}$ to 125°C | | 0.5 | 2.5 | ppm/ $^\circ\text{C}$ |
| Normal-mode rejection ratio, NMRR | | | See SBAS424. | | |
| Common-mode rejection ratio, CMRR | 60 Hz, ac ⁽³⁾ | 100 | 120 | | dB |
| AVDD, AVSS power-supply rejection ratio, PSRR | 60 Hz, ac ⁽³⁾ | 85 | 95 | | dB |
| DVDD power supply-rejection ratio, PSRR | 60 Hz, ac ⁽³⁾ | 85 | 110 | | dB |
| OUT-OF-RANGE DETECTION | | | | | |
| Threshold level | $AVSS + 150\text{ mV} \leq V_{\text{(AINP)}}; V_{\text{(AINN)}} \leq AVDD - 150\text{ mV}$ | | ± 105 | | %FSR |
| Threshold level accuracy | $AVSS + 150\text{ mV} \leq V_{\text{(AINP)}}; V_{\text{(AINN)}} \leq AVDD - 150\text{ mV}$ | | ± 0.5 | | %FSR |
| VOLTAGE REFERENCE INPUTS | | | | | |
| Average reference input current | $AVSS \leq V_{\text{(REFP)}}; V_{\text{(REFN)}} \leq AVDD$ | | 350 | | nA |
| Average reference input current drift | | | 0.2 | | nA/ $^\circ\text{C}$ |
| INTERNAL VOLTAGE REFERENCE | | | | | |
| Reference output voltage | $V_{\text{(REFOUT)}} = (\text{REFOUT} - AVSS)$ | | 2.5 | | V |
| Accuracy | $T_A = 25^\circ\text{C}$ | -0.4% | | 0.4% | |
| Temperature drift | $T_A = -40^\circ\text{C}$ to 125°C | | 10 | 40 | ppm/ $^\circ\text{C}$ |
| Drive current (sink and source) | | -10 | | 10 | mA |
| Load regulation | | | 10 | | $\mu\text{V}/\text{mA}$ |
| Turn-on settling time | $\pm 0.001\%$ settling, $C_{\text{REFIN}} = 1\text{ }\mu\text{F}$, $C_{\text{REFOUT}} = 1\text{ }\mu\text{F}$ | | 1 | | s |
| Long-term stability | 0 to 1000 hours | | 70 | | ppm |
| Thermal hysteresis | | | 30 | | ppm |
| CLOCK SOURCE (f_{CLK}) | | | | | |
| Internal oscillator frequency | | | 7.3728 | | MHz |
| Internal oscillator accuracy | | -2% | $\pm 0.2\%$ | 2% | |
| External crystal oscillator start-up time ⁽⁴⁾ | 18-pF load capacitors | | 20 | | ms |
| DIGITAL INPUTS AND OUTPUTS (DVDD = 2.7 V to 5.25 V) | | | | | |
| High-level output voltage, V_{OH} | $I_{\text{OH}} = 1\text{ mA}$ | 0.8 DVDD | | | V |
| | $I_{\text{OH}} = 8\text{ mA}$ | 0.75 DVDD | | | |
| Low-level output voltage, V_{OL} | $I_{\text{OL}} = 1\text{ mA}$ | | | 0.2 DVDD | V |
| | $I_{\text{OL}} = 8\text{ mA}$ | 0.2 DVDD | | | |
| Input hysteresis | | | 0.1 | | V |
| Input leakage | $0 < V_{\text{(DIGITAL INPUT)}} < DVDD$ | -10 | | 10 | μA |

(1) Calibration accuracy is on the level of noise (signal and ADC), reduced by the effect of 16-reading averaging.

(2) Excludes internal reference error.

(3) $f_{\text{DATA}} = 14.4\text{ kSPS}$. Placing a notch of the digital filter at 60 Hz (setting $f_{\text{DATA}} = 10\text{ SPS}$ or 60 SPS) further improves the common-mode rejection and power-supply rejection of this input frequency.

(4) External crystal start-up time can vary with crystal manufacturer and over temperature.

Electrical Characteristics (continued)

Minimum and maximum specifications are at $T_A = -40^{\circ}\text{C}$ to 125°C . Typical specifications are at $T_A = 25^{\circ}\text{C}$, $AVDD = 2.5\text{ V}$, $AVSS = -2.5\text{ V}$, $DVDD = 3.3\text{ V}$, external $f_{\text{CLK}} = 7.3728\text{ MHz}$, external $V_{\text{ref}} = 2.5\text{ V}$, and $f_{\text{DATA}} = 60\text{ SPS}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|-----|-----|-----|------|
| POWER SUPPLY | | | | | |
| Absolute analog supply current (AVDD, AVSS) | Operating (internal reference enabled) | | 2.3 | 5 | mA |
| | Standby mode (internal reference enabled) | | 200 | | μA |
| | Standby mode (internal reference disabled) | | 1 | | |
| | Power-down mode | | 1 | | |
| Digital supply current (DVDD) | Operating (internal oscillator ⁽⁵⁾) | | 500 | 700 | μA |
| | Standby mode (internal oscillator) | | 160 | 300 | |
| | Power-down mode (external CLKIN, SCLK stopped, digital inputs maintained at V_{IH} or V_{IL} voltage levels) | | 1 | 10 | |
| Power dissipation | Operating (internal reference enabled, internal oscillator) | | 13 | 28 | mW |
| | Standby mode (internal reference enabled, internal oscillator) | | 1.5 | | |
| | Standby mode (internal reference disabled, internal oscillator) | | 0.5 | | |
| | Power-down mode | | 10 | | μW |

(5) Internal oscillator current: 40 μA (typ.)

7 Residue

See [SBAS424](#) for any information on the ADS1259-Q1 device that is not covered in the foregoing sections.

8 器件文档和支持

8.1 Trademarks

SPI is a trademark of Motorola.

All other trademarks are the property of their respective owners.

8.2 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

9 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 要获得这份数据表的浏览器版本，请查阅左侧导航栏。

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|---------------|--|--------------|--|
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| 放大器和线性器件 | www.ti.com.cn/amplifiers | 计算机及周边 | www.ti.com.cn/computer |
| 数据转换器 | www.ti.com.cn/dataconverters | 消费电子 | www.ti.com.cn/consumer-apps |
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| DSP - 数字信号处理器 | www.ti.com.cn/dsp | 工业应用 | www.ti.com.cn/industrial |
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| RFID 系统 | www.ti.com.cn/rfidsys | | |
| OMAP应用处理器 | www.ti.com/omap | | |
| 无线连通性 | www.ti.com.cn/wirelessconnectivity | 德州仪器在线技术支持社区 | www.deyisupport.com |

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PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|---------|
| ADS1259QPWRQ1 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AD1259Q1 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF ADS1259-Q1 :

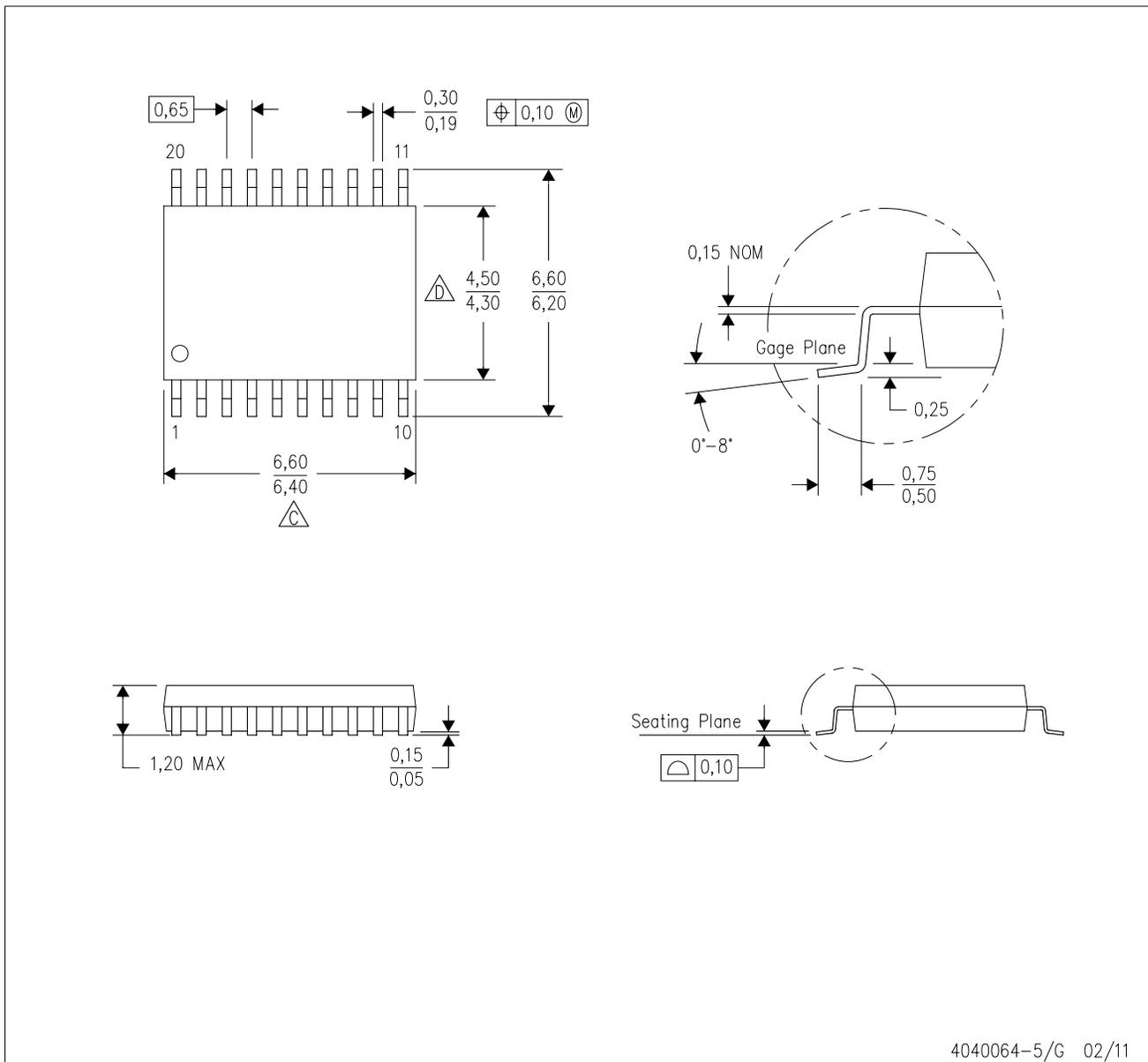
- Catalog: [ADS1259](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

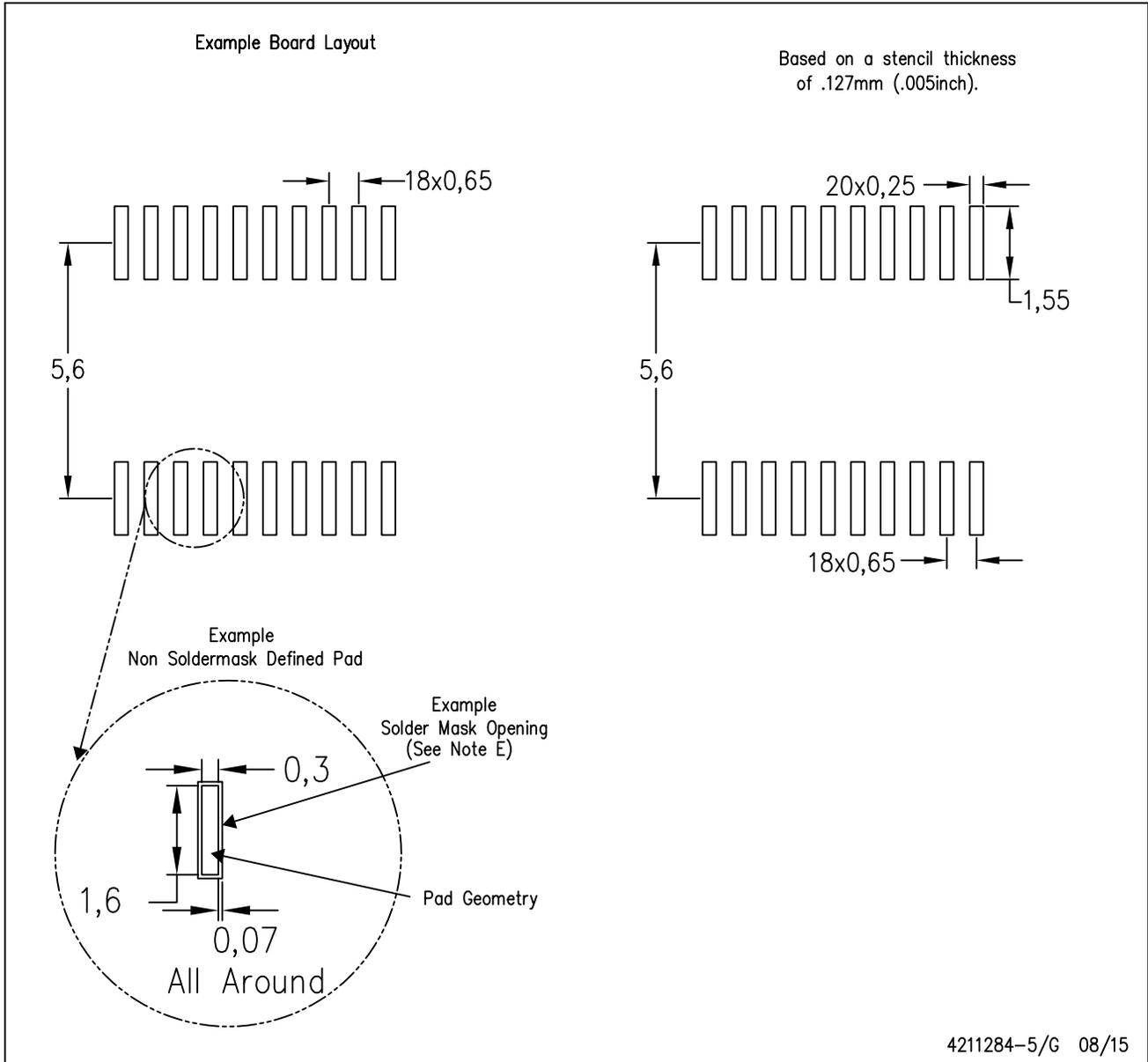


4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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