1 INTRODUCTION

The ADSP-21065L SHARC is a high-performance, 32-bit digital signal processor for communications, digital audio, and industrial instrumentation applications.

Along with a high-performance, 180 MFLOPS core, the ADSP-21065L has a dual-ported, on-chip SRAM and integrated I/O peripherals supported by a dedicated I/O processor. With its on-chip instruction cache, the processor can execute every instruction in a single cycle. The ADSP-21065L is code-compatible with other members of the SHARC family.

Four independent buses for dual data, instructions, and I/O, and cross-bar-switch memory connections implement the ADSP-21065L's Super Harvard Architecture.

The ADSP-21065L provides these features:

- 32-Bit IEEE floating-point computation units—Multiplier, ALU, and Shifter—that support 180 MFLOPS or 180, 32-bit fixed-point MOPS.
- Data Register File.
- Data Address Generators (DAG1, DAG2).
- Program Sequencer with Instruction Cache.
- 544 Kbits of user-configurable, dual-ported SRAM.
- External port for glueless interface to SDRAM and other off-chip memory and peripherals.

- Host port and multiprocessor interface.
- DMA controller to support ten DMA channels.
- Serial ports with two receivers and two transmitters that support TDM and I^2S.
- Two programmable timers and twelve programmable, general-purpose I/O ports.
- JTAG test access port.

Figure 1-1 shows the ADSP-21065L's Super Harvard Architecture, which consists of a crossbar bus switch connecting the DSP core's numeric processor to an independent I/O processor, dual-ported memory, and parallel system bus port.

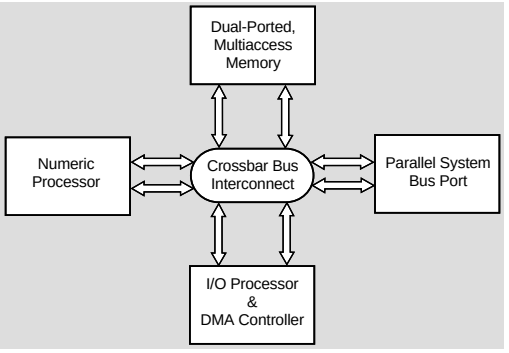

Figure 1-1. Super Harvard Architecture

Figure 1-2, a detailed block diagram of the processor, shows its architectural features.

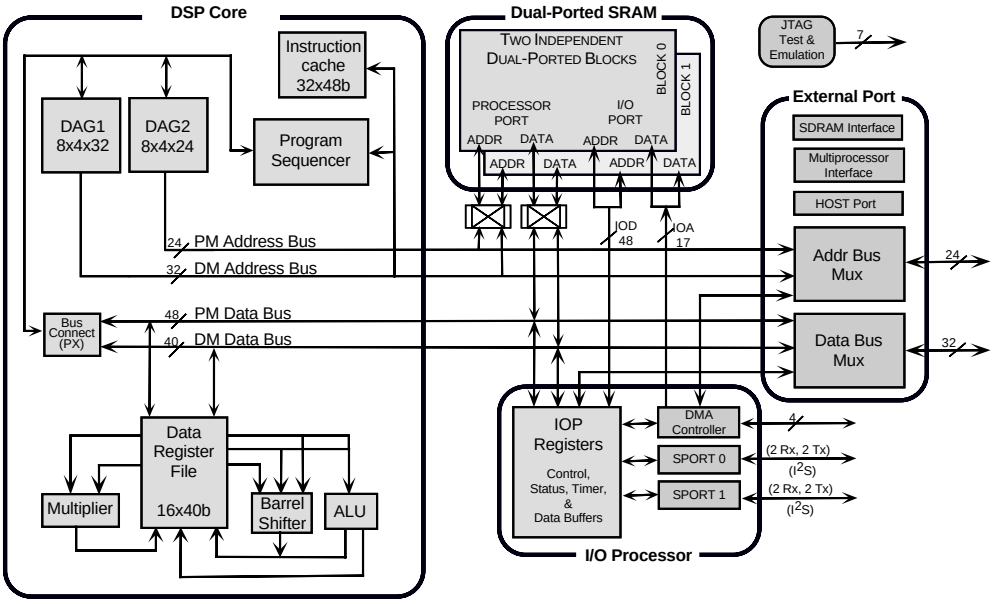

Figure 1-2. ADSP-21065L block diagram

Figure 1-2 also shows the ADSP-21065L's on-chip buses: the PM (Program Memory) bus, made up of the PMA (Program Memory Address) and PMD (Program Memory Data) buses; the DM (Data Memory) bus, made up of the DMA (Data Memory Address) and DMD (Data Memory Data) buses; and the I/O bus, made up of the IOA (I/O Address) and IOD (I/O Data) buses.

The PM bus can access either instructions or data. During a single cycle, the processor can access two data operands, one over the PM bus and one over the DM bus, access an instruction from the cache, and perform a DMA transfer.

The ADSP-21065L's external port provides the processor's interface to external memory, which is glueless to an SDRAM; memory-mapped I/O;

a host processor; and another multiprocessing ADSP-21065L. The external port performs internal and external bus arbitration and supplies control signals to shared, global memory and I/O devices.

The documentation set, *ADSP-21065L SHARC User's Manual* and *ADSP-21065L SHARC Technical Reference*, contain ADSP-21065L architectural information and the processor's instruction set, which developers need to design and program ADSP-21065L-based systems. For timing, electrical, and package specifications, see the processor's data sheet.

Features and Benefits

The ADSP-21065L possesses the five central requirements for DSPs established in the ADSP-2106x Family of 32-bit floating-point DSPs:

- Fast, flexible arithmetic computation units
- Unconstrained data flow to and from the computation units
- Extended precision and dynamic range in the computation units
- Dual address generators
- Efficient program sequencing

Fast, Flexible Arithmetic. The ADSP-21065L executes all instructions in a single cycle. It provides fast cycle times, and, in addition to traditional multiplication, addition, subtraction, and combined multiplication/addition, it also provides a complete set of arithmetic operations, including Seed 1/X, Seed $1\sqrt{X}$, Min, Max, Clip, Shift, and Rotate. The ADSP-21065L is IEEE floating-point compatible and supports either interrupt-on-arithmetic or latched-status exception handling.

Unconstrained Data Flow. The ADSP-21065L has an enhanced Super Harvard architecture combined with a 10-port data register file. In every cycle, the processor can:

- Read or write two operands to or from the Register File,
- Supply two operands to the ALU,
- Supply two operands to the multiplier, and
- Receive two results from the ALU and multiplier.

The processor's 48-bit orthogonal instruction word supports fully parallel data transfer and arithmetic operations in the same instruction.

40-Bit Extended Precision. The ADSP-21065L handles 32-bit IEEE floating-point format, 32-bit integer and fractional formats (twos-complement and unsigned), and extended-precision, 40-bit IEEE floating-point format. The processor carries extended precision throughout its computation units, limiting intermediate data truncation errors. When working with data on-chip, the processor can transfer the extended-precision, 32-bit mantissa to and from all computation units. The fixed-point formats have an 80-bit accumulator for true 32-bit fixed-point computations.

Dual Address Generators. The ADSP-21065L has two data address generators (DAGs) that provide immediate or indirect (pre- and postmodify) addressing. It supports modulus and bit-reverse operations with no constraints on data buffer placement.

Efficient Program Sequencing. In addition to zero-overhead loops, the ADSP-21065L supports single-cycle setup and exit for loops. Loops are both nestable (six levels in hardware) and interruptible. The processors support both delayed and non-delayed branches.

System-Level Enhancements

The ADSP-21065L includes several enhancements that simplify system development. The enhancements occur in three key areas:

- Architectural features supporting high-level languages and operating systems.
- IEEE 1149.1 JTAG serial scan path and on-chip emulation features.
- Support of IEEE floating-point formats.

High Level Languages. The ADSP-21065L's architecture has several features that directly support high-level language compilers and operating systems:

- General purpose data and address register files.
- 32-bit native data types.
- Large address space.
- Pre- and postmodify addressing.
- Unconstrained circular data buffer placement.
- On-chip program, loop, and interrupt stacks.

Additionally, the ADSP-21065L architecture is designed specifically to support ANSI-standard Numerical C extensions—the first compiled language to support vector data types and operators for numeric and signal processing.

Serial Scan and Emulation Features. The ADSP-21065L supports the IEEE standard P1149.1 Joint Test Action Group (JTAG) standard for system test. This standard defines a method for serially scanning the I/O status of each component in a system. The ADSP-21065L EZ-ICE in-circuit emulator also uses the JTAG serial port to access the processor's on-chip emulation features.

IEEE Formats. The ADSP-21065L supports IEEE floating-point data formats. This means that algorithms developed on IEEE-compatible processors and workstations are portable across processors without concern for possible instability introduced by biased rounding or inconsistent error handling.

Why Floating-Point DSP?

A digital signal processor's data format determines its ability to handle signals of differing precision, dynamic range, and signal-to-noise ratios. However, ease-of-use and time-to-market considerations are often equally important.

Precision. The number of bits of precision of A/D converters has continued to increase, and the trend is for both precision and sampling rates to increase.

Dynamic Range. Compression and decompression algorithms have traditionally operated on signals of known bandwidth. These algorithms were developed to behave regularly, to keep costs down and implementations easy. Increasingly, however, the trend in algorithm development is to unconstrain the regularity and dynamic range of intermediate results. Adaptive filtering and imaging are two applications that require a wide dynamic range.

Signal-to-Noise Ratio. Audio, video, imaging, and speech recognition require wide dynamic range to discern selected signals occurring in noisy environments.

Ease-of-Use. In general, 32-bit, floating-point DSPs are easier to use and enable a quicker time-to-market than 16-bit, fixed-point processors. The extent to which this is true depends on the floating-point processor's architecture. Consistency with IEEE workstation simulations and the elimination of scaling are two clear ease-of-use advantages. High-level language programmability, large address spaces, and wide dynamic range enable system development time to focus on algorithms and signal processing concerns, rather than assembly language coding, code paging, and error handling.

ADSP-21065L Architecture

The rest of this chapter summarizes the architectural features of the ADSP-21065L SHARC:

- DSP core
- Dual-ported memory
- External port interface
- Host processor interface
- I/O Processor
- Serial ports
- DMA controller
- Booting
- Development tools

The remaining chapters of this manual describe these features in detail.

DSP Core

The ADSP-21065L's DSP core consists of:

- Three computation units
- A data Register File
- A Program Sequencer and two Data Address Generators
- An Instruction Cache
- DSP core buses

- Two programmable timers and twelve general-purpose I/Os
- Four external hardware interrupts

These additional features support and enhance the DSP core's components:

- Context switching
- Comprehensive instruction set

Computation Units

The DSP core contains three independent computation units:

- ALU

  Performs a standard set of arithmetic and logic operations in both fixed-point and floating-point formats.

- Multiplier with a fixed-point accumulator

  Performs floating-point and fixed-point multiplication, and fixed-point multiply/add and multiply/subtract operations.

- Shifter

  Performs logical and arithmetic shifts, bit manipulation, field deposit and extraction, and exponent derivation operations on 32-bit operands.

For meeting a wide variety of processing needs, the computation units process data in three formats

- 32-bit, fixed-point
- 32-bit, floating-point
- 40-bit, floating-point

The floating-point operations are single-precision, IEEE-compatible. The 32-bit floating-point format is the standard IEEE format, while the 40-bit IEEE extended-precision format has eight additional LSBs of mantissa for greater accuracy.

The computation units perform single-cycle operations—there is no computation pipeline. The units connect in parallel rather than serially. On the next cycle, the output of any unit can be the input of any other unit. In a multifunction computation, the ALU and multiplier perform independent, simultaneous operations.

Register File

Applications use a general-purpose data Register File to transfer data between the computation units and the data buses and to store intermediate results.

For fast context switching, the Register File has two sets (primary and alternate) of sixteen registers. All of the registers are 40-bits wide. The Register File, combined with the core's Super Harvard architecture, enables unconstrained data flow between the computation units and internal memory.

Program Sequencer and Data Address Generators

A program sequencer and two dedicated address generators supply addresses for memory accesses. Together the Program Sequencer and Data Address Generators (DAGs) enable computational operations to execute with maximum efficiency since they free up the computation units to process data exclusively.

Using its instruction cache, the ADSP-21065L can simultaneously fetch an instruction (from the cache) and access two data operands (from memory).

The data address generators implement circular data buffers in hardware.

The Program Sequencer supplies instruction addresses to program memory. It controls loop iterations and evaluates conditional instructions. Using an internal loop counter and loop stack, the processor executes looped code with zero overhead. To loop or to decrement and test the counter requires no explicit jump instructions.

The processor uses pipelined *fetch*, *decode*, and *execute* cycles to achieve its fast execution rate. If an application uses external memories, the processor provides more time to complete an access than accesses requiring no decode cycle.

The DAGs generate memory addresses when data is transferred between memory and registers. Dual data address generators enable the processor to output simultaneous addresses for two operand reads or writes.

DAG1 supplies 32-bit addresses to data memory. DAG2 supplies 24-bit addresses to program memory for program memory data accesses.

Each DAG keeps track of up to eight address pointers, eight modifiers, and eight length values. You can modify a pointer used for indirect addressing with a value in a specified register, either before (premodify) or after (postmodify) the access. To perform automatic modulo addressing for circular data buffers, you can associate a length value with each pointer. And, you can locate circular buffers at arbitrary boundaries in memory. Each DAG register has an alternate register that you can activate for fast context switching.

Circular buffers enable efficient implementation of delay lines and other data structures required in digital signal processing and commonly used in digital filters and Fourier transforms. The DAG's automatic handling of address pointer wraparound reduces overhead, increases performance, and simplifies implementation.

Instruction Cache

The Program Sequencer includes a 32-word instruction cache that enables three-bus operation for fetching an instruction and two data values. The cache is selective—only instructions whose fetches conflict with program memory data accesses are cached. This enables full-speed execution of core looped operations, such as digital filter, multiply-accumulates and FFT butterfly processing.

DSP Core Buses

The DSP core has four buses:

- Program Memory Address

  Transfers the addresses for instructions.

- Data Memory Address

  Transfers the addresses for data.

- Program Memory Data

  Transfers instructions.

  Since the PM Data bus is 48-bits wide, it can accommodate the 48-bit instruction width. Fixed-point and single-precision floating-point data is aligned to the upper 32 bits of this bus.

- Data Memory Data

  Transfers data.

  The DM Data bus is 40-bits wide and provides a path to transfer the contents of any register in the processor to any other register or to any data memory location in a single cycle. Fixed-point and single-precision floating-point data is aligned to the upper 32 bits of this bus.

On the ADSP-21065L, data memory stores data operands, and program memory stores both instructions and data (filter coefficients, for example). This configuration enables the processor to perform dual data fetches when the instruction cache supplies the instruction.

The data memory address comes from one of two sources—an absolute value specified in the instruction code (direct addressing) or the output of a data address generator (indirect addressing).

Nearly every register in the ADSP-21065L's core is classified as a universal register. Instructions are provided specifically for transferring data between universal registers or between a universal register and memory and for performing bitwise operations on their contents. Control registers, status registers, and individual data registers in the Register File are all universal registers.

The PX (bus connect) registers provide the path to pass data between the 48-bit PM Data bus and the 40-bit DM Data bus or between the 40-bit Register File and the PM Data bus. The hardware that implements these registers handles the 8-bit difference in width.

Programmable Timers and General-Purpose I/O Ports

The ADSP-21065L provides two independent programmable timer blocks. Each block can function in one of two modes—Timer Counter mode or Pulse Count and Capture mode.

In Timer Counter mode, the processor can generate a waveform with an arbitrary pulse width within a maximum period of 71.5 seconds. In Pulse Count and Capture mode, the processor can measure either the high or the low pulse width and period of an input waveform.

The ADSP-21065L provides twelve programmable, general-purpose I/O pins that can function as either input or output. As output, these pins can signal peripheral devices; as input, they can provide the test for conditional branching.

Interrupts

The ADSP-21065L has four external hardware interrupts: three general-purpose interrupts $\overline{IRQ}_{2\text{-}0}$, and a special interrupt for reset. The processor also has internally generated interrupts for the timer, DMA controller operations, circular buffer overflow, stack overflows, arithmetic exceptions, multiprocessor vector interrupts, and user-defined software interrupts.

For the general-purpose external interrupts and the internal timer interrupt, the ADSP-21065L automatically stacks the arithmetic status and mode (MODE1) registers in parallel with the interrupt servicing. This enables four nesting levels of very fast service for these interrupts.

Context Switching

Many of the processor's registers have alternate registers that applications can activate and use during interrupt servicing to implement a fast context switch.

Each of the data registers in the Register File, the DAG registers, and the multiplier result register have alternates. Registers active at reset are called *primary* registers, and the others are called *alternate* (or *secondary*) registers. Control bits in a mode control register determine which set of registers is active at any particular time.

Comprehensive Instruction Set

The ADSP-21065L instruction set provides a wide variety of programming capabilities. Multifunction instructions enable computations in parallel with data transfers and as simultaneous multiplier and ALU operations.

The addressing power of the ADSP-21065L provides flexibility in moving data both internally and externally. Every instruction can be executed in a single processor cycle. The ADSP-2106x Family Assembly language uses

an algebraic syntax for ease of coding and readability. A comprehensive set of development tools supports program development.

Dual-Ported Memory

The ADSP-21065L contains 544 Kbits of on-chip SRAM, organized into two banks: Bank 0 has 288 Kbits, and Bank 1 has 256 Kbits. Bank 0 is configured with 9 columns of 2Kx16 bits, and Bank 1 is configured with 8 columns of 2Kx16 bits. Each memory block is dual-ported for single-cycle, independent accesses by the processor's core and either its I/O processor or DMA controller. The dual-ported memory and separate on-chip buses allow two data transfers from the core and one from I/O, all in a single cycle.

On the ADSP-21065L, the memory can be configured as a maximum of 16K words of 32-bit data, 34K words for 16-bit data, 10K words of 48-bit instructions (and 40-bit data) or combinations of different word sizes up to 544 Kbits. All the memory can be accessed as 16-bit, 32-bit, or 48-bit.

The ADSP-21065L supports a 16-bit floating-point storage format, which effectively doubles the amount of data that it can store on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is done in a single instruction.

While each memory block can store combinations of code and data, accesses are most efficient when one block stores data, using the DM bus for transfers, and the other block stores instructions and data, using the PM bus for transfers. Using the DM and PM buses in this way, with one dedicated to each memory block, assures single-cycle execution with two data transfers, providing the instruction is available in the cache. Single-cycle execution is also maintained when one of the data operands is transferred to or from off-chip, through the ADSP-21065L's external port.

External Port Interface

The ADSP-21065L's external port provides the processor's interface to off-chip memory and peripherals. The 64M × 32-bit word, off-chip address space is included in the ADSP-21065L's unified address space. The separate on-chip buses—for PM addresses, PM data, DM addresses, DM data, I/O addresses, and I/O data—are multiplexed at the external port to create an external system bus with a single 24-bit address bus and a single 32-bit data bus.

The ADSP-21065L provides an on-chip SDRAM controller that supports a glueless interface to standard 16Mb and 64Mb SDRAMs.

The on-chip decoding of high-order address lines to generate memory bank select signals facilitates the addressing of external memory devices.

The ADSP-21065L provides programmable memory wait states and external memory acknowledge controls to enable the processor to interface with peripherals with variable access, hold, and disable time requirements.

Host Interface

The ADSP-21065L's host interface provides a connection to standard 8-, 16-, or 32-bit microprocessor buses that is easy and requires little additional hardware.

The ADSP-21065L supports asynchronous transfers at speeds up to the processor's full clock rate. The ADSP-21065L's external port provides access to the processor's host interface, which is memory-mapped into the processor's unified address space.

Two channels of DMA are available for the host interface, and they perform code and data transfers with low software overhead. The host can directly read and write the IOP registers of the ADSP-21065L and can access the DMA channel setup and mailbox registers.

Vector interrupt support provides efficient execution of host commands.

I/O Processor

The ADSP-21065L's I/O Processor (IOP) includes two serial ports, each with two transmitters and two receivers, and a DMA controller.

Serial Ports

The ADSP-21065L features two synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices.

The serial ports can operate at the full clock rate of the processor, providing each with a maximum data rate of 30 Mbit/s. Each serial port has a primary and a secondary set of Tx and Rx channels, as shown in Figure 1-3.

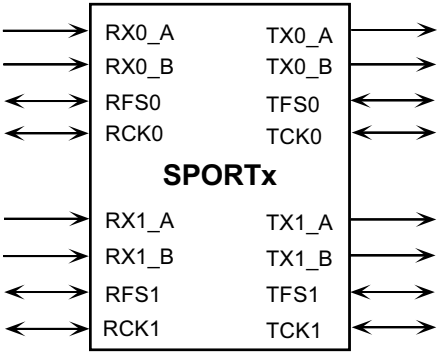

Figure 1-3. Serial port input/output configuration

Independent transmit and receive functions provide greater flexibility for serial communications. Serial port data can be automatically transferred to and from on-chip memory through DMA. Each of the serial ports supports three operation modes: standard mode, I^2S mode (an interface

commonly used by audio codecs), and TDM (Time Division Multiplex) multichannel mode.

The serial ports can operate with little-endian or big-endian transmission formats, with selectable word lengths of three to thirty-two bits. They offer selectable synchronization and transmit modes and optional µ-law or A-law companding. Serial port clocks and frame syncs can be internally or externally generated. The serial ports also include keyword and keymask features to enhance interprocessor communication.

DMA Controller

The ADSP-21065L's on-chip DMA controller enables zero-overhead data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor's core, enabling DMA operations to occur while the core is simultaneously executing its program. Applications can use DMA transfers to download both code and data to the ADSP-21065L.

DMA transfers can occur between the ADSP-21065L's internal memory and external memory, the processor's serial ports, external peripherals, or a host processor. DMA transfers between external memory and external peripheral devices are another option. During DMA transfers, the DMA controller automatically packs and unpacks external bus words.

Ten channels of DMA are available on the ADSP-21065L—eight via the serial ports and two via the processor's external port (for either host processor or other ADSP-21065L memory or I/O transfers).

Asynchronous off-chip peripherals can control the two external port DMA channels using the DMA request and grant lines ($\overline{\text{DMAR}}_{1\text{-}2}$ and $\overline{\text{DMAG}}_{1\text{-}2}$).

Other DMA features include interrupt generation upon completion of DMA transfers and DMA chaining for automatically linked DMA transfers.

Booting

Applications can boot the internal memory of the ADSP-21065L at system powerup from an 8-bit EPROM, a host processor, or external memory. The $\overline{\text{BMS}}$ (Boot Memory Select) and BSEL (EPROM Boot) pins select the boot source. Either 8-, 16-, or a 32-bit host processor can boot the ADSP-21065L.

Development Tools

The ADSP-21065L is supported with a complete set of software and hardware development tools, including the EZ-ICE® In-Circuit Emulator and VisualDSP® and SHARC® Tools development software.

The same EZ-ICE hardware that you use for the ADSP-21060/62, also fully emulates the ADSP-21065L, with the exception of displaying and modifying the two new SPORTs registers. The emulator will not display these two registers, but your code can still use them.

Both the SHARC Development Tools family and the VisualDSP integrated project management and debugging environment support the ADSP21065L. The VisualDSP project management environment enables you to develop and debug an application from within a single integrated program.

The SHARC Development Tools include an easy to use Assembler with instructions based on an algebraic syntax; a linker; a loader; a cycle-accurate, instruction-level simulator; a C compiler; and a C run-time library that includes DSP and mathematical functions.

Debugging both C and Assembly programs with the VisualDSP debugger, you can:

- View mixed C and Assembly code
- Insert break points

- Set watch points
- Trace program execution
- Profile program execution
- Fill and dump memory
- Create custom debugger windows

The VisualDSP Integrated Development Environment (IDE) enables you to define and manage multiuser projects. Its dialog boxes and property pages enable you to configure and manage all of the SHARC Development Tools. This capability enables you to:

- Control how the development tools process inputs and generate outputs.
- Maintain a one-to-one correspondence with the tool's command line switches.

The EZ-ICE Emulator uses the IEEE 1149.1 JTAG test access port of the ADSP-21065L processor to monitor and control the target board processor during emulation. The EZ-ICE provides full-speed emulation to enable inspection and modification of memory, registers, and processor stacks. Use of the processor's JTAG interface assures nonintrusive in-circuit emulation—the emulator does not affect target system loading or timing.

In addition to the software and hardware development tools available from Analog Devices, third parties provide a wide range of tools supporting the SHARC processor family.

Summary of Features

This section summarizes the functional features and benefits of the ADSP-21065L, the design features that balance its DSP core with its I/O components, and lists additional, related ADI literature.

Features and Benefits

Table 1-1. Summary of ADSP-21065L features and benefits

Feature	Benefits
32-bit processing	• More precise processing of 16-bit signals. • 32-bit words essential for processing 20- and 24-bit input signals. • Improved signal-to-noise ratio at low levels. • Faster processing due to compact code. • Wide dynamic range.
Fixed- and floating-point on one chip	• Greater flexibility. • Reduced development time because need to rewrite standard floating- or fixed-point algorithms is eliminated.
60 MIPS/180 MFLOPS	• More processing implemented with a single chip. • Eliminates bus bottlenecks.

Table 1-1. Summary of ADSP-21065L features and benefits (Cont'd)

Feature	Benefits
16K × 32bit (544 Kbits) of user-configurable internal memory	• Reduces bottlenecks over accesses of off-chip memory. • Reduces overall system cost, size, and power consumption. • Provides freedom in allocating data and program memory.
240 Mbit/sec. I/O • 2 serial Tx and 2 serial Rx serial ports • I^2S Interface	• Process more audio channels using just one DSP. • Multiple channels supported in communication systems.
10 DMA channels	Implement multifunction applications on one chip.
TDM serial ports	• Direct interface to T1 and E1 lines. • Ability to communicate with other ADSP-21065Ls.
Glueless SDRAM interface	• Maximize synchronous data transfer rate. • Reduce overall system cost.

Balanced Performance

Figure 1-4 shows how the ADSP-21065L's design optimally balances its high-performance DSP core with its high-speed I/Os.

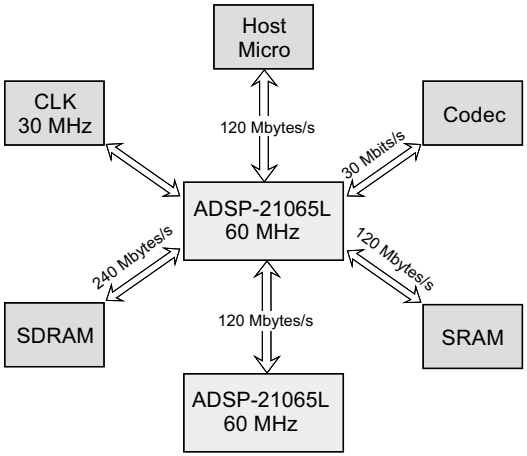

Figure 1-4. Balanced performance between the DSP core and I/O

Additional Literature

The following publications can be ordered from any Analog Devices sales office.

ADSP-21000 Family Hardware & Software Development Tools Data Sheet
ADSP-21065L SHARC Data Sheet
C Compiler Guide and Reference for the ADSP-2106x Family DSPs
Debugger Tutorial for the ADSP-2106x Family DSPs
VisualDSP Debugger Guide and Reference
VisualDSP Release Notes
VisualDSP User's Guide and Reference