4. DC and Switching Characteristics

SIIGX51006-4.6

Operating Conditions

Stratix® II GX devices are offered in both commercial and industrial grades. Industrial devices are offered in -4 speed grade and commercial devices are offered in -3 (fastest), -4, and -5 speed grades.

Tables 4–1 through 4–51 provide information on absolute maximum ratings, recommended operating conditions, DC electrical characteristics, and other specifications for Stratix II GX devices.

Absolute Maximum Ratings

Table 4–1 contains the absolute maximum ratings for the Stratix II GX device family.

Table 4–1. Stratix II GX Device Absolute Maximum Ratings *Notes (1), (2), (3)*

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage	With respect to ground	–0.5	1.8	V
V_{CCIO}	Supply voltage	With respect to ground	–0.5	4.6	V
V_{CCPD}	Supply voltage	With respect to ground	–0.5	4.6	V
V_I	DC input voltage *(4)*		–0.5	4.6	V
I_{OUT}	DC output current, per pin		–25	40	mA
T_{STG}	Storage temperature	No bias	–65	150	C
T_J	Junction temperature	BGA packages under bias	–55	125	C

Notes to Table 4–1:

(1) See the *Operating Requirements for Altera Devices Data Sheet* for more information.

(2) Conditions beyond those listed in Table 4–1 may cause permanent damage to a device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse affects on the device.

(3) Supply voltage specifications apply to voltage readings taken at the device pins, not at the power supply.

(4) During transitions, the inputs may overshoot to the voltage shown in Table 4–2 based upon the input duty cycle. The DC case is equivalent to 100% duty cycle. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 4–2. Maximum Duty Cycles in Voltage Transitions			
Symbol	**Parameter**	**Condition**	**Maximum Duty Cycles (%)** *(1)*
V_I	Maximum duty cycles in voltage transitions	V_I = 4.0 V	100
		V_I = 4.1 V	90
		V_I = 4.2 V	50
		V_I = 4.3 V	30
		V_I = 4.4 V	17
		V_I = 4.5 V	10

Note to Table 4–2:

(1) During transition, the inputs may overshoot to the voltages shown based on the input duty cycle. The duty cycle case is equivalent to 100% duty cycle.

Recommended Operating Conditions

Table 4–3 contains the Stratix II GX device family recommended operating conditions.

Table 4–3. Stratix II GX Device Recommended Operating Conditions (Part 1 of 2) Note (1)					
Symbol	**Parameter**	**Conditions**	**Minimum**	**Maximum**	**Unit**
V_{CCINT}	Supply voltage for internal logic and input buffers	100 µs ≤rise time ≤100 ms *(3)*	1.15	1.25	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	100 µs ≤rise time ≤100 ms *(3)*, *(6)*	3.135 (3.00)	3.465 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	100 µs ≤rise time ≤100 ms *(3)*	2.375	2.625	V
	Supply voltage for output buffers, 1.8-V operation	100 µs ≤rise time ≤100 ms *(3)*	1.71	1.89	V
	Supply voltage for output buffers, 1.5-V operation	100 µs ≤rise time ≤100 ms *(3)*	1.425	1.575	V
	Supply voltage for output buffers, 1.2-V operation	100 µs ≤rise time ≤100 ms *(3)*	1.15	1.25	V
V_{CCPD}	Supply voltage for pre-drivers as well as configuration and JTAG I/O buffers.	100 µs ≤rise time ≤100 ms *(4)*	3.135	3.465	V
V_I	Input voltage (see Table 4–2)	*(2)*, *(5)*	–0.5	4.0	V
V_O	Output voltage		0	V_{CCIO}	V

Table 4–3. Stratix II GX Device Recommended Operating Conditions (Part 2 of 2) Note (1)					
Symbol	**Parameter**	**Conditions**	**Minimum**	**Maximum**	**Unit**
T_J	Operating junction temperature	For commercial use	0	85	C
		For industrial use	–40	100	C

Notes to Table 4–3:
(1) Supply voltage specifications apply to voltage readings taken at the device pins, not at the power supply.
(2) During transitions, the inputs may overshoot to the voltage shown in Table 4–2 based upon the input duty cycle. The DC case is equivalent to 100% duty cycle. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically from ground to V_{CC}.
(4) V_{CCPD} must ramp-up from 0 V to 3.3 V within 100 µs to 100 ms. If V_{CCPD} is not ramped up within this specified time, the Stratix II GX device will not configure successfully. If the system does not allow for a V_{CCPD} ramp-up time of 100 ms or less, hold `nCONFIG` low until all power supplies are reliable.
(5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT}, V_{CCPD}, and V_{CCIO} are powered.
(6) V_{CCIO} maximum and minimum conditions for PCI and PCI-X are shown in parentheses.

Transceiver Block Characteristics

Tables 4–4 through 4–6 contain transceiver block specifications.

Table 4–4. Stratix II GX Transceiver Block Absolute Maximum Ratings Note (1)					
Symbol	**Parameter**	**Conditions**	**Minimum**	**Maximum**	**Units**
V_{CCA}	Transceiver block supply voltage	Commercial and industrial	–0.5	4.6	V
V_{CCP}	Transceiver block supply voltage	Commercial and industrial	–0.5	1.8	V
V_{CCR}	Transceiver block supply Voltage	Commercial and industrial	–0.5	1.8	V
V_{CCT}	Transceiver block supply voltage	Commercial and industrial	–0.5	1.8	V
V_{CCT_B}	Transceiver block supply voltage	Commercial and industrial	–0.5	1.8	V
V_{CCL}	Transceiver block supply voltage	Commercial and industrial	–0.5	1.8	V
V_{CCH_B}	Transceiver block supply voltage	Commercial and industrial	–0.5	2.4	V

Note to Table 4–4:
(1) The device can tolerate prolonged operation at this absolute maximum, as long as the maximum specification is not violated.

Table 4–5. Stratix II GX Transceiver Block Operating Conditions

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCA}	Transceiver block supply voltage	Commercial and industrial	3.135	3.3	3.465	V
V_{CCP}	Transceiver block supply voltage	Commercial and industrial	1.15	1.2	1.25	V
V_{CCR}	Transceiver block supply voltage	Commercial and industrial	1.15	1.2	1.25	V
V_{CCT}	Transceiver block supply voltage	Commercial and industrial	1.15	1.2	1.25	V
V_{CCT_B}	Transceiver block supply voltage	Commercial and industrial	1.15	1.2	1.25	V
V_{CCL}	Transceiver block supply voltage	Commercial and industrial	1.15	1.2	1.25	V
V_{CCH_B} *(2)*	Transceiver block supply voltage	Commercial and industrial	1.15	1.2	1.25	V
			1.425	1.5	1.575	V
R_{REF} *(1)*	Reference resistor	Commercial and industrial	2000 –1%	2000	2000 +1%	Ω

Notes to Table 4–5:
(1) The DC signal on this pin must be as clean as possible. Ensure that no noise is coupled to this pin.
(2) Refer to the *Stratix II GX Device Handbook*, volume 2, for more information.

Table 4–6. Stratix II GX Transceiver Block AC Specification (Part 1 of 6)

Symbol / Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference clock											
Input frequency from REFCLK input		50	-	622.08	50	-	622.08	50	-	622.08	MHz
Input frequency from PLD input		50	-	325	50	-	325	50	-	325	MHz
Input clock jitter		Refer to Table 4–20 on page 4–36 for the input jitter specifications for the reference clock.									
Absolute V_{MAX} for a REFCLK pin *(12)*		-	-	3.3	-	-	3.3	-	-	3.3	V

Table 4–6. Stratix II GX Transceiver Block AC Specification (Part 2 of 6)

Symbol / Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Absolute V_{MIN} for a REFCLK pin *(12)*		-0.3	-	-	-0.3	-	-	-0.3	-	-	V
Rise/fall time		-	0.2	-	-	0.2	-	-	0.2	-	UI
Duty cycle		40	-	60	40	-	60	40	-	60	%
Peak-to-peak differential input voltage		200	-	2000	200	-	2000	200	-	2000	mV
Spread-spectrum clocking		30 0 to -0.5%	-	33 0 to -0.5%	30 0 to -0.5%	-	33 0 to -0.5%	30 0 to -0.5%	-	33 0 to -0.5%	kHz
On-chip termination resistors		115 ±20%			115 ±20%			115 ±20%			Ω
V_{ICM} (AC coupled) *(12)*		1200 ±5%			1200 ±5%			1200 ±5%			mV
V_{ICM} (DC coupled) *(4)*		0.25	-	0.55	0.25	-	0.55	0.25	-	0.55	V
Rref		2000 ±1%			2000 ±1%			2000 ±1%			Ω
Transceiver Clocks											
Calibration block clock frequency		10	-	125	10	-	125	10	-	125	MHz
Calibration block minimum power-down pulse width		30	-	-	30	-	-	30	-	-	ns
Time taken for one-time calibration		-	-	8	-	-	8	-	-	8	ms
fixedclk clock frequency	PCI Express Receiver Detect	-	125	-	-	125	-	-	125	-	MHz
	Adaptive Equalization (AEQ)	2.5	-	125	2.5	-	125	-	-	-	MHz

Table 4–6. Stratix II GX Transceiver Block AC Specification (Part 3 of 6)

Symbol / Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
reconfig_clk clock frequency		2.5	-	50	2.5	-	50	2.5	-	50	MHz
Transceiver block minimum power-down pulse width		100	-	-	100	-	-	100	-	-	ns
Receiver											
Data rate		600	-	6375	600	-	5000	600	-	4250	Mbps
Absolute V_{MAX} for a receiver pin *(1)*		-	-	2.0	-	-	2.0	-	-	2.0	V
Absolute V_{MIN} for a receiver pin		-0.4	-	-	-0.4	-	-	-0.4	-	-	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p)	V_{CM} = 0.85 V	-	-	3.3	-	-	3.3	-	-	3.3	V
Minimum peak-to-peak differential input voltage V_{ID} (diff p-p)	V_{CM} = 0.85 V DC Gain = ≥ 3 dB	160	-	-	160	-	-	160	-	-	mV
V_{ICM}	V_{ICM} = 0.85 V setting	850±10%			850±10%			850±10%			mV
	V_{ICM} = 1.2 V setting *(11)*	1200±10%			1200±10%			1200±10%			mV
On-chip termination resistors	100 Ω setting	100±15%			100±15%			100±15%			Ω
	120 Ω setting	120±15%			120±15%			120±15%			Ω
	150 Ω setting	150±15%			150±15%			150±15%			Ω
Bandwidth at 6.375 Gbps	BW = Low	-	20	-	-	-	-	-	-	-	MHz
	BW = Med	-	35	-	-	-	-	-	-	-	MHz
	BW = High	-	45	-	-	-	-	-	-	-	MHz

Table 4–6. Stratix II GX Transceiver Block AC Specification (Part 4 of 6)

Symbol / Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Bandwidth at 3.125 Gbps	BW = Low	-	30	-	-	30	-	-	30	-	MHz
	BW = Med	-	40	-	-	40	-	-	40	-	MHz
	BW = High	-	50	-	-	50	-	-	50	-	MHz
Bandwidth at 2.5 Gbps	BW = Low	-	35	-	-	35	-	-	35	-	MHz
	BW = Med	-	50	-	-	50	-	-	50	-	MHz
	BW = High	-	60	-	-	60	-	-	60	-	MHz
Return loss differential mode		100 MHz to 2.5 GHz (XAUI): -10 dB 50 MHz to 1.25 GHz (PCI-E): -10 dB 100 MHz to 4.875 GHz (OIF/CEI): -8dB 4.875 GHz to 10 GHz (OIF/CEI): 16.6 dB/decade slope									
Return loss common mode		100 MHz to 2.5 GHz (XAUI): -6 dB 50 MHz to 1.25 GHz (PCI-E): -6 dB 100 MHz to 4.875 GHz (OIF/CEI): -6dB 4.875 GHz to 10 GHz (OIF/CEI): 16.6 dB/decade slope									
Programmable PPM detector *(2)*		±62.5, 100, 125, 200, 250, 300, 500, 1000			±62.5, 100, 125, 200, 250, 300, 500, 1000			±62.5, 100, 125, 200, 250, 300, 500, 1000			ppm
Run length *(3)*, *(9)*		80			80			80			UI
Programmable equalization		-	-	16	-	-	16	-	-	16	dB
Signal detect/loss threshold *(4)*		65	-	175	65	-	175	65	-	175	mV
CDR LTR TIme *(5)*, *(9)*		-	-	75	-	-	75	-	-	75	us
CDR Minimum T1b *(6)*, *(9)*		15	-	-	15	-	-	15	-	-	us
LTD lock time *(7)*, *(9)*		0	100	4000	0	100	4000	0	100	4000	ns
Data lock time from `rx_freqlocked` *(8)*, *(9)*		-	-	4	-	-	4	-	-	4	us
Programmable DC gain		0, 3, 6			0, 3, 6			0, 3, 6			dB
Transmitter											

Table 4–6. Stratix II GX Transceiver Block AC Specification (Part 5 of 6)

Symbol / Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Data rate		600	-	6375	600	-	5000	600	-	4250	Mbps
V_{OCM}	V_{OCM} = 0.6 V setting	580±10%			580±10%			580±10%			mV
	V_{OCM} = 0.7 V setting	680±10%			680±10%			680±10%			mV
On-chip termination resistors	100 Ω setting	108±10%			108±10%			108±10%			Ω
	120 Ω setting	125±10%			125±10%			125±10%			Ω
	150 Ω setting	152±10%			152±10%			152±10%			Ω
Return loss differential mode	312 MHz to 625 MHz (XAUI): -10 dB 625 MHz to 3.125 GHz (XAUI): -10 dB/decade slope 50 MHz to 1.25 GHz (PCI-E): -10dB 100 MHz to 4.875 GHz (OIF/CEI): -8db 4.875 GHz to 10 GHz (OIF/CEI): 16.6 dB/decade slope										
Return loss common mode	50 MHz to 1.25 GHz (PCI-E): -6dB 100 MHz to 4.875 GHz (OIF/CEI): -6db 4.875 GHz to 10 GHz (OIF/CEI): 16.6 dB/decade slope										
Rise time		35	-	65	35	-	65	35	-	65	ps
Fall time		35	-	65	35	-	65	35	-	65	ps
Intra differential pair skew	V_{OD} = 800 mV	-	-	15	-	-	15	-	-	15	ps
Intra-transceiver block skew (x4)		-	-	100	-	-	100	-	-	100	ps
Inter-transceiver block skew (x8)		-	-	300	-	-	300	-	-	300	ps
TXPLL (TXPLL0 and TXPLL1)											
VCO frequency range (low gear)		500	-	1562.5	500	-	1562.5	500	-	1562.5	MHz
VCO frequency range (high gear)		1562.5		3187.5	1562.5		2500	1562.5	-	2125	MHz

Table 4–6. Stratix II GX Transceiver Block AC Specification (Part 6 of 6)

Symbol / Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Bandwidth at 6.375 Gbps	BW = Low	-	2	-	-	-	-	-	-	-	MHz
	BW = Med	-	3	-	-	-	-	-	-	-	MHz
	BW = High	-	7	-	-	-	-	-	-	-	MHz
Bandwidth at 3.125 Gbps	BW = Low	-	3	-	-	3	-	-	3	-	MHz
	BW = Med	-	5	-	-	5	-	-	5	-	MHz
	BW = High	-	9	-	-	9	-	-	9	-	MHz
Bandwidth at 2.5 Gbps	BW = Low	-	1	-	-	1	-	-	1	-	MHz
	BW = Med	-	2	-	-	2	--	-	2	-	MHz
	BW = High	-	4	-	-	4	-	-	4	-	MHz
TX PLL lock time from `gxb_powerdown` deassertion *(9)*, *(10)*		-	-	100	-	-	100	-	-	100	us
PLD-Transceiver Interface											
Interface speed		25	-	250	25	-	250	25	-	200	MHz
Digital Reset Pulse Width		Minimum is 2 parallel clock cycles									

Notes to Table 4–6:

(1) The device cannot tolerate prolonged operation at this absolute maximum. Refer to Figure 4–5 for more information.
(2) The rate matcher supports only up to +/-300 ppm.
(3) This parameter is measured by embedding the run length data in a PRBS sequence.
(4) This feature is only available in PCI-Express (PIPE) mode.
(5) Time taken to `rx_pll_locked` goes high from `rx_analogreset` deassertion. Refer to Figure 4–1.
(6) This is how long GXB needs to stay in LTR mode after `rx_pll_locked` is asserted and before `rx_locktodata` is asserted in manual mode. Refer to Figure 4–1.
(7) Time taken to recover valid data from GXB after `rx_locktodata` signal is asserted in manual mode. Measurement results are based on PRBS31, for native data rates only. Refer to Figure 4–1.
(8) Time taken to recover valid data from GXB after `rx_freqlocked` signal goes high in automatic mode. Measurement results are based on PRBS31, for native data rates only. Refer to Figure 4–1.
(9) Please refer to the Protocol Characterization documents for lock times specific to the protocols.
(10) Time taken to lock TX PLL from `gxb_powerdown` deassertion.
(11) The 1.2 V RX V_{ICM} setting is intended for DC-coupled LVDS links.
(12) For AC-coupled links, the on-chip biasing circuit is switched off before and during configuration. Make sure that input specifications are not violated during this period.

Figure 4–1 shows the lock time parameters in manual mode, Figure 4–2 shows the lock time parameters in automatic mode.

LTD = Lock to data
LTR = Lock to reference clock

Figure 4–1. Lock Time Parameters for Manual Mode

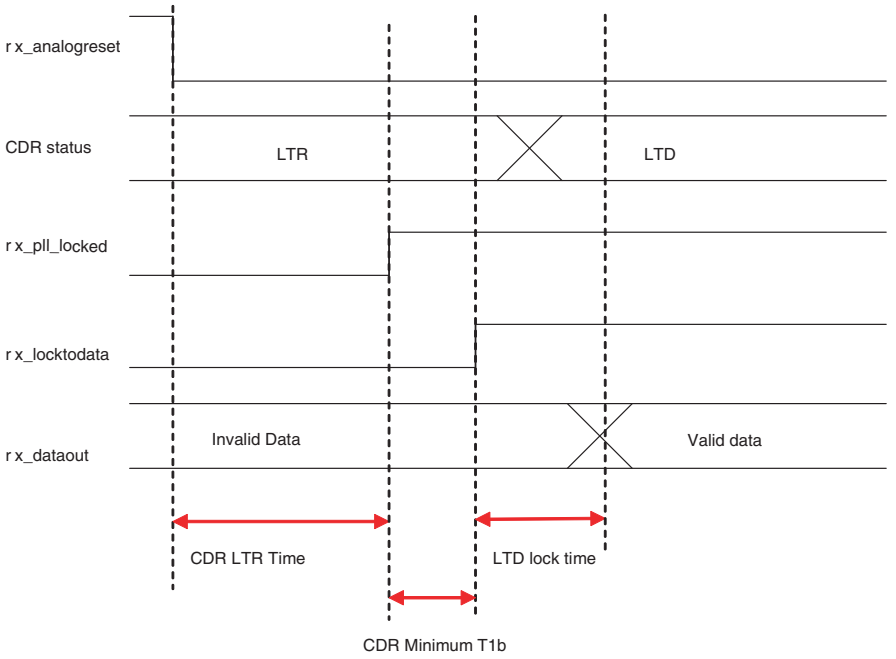
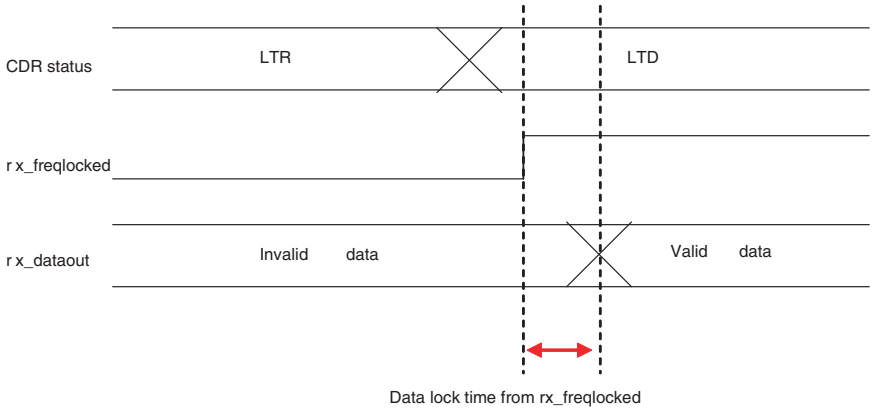


Figure 4–2. Lock Time Parameters for Automatic Mode



Figures 4–3 and 4–4 show differential receiver input and transmitter output waveforms, respectively.

Figure 4–3. Receiver Input Waveform

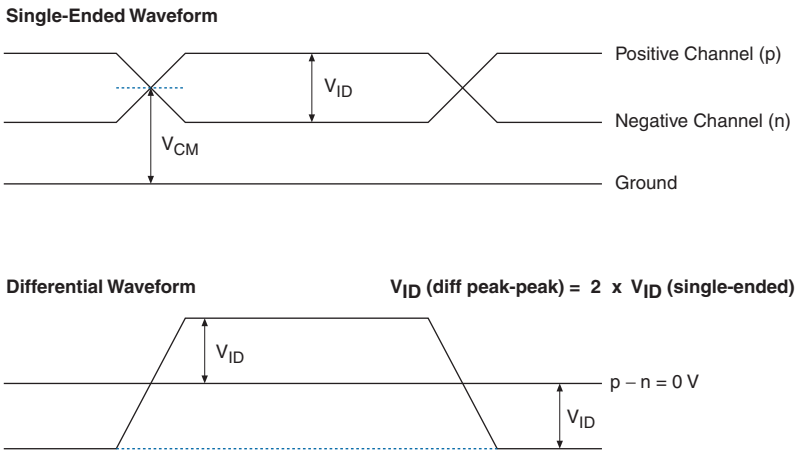


Figure 4–4. Transmitter Output Waveform

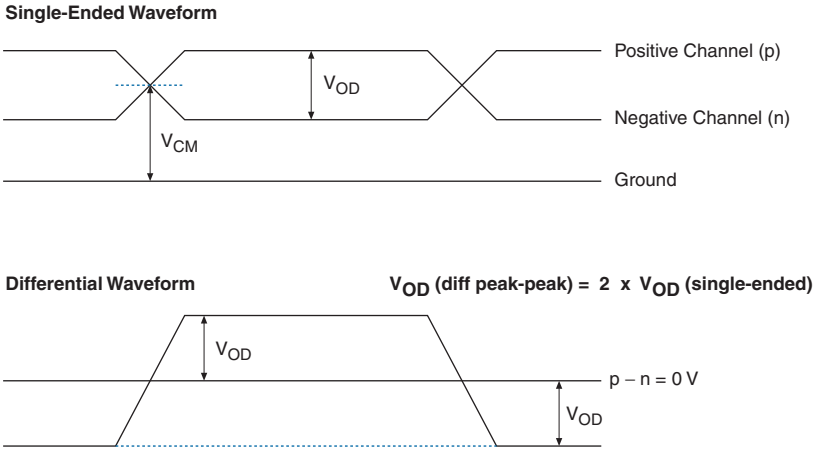
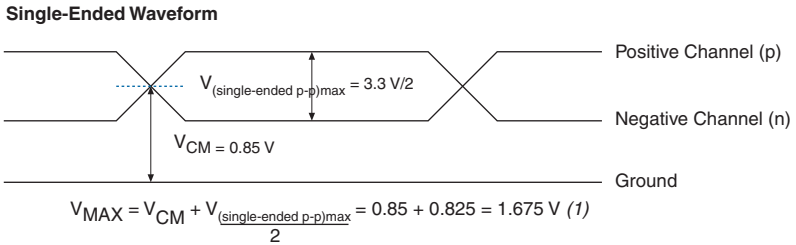


Figure 4–5. Maximum Receiver Input Pin Voltage



Note to Figure 4–5:
(1) The absolute V_{MAX} that the receiver input pins can tolerate is 2 V.

Tables 4–7 through 4–12 show the typical V_{OD} for data rates from 600 Mbps to 6.375 Gbps. The specification is for measurement at the package ball.

Table 4–7. Typical V_{OD} Setting, TX Term = 100 Ω Note (1)

V_{CCH} TX = 1.5 V	V_{OD} Setting (mV)						
	200	400	600	800	1000	1200	1400
V_{OD} Typical (mV)	220	430	625	830	1020	1200	1350

Note to Table 4–7:
(1) Applicable to data rates from 600 Mbps to 6.375 Gbps. Specification is for measurement at the package ball.

Table 4–8. Typical V_{OD} Setting, TX Term = 120 Ω Note (1)					
V_{CCH} TX = 1.5 V	**V_{OD} Setting (mV)**				
	240	**480**	**720**	**960**	**1200**
V_{OD} Typical (mV)	260	510	750	975	1200

Note to Table 4–8:
(1) Applicable to data rates from 600 Mbps to 6.375 Gbps. Specification is for measurement at the package ball.

Table 4–9. Typical V_{OD} Setting, TX Term = 150 Ω Note (1)				
V_{CCH} TX = 1.5 V	**V_{OD} Setting (mV)**			
	300	**600**	**900**	**1200**
V_{OD} Typical (mV)	325	625	920	1200

Note to Table 4–9:
(1) Applicable to data rates from 600 Mbps to 6.375 Gbps. Specification is for measurement at the package ball.

Table 4–10. Typical V_{OD} Setting, TX Term = 100 Ω Note (1)					
V_{CCH} TX = 1.2 V	**V_{OD} Setting (mV)**				
	320	**480**	**640**	**800**	**960**
V_{OD} Typical (mV)	344	500	664	816	960

Note to Table 4–10:
(1) Applicable to data rates from 600 Mbps to 3.125 Gbps. Specification is for measurement at the package ball.

Table 4–11. Typical V_{OD} Setting, TX Term = 120 Ω Note (1)					
V_{CCH} TX = 1.2 V	V_{OD} Setting (mV)				
	192	384	576	768	960
V_{OD} Typical (mV)	210	410	600	780	960

Note to Table 4–11:
(1) Applicable to data rates from 600 Mbps to 3.125 Gbps. Specification is for measurement at the package ball.

Table 4–12. Typical V_{OD} Setting, TX Term = 150 Ω Note (1)				
V_{CCH} TX = 1.2 V	V_{OD} Setting (mV)			
	240	480	720	960
V_{OD} Typical (mV)	260	500	730	960

Note to Table 4–12:
(1) Applicable to data rates from 600 Mbps to 3.125 Gbps. Specification is for measurement at the package ball.

Tables 4–13 through 4–18 show the typical first post-tap pre-emphasis.

Table 4–13. Typical Pre-Emphasis (First Post-Tap), Note (1) (Part 1 of 2)												
V_{CCH} TX = 1.5 V	First Post Tap Pre-Emphasis Level											
V_{OD} Setting (mV)	1	2	3	4	5	6	7	8	9	10	11	12
	TX Term = 100 Ω											
400	24%	62%	112%	184%								
600		31%	56%	86%	122%	168%	230%	329%	457%			
800		20%	35%	53%	73%	96%	123%	156%	196%	237%	312%	387%
1000			23%	36%	49%	64%	79%	97%	118%	141%	165%	200%
1200			17%	25%	35%	45%	56%	68%	82%	95%	110%	125%

Table 4–13. Typical Pre-Emphasis (First Post-Tap), Note (1) (Part 2 of 2)

V_{CCH} TX = 1.5 V	First Post Tap Pre-Emphasis Level											
V_{OD} Setting (mV)	1	2	3	4	5	6	7	8	9	10	11	12
1400				20%	26%	33%	41%	51%	58%	67%	77%	86%

Note to Table 4–13:
(1) Applicable to data rates from 600 Mbps to 6.375 Gbps. Specification is for measurement at the package ball.

Table 4–14. Typical Pre-Emphasis (First Post-Tap), Note (1)

V_{CCH} TX = 1.5 V	First Post Tap Pre-Emphasis Level											
V_{OD} Setting (mV)	1	2	3	4	5	6	7	8	9	10	11	12
	TX Term = 120 Ω											
240	45%											
480		41%	76%	114%	166%	257%	355%					
720		23%	38%	55%	84%	108%	137%	179%	226%	280%	405%	477%
960		15%	24%	36%	47%	64%	80%	97%	122%	140%	170%	196%
1200			18%	22%	30%	41%	51%	63%	77%	86%	98%	116%

Note to Table 4–14:
(1) Applicable to data rates from 600 Mbps to 6.375 Gbps. Specification is for measurement at the package ball.

Table 4–15. Typical Pre-Emphasis (First Post-Tap), Note (1) (Part 1 of 2)

V_{CCH} TX = 1.5 V	First Post Tap Pre-Emphasis Level											
V_{OD} Setting (mV)	1	2	3	4	5	6	7	8	9	10	11	12
	TX Term = 150 Ω											
300	32%	85%										

Table 4–15. Typical Pre-Emphasis (First Post-Tap), Note (1) (Part 2 of 2)

V_{CCH} TX = 1.5 V	First Post Tap Pre-Emphasis Level											
V_{OD} Setting (mV)	1	2	3	4	5	6	7	8	9	10	11	12
600		33%	53%	80%	115%	157%	195%	294%	386%			
900		19%	28%	38%	56%	70%	86%	113%	133%	168%	196%	242%
1200			17%	22%	31%	40%	52%	62%	75%	86%	96%	112%

Note to Table 4–15:
(1) Applicable to data rates from 600 Mbps to 6.375 Gbps. Specification is for measurement at the package ball.

Table 4–16. Typical Pre-Emphasis (First Post-Tap), Note (1)

V_{CCH} TX = 1.2 V	First Post Tap Pre-Emphasis Level											
V_{OD} Setting (mV)	1	2	3	4	5	6	7	8	9	10	11	12
	TX Term = 100 Ω											
320	24%	61%	114%									
480		31%	55%	86%	121%	170%	232%	333%				
640		20%	35%	54%	72%	95%	124%	157%	195%	233%	307%	373%
800			23%	36%	49%	64%	81%	97%	117%	140%	161%	195%
960			18%	25%	35%	44%	57%	69%	82%	94%	108%	127%

Note to Table 4–16:
(1) Applicable to data rates from 600 Mbps to 3.125 Gbps. Specification is for measurement at the package ball.

Table 4–17. Typical Pre-Emphasis (First Post-Tap), Note (1)

V_{CCH} TX = 1.2 V	First Post Tap Pre-Emphasis Level											
V_{OD} Setting (mV)	1	2	3	4	5	6	7	8	9	10	11	12
	TX Term = 120 Ω											
192	45%											
384		41%	76%	114%	166%	257%	355%					
576		23%	38%	55%	84%	108%	137%	179%	226%	280%	405%	477%
768		15%	24%	36%	47%	64%	80%	97%	122%	140%	170%	196%
960			18%	22%	30%	41%	51%	63%	77%	86%	98%	116%

Note to Table 4–17:
(1) Applicable to data rates from 600 Mbps to 3.125 Gbps. Specification is for measurement at the package ball.

Table 4–18. Typical Pre-Emphasis (First Post-Tap), Note (1)

V_{CCH} TX = 1.2 V	First Post Tap Pre-Emphasis Level											
V_{OD} Setting (mV)	1	2	3	4	5	6	7	8	9	10	11	12
	TX Term = 150 Ω											
240	31%	85%										
480		32%	52%	78%	112%	152%	195%	275%				
720		19%	28%	37%	56%	68%	86%	108%	133%	169%	194%	239%
960			17%	22%	30%	39%	51%	59%	75%	85%	94%	109%

Note to Table 4–18:
(1) Applicable to data rates from 600 Mbps to 3.125 Gbps. Specification is for measurement at the package ball.

Table 4–19 shows the Stratix II GX transceiver block AC specifications.

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 1 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SONET/SDH Transmit Jitter Generation *(7)*											
Peak-to-peak jitter at 622.08 Mbps	REFCLK = 77.76 MHz Pattern = PRBS23 V_{OD} = 800 mV No Pre-emphasis	-	-	0.1	-	-	0.1	-	-	0.1	UI
RMS jitter at 622.08 Mbps	REFCLK = 77.76 MHz Pattern = PRBS23 V_{OD} = 800 mV No Pre-emphasis	-	-	0.01	-	-	0.01	-	-	0.01	UI
Peak-to-peak jitter at 2488.32 Mbps	REFCLK = 155.52 MHz Pattern = PRBS23 V_{OD} = 800 mV No Pre-emphasis	-	-	0.1	-	-	0.1	-	-	0.1	UI
RMS jitter at 2488.32 Mbps	REFCLK = 155.52 MHz Pattern = PRBS23 V_{OD} = 800 mV No Pre-emphasis	-	-	0.01	-	-	0.01	-	-	0.01	UI

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 2 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SONET/SDH Receiver Jitter Tolerance *(7)*											
Jitter tolerance at 622.08 Mbps	Jitter frequency = 0.03 KHz Pattern = PRBS23 No Equalization DC Gain = 0 dB		> 15			> 15			> 15		UI
	Jitter frequency = 25 KHZ Pattern = PRBS23 No Equalization DC Gain = 0 dB		> 1.5			> 1.5			> 1.5		UI
	Jitter frequency = 250 KHz Pattern = PRBS23 No Equalization DC Gain = 0 dB		> 0.15			> 0.15			> 0.15		UI
Jitter tolerance at 2488.32 MBps	Jitter frequency = 0.06 KHz Pattern = PRBS23 No Equalization DC Gain = 0 dB		> 15			> 15			> 15		UI
	Jitter frequency = 100 KHZ Pattern = PRBS23 No Equalization DC Gain = 0 dB		> 1.5			> 1.5			> 1.5		UI
	Jitter frequency = 1 MHz Pattern = PRBS23 No Equalization DC Gain = 0 dB		> 0.15			> 0.15			> 0.15		UI
	Jitter frequency = 10 MHz Pattern = PRBS23 No Equalization DC Gain = 0 dB		> 0.15			> 0.15			> 0.15		UI

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 3 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Fibre Channel Transmit Jitter Generation *(8), (17)*											
Total jitter FC-1	REFCLK = 106.25 MHz Pattern = CRPAT V_{OD} = 800 mV No Pre-emphasis	-	-	0.23	-	-	0.23	-	-	0.23	UI
Deterministic jitter FC-1	REFCLK = 106.25 MHz Pattern = CRPAT V_{OD} = 800 mV No Pre-emphasis	-	-	0.11	-	-	0.11	-	-	0.11	UI
Total jitter FC-2	REFCLK = 106.25 MHz Pattern = CRPAT V_{OD} = 800 mV No Pre-emphasis	-	-	0.33	-	-	0.33	-	-	0.33	UI
Deterministic jitter FC-2	REFCLK = 106.25 MHz Pattern = CRPAT V_{OD} = 800 mV No Pre-emphasis	-	-	0.2	-	-	0.2	-	-	0.2	UI
Total jitter FC-4	REFCLK = 106.25 MHz Pattern = CRPAT V_{OD} = 800 mV No Pre-emphasis	-	-	0.52	-	-	0.52	-	-	0.52	UI
Deterministic jitter FC-4	REFCLK = 106.25 MHz Pattern = CRPAT V_{OD} = 800 mV No Pre-emphasis	-	-	0.33	-	-	0.33	-	-	0.33	UI
Fibre Channel Receiver Jitter Tolerance *(8), (18)*											
Deterministic jitter FC-1	Pattern = CJTPAT No Equalization DC Gain = 0 dB	> 0.37			> 0.37			> 0.37			UI
Random jitter FC-1	Pattern = CJTPAT No Equalization DC Gain = 0 dB	> 0.31			> 0.31			> 0.31			UI

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 4 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Sinusoidal jitter FC-1	Fc/25000	> 1.5			> 1.5			> 1.5			UI
	Fc/1667	> 0.1			> 0.1			> 0.1			UI
Deterministic jitter FC-2	Pattern = CJTPAT No Equalization DC Gain = 0 dB	> 0.33			> 0.33			> 0.33			UI
Random jitter FC-2	Pattern = CJTPAT No Equalization DC Gain = 0 dB	> 0.29			> 0.29			> 0.29			UI
Sinusoidal jitter FC-2	Fc/25000	> 1.5			> 1.5			> 1.5			UI
	Fc/1667	> 0.1			> 0.1			> 0.1			UI
Deterministic jitter FC-4	Pattern = CJTPAT No Equalization DC Gain = 0 dB	> 0.33			> 0.33			> 0.33			UI
Random jitter FC-4	Pattern = CJTPAT No Equalization DC Gain = 0 dB	> 0.29			> 0.29			> 0.29			UI
Sinusoidal jitter FC-4	Fc/25000	> 1.5			> 1.5			> 1.5			UI
	Fc/1667	> 0.1			> 0.1			> 0.1			UI
XAUI Transmit Jitter Generation *(9)*											
Total jitter at 3.125 Gbps	REFCLK = 156.25 MHz Pattern = CJPAT V_{OD} = 1200 mV No Pre-emphasis	-	-	0.3	-	-	0.3	-	-	0.3	UI
Deterministic jitter at 3.125 Gbps	REFCLK = 156.25 MHz Pattern = CJPAT V_{OD} = 1200 mV No Pre-emphasis	-	-	0.17	-	-	0.17	-	-	0.17	UI
XAUI Receiver Jitter Tolerance *(9)*											
Total jitter	Pattern = CJPAT No Equalization DC Gain = 3 dB	> 0.65			> 0.65			> 0.65			UI
Deterministic jitter	Pattern = CJPAT No Equalization DC Gain = 3 dB	> 0.37			> 0.37			> 0.37			UI

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 5 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Peak-to-peak jitter	Jitter frequency = 22.1 KHz		> 8.5			> 8.5			> 8.5		UI
Peak-to-peak jitter	Jitter frequency = 1.875 MHz		> 0.1			> 0.1			> 0.1		UI
Peak-to-peak jitter	Jitter frequency = 20 MHz		> 0.1			> 0.1			> 0.1		UI
PCI Express Transmit Jitter Generation *(10)*											
Total jitter at 2.5 Gbps	Compliance pattern V_{OD} = 800 mV Pre-emphasis (1st post-tap) = Setting 5	-	-	0.25	-	-	0.25	-	-	0.25	UI
PCI Express Receiver Jitter Tolerance *(10)*											
Total jitter at 2.5 Gbps	Compliance pattern No Equalization DC gain = 3 dB		> 0.6			> 0.6			> 0.6		UI
Serial RapidIO Transmit Jitter Generation *(11)*											
Deterministic Jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps REFCLK = 125 MHz Pattern = CJPAT V_{OD} = 800 mV No Pre-emphasis	-	-	0.17	-	-	0.17	-	-	0.17	UI
Total Jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps REFCLK = 125 MHz Pattern = CJPAT V_{OD} = 800 mV No Pre-emphasis	-	-	0.35	-	-	0.35	-	-	0.35	UI

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 6 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Serial RapidIO Receiver Jitter Tolerance *(11)*											
Deterministic Jitter Tolerance (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps REFCLK = 125 MHz Pattern = CJPAT Equalizer Setting = 0 for 1.25 Gbps Equalizer Setting = 6 for 2.5 Gbps Equalizer Setting = 6 for 3.125 Gbps	> 0.37			> 0.37			> 0.37			UI
Combined Deterministic and Random Jitter Tolerance (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps REFCLK = 125 MHz Pattern = CJPAT Equalizer Setting = 0 for 1.25 Gbps Equalizer Setting = 6 for 2.5 Gbps Equalizer Setting = 6 for 3.125 Gbps	> 0.55			> 0.55			> 0.55			UI

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 7 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Sinusoidal Jitter Tolerance (peak-to-peak)	Jitter Frequency = 22.1 KHz Data Rate = 1.25, 2.5, 3.125 Gbps REFCLK = 125 MHz Pattern = CJPAT Equalizer Setting = 0 for 1.25 Gbps Equalizer Setting = 6 for 2.5 Gbps Equalizer Setting = 6 for 3.125 Gbps		> 8.5			> 8.5			> 8.5		UI
	Jitter Frequency = 1.875 MHz Data Rate = 1.25, 2.5, 3.125 Gbps REFCLK = 125 MHz Pattern = CJPAT Equalizer Setting = 0 for 1.25 Gbps Equalizer Setting = 6 for 2.5 Gbps Equalizer Setting = 6 for 3.125 Gbps		> 0.1			> 0.1			> 0.1		UI
	Jitter Frequency = 20 MHz Data Rate = 1.25, 2.5, 3.125 Gbps REFCLK = 125 MHz Pattern = CJPAT Equalizer Setting = 0 for 1.25 Gbps Equalizer Setting = 6 for 2.5 Gbps Equalizer Setting = 6 for 3.125 Gbps		> 0.1			> 0.1			> 0.1		UI

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 8 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
GIGE Transmit Jitter Generation *(12)*											
Deterministic Jitter (peak-to-peak)	Data Rate = 1.25 Gbps REFCLK = 125 MHz Pattern = CRPAT V_{OD} = 1400 mV No Pre-emphasis	-	-	0.14	-	-	0.14	-	-	0.14	UI
Total Jitter (peak-to-peak)	Data Rate = 1.25 Gbps REFCLK = 125 MHz Pattern = CRPAT V_{OD} = 1400 mV No Pre-emphasis	-	-	0.279	-	-	0.279	-	-	0.279	UI
GIGE Receiver Jitter Tolerance *(12)*											
Deterministic Jitter Tolerance (peak-to-peak)	Data Rate = 1.25 Gbps REFCLK = 125 MHz Pattern = CJPAT No Equalization	> 0.4			> 0.4			> 0.4			UI
Combined Deterministic and Random Jitter Tolerance (peak-to-peak)	Data Rate = 1.25 Gbps REFCLK = 125 MHz Pattern = CJPAT No Equalization	> 0.66			> 0.66			> 0.66			UI
HiGig Transmit Jitter Generation *(4), (13)*											
Deterministic Jitter (peak-to-peak)	Data Rate = 3.75 Gbps REFCLK = 187.5 MHz Pattern = CJPAT V_{OD} = 1200 mV No Pre-emphasis	-	-	0.17	-						UI
Total Jitter (peak-to-peak)	Data Rate = 3.75 Gbps REFCLK = 187.5 MHz Pattern = CJPAT V_{OD} = 1200 mV No Pre-emphasis	-	-	0.35	-						UI

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 9 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
HiGig Receiver Jitter Tolerance *(13)*											
Deterministic Jitter Tolerance (peak-to-peak)	Data Rate = 3.75 Gbps REFCLK = 187.5 MHz Pattern = CJPAT No Equalization DC Gain = 3 dB		> 0.37			-			-		UI
Combined Deterministic and Random Jitter Tolerance (peak-to-peak)	Data Rate = 3.75 Gbps REFCLK = 187.5 MHz Pattern = CJPAT No Equalization DC Gain = 3 dB		> 0.65			-			-		UI
	Jitter Frequency = 22.1 KHz Data Rate = 3.75 Gbps REFCLK = 187.5 MHz Pattern = CJPAT No Equalization DC Gain = 3 dB		> 8.5			-			-		UI

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 10 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Sinusoidal Jitter Tolerance (peak-to-peak)	Jitter Frequency = 1.875 MHz Data Rate = 3.75 Gbps REFCLK = 187.5 MHz Pattern = CJPAT No Equalization DC Gain = 3 dB	> 0.1			-			-			UI
	Jitter Frequency = 20 MHz Data Rate = 3.75 Gbps REFCLK = 187.5 MHz Pattern = CJPAT No Equalization DC Gain = 3 dB	> 0.1			-			-			UI
(OIF) CEI Transmitter Jitter Generation *(14)*											
Total Jitter (peak-to-peak)	Data Rate = 6.375 Gbps REFCLK = 318.75 MHz Pattern = PRBS15 Vod=1000 mV *(5)* No Pre-emphasis BER = 10^{-12}			0.3			N/A			N/A	UI
(OIF) CEI Receiver Jitter Tolerance *(14)*											
Deterministic Jitter Tolerance (peak-to-peak)	Data Rate = 6.375 Gbps Pattern = PRBS31 Equalizer Setting = 15 DC Gain = 0 dB BER = 10^{-12}	> 0.675			N/A			N/A			UI

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 11 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Combined Deterministic and Random Jitter Tolerance (peak-to-peak)	Data Rate = 6.375 Gbps Pattern = PRBS31 Equalizer Setting = 15 DC Gain = 0 dB BER = 10^{-12}	> 0.988			N/A			N/A			UI
Sinusoidal Jitter Tolerance (peak-to-peak)	Jitter Frequency = 38.2 KHz Data Rate = 6.375 Gbps Pattern = PRBS31 Equalizer Setting = 15 DC Gain = 0 dB BER = 10^{-12}	> 5			N/A			N/A			UI
	Jitter Frequency = 3.82 MHz Data Rate=6.375 Gbps Pattern = PRBS31 Equalizer Setting = 15 DC Gain = 0 dB BER = 10^{-12}	> 0.05			N/A			N/A			UI
	Jitter Frequency = 20 MHz Data Rate = 6.375 Gbps Pattern = PRBS31 Equalizer Setting = 15 DC Gain = 0 dB BER = 10^{-12}	> 0.05			N/A			N/A			UI

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 12 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
CPRI Transmitter Jitter Generation *(15)*											
Deterministic Jitter (peak-to-peak)	Data Rate = 614.4 Mbps, 1.2288 Gbps, 2.4576 Gbps REFCLK = 61.44 MHz for 614.4 Mbps and 1.2288 Gbps REFCLK = 122.88 MHz for 2.4576 Gbps Pattern = CJPAT Vod = 1400 mV No Pre-emphasis			0.14			0.14			N/A	UI
Total Jitter (peak-to-peak)	Data Rate = 614.4 Mbps, 1.2288 Gbps, 2.4576 Gbps REFCLK = 61.44 MHz for 614.4 Mbps and 1.2288 Gbps REFCLK = 122.88 MHz for 2.4576 Gbps Pattern = CJPAT Vod = 1400 mV No Pre-emphasis			0.279			0.279			N/A	UI

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 13 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
CPRI Receiver Jitter Tolerance *(15)*											
Deterministic Jitter Tolerance (peak-to-peak)	Data Rate = 614.4 Mbps, 1.2288 Gbps, 2.4576 Gbps REFCLK = 61.44 MHz for 614.4 Mbps REFCLK = 122.88 MHz for 1.2288 Gbps and 2.4576 Gbps Pattern = CJPAT Equalizer Setting = 6 DC Gain = 0 dB		> 0.4			> 0.4			N/A		UI
Combined Deterministic and Random Jitter Tolerance (peak-to-peak)	Data Rate = 614.4 Mbps, 1.2288 Gbps, 2.4576 Gbps REFCLK = 61.44 MHz for 614.4 Mbps REFCLK = 122.88 MHz for 1.2288 Gbps and 2.4576 Gbps Pattern = CJPAT Equalizer Setting = 6 DC Gain = 0 dB		> 0.66			> 0.66			N/A		UI

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 14 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Sinusoidal Jitter Tolerance (peak-to-peak) *(6)*	Jitter Frequency = 22.1 KHz Data Rate = 614.4 Mbps, 1.2288 Gbps, 2.4576 Gbps REFCLK = 61.44 MHz for 614.4 Mbps REFCLK = 122.88 MHz for 1.2288 Gbps and 2.4576 Gbps Pattern = CJPAT Equalizer Setting = 6 DC Gain = 0 dB		> 8.5			> 8.5			N/A		UI
	Jitter Frequency = 1.875 MHz Data Rate = 614.4 Mbps, 1.2288 Gbps, 2.4576 Gbps REFCLK = 61.44 MHz for 614.4 Mbps REFCLK = 122.88 MHz for 1.2288 Gbps and 2.4576 Gbps Pattern = CJPAT Equalizer Setting = 6 DC Gain = 0 dB		> 0.1			> 0.1			N/A		UI

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 15 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Sinusoidal Jitter Tolerance (peak-to-peak) *(6)* (cont.)	Jitter Frequency = 20 MHz Data Rate = 614.4 Mbps, 1.2288 Gbps, 2.4576 Gbps REFCLK = 61.44 MHz for 614.4 Mbps REFCLK = 122.88 MHz for 1.2288 Gbps and 2.4576 Gbps Pattern = CJPAT Equalizer Setting = 6 DC Gain = 0 dB	> 0.1			> 0.1			N/A			UI

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 16 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SDI Transmitter Jitter Generation *(16)*											
Alignment Jitter (peak-to-peak)	Data Rate = 1.485 Gbps (HD) REFCLK = 74.25 MHz Pattern = ColorBar Vod = 800 mV No Pre-emphasis Low-Frequency Roll-Off = 100 KHz		0.2			0.2			0.2		UI
	Data Rate = 2.97 Gbps (3G) REFCLK = 148.5 MHz Pattern = ColorBar Vod = 800 mV No Pre-emphasis Low-Frequency Roll-Off = 100 KHz		0.3			0.3			0.3		UI

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 17 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SDI Receiver Jitter Tolerance *(16)*											
Sinusoidal Jitter Tolerance (peak-to-peak)	Jitter Frequency = 15 KHz Data Rate = 2.97 Gbps (3G) REFCLK = 148.5 MHz Pattern = Single Line Scramble Color Bar No Equalization DC Gain = 0 dB		> 2			> 2			> 2		UI
	Jitter Frequency = 100 KHz Data Rate = 2.97 Gbps (3G) REFCLK = 148.5 MHz Pattern = Single Line Scramble Color Bar No Equalization DC Gain = 0 dB		> 0.3			> 0.3			> 0.3		UI
	Jitter Frequency = 148.5 MHz Data Rate = 2.97 Gbps (3G) REFCLK = 148.5 MHz Pattern = Single Line Scramble Color Bar No Equalization DC Gain = 0 dB		> 0.3			> 0.3			> 0.3		UI

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 18 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Sinusoidal Jitter Tolerance (peak-to-peak)	Jitter Frequency = 20 KHz Data Rate = 1.485 Gbps (HD) REFCLK = 74.25 MHz Pattern = 75% Color Bar No Equalization DC Gain = 0 dB		> 1			> 1			> 1		UI
	Jitter Frequency = 100 KHz Data Rate = 1.485 Gbps (HD) REFCLK = 74.25 MHz Pattern = 75% Color Bar No Equalization DC Gain = 0 dB		> 0.2			> 0.2			> 0.2		UI
	Jitter Frequency = 148.5 MHz Data Rate = 1.485 Gbps (HD) REFCLK = 74.25 MHz Pattern = 75% Color Bar No Equalization DC Gain = 0 dB		> 0.2			> 0.2			> 0.2		UI

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 19 of 19)											
Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	

Notes to Table 4–19:

(1) Dedicated REFCLK pins were used to drive the input reference clocks.
(2) Jitter numbers specified are valid for the stated conditions only.
(3) Refer to the protocol characterization documents for detailed information.
(4) HiGig configuration is available in a -3 speed grade only. For more information, refer to the *Stratix II GX Transceiver Architecture Overview* chapter in volume 2 of the *Stratix II GX Device Handbook*.
(5) Stratix II GX transceivers meet CEI jitter generation specification of 0.3 UI for a V_{OD} range of 400 mV to 1000 mV.
(6) The Sinusoidal Jitter Tolerance Mask is defined only for low voltage (LV) variant of CPRI.
(7) The jitter numbers for SONET/SDH are compliant to the GR-253-CORE Issue 3 Specification.
(8) The jitter numbers for Fibre Channel are compliant to the FC-PI-4 Specification revision 6.10.
(9) The jitter numbers for XAUI are compliant to the IEEE802.3ae-2002 Specification.
(10) The jitter numbers for PCI Express are compliant to the PCIe Base Specification 2.0.
(11) The jitter numbers for Serial RapidIO are compliant to the RapidIO Specification 1.3.
(12) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.
(13) The jitter numbers for HiGig are compliant to the IEEE802.3ae-2002 Specification.
(14) The jitter numbers for (OIF) CEI are compliant to the OIF-CEI-02.0 Specification.
(15) The jitter numbers for CPRI are compliant to the CPRI Specification V2.1.
(16) The HD-SDI and 3G-SDI jitter numbers are compliant to the SMPTE292M and SMPTE424M Specifications.
(17) The Fibre Channel transmitter jitter generation numbers are compliant to the specification at β_T interoperability point.
(18) The Fibre Channel receiver jitter tolerance numbers are compliant to the specification at β_R interoperability point.

Table 4–20 provides information on recommended input clock jitter for each mode.

Table 4–20. Recommended Input Clock Jitter (Part 1 of 2)						
Mode	Reference Clock (MHz)	Vectron LVPECL XO Type/Model	Frequency Range (MHz)	RMS Jitter (12 kHz to 20 MHz) (ps)	Period Jitter (Peak to Peak) (ps)	Phase Noise at 1 MHz (dB c/Hz)
PCI-E	100	VCC6-Q/R	10 to 270	0.3	23	-149.9957
(OIF) CEI PHY	156.25	VCC6-Q/R	10 to 270	0.3	23	-146.2169
	622.08	VCC6-Q	270 to 800	2	30	Not available
GIGE	62.5	VCC6-Q/R	10 to 270	0.3	23	-149.9957
	125	VCC6-Q/R	10 to 270	0.3	23	-146.9957
XAUI	156.25	VCC6-Q/R	10 to 270	0.3	23	-146.2169

Table 4–20. Recommended Input Clock Jitter (Part 2 of 2)

Mode	Reference Clock (MHz)	Vectron LVPECL XO Type/Model	Frequency Range (MHz)	RMS Jitter (12 kHz to 20 MHz) (ps)	Period Jitter (Peak to Peak) (ps)	Phase Noise at 1 MHz (dB c/Hz)
SONET/SDH OC-48	77.76	VCC6-Q/R	10 to 270	0.3	23	-149.5476
	155.52	VCC6-Q/R	10 to 270	0.3	23	-149.1903
	311.04	VCC6-Q	270 to 800	2	30	Not available
	622.08	VCC6-Q	270 to 800	2	30	Not available
SONET/SDH OC-12	62.2	VCC6-Q/R	10 to 270	0.3	23	-149.6289
	311	VCC6-Q	270 to 800	2	30	Not available
	77.76	VCC6-Q/R	10 to 270	0.3	23	-149.5476
	155.52	VCC6-Q/R	10 to 270	0.3	23	-149.1903
	622.08	VCC6-Q	270 to 800	2	30	Not available

Tables 4–21 and 4–22 show the transmitter and receiver PCS latency for each mode, respectively.

Table 4–21. PCS Latency (Part 1 of 2) *Note (1)*

Functional Mode	Configuration	Transmitter PCS Latency					
		TX PIPE	TX Phase Comp FIFO	Byte Serializer	TX State Machine	8B/10B Encoder	Sum *(2)*
XAUI		-	2-3	1	0.5	0.5	4-5
PIPE	×1, ×4, ×8 8-bit channel width	1	3-4	1	-	1	6-7
	×1, ×4, ×8 16-bit channel width	1	3-4	1	-	0.5	6-7
GIGE		-	2-3	1	-	1	4-5
SONET/SDH	OC-12	-	2-3	1	-	1	4-5
	OC-48	-	2-3	1	-	0.5	4-5
	OC-96	-	2-3	1	-	0.5	4-5
(OIF) CEI PHY		-	2-3	1	-	0.5	4-5
CPRI *(3)*	614 Mbps, 1.228 Gbps	-	2	1	-	1	4
	2.456 Gbps	-	2-3	1	-	1	4-5

Table 4–21. PCS Latency (Part 2 of 2) Note (1)

Functional Mode	Configuration	Transmitter PCS Latency					
		TX PIPE	TX Phase Comp FIFO	Byte Serializer	TX State Machine	8B/10B Encoder	Sum (2)
Serial RapidIO	1.25 Gbps, 2.5 Gbps, 3.125 Gbps	-	2-3	1	-	0.5	4-5
SDI	HD 10-bit channel width	-	2-3	1	-	1	4-5
	HD, 3G 20-bit channel width	-	2-3	1	-	0.5	4-5
BASIC Single Width	8-bit/10-bit channel width	-	2-3	1	-	1	4-5
	16-bit/20-bit channel width	-	2-3	1	-	0.5	4-5
BASIC Double Width	16-bit/20-bit channel width	-	2-3	1	-	1	4-5
	32-bit/40-bit channel width	-	2-3	1	-	0.5	4-5
	Parallel Loopback/ BIST	-	2-3	1	-	1	4-5

Notes to Table 4–21:

(1) The latency numbers are with respect to the PLD-transceiver interface clock cycles.

(2) The total latency number is rounded off in the Sum column.

(3) For CPRI 614 Mbps and 1.228 Gbps data rates, the Quartus II software customizes the PLD-transceiver interface clocking to achieve zero clock cycle uncertainty in the transmitter phase compensation FIFO latency. For more details, refer to the *CPRI Mode* section in the *Stratix II GX Transceiver Architecture Overview* chapter in volume 2 of the *Stratix II GX Device Handbook*.

Table 4–22. PCS Latency (Part 1 of 3) *Note (1)*

Functional Mode	Configuration	Receiver PCS Latency									
		Word Aligner	Deskew FIFO	Rate Matcher *(3)*	8B/10B Decoder	Receiver State Machine	Byte De-serializer	Byte Order	Receiver Phase Comp FIFO	Receiver PIPE	Sum *(2)*
XAUI		2-2.5	2-2.5	5.5-6.5	0.5	1	1	1	1-2	-	14-17
PIPE	×1, ×4, ×8 8-bit channel width	4-5	-	11-13	1	-	1	1	2-3	1	21-25
	×1, ×4, ×8 16-bit channel width	2-2.5	-	5.5-6.5	0.5	-	1	1	2-3	1	13-16
GIGE		4-5	-	11-13	1	-	1	1	1-2	-	19-23
SONET/ SDH	OC-12	6-7	-	-	1	-	1	1	1-2	-	10-12
	OC-48	3-3.5	-	-	0.5	-	1	1-2	1-2	-	7-9
	OC-96	2-2.5	-	-	0.5	-	1	1	1-2	-	6-7
(OIF) CEI PHY		2.5	-	-	0.5	-	1	1	1-2	-	6-7
CPRI *(4)*	614 Mbps, 1.228 Gbps	4-5	-	-	1	-	1	1	1	-	8-9
	2.456 Gbps	4-5	-	-	1	-	1	1	1-2	-	8-10
Serial RapidIO	1.25 Gbps, 2.5 Gbps, 3.125 Gbps	2-2.5	-	-	0.5	-	1	1	1-2	-	6-7
SDI	HD 10-bit channel width	5	-	-	1	-	1	1	1-2	-	9-10
	HD, 3G 20-bit channel width	2.5	-	-	0.5	-	1	1	1-2	-	6-7

Table 4–22. PCS Latency (Part 2 of 3) Note (1)

Functional Mode	Configuration	Receiver PCS Latency									
		Word Aligner	Deskew FIFO	Rate Matcher (3)	8B/10B Decoder	Receiver State Machine	Byte De-serializer	Byte Order	Receiver Phase Comp FIFO	Receiver PIPE	Sum (2)
BASIC Single Width	8/10-bit channel width; with Rate Matcher	4-5	-	11-13	1	-	1	1	1-2	1	19-23
	8/10-bit channel width; without Rate Matcher	4-5	-	-	1	-	1	1	1-2	-	8-10
	16/20-bit channel width; with Rate Matcher	2-2.5	-	5.5-6.5	0.5	-	1	1	1-2	-	11-14
	16/20-bit channel width; without Rate Matcher	2-2.5	-	-	0.5	-	1	1	1-2	-	6-7

Table 4–22. PCS Latency (Part 3 of 3) Note (1)

Functional Mode	Configuration	Receiver PCS Latency									
		Word Aligner	Deskew FIFO	Rate Matcher (3)	8B/10B Decoder	Receiver State Machine	Byte De-serializer	Byte Order	Receiver Phase Comp FIFO	Receiver PIPE	Sum (2)
BASIC Double Width	16/20-bit channel width; with Rate Matcher	4-5	-	11-13	1	-	1	1	1-2	-	19-23
	16/20-bit channel width; without Rate Matcher	4-5	-	-	1	-	1	1	1-2	-	8-10
	32/40-bit channel width; with Rate Matcher	2-2.5	-	5.5-6.5	0.5	-	1	1	1-2	-	11-14
	32/40-bit channel width; without Rate Matcher	2-2.5	-	-	0.5	-	1	1-3	1-2	-	6-9

Notes to Table 4–21:

(1) The latency numbers are with respect to the PLD-transceiver interface clock cycles.

(2) The total latency number is rounded off in the Sum column.

(3) The rate matcher latency shown is the steady state latency. Actual latency may vary depending on the skip ordered set gap allowed by the protocol, actual PPM difference between the reference clocks, and so forth.

(4) For CPRI 614 Mbps and 1.228 Gbps data rates, the Quartus II software customizes the PLD-transceiver interface clocking to achieve zero clock cycle uncertainty in the receiver phase compensation FIFO latency. For more details, refer to the *CPRI Mode* section in the *Stratix II GX Transceiver Architecture Overview* chapter in volume 2 of the *Stratix II GX Device Handbook*

DC Electrical Characteristics

Table 4–23 shows the Stratix II GX device family DC electrical characteristics.

Table 4–23. Stratix II GX Device DC Operating Conditions (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Device	Minimum	Typical	Maximum	Unit
I_I	Input pin leakage current	$V_I = V_{CCIOmax}$ to 0 V *(2)*	All	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIOmax}$ to 0 V *(2)*	All	–10		10	µA
I_{CCINT0}	V_{CCINT} supply current (standby)	V_I = ground, no load, no toggling inputs T_J = 25 °C	EP2SGX30		0.30	*(3)*	A
			EP2SGX60		0.50	*(3)*	A
			EP2SGX90		0.62	*(3)*	A
			EP2SGX130		0.82	*(3)*	A
I_{CCPD0}	V_{CCPD} supply current (standby)	V_I = ground, no load, no toggling inputs T_J = 25 °C, V_{CCPD} = 3.3V	EP2SGX30		2.7	*(3)*	mA
			EP2SGX60		3.6	*(3)*	mA
			EP2SGX90		4.3	*(3)*	mA
			EP2SGX130		5.4	*(3)*	mA
I_{CCIO0}	V_{CCIO} supply current (standby)	V_I = ground, no load, no toggling inputs T_J = 25 °C	EP2SGX30		4.0	*(3)*	mA
			EP2SGX60		4.0	*(3)*	mA
			EP2SGX90		4.0	*(3)*	mA
			EP2SGX130		4.0	*(3)*	mA

Table 4–23. Stratix II GX Device DC Operating Conditions (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Device	Minimum	Typical	Maximum	Unit
R_{CONF} *(4)*	Value of I/O pin pull-up resistor before and during configuration	Vi = 0, V_{CCIO} = 3.3 V		10	25	50	KOhm
		Vi = 0, V_{CCIO} = 2.5 V		15	35	70	KOhm
		Vi = 0, V_{CCIO} = 1.8 V		30	50	100	KOhm
		Vi = 0, V_{CCIO} = 1.5 V		40	75	150	KOhm
		Vi = 0, V_{CCIO} = 1.2 V		50	90	170	KOhm
	Recommended value of I/O pin external pull-down resistor before and during configuration				1	2	KOhm

Notes to Table 4–23:

(1) Typical values are for T_A = 25 °C, V_{CCINT} = 1.2 V, and V_{CCIO} = 1.5 V, 1.8 V, 2.5 V, and 3.3 V.

(2) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 2.5, 1.8, and 1.5 V).

(3) Maximum values depend on the actual TJ and design utilization. See *PowerPlay Early Power Estimator (EPE) and Power Analyzer* or the *Quartus II PowerPlay Power Analyzer and Optimization Technology* (available at **www.altera.com**) for maximum values. See the section "Power Consumption" on page 4–59 for more information.

(4) Pin pull-up resistance values will lower if an external source drives the pin higher than V_{CCIO}.

I/O Standard Specifications

Tables 4–24 through 4–47 show the Stratix II GX device family I/O standard specifications.

Table 4–24. LVTTL Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO} *(1)*	Output supply voltage		3.135	3.465	V
V_{IH}	High-level input voltage		1.7	4.0	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	High-level output voltage	I_{OH} = –4 mA *(2)*	2.4		V

Table 4–24. LVTTL Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{OL}	Low-level output voltage	I_{OL} = 4 mA *(2)*		0.45	V

Notes to Table 4–24:
(1) Stratix II GX devices comply to the narrow range for the supply voltage as specified in the EIA/JEDEC Standard, JESD8-B.
(2) This specification is supported across all the programmable drive strength settings available for this I/O standard as shown in the *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Table 4–25. LVCMOS Specifications Note (1)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO} *(1)*	Output supply voltage		3.135	3.465	V
V_{IH}	High-level input voltage		1.7	4.0	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	High-level output voltage	V_{CCIO} = 3.0, I_{OH} = –0.1 mA *(2)*	V_{CCIO} – 0.2		V
V_{OL}	Low-level output voltage	V_{CCIO} = 3.0, I_{OL} = 0.1 mA *(2)*		0.2	V

Notes to Table 4–25:
(1) Stratix II GX devices comply to the narrow range for the supply voltage as specified in the EIA/JEDEC Standard, JESD8-B.
(2) This specification is supported across all the programmable drive strength available for this I/O standard as shown in *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Table 4–26. 2.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO} *(1)*	Output supply voltage		2.375	2.625	V
V_{IH}	High-level input voltage		1.7	4.0	V
V_{IL}	Low-level input voltage		–0.3	0.7	V
V_{OH}	High-level output voltage	I_{OH} = –1 mA *(2)*	2.0		V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA *(2)*		0.4	V

Notes to Table 4–26:
(1) The Stratix II GX device V_{CCIO} voltage level support of 2.5 to 5% is narrower than defined in the Normal Range of the EIA/JEDEC standard.
(2) This specification is supported across all the programmable drive settings available for this I/O standard as shown in *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Table 4–27. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO} *(1)*	Output supply voltage		1.71	1.89	V
V_{IH}	High-level input voltage		0.65 × V_{CCIO}	2.25	V
V_{IL}	Low-level input voltage		–0.3	0.35 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OH} = –2 mA *(2)*	V_{CCIO} – 0.45		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA *(2)*		0.45	V

Notes to Table 4–27:

(1) The Stratix II GX device V_{CCIO} voltage level support of 1.8 to 5% is narrower than defined in the Normal Range of the EIA/JEDEC standard.

(2) This specification is supported across all the programmable drive settings available for this I/O standard as shown in *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Table 4–28. 1.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO} *(1)*	Output supply voltage		1.425	1.575	V
V_{IH}	High-level input voltage		0.65 V_{CCIO}	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.35 V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OH} = –2 mA *(2)*	0.75 V_{CCIO}		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA *(2)*		0.25 V_{CCIO}	V

Notes to Table 4–28:

(1) The Stratix II GX device V_{CCIO} voltage level support of 1.5 to 5% is narrower than defined in the Normal Range of the EIA/JEDEC standard.

(2) This specification is supported across all the programmable drive settings available for this I/O standard as shown in *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Figures 4–6 and 4–7 show receiver input and transmitter output waveforms, respectively, for all differential I/O standards (LVDS and LVPECL).

Figure 4–6. Receiver Input Waveforms for Differential I/O Standards

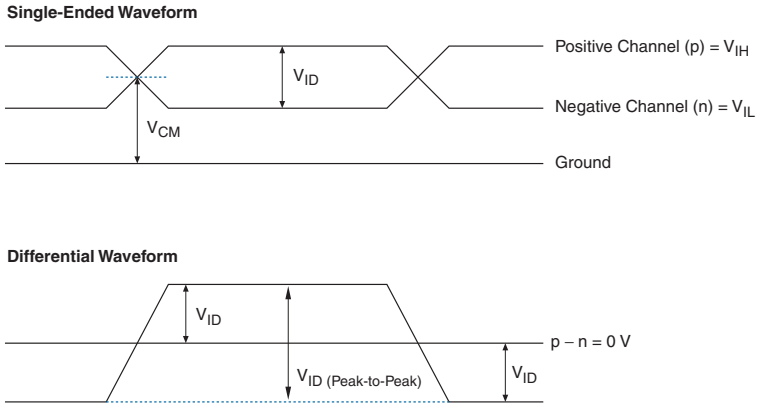


Figure 4–7. Transmitter Output Waveforms for Differential I/O Standards

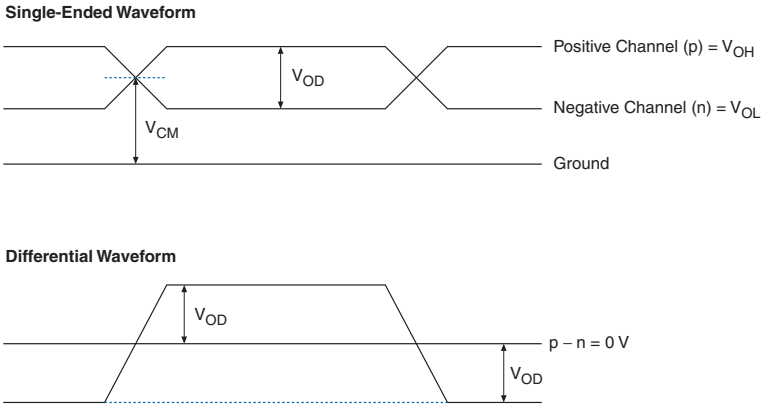


Table 4–29. 2.5-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage for left and right I/O banks (1, 2, 5, and 6)		2.375	2.5	2.625	V
V_{ID}	Input differential voltage swing (single-ended)		100	350	900	mV
V_{ICM}	Input common mode voltage		200	1,250	1,800	mV
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	250		450	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	1.125		1.375	V
R_L	Receiver differential input discrete resistor (external to Stratix II GX devices)		90	100	110	Ω

Table 4–30. 3.3-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO} *(1)*	I/O supply voltage for top and bottom PLL banks (9, 10, 11, and 12)		3.135	3.3	3.465	V
V_{ID}	Input differential voltage swing (single-ended)		100	350	900	mV
V_{ICM}	Input common mode voltage		200	1,250	1,800	mV
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	250		710	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	840		1,570	mV
R_L	Receiver differential input discrete resistor (external to Stratix II GX devices)		90	100	110	Ω

Note to Table 4–30:

(1) The top and bottom clock input differential buffers in I/O banks 3, 4, 7, and 8 are powered by V_{CCINT}, not V_{CCIO}. The PLL clock output/feedback differential buffers are powered by VCC_PLL_OUT. For differential clock output/feedback operation, connect VCC_PLL_OUT to 3.3 V.

Table 4–31. PCML Specifications *Note (1)*

Symbol	Parameter	References
Reference Clock		
3.3-V PCML 1.5-V PCML 1.2-V PCML	Reference clock supported PCML standards	
V_{ID}	Peak-to-peak differential input voltage	The specifications are located in the Reference Clock section of Table 4–6 on page 4–4. The specifications listed in Table 4–6 are applicable to PCML input standards.
V_{ICM}	Input common mode voltage	
R	On-chip termination resistors	
Receiver		
3.3-V PCML 1.5-V PCML 1.2-V PCML	Receiver supported PCML standards	
V_{ID}	Peak-to-peak differential input voltage	The specifications are located in the Receiver section of Table 4–6 on page 4–4. The specifications listed in Table 4–6 are applicable to PCML input standards.
V_{ICM}	Input common mode voltage	
R	On-chip termination resistors	
Transmitter		
1.5-V PCML 1.2-V PCML	Transmitter supported PCML standards	
V_{CCH}	Output buffer supply voltage	The specifications are located in Table 4–5 on page 4–4.
V_{OD}	Peak-to-peak differential output voltage	The specifications are located in Tables 4–7, 4–8, 4–9, 4–10, 4–11, and 4–12. The specifications listed in these tables are applicable to PCML output standards.
V_{OCM}	Output common mode voltage	The specifications are located in the Transmitter section of Table 4–6 on page 4–4. The specifications listed in Table 4–6 are applicable to PCML output standards.
R	On-chip termination resistors	

Note to Table 4–31:

(1) Stratix II GX devices support PCML input and output on GXB banks 13, 14, 15, 16, and 17. This table references Stratix II GX PCML specifications that are located in other sections of the *Stratix II GX Device Handbook*.

Table 4–32. LVPECL Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO} *(1)*	I/O supply voltage		3.135	3.3	3.465	V
V_{ID}	Input differential voltage swing (single-ended)		300	600	1,000	mV
V_{ICM}	Input common mode voltage		1.0		2.5	V
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	525		970	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	1,650		2,250	mV
R_L	Receiver differential input resistor		90	100	110	Ω

Note to Table 4–32:

(1) The top and bottom clock input differential buffers in I/O banks 3, 4, 7, and 8 are powered by V_{CCINT}, not V_{CCIO}. The PLL clock output/feedback differential buffers are powered by VCC_PLL_OUT. For differential clock output/feedback operation, connect VCC_PLL_OUT to 3.3 V.

Table 4–33. 3.3-V PCI Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{IH}	High-level input voltage		0.5 V_{CCIO}		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage		–0.3		0.3 V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	0.9 V_{CCIO}			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			0.1 V_{CCIO}	V

Table 4–34. PCI-X Mode 1 Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		3.0		3.6	V
V_{IH}	High-level input voltage		0.5 V_{CCIO}		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage		–0.3		0.35 V_{CCIO}	V
V_{IPU}	Input pull-up voltage		0.7 V_{CCIO}			V
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	0.9 V_{CCIO}			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			0.1 V_{CCIO}	V

Table 4–35. SSTL-18 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.71	1.8	1.89	V
V_{REF}	Reference voltage		0.855	0.9	0.945	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{IH} (DC)	High-level DC input voltage		V_{REF} + 0.125			V
V_{IL} (DC)	Low-level DC input voltage				V_{REF} – 0.125	V
V_{IH} (AC)	High-level AC input voltage		V_{REF} + 0.25			V
V_{IL} (AC)	Low-level AC input voltage				V_{REF} – 0.25	V
V_{OH}	High-level output voltage	I_{OH} = –6.7 mA *(1)*	V_{TT} + 0.475			V
V_{OL}	Low-level output voltage	I_{OL} = 6.7 mA *(1)*			V_{TT} – 0.475	V

Note to Table 4–35:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Table 4–36. SSTL-18 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.71	1.8	1.89	V
V_{REF}	Reference voltage		0.855	0.9	0.945	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{IH} (DC)	High-level DC input voltage		V_{REF} + 0.125			V
V_{IL} (DC)	Low-level DC input voltage				V_{REF} – 0.125	V
V_{IH} (AC)	High-level AC input voltage		V_{REF} + 0.25			V
V_{IL} (AC)	Low-level AC input voltage				V_{REF} – 0.25	V
V_{OH}	High-level output voltage	I_{OH} = –13.4 mA *(1)*	V_{CCIO} – 0.28			V
V_{OL}	Low-level output voltage	I_{OL} = 13.4 mA *(1)*			0.28	V

Note to Table 4–36:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Table 4–37. SSTL-18 Class I and II Differential Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.71	1.8	1.89	V
V_{SWING} (DC)	DC differential input voltage		0.25			V
V_X (AC)	AC differential input cross point voltage		(V_{CCIO}/2) – 0.175		(V_{CCIO}/2) + 0.175	V
V_{SWING} (AC)	AC differential input voltage		0.5			V
V_{ISO}	Input clock signal offset voltage			0.5 V_{CCIO}		V
ΔV_{ISO}	Input clock signal offset voltage variation			200		mV
V_{OX} (AC)	AC differential cross point voltage		(V_{CCIO}/2) – 0.125		(V_{CCIO}/2) + 0.125	V

Table 4–38. SSTL-2 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.188	1.25	1.313	V
V_{IH} (DC)	High-level DC input voltage		V_{REF} + 0.18		3.0	V
V_{IL} (DC)	Low-level DC input voltage		–0.3		V_{REF} – 0.18	V
V_{IH} (AC)	High-level AC input voltage		V_{REF} + 0.35			V
V_{IL} (AC)	Low-level AC input voltage				V_{REF} – 0.35	V
V_{OH}	High-level output voltage	I_{OH} = –8.1 mA *(1)*	V_{TT} + 0.57			V
V_{OL}	Low-level output voltage	I_{OL} = 8.1 mA *(1)*			V_{TT} – 0.57	V

Note to Table 4–38:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Table 4–39. SSTL-2 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.188	1.25	1.313	V

Table 4–39. SSTL-2 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{IH} (DC)	High-level DC input voltage		V_{REF} + 0.18		V_{CCIO} + 0.3	V
V_{IL} (DC)	Low-level DC input voltage		–0.3		V_{REF} – 0.18	V
V_{IH} (AC)	High-level AC input voltage		V_{REF} + 0.35			V
V_{IL} (AC)	Low-level AC input voltage				V_{REF} – 0.35	V
V_{OH}	High-level output voltage	I_{OH} = –16.4 mA *(1)*	V_{TT} + 0.76			V
V_{OL}	Low-level output voltage	I_{OL} = 16.4 mA *(1)*			V_{TT} – 0.76	V

Note to Table 4–39:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Table 4–40. SSTL-2 Class I and II Differential Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
V_{SWING} (DC)	DC differential input voltage		0.36			V
V_X (AC)	AC differential input cross point voltage		(V_{CCIO}/2) – 0.2		(V_{CCIO}/2) + 0.2	V
V_{SWING} (AC)	AC differential input voltage		0.7			V
V_{ISO}	Input clock signal offset voltage			0.5 V_{CCIO}		V
ΔV_{ISO}	Input clock signal offset voltage variation			200		mV
V_{OX} (AC)	AC differential output cross point voltage		(V_{CCIO}/2) – 0.2		(V_{CCIO}/2) + 0.2	V

Table 4–41. 1.2-V HSTL Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.14	1.2	1.26	V
V_{REF}	Reference voltage		0.48 V_{CCIO}	0.5 V_{CCIO}	0.52 V_{CCIO}	V
V_{IH} (DC)	High-level DC input voltage		V_{REF} + 0.08		V_{CCIO} + 0.15	V
V_{IL} (DC)	Low-level DC input voltage		–0.15		V_{REF} – 0.08	V
V_{IH} (AC)	High-level AC input voltage		V_{REF} + 0.15		V_{CCIO} + 0.24	V
V_{IL} (AC)	Low-level AC input voltage		–0.24		V_{REF} – 0.15	V

Table 4–41. 1.2-V HSTL Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{OH}	High-level output voltage	I_{OH} = 8 mA	V_{REF} + 0.15		V_{CCIO} + 0.15	V
V_{OL}	Low-level output voltage	I_{OH} = –8 mA	–0.15		V_{REF} – 0.15	V

Table 4–42. 1.5-V HSTL Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.425	1.5	1.575	V
V_{REF}	Input reference voltage		0.713	0.75	0.788	V
V_{TT}	Termination voltage		0.713	0.75	0.788	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 8 mA *(1)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OH} = –8 mA *(1)*			0.4	V

Note to Table 4–42:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Table 4–43. 1.5-V HSTL Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.425	1.50	1.575	V
V_{REF}	Input reference voltage		0.713	0.75	0.788	V
V_{TT}	Termination voltage		0.713	0.75	0.788	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 16 mA *(1)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OH} = –16 mA *(1)*			0.4	V

Note to Table 4–43:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Table 4–44. 1.5-V HSTL Class I and II Differential Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage		1.425	1.5	1.575	V
V_{DIF} (DC)	DC input differential voltage		0.2			V
V_{CM} (DC)	DC common mode input voltage		0.68		0.9	V
V_{DIF} (AC)	AC differential input voltage		0.4			V
V_{OX} (AC)	AC differential cross point voltage		0.68		0.9	V

Table 4–45. 1.8-V HSTL Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.71	1.80	1.89	V
V_{REF}	Input reference voltage		0.85	0.90	0.95	V
V_{TT}	Termination voltage		0.85	0.90	0.95	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 8 mA *(1)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OH} = –8 mA *(1)*			0.4	V

Note to Table 4–45:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Table 4–46. 1.8-V HSTL Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.71	1.80	1.89	V
V_{REF}	Input reference voltage		0.85	0.90	0.95	V
V_{TT}	Termination voltage		0.85	0.90	0.95	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 16 mA *(1)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OH} = –16 mA *(1)*			0.4	V

Note to Table 4–46:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Table 4–47. 1.8-V HSTL Class I and II Differential Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage		1.71	1.80	1.89	V
V_{DIF} (DC)	DC input differential voltage		0.2			V
V_{CM} (DC)	DC common mode input voltage		0.78		1.12	V
V_{DIF} (AC)	AC differential input voltage		0.4			V
V_{OX} (AC)	AC differential cross point voltage		0.68		0.9	V

Bus Hold Specifications

Table 4–48 shows the Stratix II GX device family bus hold specifications.

Table 4–48. Bus Hold Parameters

Parameter	Conditions	V_{CCIO} Level										Unit
		1.2 V		1.5 V		1.8 V		2.5 V		3.3 V		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	$V_{IN} > V_{IL}$ (maximum)	22.5		25		30		50		70		µA
High sustaining current	$V_{IN} < V_{IH}$ (minimum)	–22.5		–25		–30		–50		–70		µA
Low overdrive current	$0 V < V_{IN} < V_{CCIO}$		120		160		200		300		500	µA
High overdrive current	$0 V < V_{IN} < V_{CCIO}$		–120		–160		–200		–300		–500	µA
Bus-hold trip point		0.45	0.95	0.5	1.0	0.68	1.07	0.7	1.7	0.8	2.0	V

On-Chip Termination Specifications

Tables 4–49 and 4–50 define the specification for internal termination resistance tolerance when using series or differential on-chip termination.

Table 4–49. On-Chip Termination Specification for Top and Bottom I/O Banks (Part 1 of 2) *Notes (1), (2)*

Symbol	Description	Conditions	Resistance Tolerance		
			Commercial Max	Industrial Max	Unit
25-Ω R_S 3.3/2.5	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 3.3/2.5 V	±5	±10	%
	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 3.3/2.5 V	±30	±30	%
50-Ω R_S 3.3/2.5	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 3.3/2.5 V	±5	±10	%
	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 3.3/2.5 V	±30	± 30	%

Table 4–49. On-Chip Termination Specification for Top and Bottom I/O Banks (Part 2 of 2) *Notes (1), (2)*

Symbol	Description	Conditions	Resistance Tolerance		
			Commercial Max	Industrial Max	Unit
50-Ω R_T 2.5	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.8 V	±30	± 30	%
25-Ω R_S 1.8	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 1.8 V	±5	±10	%
	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.8 V	±30	±30	%
50-Ω R_S 1.8	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 1.8 V	±5	±10	%
	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.8 V	±30	±30	%
50-Ω R_T 1.8	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.8 V	±10	±15	%
50-Ω R_S 1.5	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 1.5 V	±8	±10	%
	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.5 V	±36	±36	%
50-Ω R_T 1.5	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.5 V	±10	±15	%
50-Ω R_S 1.2	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 1.2 V	±8	±10	%
	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.2 V	±50	±50	%
50-Ω R_T 1.2	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.2 V	±10	±15	%

Note for Table 4–49:

(1) The resistance tolerance for calibrated SOCT is for the moment of calibration. If the temperature or voltage changes over time, the tolerance may also change.

(2) On-chip parallel termination with calibration is only supported for input pins.

Table 4–50. Series and Differential On-Chip Termination Specification for Left I/O Banks Note (1)					
Symbol	Description	Conditions	Resistance Tolerance		
			Commercial Max	Industrial Max	Unit
25-Ω R_S 3.3/2.5	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 3.3/2.5V	±30	±30	%
50-Ω R_S 3.3/2.5/1.8	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 3.3/2.5/1.8V	±30	±30	%
50-Ω R_S 1.5	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.5V	±36	±36	%
R_D	Internal differential termination for LVDS (100-Ω setting)	V_{CCIO} = 2.5 V	±20	±25	%

Note to Table 4–50:
(1) On-chip parallel termination with calibration is only supported for input pins.

Pin Capacitance

Table 4–51 shows the Stratix II GX device family pin capacitance.

Table 4–51. Stratix II GX Device Capacitance Note (1)			
Symbol	Parameter	Typical	Unit
C_{IOTB}	Input capacitance on I/O pins in I/O banks 3, 4, 7, and 8.	5.0	pF
C_{IOL}	Input capacitance on I/O pins in I/O banks 1 and 2, including high-speed differential receiver and transmitter pins.	6.1	pF
C_{CLKTB}	Input capacitance on top/bottom clock input pins: `CLK[4..7]` and `CLK[12..15]`.	6.0	pF
C_{CLKL}	Input capacitance on left clock inputs: `CLK0` and `CLK2`.	6.1	pF
C_{CLKL+}	Input capacitance on left clock inputs: `CLK1` and `CLK3`.	3.3	pF
C_{OUTFB}	Input capacitance on dual-purpose clock output/feedback pins in PLL banks 11 and 12.	6.7	pF

Note to Table 4–51:
(1) Capacitance is sample-tested only. Capacitance is measured using time-domain reflections (TDR). Measurement accuracy is within ±0.5 pF.

Power Consumption

Altera offers two ways to calculate power for a design: the Excel-based PowerPlay early power estimator power calculator and the Quartus® II PowerPlay power analyzer feature.

The interactive Excel-based PowerPlay early power estimator is typically used prior to designing the FPGA in order to get an estimate of device power. The Quartus II PowerPlay power analyzer provides better quality estimates based on the specifics of the design after place-and-route is complete. The power analyzer can apply a combination of user-entered, simulation-derived and estimated signal activities which, combined with detailed circuit models, can yield very accurate power estimates.

In both cases, these calculations should only be used as an estimation of power, not as a specification.

For more information on PowerPlay tools, refer to the *PowerPlay Early Power Estimators (EPE) and Power Analyzer,* the *Quartus II PowerPlay Analysis and Optimization Technology*, and the *PowerPlay Power Analyzer* chapter in volume 3 of the *Quartus II Handbook*. The PowerPlay early power estimators are available on the Altera web site at **www.altera. com**.

See Table 4–23 on page 42 for typical I_{CC} standby specifications.

Timing Model

The DirectDrive technology and MultiTrack interconnect ensure predictable performance, accurate simulation, and accurate timing analysis across all Stratix II GX device densities and speed grades. This section describes and specifies the performance, internal, external, and PLL timing specifications.

All specifications are representative of worst-case supply voltage and junction temperature conditions.

Preliminary and Final Timing

Timing models can have either preliminary or final status. The Quartus II software issues an informational message during the design compilation if the timing models are preliminary. Table 4–52 shows the status of the Stratix II GX device timing models.

Preliminary status means the timing model is subject to change. Initially, timing numbers are created using simulation results, process data, and other known parameters. These tests are used to make the preliminary numbers as close to the actual timing parameters as possible.

Final timing numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under worst-case voltage and junction temperature conditions.

Table 4–52. Stratix II GX Device Timing Model Status

Device	Preliminary	Final
EP2SGX30		✓
EP2SGX60		✓
EP2SGX90		✓
EP2SGX130		✓

I/O Timing Measurement Methodology

Different I/O standards require different baseline loading techniques for reporting timing delays. Altera characterizes timing delays with the required termination for each I/O standard and with 0 pF (except for PCI and PCI-X which use 10 pF) loading and the timing is specified up to the output pin of the FPGA device. The Quartus II software calculates the I/O timing for each I/O standard with a default baseline loading as specified by the I/O standards.

The following measurements are made during device characterization. Altera measures clock-to-output delays (t_{CO}) at worst-case process, minimum voltage, and maximum temperature (PVT) for default loading conditions shown in Table 4–53. Use the following equations to calculate clock pin to output pin timing for Stratix II GX devices.

t_{CO} from clock pin to I/O pin = delay from clock pad to I/O output register + IOE output register clock-to-output delay + delay from output register to output pin + I/O output delay

t_{xz}/t_{zx} from clock pin to I/O pin = delay from clock pad to I/O output register + IOE output register clock-to-output delay + delay from output register to output pin + I/O output delay + output enable pin delay

Simulation using IBIS models is required to determine the delays on the PCB traces in addition to the output pin delay timing reported by the Quartus II software and the timing model in the device handbook.

1. Simulate the output driver of choice into the generalized test setup, using values from Table 4–53.
2. Record the time to V_{MEAS}.

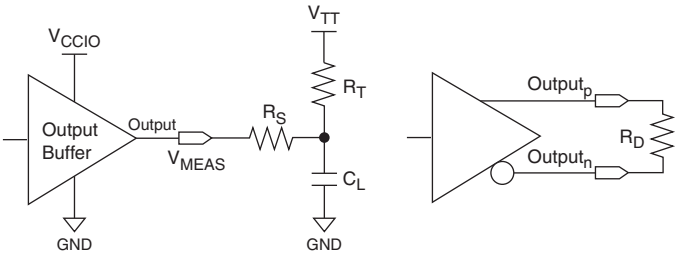
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.

4. Record the time to V_{MEAS}.

5. Compare the results of steps 2 and 4. The increase or decrease in delay should be added to or subtracted from the I/O Standard Output Adder delays to yield the actual worst-case propagation delay (clock-to-output) of the PCB trace.

The Quartus II software reports the timing with the conditions shown in Table 4–53 using the above equation. Figure 4–8 shows the model of the circuit that is represented by the output timing of the Quartus II software.

Figure 4–8. Output Delay Timing Reporting Setup Modeled by Quartus II



Notes to Figure 4–8:

(1) Output pin timing is reported at the output pin of the FPGA device. Additional delays for loading and board trace delay need to be accounted for with IBIS model simulations.
(2) V_{CCPD} is 3.085 V unless otherwise specified.
(3) V_{CCINT} is 1.12 V unless otherwise specified.

Table 4–53. Output Timing Measurement Methodology for Output Pins (Part 1 of 2) *Notes (1), (2), (3)*

I/O Standard	Loading and Termination						Measurement Point
	R_S (Ω)	R_D (Ω)	R_T (Ω)	V_{CCIO} (V)	V_{TT} (V)	C_L (pF)	V_{MEAS} (V)
LVTTL *(4)*				3.135		0	1.5675
LVCMOS *(4)*				3.135		0	1.5675
2.5 V *(4)*				2.375		0	1.1875
1.8 V *(4)*				1.710		0	0.855
1.5 V *(4)*				1.425		0	0.7125

Table 4–53. Output Timing Measurement Methodology for Output Pins (Part 2 of 2) Notes (1), (2), (3)

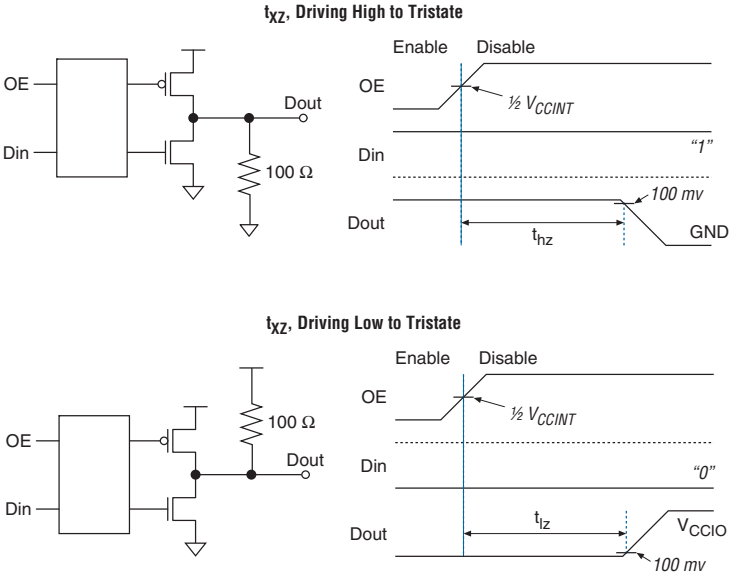
I/O Standard	Loading and Termination						Measurement Point
	R_S (Ω)	R_D (Ω)	R_T (Ω)	V_{CCIO} (V)	V_{TT} (V)	C_L (pF)	V_{MEAS} (V)
PCI (5)				2.970		10	1.485
PCI-X (5)				2.970		10	1.485
SSTL-2 Class I	25		50	2.325	1.123	0	1.1625
SSTL-2 Class II	25		25	2.325	1.123	0	1.1625
SSTL-18 Class I	25		50	1.660	0.790	0	0.83
SSTL-18 Class II	25		25	1.660	0.790	0	0.83
1.8-V HSTL Class I			50	1.660	0.790	0	0.83
1.8-V HSTL Class II			25	1.660	0.790	0	0.83
1.5-V HSTL Class I			50	1.375	0.648	0	0.6875
1.5-V HSTL Class II			25	1.375	0.648	0	0.6875
1.2-V HSTL with OCT				1.140		0	0.570
Differential SSTL-2 Class I	25		50	2.325	1.123	0	1.1625
Differential SSTL-2 Class II	25		25	2.325	1.123	0	1.1625
Differential SSTL-18 Class I	50		50	1.660	0.790	0	0.83
Differential SSTL-18 Class II	25		25	1.660	0.790	0	0.83
1.5-V differential HSTL Class I			50	1.375	0.648	0	0.6875
1.5-V differential HSTL Class II			25	1.375	0.648	0	0.6875
1.8-V differential HSTL Class I			50	1.660	0.790	0	0.83
1.8-V differential HSTL Class II			25	1.660	0.790	0	0.83
LVDS		100		2.325		0	1.1625
LVPECL		100		3.135		0	1.5675

Notes to Table 4–53:

(1) Input measurement point at internal node is 0.5 V_{CCINT}.
(2) Output measuring point for V_{MEAS} at buffer output is 0.5 V_{CCIO}.
(3) Input stimulus edge rate is 0 to V_{CC} in 0.2 ns (internal signal) from the driver preceding the I/O buffer.
(4) Less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V with less than 30-mV ripple.
(5) V_{CCPD} = 2.97 V, less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V.

Figures 4–9 and 4–10 show the measurement setup for output disable and output enable timing.

Figure 4–9. Measurement Setup for t_{xz} *Note (1)*



Note to Figure 4–9:

(1) V_{CCINT} is 1.12 V for this measurement.

Figure 4–10. Measurement Setup for t_{zx}

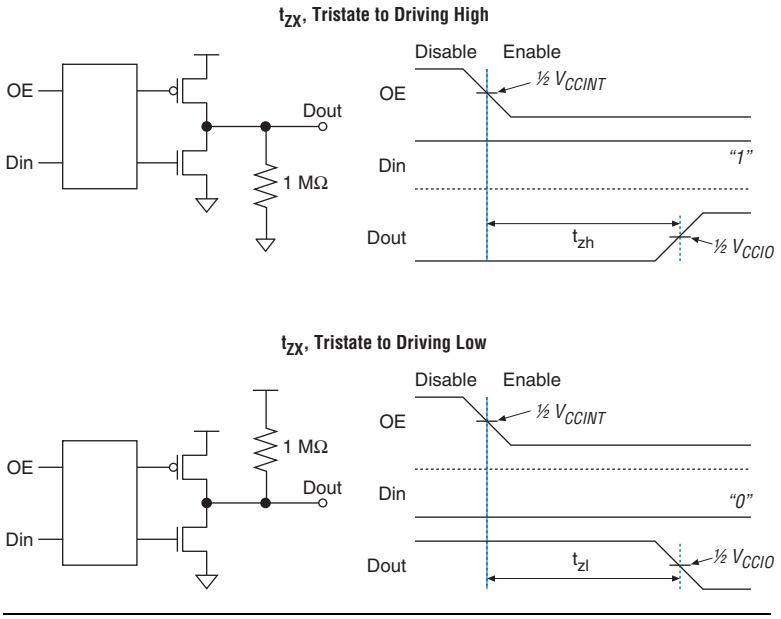


Table 4–54 specifies the input timing measurement setup.

Table 4–54. Timing Measurement Methodology for Input Pins (Part 1 of 2) *Notes (1), (2), (3), (4)*

I/O Standard	Measurement Conditions			Measurement Point
	V_{CCIO} (V)	V_{REF} (V)	Edge Rate (ns)	VMEAS (V)
LVTTL *(5)*	3.135		3.135	1.5675
LVCMOS *(5)*	3.135		3.135	1.5675
2.5 V *(5)*	2.375		2.375	1.1875
1.8 V *(5)*	1.710		1.710	0.855
1.5 V *(5)*	1.425		1.425	0.7125
PCI *(6)*	2.970		2.970	1.485
PCI-X *(6)*	2.970		2.970	1.485
SSTL-2 Class I	2.325	1.163	2.325	1.1625
SSTL-2 Class II	2.325	1.163	2.325	1.1625
SSTL-18 Class I	1.660	0.830	1.660	0.83
SSTL-18 Class II	1.660	0.830	1.660	0.83
1.8-V HSTL Class I	1.660	0.830	1.660	0.83

Table 4–54. Timing Measurement Methodology for Input Pins (Part 2 of 2) *Notes (1), (2), (3), (4)*

I/O Standard	Measurement Conditions			Measurement Point
	V_{CCIO} (V)	V_{REF} (V)	Edge Rate (ns)	VMEAS (V)
1.8-V HSTL Class II	1.660	0.830	1.660	0.83
1.5-V HSTL Class I	1.375	0.688	1.375	0.6875
1.5-V HSTL Class II	1.375	0.688	1.375	0.6875
1.2-V HSTL with OCT	1.140	0.570	1.140	0.570
Differential SSTL-2 Class I	2.325	1.163	2.325	1.1625
Differential SSTL-2 Class II	2.325	1.163	2.325	1.1625
Differential SSTL-18 Class I	1.660	0.830	1.660	0.83
Differential SSTL-18 Class II	1.660	0.830	1.660	0.83
1.5-V differential HSTL Class I	1.375	0.688	1.375	0.6875
1.5-V differential HSTL Class II	1.375	0.688	1.375	0.6875
1.8-V differential HSTL Class I	1.660	0.830	1.660	0.83
1.8-V differential HSTL Class II	1.660	0.830	1.660	0.83
LVDS	2.325		0.100	1.1625
LVPECL	3.135		0.100	1.5675

Notes to Table 4–54:

(1) Input buffer sees no load at buffer input.
(2) Input measuring point at buffer input is 0.5 V_{CCIO}.
(3) Output measuring point is 0.5 V_{CC} at internal node.
(4) Input edge rate is 1 V/ns.
(5) Less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V with less than 30-mV ripple.
(6) V_{CCPD} = 2.97 V, less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V.

Table 4–55 shows the Stratix II GX performance for some common designs. All performance values were obtained with the Quartus II software compilation of LPM or MegaCore functions for FIR and FFT designs.

Table 4–55. Stratix II GX Performance Notes (Part 1 of 3) *Note (1)*

Applications		Resources Used			Performance				
		ALUTs	TriMatrix Memory Blocks	DSP Blocks	-3 Speed Grade (2)	-3 Speed Grade (3)	-4 Speed Grade	-5 Speed Grade	Units
LE	16-to-1 multiplexer (4)	21	0	0	657.03	620.73	589.62	477.09	MHz
	32-to-1 multiplexer (4)	38	0	0	534.75	517.33	472.81	369.27	MHz
	16-bit counter	16	0	0	568.18	539.66	507.61	422.47	MHz
	64-bit counter	64	0	0	242.54	231.0	217.77	180.31	MHz
TriMatrix Memory M512 block	Simple dual-port RAM 32 x 18bit	0	1	0	500.0	476.19	447.22	373.13	MHz
	FIFO 32 x 18 bit	22	1	0	500.00	476.19	460.82	373.13	MHz
TriMatrix Memory M4K block	Simple dual-port RAM 128 x 36bit	0	1	0	540.54	515.46	483.09	401.6	MHz
	True dual-port RAM 128 x 18bit	0	1	0	540.54	515.46	483.09	401.6	MHz
	FIFO 128 x 36 bit	22	1	0	524.10	500.25	466.41	381.38	MHz

Table 4–55. Stratix II GX Performance Notes (Part 2 of 3) *Note (1)*

Applications		Resources Used			Performance				
		ALUTs	TriMatrix Memory Blocks	DSP Blocks	-3 Speed Grade (2)	-3 Speed Grade (3)	-4 Speed Grade	-5 Speed Grade	Units
TriMatrix Memory MegaRAM block	Single port RAM 4K x 144bit	0	1	0	349.65	333.33	313.47	261.09	MHz
	Simple dual-port RAM 4K x 144bit	0	1	0	420.16	400.0	375.93	313.47	MHz
	True dual-port RAM 4K x 144 bit	0	1	0	349.65	333.33	313.47	261.09	MHz
	Single port RAM 8K x 72 bit	0	1	0	354.6	337.83	317.46	263.85	MHz
	Simple dual-port RAM 8K x 72 bit	0	1	0	420.16	400.0	375.93	313.47	MHz
	True dual-port RAM 8K x 72 bit	0	1	0	349.65	333.33	313.47	261.09	MHz
	Single port RAM 16K x 36 bit	0	1	0	364.96	347.22	325.73	271.73	MHz
	Simple dual-port RAM 16K x 36 bit	0	1	0	420.16	400.0	375.93	313.47	MHz
	True dual-port RAM 16K x 36 bit	0	1	0	359.71	342.46	322.58	268.09	MHz
	Single port RAM 32K x 18 bit	0	1	0	364.96	347.22	325.73	271.73	MHz
	Simple dual-port RAM 32K x 18 bit	0	1	0	420.16	400.0	375.93	313.47	MHz
	True dual-port RAM 32K x 18 bit	0	1	0	359.71	342.46	322.58	268.09	MHz

Table 4–55. Stratix II GX Performance Notes (Part 3 of 3) *Note (1)*

Applications		Resources Used			Performance				
		ALUTs	TriMatrix Memory Blocks	DSP Blocks	-3 Speed Grade *(2)*	-3 Speed Grade *(3)*	-4 Speed Grade	-5 Speed Grade	Units
TriMatrix Memory MegaRAM block (cont.)	Single port RAM 64K x 9 bit	0	1	0	364.96	347.22	325.73	271.73	MHz
	Simple dual-port RAM 64K x 9 bit	0	1	0	420.16	400.0	375.93	313.47	MHz
	True dual-port RAM 64K x 9 bit	0	1	0	359.71	342.46	322.58	268.09	MHz
DSP block	9 x 9-bit multiplier *(5)*	0	0	1	430.29	409.16	385.2	320.1	MHz
	18 x 18-bit multiplier *(5)*	0	0	1	410.17	390.01	367.1	305.06	MHz
	18 x 18-bit multiplier *(7)*	0	0	1	450.04	428.08	403.22	335.12	MHz
	36 x 36-bit multiplier *(5)*	0	0	1	250.0	238.15	224.01	186.6	MHz
	36 x 36-bit multiplier *(6)*	0	0	1	410.17	390.01	367.1	305.06	MHz
	18-bit, 4-tap FIR filter	0	0	1	410.17	390.01	367.1	305.06	MHz

Notes to Table 4–55:

(1) These design performance numbers were obtained using the Quartus II software.
(2) This column refers to -3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(3) This column refers to -3 speed grades for EP2SGX130 devices.
(4) This application uses registered inputs and outputs.
(5) This application uses registered multiplier input and output stages within the DSP block.
(6) This application uses registered multiplier input, pipeline, and output stages within the DSP block.
(7) This application uses registered multiplier inputs with outputs of the multiplier stage feeding the accumulator or subtractor within the DSP block.

Internal Timing Parameters

Refer to Tables 4–56 through 4–61 for internal timing parameters.

Table 4–56. LE_FF Internal Timing Microparameters

Symbol	Parameter	-3 Speed Grade (1)		-3 Speed Grade (2)		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{SU}	LE register setup time before clock	90		95		101		121		ps
t_{H}	LE register hold time after clock	149		157		167		200		ps
t_{CO}	LE register clock-to-output delay	62	94	62	99	62	105	62	127	ps
t_{CLR}	Minimum clear pulse width	204		214		227		273		ps
t_{PRE}	Minimum preset pulse width	204		214		227		273		ps
t_{CLKL}	Minimum clock low time	612		642		683		820		ps
t_{CLKH}	Minimum clock high time	612		642		683		820		ps
t_{LUT}		170	378	170	397	170	422	170	507	
t_{ADDER}		372	619	372	650	372	691	372	829	

Notes to Table 4–56:
(1) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(2) This column refers to –3 speed grades for EP2SGX130 devices.

Table 4–57. IOE Internal Timing Microparameters (Part 1 of 2)

Symbol	Parameter	-3 Speed Grade (1)		-3 Speed Grade (2)		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{SU}	IOE input and output register setup time before clock	122		128		136		163		ps
t_{H}	IOE input and output register hold time after clock	72		75		80		96		ps
t_{CO}	IOE input and output register clock-to-output delay	101	169	101	177	101	188	101	226	ps

Table 4–57. IOE Internal Timing Microparameters (Part 2 of 2)

Symbol	Parameter	-3 Speed Grade (1)		-3 Speed Grade (2)		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{PIN2COMBOUT\_R}$	Row input pin to IOE combinational output	410	760	410	798	410	848	410	1018	ps
$t_{PIN2COMBOUT\_C}$	Column input pin to IOE combinational output	428	787	428	825	428	878	428	1054	ps
$t_{COMBIN2PIN\_R}$	Row IOE data input to combinational output pin	1101	2026	1101	2127	1101	2261	1101	2439	ps
$t_{COMBIN2PIN\_C}$	Column IOE data input to combinational output pin	991	1854	991	1946	991	2069	991	2246	ps
t_{CLR}	Minimum clear pulse width	200		210		223		268		ps
t_{PRE}	Minimum preset pulse width	200		210		223		268		ps
t_{CLKL}	Minimum clock low time	600		630		669		804		ps
t_{CLKH}	Minimum clock high time	600		630		669		804		ps

Notes to Table 4–57:
(1) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(2) This column refers to –3 speed grades for EP2SGX130 devices.

Table 4–58. DSP Block Internal Timing Microparameters (Part 1 of 2)

Symbol	Parameter	-3 Speed Grade (1)		-3 Speed Grade (2)		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{SU}	Input, pipeline, and output register setup time before clock	50		52		55		67		ps
t_{H}	Input, pipeline, and output register hold time after clock	180		189		200		241		ps
t_{CO}	Input, pipeline, and output register clock-to-output delay	0	0	0	0	0	0	0	0	ps

Table 4–58. DSP Block Internal Timing Microparameters (Part 2 of 2)

Symbol	Parameter	-3 Speed Grade (1)		-3 Speed Grade (2)		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{INREG2PIPE9}$	Input register to DSP block pipeline register in 9 × 9-bit mode	1312	2030	1312	2131	1312	2266	1312	2720	ps
$t_{INREG2PIPE18}$	Input register to DSP block pipeline register in 18 × 18-bit mode	1302	2010	1302	2110	1302	2244	1302	2693	ps
$t_{INREG2PIPE36}$	Input register to DSP block pipeline register in 36 × 36-bit mode	1302	2010	1302	2110	1302	2244	1302	2693	ps
$t_{PIPE2OUTREG2ADD}$	DSP block pipeline register to output register delay in two-multipliers adder mode	924	1450	924	1522	924	1618	924	1943	ps
$t_{PIPE2OUTREG4ADD}$	DSP block pipeline register to output register delay in four-multipliers adder mode	1134	1850	1134	1942	1134	2065	1134	2479	ps
t_{PD9}	Combinational input to output delay for 9 × 9	2100	2880	2100	3024	2100	3214	2100	3859	ps
t_{PD18}	Combinational input to output delay for 18 × 18	2110	2990	2110	3139	2110	3337	2110	4006	ps
t_{PD36}	Combinational input to output delay for 36 × 36	2939	4450	2939	4672	2939	4967	2939	5962	ps
t_{CLR}	Minimum clear pulse width	2212		2322		2469		2964		ps
t_{CLKL}	Minimum clock low time	1190		1249		1328		1594		ps
t_{CLKH}	Minimum clock high time	1190		1249		1328		1594		ps

Notes to Table 4–58:
(1) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(2) This column refers to –3 speed grades for EP2SGX130 devices.

Table 4–59. M512 Block Internal Timing Microparameters (Part 1 of 2)

Symbol	Parameter	-3 Speed Grade (2)		-3 Speed Grade (3)		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{M512RC}	Synchronous read cycle time	2089	2318	2089	2433	2089	2587	2089	3104	ps
$t_{M512WERESU}$	Write or read enable setup time before clock	22		23		24		29		ps
$t_{M512WEREH}$	Write or read enable hold time after clock	203		213		226		272		ps
$t_{M512DATASU}$	Data setup time before clock	22		23		24		29		ps
$t_{M512DATAH}$	Data hold time after clock	203		213		226		272		ps
$t_{M512WADDRSU}$	Write address setup time before clock	22		23		24		29		ps
$t_{M512WADDRH}$	Write address hold time after clock	203		213		226		272		ps
$t_{M512RADDRSU}$	Read address setup time before clock	22		23		24		29		ps
$t_{M512RADDRH}$	Read address hold time after clock	203		213		226		272		ps
$t_{M512DATACO1}$	Clock-to-output delay when using output registers	298	478	298	501	298	533	298	640	ps
$t_{M512DATACO2}$	Clock-to-output delay without output registers	2102	2345	2102	2461	2102	2616	2102	3141	ps
$t_{M512CLKL}$	Minimum clock low time	1315		1380		1468		1762		ps
$t_{M512CLKH}$	Minimum clock high time	1315		1380		1468		1762		ps

Table 4–59. M512 Block Internal Timing Microparameters (Part 2 of 2)

Symbol	Parameter	-3 Speed Grade (2)		-3 Speed Grade (3)		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{M512CLR}$	Minimum clear pulse width	144		151		160		192		ps

Notes to Table 4–59:
(1) The M512 block f_{MAX} obtained using the Quartus II software does not necessarily equal to 1/TM512RC.
(2) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(3) This column refers to –3 speed grades for EP2SGX130 devices.

Table 4–60. M4K Block Internal Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	-3 Speed Grade (2)		-3 Speed Grade (3)		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{M4KRC}	Synchronous read cycle time	1462	2240	1462	2351	1462	2500	1462	3000	ps
$t_{M4KWERESU}$	Write or read enable setup time before clock	22		23		24		29		ps
$t_{M4KWEREH}$	Write or read enable hold time after clock	203		213		226		272		ps
$t_{M4KBESU}$	Byte enable setup time before clock	22		23		24		29		ps
t_{M4KBEH}	Byte enable hold time after clock	203		213		226		272		ps
$t_{M4KDATAASU}$	A port data setup time before clock	22		23		24		29		ps
$t_{M4KDATAAH}$	A port data hold time after clock	203		213		226		272		ps
$t_{M4KADDRASU}$	A port address setup time before clock	22		23		24		29		ps
$t_{M4KADDRAH}$	A port address hold time after clock	203		213		226		272		ps
$t_{M4KDATABSU}$	B port data setup time before clock	22		23		24		29		ps

Table 4–60. M4K Block Internal Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	-3 Speed Grade (2)		-3 Speed Grade (3)		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{M4KDATABH}$	B port data hold time after clock	203		213		226		272		ps
$t_{M4KRADDRBSU}$	B port address setup time before clock	22		23		24		29		ps
$t_{M4KRADDRBH}$	B port address hold time after clock	203		213		226		272		ps
$t_{M4KDATACO1}$	Clock-to-output delay when using output registers	334	524	334	549	334	584	334	701	ps
$t_{M4KDATACO2}$	Clock-to-output delay without output registers	1616	2453	1616	2574	1616	2737	1616	3286	ps
$t_{M4KCLKH}$	Minimum clock high time	1250		1312		1395		1675		ps
$t_{M4KCLKL}$	Minimum clock low time	1250		1312		1395		1675		ps
t_{M4KCLR}	Minimum clear pulse width	144		151		160		192		ps

Notes to Table 4–60:

(1) The M512 block f_{MAX} obtained using the Quartus II software does not necessarily equal to 1/TM4KRC.

(2) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.

(3) This column refers to –3 speed grades for EP2SGX130 devices.

Table 4–61. M-RAM Block Internal Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	-3 Speed Grade (2)		-3 Speed Grade (3)		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{MEGARC}	Synchronous read cycle time	1866	2774	1866	2911	1866	3096	1866	3716	ps
$t_{MEGAWERESU}$	Write or read enable setup time before clock	144		151		160		192		ps
$t_{MEGAWEREH}$	Write or read enable hold time after clock	39		40		43		52		ps

Table 4–61. M-RAM Block Internal Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	-3 Speed Grade *(2)*		-3 Speed Grade *(3)*		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{MEGABESU}$	Byte enable setup time before clock	-9		-10		-11		-13		ps
$t_{MEGABEH}$	Byte enable hold time after clock	39		40		43		52		ps
$t_{MEGADATAASU}$	A port data setup time before clock	50		52		55		67		ps
$t_{MEGADATAAH}$	A port data hold time after clock	243		255		271		325		ps
$t_{MEGAADDRASU}$	A port address setup time before clock	589		618		657		789		ps
$t_{MEGAADDRAH}$	A port address hold time after clock	-347		-365		-388		-465		ps
$t_{MEGADATABSU}$	B port setup time before clock	50		52		55		67		ps
$t_{MEGADATABH}$	B port hold time after clock	243		255		271		325		ps
$t_{MEGAADDRBSU}$	B port address setup time before clock	589		618		657		789		ps
$t_{MEGAADDRBH}$	B port address hold time after clock	-347		-365		-388		-465		ps
$t_{MEGADATACO1}$	Clock-to-output delay when using output registers	480	715	480	749	480	797	480	957	ps
$t_{MEGADATACO2}$	Clock-to-output delay without output registers	1950	2899	1950	3042	1950	3235	1950	3884	ps
$t_{MEGACLKL}$	Minimum clock low time	1250		1312		1395		1675		ps
$t_{MEGACLKH}$	Minimum clock high time	1250		1312		1395		1675		ps
$t_{MEGACLR}$	Minimum clear pulse width	144		151		160		192		ps

Notes to Table 4–61:

(1) The M512 block f_{MAX} obtained using the Quartus II software does not necessarily equal to 1/TMEGARC.

(2) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.

(3) This column refers to –3 speed grades for EP2SGX130 devices.

Stratix II GX Clock Timing Parameters

See Tables 4–62 through 4–78 for Stratix II GX clock timing parameters.

Table 4–62. Stratix II GX Clock Timing Parameters

Symbol	Parameter
t_{CIN}	Delay from clock pad to I/O input register
t_{COUT}	Delay from clock pad to I/O output register
t_{PLLCIN}	Delay from PLL `inclk` pad to I/O input register
$t_{PLLCOUT}$	Delay from PLL `inclk` pad to I/O output register

EP2SGX30 Clock Timing Parameters

Tables 4–63 through 4–66 show the maximum clock timing parameters for EP2SGX30 devices.

Table 4–63. EP2SGX30 Column Pins Global Clock Timing Parameters

Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.615	1.633	2.669	2.968	3.552	ns
t_{COUT}	1.450	1.468	2.427	2.698	3.228	ns
t_{PLLCIN}	0.11	0.129	0.428	0.466	0.547	ns
$t_{PLLCOUT}$	-0.055	-0.036	0.186	0.196	0.223	ns

Table 4–64. EP2SGX30 Row Pins Global Clock Timing Parameters

Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.365	1.382	2.280	2.535	3.033	ns
t_{COUT}	1.370	1.387	2.276	2.531	3.028	ns
t_{PLLCIN}	-0.151	-0.136	0.043	0.037	0.032	ns
$t_{PLLCOUT}$	-0.146	-0.131	0.039	0.033	0.027	ns

Table 4–65. EP2SGX30 Column Pins Regional Clock Timing Parameters

Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.493	1.507	2.522	2.806	3.364	ns
t_{COUT}	1.353	1.372	2.525	2.809	3.364	ns
t_{PLLCIN}	0.087	0.104	0.237	0.253	0.292	ns
$t_{PLLCOUT}$	-0.078	-0.061	0.237	0.253	0.29	ns

Table 4–66. EP2SGX30 Row Pins Regional Clock Timing Parameters

Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.246	1.262	2.437	2.712	3.246	ns
t_{COUT}	1.251	1.267	2.437	2.712	3.246	ns
t_{PLLCIN}	-0.18	-0.167	0.215	0.229	0.263	ns
$t_{PLLCOUT}$	-0.175	-0.162	0.215	0.229	0.263	ns

EP2SGX60 Clock Timing Parameters

Tables 4–67 through 4–70 show the maximum clock timing parameters for EP2SGX60 devices.

Table 4–67. EP2SGX60 Column Pins Global Clock Timing Parameters

Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.722	1.736	2.940	3.275	3.919	ns
t_{COUT}	1.557	1.571	2.698	3.005	3.595	ns
t_{PLLCIN}	0.037	0.051	0.474	0.521	0.613	ns
$t_{PLLCOUT}$	-0.128	-0.114	0.232	0.251	0.289	ns

Table 4–68. EP2SGX60 Row Pins Global Clock Timing Parameters

Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.494	1.508	2.582	2.875	3.441	ns
t_{COUT}	1.499	1.513	2.578	2.871	3.436	ns
t_{PLLCIN}	-0.183	-0.168	0.116	0.122	0.135	ns
$t_{PLLCOUT}$	-0.178	-0.163	0.112	0.118	0.13	ns

Table 4–69. EP2SGX60 Column Pins Regional Clock Timing Parameters

Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.577	1.591	2.736	3.048	3.648	ns
t_{COUT}	1.412	1.426	2.740	3.052	3.653	ns
t_{PLLCIN}	0.065	0.08	0.334	0.361	0.423	ns
$t_{PLLCOUT}$	-0.1	-0.085	0.334	0.361	0.423	ns

Table 4–70. EP2SGX60 Row Pins Regional Clock Timing Parameters

Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.342	1.355	2.716	3.024	3.622	ns
t_{COUT}	1.347	1.360	2.716	3.024	3.622	ns
t_{PLLCIN}	-0.18	-0.166	0.326	0.352	0.412	ns
$t_{PLLCOUT}$	-0.175	-0.161	0.334	0.361	0.423	ns

EP2SGX90 Clock Timing Parameters

Tables 4–71 through 4–74 show the maximum clock timing parameters for EP2SGX90 devices.

Table 4–71. EP2SGX90 Column Pins Global Clock Timing Parameters

Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.861	1.878	3.115	3.465	4.143	ns
t_{COUT}	1.696	1.713	2.873	3.195	3.819	ns
t_{PLLCIN}	-0.254	-0.237	0.171	0.179	0.206	ns
$t_{PLLCOUT}$	-0.419	-0.402	-0.071	-0.091	-0.118	ns

Table 4–72. EP2SGX90 Row Pins Global Clock Timing Parameters

Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.634	1.650	2.768	3.076	3.678	ns
t_{COUT}	1.639	1.655	2.764	3.072	3.673	ns
t_{PLLCIN}	-0.481	-0.465	-0.189	-0.223	-0.279	ns
$t_{PLLCOUT}$	-0.476	-0.46	-0.193	-0.227	-0.284	ns

Table 4–73. EP2SGX90 Column Pins Regional Clock Timing Parameters

Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.688	1.702	2.896	3.224	3.856	ns
t_{COUT}	1.551	1.569	2.893	3.220	3.851	ns
t_{PLLCIN}	-0.105	-0.089	0.224	0.241	0.254	ns
$t_{PLLCOUT}$	-0.27	-0.254	0.224	0.241	0.254	ns

Table 4–74. EP2SGX90 Row Pins Regional Clock Timing Parameters						
Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.444	1.461	2.792	3.108	3.716	ns
t_{COUT}	1.449	1.466	2.792	3.108	3.716	ns
t_{PLLCIN}	-0.348	-0.333	0.204	0.217	0.243	ns
$t_{PLLCOUT}$	-0.343	-0.328	0.212	0.217	0.254	ns

EP2SGX130 Clock Timing Parameters

Tables 4–75 through 4–78 show the maximum clock timing parameters for EP2SGX130 devices.

Table 4–75. EP2SGX130 Column Pins Global Clock Timing Parameters						
Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.980	1.998	3.491	3.706	4.434	ns
t_{COUT}	1.815	1.833	3.237	3.436	4.110	ns
t_{PLLCIN}	-0.027	-0.009	0.307	0.322	0.376	ns
$t_{PLLCOUT}$	-0.192	-0.174	0.053	0.052	0.052	ns

Table 4–76. EP2SGX130 Row Pins Global Clock Timing Parameters						
Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.741	1.759	3.112	3.303	3.950	ns
t_{COUT}	1.746	1.764	3.108	3.299	3.945	ns
t_{PLLCIN}	-0.261	-0.243	-0.089	-0.099	-0.129	ns
$t_{PLLCOUT}$	-0.256	-0.238	-0.093	-0.103	-0.134	ns

Table 4–77. EP2SGX130 Column Pins Regional Clock Timing Parameters

Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.815	1.834	3.218	3.417	4.087	ns
t_{COUT}	1.650	1.669	3.218	3.417	4.087	ns
t_{PLLCIN}	0.116	0.134	0.349	0.364	0.426	ns
$t_{PLLCOUT}$	-0.049	-0.031	0.361	0.378	0.444	ns

Table 4–78. EP2SGX130 Row Pins Regional Clock Timing Parameters

Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.544	1.560	3.195	3.395	4.060	ns
t_{COUT}	1.549	1.565	3.195	3.395	4.060	ns
t_{PLLCIN}	-0.149	-0.132	0.34	0.356	0.417	ns
$t_{PLLCOUT}$	-0.144	-0.127	0.342	0.356	0.417	ns

Clock Network Skew Adders

The Quartus II software models skew within dedicated clock networks such as global and regional clocks. Therefore, the intra-clock network skew adder is not specified. Table 4–79 specifies the intra-clock skew between any two clock networks driving any registers in the Stratix II GX device.

Table 4–79. Clock Network Specifications (Part 1 of 2)

Name	Description	Min	Typ	Max	Unit
Clock skew adder EP2SGX30 *(1)*	Inter-clock network, same side			±50	ps
	Inter-clock network, entire chip			±100	ps
Clock skew adder EP2SGX60 *(1)*	Inter-clock network, same side			±50	ps
	Inter-clock network, entire chip			±100	ps
Clock skew adder EP2SGX90 *(1)*	Inter-clock network, same side			±55	ps
	Inter-clock network, entire chip			±110	ps

Table 4–79. Clock Network Specifications (Part 2 of 2)

Name	Description	Min	Typ	Max	Unit
Clock skew adder EP2SGX130 *(1)*	Inter-clock network, same side			±63	ps
	Inter-clock network, entire chip			±125	ps

Note to Table 4–79:
(1) This is in addition to intra-clock network skew, which is modeled in the Quartus II software.

IOE Programmable Delay

See Tables 4–80 and 4–81 for IOE programmable delay.

Table 4–80. Stratix II GX IOE Programmable Delay on Column Pins *Note (1)*

Parameter	Paths Affected	Available Settings	Minimum Timing		-3 Speed Grade *(2)*		-3 Speed Grade *(3)*		-4 Speed Grade		-5 Speed Grade		Unit
			Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	
Input delay from pin to internal cells	Pad to I/O dataout to core	8	0	1781	0	2881	0	3025	0	3217	0	3,860	ps
Input delay from pin to input register	Pad to I/O input register	64	0	2053	0	3275	0	3439	0	3657	0	4388	ps
Delay from output register to output pin	I/O output register to pad	2	0	332	0	500	0	525	0	559	0	670	ps
Output enable pin delay	t_{XZ}, t_{ZX}	2	0	320	0	483	0	507	0	539	0	647	ps

Notes to Table 4–80:
(1) The incremental values for the settings are generally linear. For the exact delay associated with each setting, use the latest version of the Quartus II software.
(2) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(3) This column refers to –3 speed grades for EP2SGX130 devices.

Table 4–81. Stratix II GX IOE Programmable Delay on Row Pins *Note (1)*

Parameter	Paths Affected	Available Settings	Minimum Timing		-3 Speed Grade		-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
			Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	
Input delay from pin to internal cells	Pad to I/O dataout to logic array	8	0	1782	0	2876	0	3020	0	3212	0	3853	ps
Input delay from pin to input register	Pad to I/O input register	64	0	2054	0	3270	0	3434	0	3652	0	4381	ps
Delay from output register to output pin	I/O output register to pad	2	0	332	0	500	0	525	0	559	0	670	ps
Output enable pin delay	t_{XZ}, t_{ZX}	2	0	320	0	483	0	507	0	539	0	647	ps

Notes to Table 4–81:

(1) The incremental values for the settings are generally linear. For the exact delay associated with each setting, use the latest version of the Quartus II software.

Default Capacitive Loading of Different I/O Standards

See Table 4–82 for default capacitive loading of different I/O standards.

Table 4–82. Default Loading of Different I/O Standards for Stratix II GX Devices (Part 1 of 2)

I/O Standard	Capacitive Load	Unit
LVTTL	0	pF
LVCMOS	0	pF
2.5 V	0	pF
1.8 V	0	pF
1.5 V	0	pF
PCI	10	pF
PCI-X	10	pF
SSTL-2 Class I	0	pF
SSTL-2 Class II	0	pF

Table 4–82. Default Loading of Different I/O Standards for Stratix II GX Devices (Part 2 of 2)

I/O Standard	Capacitive Load	Unit
SSTL-18 Class I	0	pF
SSTL-18 Class II	0	pF
1.5-V HSTL Class I	0	pF
1.5-V HSTL Class II	0	pF
1.8-V HSTL Class I	0	pF
1.8-V HSTL Class II	0	pF
Differential SSTL-2 Class I	0	pF
Differential SSTL-2 Class II	0	pF
Differential SSTL-18 Class I	0	pF
Differential SSTL-18 Class II	0	pF
1.5-V differential HSTL Class I	0	pF
1.5-V differential HSTL Class II	0	pF
1.8-V differential HSTL Class I	0	pF
1.8-V differential HSTL Class II	0	pF
LVDS	0	pF

I/O Delays

See Tables 4–83 through 4–87 for I/O delays.

Table 4–83. I/O Delay Parameters

Symbol	Parameter
t_{DIP}	Delay from I/O datain to output pad
t_{OP}	Delay from I/O output register to output pad
t_{PCOUT}	Delay from input pad to I/O dataout to core
t_{PI}	Delay from input pad to I/O input register

Table 4–84. Stratix II GX I/O Input Delay for Column Pins (Part 1 of 3)

I/O Standard	Parameter	Fast Corner Industrial/ Commercial	-3 Speed Grade *(2)*	-3 Speed Grade *(3)*	-4 Speed Grade	-5 Speed Grade	Unit
LVTTL	t_{PI}	707	1223	1282	1364	1637	ps
	t_{PCOUT}	428	787	825	878	1054	ps

Table 4–84. Stratix II GX I/O Input Delay for Column Pins (Part 2 of 3)

I/O Standard	Parameter	Fast Corner Industrial/ Commercial	-3 Speed Grade *(2)*	-3 Speed Grade *(3)*	-4 Speed Grade	-5 Speed Grade	Unit
2.5 V	t_{PI}	717	1210	1269	1349	1619	ps
	t_{PCOUT}	438	774	812	863	1036	ps
1.8 V	t_{PI}	783	1366	1433	1523	1829	ps
	t_{PCOUT}	504	930	976	1037	1246	ps
1.5 V	t_{PI}	786	1436	1506	1602	1922	ps
	t_{PCOUT}	507	1000	1049	1116	1339	ps
LVCMOS	t_{PI}	707	1223	1282	1364	1637	ps
	t_{PCOUT}	428	787	825	878	1054	ps
SSTL-2 Class I	t_{PI}	530	818	857	912	1094	ps
	t_{PCOUT}	251	382	400	426	511	ps
SSTL-2 Class II	t_{PI}	530	818	857	912	1094	ps
	t_{PCOUT}	251	382	400	426	511	ps
SSTL-18 Class I	t_{PI}	569	898	941	1001	1201	ps
	t_{PCOUT}	290	462	484	515	618	ps
SSTL-18 Class II	t_{PI}	569	898	941	1001	1201	ps
	t_{PCOUT}	290	462	484	515	618	ps
1.5-V HSTL Class I	t_{PI}	587	993	1041	1107	1329	ps
	t_{PCOUT}	308	557	584	621	746	ps
1.5-V HSTL Class II	t_{PI}	587	993	1041	1107	1329	ps
	t_{PCOUT}	308	557	584	621	746	ps
1.8-V HSTL Class I	t_{PI}	569	898	941	1001	1201	ps
	t_{PCOUT}	290	462	484	515	618	ps
1.8-V HSTL Class II	t_{PI}	569	898	941	1001	1201	ps
	t_{PCOUT}	290	462	484	515	618	ps
PCI	t_{PI}	712	1214	1273	1354	1625	ps
	t_{PCOUT}	433	778	816	868	1042	ps
PCI-X	t_{PI}	712	1214	1273	1354	1625	ps
	t_{PCOUT}	433	778	816	868	1042	ps
Differential SSTL-2 Class I *(1)*	t_{PI}	530	818	857	912	1094	ps
	t_{PCOUT}	251	382	400	426	511	ps

Table 4–84. Stratix II GX I/O Input Delay for Column Pins (Part 3 of 3)

I/O Standard	Parameter	Fast Corner Industrial/ Commercial	-3 Speed Grade *(2)*	-3 Speed Grade *(3)*	-4 Speed Grade	-5 Speed Grade	Unit
Differential SSTL-2 Class II *(1)*	t_{PI}	530	818	857	912	1094	ps
	t_{PCOUT}	251	382	400	426	511	ps
Differential SSTL-18 Class I *(1)*	t_{PI}	569	898	941	1001	1201	ps
	t_{PCOUT}	290	462	484	515	618	ps
Differential SSTL-18 Class II *(1)*	t_{PI}	569	898	941	1001	1201	ps
	t_{PCOUT}	290	462	484	515	618	ps
1.8-V differential HSTL Class I *(1)*	t_{PI}	569	898	941	1001	1201	ps
	t_{PCOUT}	290	462	484	515	618	ps
1.8-V differential HSTL Class II *(1)*	t_{PI}	569	898	941	1001	1201	ps
	t_{PCOUT}	290	462	484	515	618	ps
1.5-V differential HSTL Class I *(1)*	t_{PI}	587	993	1041	1107	1329	ps
	t_{PCOUT}	308	557	584	621	746	ps
1.5-V differential HSTL Class II *(1)*	t_{PI}	587	993	1041	1107	1329	ps
	t_{PCOUT}	308	557	584	621	746	ps

Notes for Table 4–84:
(1) These I/O standards are only supported on DQS pins.
(2) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(3) This column refers to –3 speed grades for EP2SGX130 devices.

Table 4–85. Stratix II GX I/O Input Delay for Row Pins (Part 1 of 3)

I/O Standard	Parameter	Fast Corner Industrial/ Commercial	-3 Speed Grade *(2)*	-3 Speed Grade *(3)*	-4 Speed Grade	-5 Speed Grade	Unit
LVTTL	t_{PI}	749	1287	1350	1435	1723	ps
	t_{PCOUT}	410	760	798	848	1018	ps
2.5 V	t_{PI}	761	1273	1335	1419	1704	ps
	t_{PCOUT}	422	746	783	832	999	ps
1.8 V	t_{PI}	827	1427	1497	1591	1911	ps
	t_{PCOUT}	488	900	945	1004	1206	ps
1.5 V	t_{PI}	830	1498	1571	1671	2006	ps
	t_{PCOUT}	491	971	1019	1084	1301	ps

Table 4–85. Stratix II GX I/O Input Delay for Row Pins (Part 2 of 3)

I/O Standard	Parameter	Fast Corner Industrial/ Commercial	-3 Speed Grade *(2)*	-3 Speed Grade *(3)*	-4 Speed Grade	-5 Speed Grade	Unit
LVCMOS	t_{PI}	749	1287	1350	1435	1723	ps
	t_{PCOUT}	410	760	798	848	1018	ps
SSTL-2 Class I	t_{PI}	573	879	921	980	1176	ps
	t_{PCOUT}	234	352	369	393	471	ps
SSTL-2 Class II	t_{PI}	573	879	921	980	1176	ps
	t_{PCOUT}	234	352	369	393	471	ps
SSTL-18 Class I	t_{PI}	605	960	1006	1070	1285	ps
	t_{PCOUT}	266	433	454	483	580	ps
SSTL-18 Class II	t_{PI}	605	960	1006	1070	1285	ps
	t_{PCOUT}	266	433	454	483	580	ps
1.5-V HSTL Class I	t_{PI}	631	1056	1107	1177	1413	ps
	t_{PCOUT}	292	529	555	590	708	ps
1.5-V HSTL Class II	t_{PI}	631	1056	1107	1177	1413	ps
	t_{PCOUT}	292	529	555	590	708	ps
1.8-V HSTL Class I	t_{PI}	605	960	1006	1070	1285	ps
	t_{PCOUT}	266	433	454	483	580	ps
1.8-V HSTL Class II	t_{PI}	605	960	1006	1070	1285	ps
	t_{PCOUT}	266	433	454	483	580	ps
PCI	t_{PI}	830	1498	1571	1671	2006	ps
	t_{PCOUT}	491	971	1019	1084	1301	ps
PCI-X	t_{PI}	830	1498	1571	1671	2006	ps
	t_{PCOUT}	491	971	1019	1084	1301	ps
LVDS *(1)*	t_{PI}	540	948	994	1057	1269	ps
	t_{PCOUT}	201	421	442	470	564	ps
HyperTransport	t_{PI}	540	948	994	1057	1269	ps
	t_{PCOUT}	201	421	442	470	564	ps
Differential SSTL-2 Class I	t_{PI}	573	879	921	980	1176	ps
	t_{PCOUT}	234	352	369	393	471	ps
Differential SSTL-2 Class II	t_{PI}	573	879	921	980	1176	ps
	t_{PCOUT}	234	352	369	393	471	ps

Table 4–85. Stratix II GX I/O Input Delay for Row Pins (Part 3 of 3)

I/O Standard	Parameter	Fast Corner Industrial/ Commercial	-3 Speed Grade *(2)*	-3 Speed Grade *(3)*	-4 Speed Grade	-5 Speed Grade	Unit
Differential SSTL-18 Class I	t_{PI}	605	960	1006	1070	1285	ps
	t_{PCOUT}	266	433	454	483	580	ps
Differential SSTL-18 Class II	t_{PI}	605	960	1006	1070	1285	ps
	t_{PCOUT}	266	433	454	483	580	ps
1.8-V differential HSTL Class I	t_{PI}	605	960	1006	1070	1285	ps
	t_{PCOUT}	266	433	454	483	580	ps
1.8-V differential HSTL Class II	t_{PI}	605	960	1006	1070	1285	ps
	t_{PCOUT}	266	433	454	483	580	ps
1.5-V differential HSTL Class I	t_{PI}	631	1056	1107	1177	1413	ps
	t_{PCOUT}	292	529	555	590	708	ps
1.5-V differential HSTL Class II	t_{PI}	631	1056	1107	1177	1413	ps
	t_{PCOUT}	292	529	555	590	708	ps

Notes to Table 4–85:

(1) The parameters are only available on the left side of the device.
(2) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(3) This column refers to –3 speed grades for EP2SGX130 devices.

Table 4–86. Stratix II GX I/O Output Delay for Column Pins (Part 1 of 7)

I/O Standard	Drive Strength	Parameter	Fast Corner Industrial/ Commercial	-3 Speed Grade *(3)*	-3 Speed Grade *(4)*	-4 Speed Grade	-5 Speed Grade	Unit
LVTTL	4 mA	t_{OP}	1236	2351	2467	2624	2820	ps
		t_{DIP}	1258	2417	2537	2698	2910	ps
	8 mA	t_{OP}	1091	2036	2136	2272	2448	ps
		t_{DIP}	1113	2102	2206	2346	2538	ps
	12 mA	t_{OP}	1024	2036	2136	2272	2448	ps
		t_{DIP}	1046	2102	2206	2346	2538	ps
	16 mA	t_{OP}	998	1893	1986	2112	2279	ps
		t_{DIP}	1020	1959	2056	2186	2369	ps
	20 mA	t_{OP}	976	1787	1875	1994	2154	ps
		t_{DIP}	998	1853	1945	2068	2244	ps
	24 mA *(1)*	t_{OP}	969	1788	1876	1995	2156	ps
		t_{DIP}	991	1854	1946	2069	2246	ps
LVCMOS	4 mA	t_{OP}	1091	2036	2136	2272	2448	ps
		t_{DIP}	1113	2102	2206	2346	2538	ps
	8 mA	t_{OP}	999	1786	1874	1993	2153	ps
		t_{DIP}	1021	1852	1944	2067	2243	ps
	12 mA	t_{OP}	971	1720	1805	1919	2075	ps
		t_{DIP}	993	1786	1875	1993	2165	ps
	16 mA	t_{OP}	978	1693	1776	1889	2043	ps
		t_{DIP}	1000	1759	1846	1963	2133	ps
	20 mA	t_{OP}	965	1677	1759	1871	2025	ps
		t_{DIP}	987	1743	1829	1945	2115	ps
	24 mA *(1)*	t_{OP}	954	1659	1741	1851	2003	ps
		t_{DIP}	976	1725	1811	1925	2093	ps

Table 4–86. Stratix II GX I/O Output Delay for Column Pins (Part 2 of 7)

I/O Standard	Drive Strength	Parameter	Fast Corner Industrial/ Commercial	-3 Speed Grade *(3)*	-3 Speed Grade *(4)*	-4 Speed Grade	-5 Speed Grade	Unit
2.5 V	4 mA	t_{OP}	1053	2063	2165	2302	2480	ps
		t_{DIP}	1075	2129	2235	2376	2570	ps
	8 mA	t_{OP}	1001	1841	1932	2054	2218	ps
		t_{DIP}	1023	1907	2002	2128	2308	ps
	12 mA	t_{OP}	980	1742	1828	1944	2101	ps
		t_{DIP}	1002	1808	1898	2018	2191	ps
	16 mA *(1)*	t_{OP}	962	1679	1762	1873	2027	ps
		t_{DIP}	984	1745	1832	1947	2117	ps
1.8 V	2 mA	t_{OP}	1093	2904	3048	3241	3472	ps
		t_{DIP}	1115	2970	3118	3315	3562	ps
	4 mA	t_{OP}	1098	2248	2359	2509	2698	ps
		t_{DIP}	1120	2314	2429	2583	2788	ps
	6 mA	t_{OP}	1022	2024	2124	2258	2434	ps
		t_{DIP}	1044	2090	2194	2332	2524	ps
	8 mA	t_{OP}	1024	1947	2043	2172	2343	ps
		t_{DIP}	1046	2013	2113	2246	2433	ps
	10 mA	t_{OP}	978	1882	1975	2100	2266	ps
		t_{DIP}	1000	1948	2045	2174	2356	ps
	12 mA *(1)*	t_{OP}	979	1833	1923	2045	2209	ps
		t_{DIP}	1001	1899	1993	2119	2299	ps
1.5 V	2 mA	t_{OP}	1073	2505	2629	2795	3002	ps
		t_{DIP}	1095	2571	2699	2869	3092	ps
	4 mA	t_{OP}	1009	2023	2123	2257	2433	ps
		t_{DIP}	1031	2089	2193	2331	2523	ps
	6 mA	t_{OP}	1012	1923	2018	2146	2315	ps
		t_{DIP}	1034	1989	2088	2220	2405	ps
	8 mA *(1)*	t_{OP}	971	1878	1970	2095	2262	ps
		t_{DIP}	993	1944	2040	2169	2352	ps

Table 4–86. Stratix II GX I/O Output Delay for Column Pins (Part 3 of 7)

I/O Standard	Drive Strength	Parameter	Fast Corner Industrial/ Commercial	-3 Speed Grade *(3)*	-3 Speed Grade *(4)*	-4 Speed Grade	-5 Speed Grade	Unit
SSTL-2 Class I	8 mA	t_{OP}	957	1715	1799	1913	2041	ps
		t_{DIP}	979	1781	1869	1987	2131	ps
	12 mA *(1)*	t_{OP}	940	1672	1754	1865	1991	ps
		t_{DIP}	962	1738	1824	1939	2081	ps
SSTL-2 Class II	16 mA	t_{OP}	918	1609	1688	1795	1918	ps
		t_{DIP}	940	1675	1758	1869	2008	ps
	20 mA	t_{OP}	919	1598	1676	1783	1905	ps
		t_{DIP}	941	1664	1746	1857	1995	ps
	24 mA *(1)*	t_{OP}	915	1596	1674	1781	1903	ps
		t_{DIP}	937	1662	1744	1855	1993	ps
SSTL-18 Class I	4 mA	t_{OP}	953	1690	1773	1886	2012	ps
		t_{DIP}	975	1756	1843	1960	2102	ps
	6 mA	t_{OP}	958	1656	1737	1848	1973	ps
		t_{DIP}	980	1722	1807	1922	2063	ps
	8 mA	t_{OP}	937	1640	1721	1830	1954	ps
		t_{DIP}	959	1706	1791	1904	2044	ps
	10 mA	t_{OP}	942	1638	1718	1827	1952	ps
		t_{DIP}	964	1704	1788	1901	2042	ps
	12 mA *(1)*	t_{OP}	936	1626	1706	1814	1938	ps
		t_{DIP}	958	1692	1776	1888	2028	ps
SSTL-18 Class II	8 mA	t_{OP}	925	1597	1675	1782	1904	ps
		t_{DIP}	947	1663	1745	1856	1994	ps
	16 mA	t_{OP}	937	1578	1655	1761	1882	ps
		t_{DIP}	959	1644	1725	1835	1972	ps
	18 mA	t_{OP}	933	1585	1663	1768	1890	ps
		t_{DIP}	955	1651	1733	1842	1980	ps
	20 mA *(1)*	t_{OP}	933	1583	1661	1766	1888	ps
		t_{DIP}	955	1649	1731	1840	1978	ps

Table 4–86. Stratix II GX I/O Output Delay for Column Pins (Part 4 of 7)

I/O Standard	Drive Strength	Parameter	Fast Corner Industrial/ Commercial	-3 Speed Grade *(3)*	-3 Speed Grade *(4)*	-4 Speed Grade	-5 Speed Grade	Unit
1.8-V HSTL Class I	4 mA	t_{OP}	956	1608	1687	1794	1943	ps
		t_{DIP}	978	1674	1757	1868	2033	ps
	6 mA	t_{OP}	962	1595	1673	1779	1928	ps
		t_{DIP}	984	1661	1743	1853	2018	ps
	8 mA	t_{OP}	940	1586	1664	1769	1917	ps
		t_{DIP}	962	1652	1734	1843	2007	ps
	10 mA	t_{OP}	944	1591	1669	1775	1923	ps
		t_{DIP}	966	1657	1739	1849	2013	ps
	12 mA *(1)*	t_{OP}	936	1585	1663	1768	1916	ps
		t_{DIP}	958	1651	1733	1842	2006	ps
1.8-V HSTL Class II	16 mA	t_{OP}	919	1385	1453	1545	1680	ps
		t_{DIP}	941	1451	1523	1619	1770	ps
	18 mA	t_{OP}	921	1394	1462	1555	1691	ps
		t_{DIP}	943	1460	1532	1629	1781	ps
	20 mA *(1)*	t_{OP}	921	1402	1471	1564	1700	ps
		t_{DIP}	943	1468	1541	1638	1790	ps
1.5-V HSTL Class I	4 mA	t_{OP}	956	1607	1686	1793	1942	ps
		t_{DIP}	978	1673	1756	1867	2032	ps
	6 mA	t_{OP}	961	1588	1666	1772	1920	ps
		t_{DIP}	983	1654	1736	1846	2010	ps
	8 mA	t_{OP}	943	1590	1668	1774	1922	ps
		t_{DIP}	965	1656	1738	1848	2012	ps
	10 mA	t_{OP}	943	1592	1670	1776	1924	ps
		t_{DIP}	965	1658	1740	1850	2014	ps
	12 mA *(1)*	t_{OP}	937	1590	1668	1774	1922	ps
		t_{DIP}	959	1656	1738	1848	2012	ps

Table 4–86. Stratix II GX I/O Output Delay for Column Pins (Part 5 of 7)

I/O Standard	Drive Strength	Parameter	Fast Corner Industrial/ Commercial	-3 Speed Grade *(3)*	-3 Speed Grade *(4)*	-4 Speed Grade	-5 Speed Grade	Unit
1.5-V HSTL Class II	16 mA	t_{OP}	924	1431	1501	1596	1734	ps
		t_{DIP}	946	1497	1571	1670	1824	ps
	18 mA	t_{OP}	927	1439	1510	1605	1744	ps
		t_{DIP}	949	1505	1580	1679	1834	ps
	20 mA *(1)*	t_{OP}	929	1450	1521	1618	1757	ps
		t_{DIP}	951	1516	1591	1692	1847	ps
PCI	-	t_{OP}	1082	1956	2051	2176	2070	ps
		t_{DIP}	1104	2022	2121	2250	2160	ps
PCI-X	-	t_{OP}	1082	1956	2051	2176	2070	ps
		t_{DIP}	1104	2022	2121	2250	2160	ps
Differential SSTL-2 Class I *(2)*	8 mA	t_{OP}	957	1715	1799	1913	2041	ps
		t_{DIP}	979	1781	1869	1987	2131	ps
	12 mA	t_{OP}	940	1672	1754	1865	1991	ps
		t_{DIP}	962	1738	1824	1939	2081	ps
Differential SSTL-2 Class II *(2)*	16 mA	t_{OP}	918	1609	1688	1795	1918	ps
		t_{DIP}	940	1675	1758	1869	2008	ps
	20 mA	t_{OP}	919	1598	1676	1783	1905	ps
		t_{DIP}	941	1664	1746	1857	1995	ps
	24 mA	t_{OP}	915	1596	1674	1781	1903	ps
		t_{DIP}	937	1662	1744	1855	1993	ps
Differential SSTL-18 Class I *(2)*	4 mA	t_{OP}	953	1690	1773	1886	2012	ps
		t_{DIP}	975	1756	1843	1960	2102	ps
	6 mA	t_{OP}	958	1656	1737	1848	1973	ps
		t_{DIP}	980	1722	1807	1922	2063	ps
	8 mA	t_{OP}	937	1640	1721	1830	1954	ps
		t_{DIP}	959	1706	1791	1904	2044	ps
	10 mA	t_{OP}	942	1638	1718	1827	1952	ps
		t_{DIP}	964	1704	1788	1901	2042	ps
	12 mA	t_{OP}	936	1626	1706	1814	1938	ps
		t_{DIP}	958	1692	1776	1888	2028	ps

Table 4–86. Stratix II GX I/O Output Delay for Column Pins (Part 6 of 7)

I/O Standard	Drive Strength	Parameter	Fast Corner Industrial/ Commercial	-3 Speed Grade *(3)*	-3 Speed Grade *(4)*	-4 Speed Grade	-5 Speed Grade	Unit
Differential SSTL-18 Class II *(2)*	8 mA	t_{OP}	925	1597	1675	1782	1904	ps
		t_{DIP}	947	1663	1745	1856	1994	ps
	16 mA	t_{OP}	937	1578	1655	1761	1882	ps
		t_{DIP}	959	1644	1725	1835	1972	ps
	18 mA	t_{OP}	933	1585	1663	1768	1890	ps
		t_{DIP}	955	1651	1733	1842	1980	ps
	20 mA	t_{OP}	933	1583	1661	1766	1888	ps
		t_{DIP}	955	1649	1731	1840	1978	ps
1.8-V differential HSTL Class I *(2)*	4 mA	t_{OP}	956	1608	1687	1794	1943	ps
		t_{DIP}	978	1674	1757	1868	2033	ps
	6 mA	t_{OP}	962	1595	1673	1779	1928	ps
		t_{DIP}	984	1661	1743	1853	2018	ps
	8 mA	t_{OP}	940	1586	1664	1769	1917	ps
		t_{DIP}	962	1652	1734	1843	2007	ps
	10 mA	t_{OP}	944	1591	1669	1775	1923	ps
		t_{DIP}	966	1657	1739	1849	2013	ps
	12 mA	t_{OP}	936	1585	1663	1768	1916	ps
		t_{DIP}	958	1651	1733	1842	2006	ps
1.8-V differential HSTL Class II *(2)*	16 mA	t_{OP}	919	1385	1453	1545	1680	ps
		t_{DIP}	941	1451	1523	1619	1770	ps
	18 mA	t_{OP}	921	1394	1462	1555	1691	ps
		t_{DIP}	943	1460	1532	1629	1781	ps
	20 mA	t_{OP}	921	1402	1471	1564	1700	ps
		t_{DIP}	943	1468	1541	1638	1790	ps

Table 4–86. Stratix II GX I/O Output Delay for Column Pins (Part 7 of 7)

I/O Standard	Drive Strength	Parameter	Fast Corner Industrial/ Commercial	-3 Speed Grade *(3)*	-3 Speed Grade *(4)*	-4 Speed Grade	-5 Speed Grade	Unit
1.5-V differential HSTL Class I *(2)*	4 mA	t_{OP}	956	1607	1686	1793	1942	ps
		t_{DIP}	978	1673	1756	1867	2032	ps
	6 mA	t_{OP}	961	1588	1666	1772	1920	ps
		t_{DIP}	983	1654	1736	1846	2010	ps
	8 mA	t_{OP}	943	1590	1668	1774	1922	ps
		t_{DIP}	965	1656	1738	1848	2012	ps
	10 mA	t_{OP}	943	1592	1670	1776	1924	ps
		t_{DIP}	965	1658	1740	1850	2014	ps
	12 mA	t_{OP}	937	1590	1668	1774	1922	ps
		t_{DIP}	959	1656	1738	1848	2012	ps
1.5-V differential HSTL Class II *(2)*	16 mA	t_{OP}	924	1431	1501	1596	1734	ps
		t_{DIP}	946	1497	1571	1670	1824	ps
	18 mA	t_{OP}	927	1439	1510	1605	1744	ps
		t_{DIP}	949	1505	1580	1679	1834	ps
	20 mA	t_{OP}	929	1450	1521	1618	1757	ps
		t_{DIP}	951	1516	1591	1692	1847	ps

Notes to Table 4–86:
(1) This is the default setting in the Quartus II software.
(2) These I/O standards are only supported on DQS pins.
(3) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(4) This column refers to –3 speed grades for EP2SGX130 devices.

Table 4–87. Stratix II GX I/O Output Delay for Row Pins (Part 1 of 4)

I/O Standard	Drive Strength	Parameter	Fast Corner Industrial/ Commercial	-3 Speed Grade *(3)*	-3 Speed Grade *(4)*	-4 Speed Grade	-5 Speed Grade	Unit
LVTTL	4 mA	t_{OP}	1328	2655	2786	2962	3189	ps
		t_{DIP}	1285	2600	2729	2902	3116	ps
	8 mA	t_{OP}	1200	2113	2217	2357	2549	ps
		t_{DIP}	1157	2058	2160	2297	2476	ps
	12 mA *(1)*	t_{OP}	1144	2081	2184	2321	2512	ps
		t_{DIP}	1101	2026	2127	2261	2439	ps

Table 4–87. Stratix II GX I/O Output Delay for Row Pins (Part 2 of 4)

I/O Standard	Drive Strength	Parameter	Fast Corner Industrial/ Commercial	-3 Speed Grade *(3)*	-3 Speed Grade *(4)*	-4 Speed Grade	-5 Speed Grade	Unit
LVCMOS	4 mA	t_{OP}	1200	2113	2217	2357	2549	ps
		t_{DIP}	1157	2058	2160	2297	2476	ps
	8 mA *(1)*	t_{OP}	1094	1853	1944	2067	2243	ps
		t_{DIP}	1051	1798	1887	2007	2170	ps
	12 mA *(1)*	t_{OP}	1061	1723	1808	1922	2089	ps
		t_{DIP}	1018	1668	1751	1862	2016	ps
2.5 V	4 mA	t_{OP}	1183	2091	2194	2332	2523	ps
		t_{DIP}	1140	2036	2137	2272	2450	ps
	8 mA	t_{OP}	1080	1872	1964	2088	2265	ps
		t_{DIP}	1037	1817	1907	2028	2192	ps
	12 mA *(1)*	t_{OP}	1061	1775	1862	1980	2151	ps
		t_{DIP}	1018	1720	1805	1920	2078	ps
1.8 V	2 mA	t_{OP}	1253	2954	3100	3296	3542	ps
		t_{DIP}	1210	2899	3043	3236	3469	ps
	4 mA	t_{OP}	1242	2294	2407	2559	2763	ps
		t_{DIP}	1199	2239	2350	2499	2690	ps
	6 mA	t_{OP}	1131	2039	2140	2274	2462	ps
		t_{DIP}	1088	1984	2083	2214	2389	ps
	8 mA *(1)*	t_{OP}	1100	1942	2038	2166	2348	ps
		t_{DIP}	1057	1887	1981	2106	2275	ps
1.5 V	2 mA	t_{OP}	1213	2530	2655	2823	3041	ps
		t_{DIP}	1170	2475	2598	2763	2968	ps
	4 mA *(1)*	t_{OP}	1106	2020	2120	2253	2440	ps
		t_{DIP}	1063	1965	2063	2193	2367	ps
SSTL-2 Class I	8 mA	t_{OP}	1050	1759	1846	1962	2104	ps
		t_{DIP}	1007	1704	1789	1902	2031	ps
	12 mA *(1)*	t_{OP}	1026	1694	1777	1889	2028	ps
		t_{DIP}	983	1639	1720	1829	1955	ps
SSTL-2 Class II	16 mA *(1)*	t_{OP}	992	1581	1659	1763	1897	ps
		t_{DIP}	949	1526	1602	1703	1824	ps

Table 4–87. Stratix II GX I/O Output Delay for Row Pins (Part 3 of 4)

I/O Standard	Drive Strength	Parameter	Fast Corner Industrial/ Commercial	-3 Speed Grade *(3)*	-3 Speed Grade *(4)*	-4 Speed Grade	-5 Speed Grade	Unit
SSTL-18 Class I	4 mA	t_{OP}	1038	1709	1793	1906	2046	ps
		t_{DIP}	995	1654	1736	1846	1973	ps
	6 mA	t_{OP}	1042	1648	1729	1838	1975	ps
		t_{DIP}	999	1593	1672	1778	1902	ps
	8 mA	t_{OP}	1018	1633	1713	1821	1958	ps
		t_{DIP}	975	1578	1656	1761	1885	ps
	10 mA *(1)*	t_{OP}	1021	1615	1694	1801	1937	ps
		t_{DIP}	978	1560	1637	1741	1864	ps
1.8-V HSTL Class I	4 mA	t_{OP}	1019	1610	1689	1795	1956	ps
		t_{DIP}	976	1555	1632	1735	1883	ps
	6 mA	t_{OP}	1022	1580	1658	1762	1920	ps
		t_{DIP}	979	1525	1601	1702	1847	ps
	8 mA	t_{OP}	1004	1576	1653	1757	1916	ps
		t_{DIP}	961	1521	1596	1697	1843	ps
	10 mA	t_{OP}	1008	1567	1644	1747	1905	ps
		t_{DIP}	965	1512	1587	1687	1832	ps
	12 mA *(1)*	t_{OP}	999	1566	1643	1746	1904	ps
		t_{DIP}	956	1511	1586	1686	1831	ps
1.5-V HSTL Class I	4 mA	t_{OP}	1018	1591	1669	1774	1933	ps
		t_{DIP}	975	1536	1612	1714	1860	ps
	6 mA	t_{OP}	1021	1579	1657	1761	1919	ps
		t_{DIP}	978	1524	1600	1701	1846	ps
	8 mA *(1)*	t_{OP}	1006	1572	1649	1753	1911	ps
		t_{DIP}	963	1517	1592	1693	1838	ps
Differential SSTL-2 Class I	8 mA	t_{OP}	1050	1759	1846	1962	2104	ps
		t_{DIP}	1007	1704	1789	1902	2031	ps
	12 mA	t_{OP}	1026	1694	1777	1889	2028	ps
		t_{DIP}	983	1639	1720	1829	1955	ps
Differential SSTL-2 Class II	16 mA	t_{OP}	992	1581	1659	1763	1897	ps
		t_{DIP}	949	1526	1602	1703	1824	ps

Table 4–87. Stratix II GX I/O Output Delay for Row Pins (Part 4 of 4)

I/O Standard	Drive Strength	Parameter	Fast Corner Industrial/ Commercial	-3 Speed Grade *(3)*	-3 Speed Grade *(4)*	-4 Speed Grade	-5 Speed Grade	Unit
Differential SSTL-18 Class I	4 mA	t_{OP}	1038	1709	1793	1906	2046	ps
		t_{DIP}	995	1654	1736	1846	1973	ps
	6 mA	t_{OP}	1042	1648	1729	1838	1975	ps
		t_{DIP}	999	1593	1672	1778	1902	ps
	8 mA	t_{OP}	1018	1633	1713	1821	1958	ps
		t_{DIP}	975	1578	1656	1761	1885	ps
	10 mA	t_{OP}	1021	1615	1694	1801	1937	ps
		t_{DIP}	978	1560	1637	1741	1864	ps
LVDS *(2)*	-	t_{OP}	1067	1723	1808	1922	2089	ps
		t_{DIP}	1024	1668	1751	1862	2016	ps
HyperTransport	-	t_{OP}	1053	1723	1808	1922	2089	ps
		t_{DIP}	1010	1668	1751	1862	2016	ps

Notes to Table 4–87:
(1) This is the default setting in the Quartus II software.
(2) The parameters are only available on the left side of the device.
(3) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(4) This column refers to –3 speed grades for EP2SGX130 devices.

Maximum Input and Output Clock Toggle Rate

Maximum clock toggle rate is defined as the maximum frequency achievable for a clock type signal at an I/O pin. The I/O pin can be a regular I/O pin or a dedicated clock I/O pin.

The maximum clock toggle rate is different from the maximum data bit rate. If the maximum clock toggle rate on a regular I/O pin is 300 MHz, the maximum data bit rate for dual data rate (DDR) could be potentially as high as 600 Mbps on the same I/O pin.

Tables 4–88 through 4–90 specify the maximum input clock toggle rates. Tables 4–91 through 4–96 specify the maximum output clock toggle rates at 0 pF load. Table 4–97 specifies the derating factors for the output clock toggle rate for a non 0 pF load.

To calculate the output toggle rate for a non 0 pF load, use this formula:

The toggle rate for a non 0 pF load

= 1,000 / (1,000/ toggle rate at 0 pF load + derating factor × load value in pF /1,000)

For example, the output toggle rate at 0 pF load for SSTL-18 Class II 20 mA I/O standard is 550 MHz on a -3 device clock output pin. The derating factor is 94 ps/pF. For a 10 pF load the toggle rate is calculated as:

1,000 / (1,000/550 + 94 × 10 /1,000) = 363 (MHz)

Table 4–88 shows the maximum input clock toggle rates for Stratix II GX device column pins.

Table 4–88. Stratix II GX Maximum Input Clock Rate for Column I/O Pins (Part 1 of 2)

I/O Standard	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
LVTTL	500	500	450	MHz
2.5 V	500	500	450	MHz
1.8 V	500	500	450	MHz
1.5 V	500	500	450	MHz
LVCMOS	500	500	450	MHz
SSTL-2 Class I	500	500	500	MHz
SSTL-2 Class II	500	500	500	MHz
SSTL-18 Class I	500	500	500	MHz
SSTL-18 Class I I	500	500	500	MHz
1.5-V HSTL Class I	500	500	500	MHz
1.5-V HSTL Class I I	500	500	500	MHz
1.8-V HSTL Class I	500	500	500	MHz
1.8-V HSTL Class II	500	500	500	MHz
PCI	500	500	450	MHz
PCI-X	500	500	450	MHz
Differential SSTL-2 Class I	500	500	500	MHz
Differential SSTL-2 Class II	500	500	500	MHz
Differential SSTL-18 Class I	500	500	500	MHz

Table 4–88. Stratix II GX Maximum Input Clock Rate for Column I/O Pins (Part 2 of 2)

I/O Standard	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
Differential SSTL-18 Class I I	500	500	500	MHz
1.8-V differential HSTL Class I	500	500	500	MHz
1.8-V differential HSTL Class II	500	500	500	MHz
1.5-V differential HSTL Class I	500	500	500	MHz
1.5-V differential HSTL Class I I	500	500	500	MHz
1.2-V HSTL	280	250	250	MHz
1.2-V differential HSTL	280	250	250	MHz

Table 4–89 shows the maximum input clock toggle rates for Stratix II GX device row pins.

Table 4–89. Stratix II GX Maximum Input Clock Rate for Row I/O Pins (Part 1 of 2)

I/O Standard	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
LVTTL	500	500	450	MHz
2.5 V	500	500	450	MHz
1.8 V	500	500	450	MHz
1.5 V	500	500	450	MHz
LVCMOS	500	500	450	MHz
SSTL-2 Class I	500	500	500	MHz
SSTL-2 Class II	500	500	500	MHz
SSTL-18 Class I	500	500	500	MHz
SSTL-18 Class II	500	500	500	MHz
1.5-V HSTL Class I	500	500	500	MHz
1.5-V HSTL Class II	500	500	500	MHz
1.8-V HSTL Class I	500	500	500	MHz
1.8-V HSTL Class II	500	500	500	MHz
PCI	500	500	425	MHz
PCI-X	500	500	425	MHz
Differential SSTL-2 Class I	500	500	500	MHz

Table 4–89. Stratix II GX Maximum Input Clock Rate for Row I/O Pins (Part 2 of 2)

I/O Standard	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
Differential SSTL-2 Class II	500	500	500	MHz
Differential SSTL-18 Class I	500	500	500	MHz
Differential SSTL-18 Class I I	500	500	500	MHz
1.8-V differential HSTL Class I	500	500	500	MHz
1.8-V differential HSTL Class I I	500	500	500	MHz
1.5-V differential HSTL Class I	500	500	500	MHz
1.5-V differential HSTL Class II	500	500	500	MHz
LVDS *(1)*	520	520	420	MHz
HyperTransport	520	520	420	MHz

Note to Table 4–89:
(1) The parameters are only available on the left side of the device.

Table 4–90 shows the maximum input clock toggle rates for Stratix II GX device dedicated clock pins.

Table 4–90. Stratix II GX Maximum Input Clock Rate for Dedicated Clock Pins (Part 1 of 2)

I/O Standard	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
LVTTL	500	500	400	MHz
2.5 V	500	500	400	MHz
1.8 V	500	500	400	MHz
1.5 V	500	500	400	MHz
LVCMOS	500	500	400	MHz
SSTL-2 Class I	500	500	500	MHz
SSTL-2 Class II	500	500	500	MHz
SSTL-18 Class I	500	500	500	MHz
SSTL-18 Class II	500	500	500	MHz
1.5-V HSTL Class I	500	500	500	MHz
1.5-V HSTL Class II	500	500	500	MHz
1.8-V HSTL CLass I	500	500	500	MHz

Table 4–90. Stratix II GX Maximum Input Clock Rate for Dedicated Clock Pins (Part 2 of 2)

I/O Standard	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
1.8-V HSTL CLass I	500	500	500	MHz
PCI	500	500	400	MHz
PCI-X	500	500	400	MHz
Differential SSTL-2 Class I	500	500	500	MHz
Differential SSTL-2 Class II	500	500	500	MHz
Differential SSTL-18 Class I	500	500	500	MHz
Differential SSTL-18 Class II	500	500	500	MHz
1.8-V differential HSTL Class I	500	500	500	MHz
1.8-V differential HSTL Class II	500	500	500	MHz
1.5-V differential HSTL Class I	500	500	500	MHz
1.5-V differential HSTL Class I I	500	500	500	MHz
HyperTransport *(1)*	717	717	640	MHz
	450	450	400	MHz
LVPECL *(1)*, *(2)*	717	717	640	MHz
	450	450	400	MHz
LVDS *(1)*	717	717	640	MHz
	450	450	400	MHz

Notes to Table 4–90:

(1) The first set of numbers refers to the HIO dedicated clock pins. The second set of numbers refers to the VIO dedicated clock pins.

(2) LVPECL is only supported on column clock pins.

Table 4–91 shows the maximum output clock toggle rates for Stratix II GX device column pins.

Table 4–91. Stratix II GX Maximum Output Clock Rate for Column Pins (Part 1 of 3)

I/O Standard	Drive Strength	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
LVTTL	4 mA	270	225	210	MHz
	8 mA	435	355	325	MHz
	12 mA	580	475	420	MHz
	16 mA	720	594	520	MHz
	20 mA	875	700	610	MHz
	24 mA *(1)*	1030	794	670	MHz
LVCMOS	4 mA	290	250	230	MHz
	8 mA	565	480	440	MHz
	12 mA	790	710	670	MHz
	16 mA	1020	925	875	MHz
	20 mA	1066	985	935	MHz
	24 mA *(1)*	1100	1040	1000	MHz
2.5 V	4 mA	230	194	180	MHz
	8 mA	430	380	380	MHz
	12 mA	630	575	550	MHz
	16 mA *(1)*	930	845	820	MHz
1.8 V	2 mA	120	109	104	MHz
	4 mA	285	250	230	MHz
	6 mA	450	390	360	MHz
	8 mA	660	570	520	MHz
	10 mA	905	805	755	MHz
	12 mA *(1)*	1131	1040	990	MHz
1.5 V	2 mA	244	200	180	MHz
	4 mA	470	370	325	MHz
	6 mA	550	430	375	MHz
	8 mA *(1)*	625	495	420	MHz
SSTL-2 Class I	8 mA	400	300	300	MHz
	12 mA *(1)*	400	400	350	MHz
SSTL-2 Class II	16 mA	350	350	300	MHz
	20 mA	400	350	350	MHz
	24 mA *(1)*	400	400	350	MHz

Table 4–91. Stratix II GX Maximum Output Clock Rate for Column Pins (Part 2 of 3)

I/O Standard	Drive Strength	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
SSTL-18 Class I	4 mA	200	150	150	MHz
	6 mA	350	250	200	MHz
	8 mA	450	300	300	MHz
	10 mA	500	400	400	MHz
	12 mA *(1)*	700	550	400	MHz
SSTL-18 Class II	8 mA	200	200	150	MHz
	16 mA	400	350	350	MHz
	18 mA	450	400	400	MHz
	20 mA *(1)*	550	500	450	MHz
1.8-V HSTL Class I	4 mA	300	300	300	MHz
	6 mA	500	450	450	MHz
	8 mA	650	600	600	MHz
	10 mA	700	650	600	MHz
	12 mA *(1)*	700	700	650	MHz
1.8-V HSTL Class II	16 mA	500	500	450	MHz
	18 mA	550	500	500	MHz
	20 mA *(1)*	650	550	550	MHz
1.5-V HSTL Class I	4 mA	350	300	300	MHz
	6 mA	500	500	450	MHz
	8 mA	700	650	600	MHz
	10 mA	700	700	650	MHz
	12 mA *(1)*	700	700	700	MHz
1.5-V HSTL Class II	16 mA	600	600	550	MHz
	18 mA	650	600	600	MHz
	20 mA *(1)*	700	650	600	MHz
PCI	-	1000	790	670	MHz
PCI-X	-	1000	790	670	MHz
Differential SSTL-2 Class I	8 mA	400	300	300	MHz
	12 mA	400	400	350	MHz
Differential SSTL-2 Class II	16 mA	350	350	300	MHz
	20 mA	400	350	350	MHz
	24 mA	400	400	350	MHz

Table 4–91. Stratix II GX Maximum Output Clock Rate for Column Pins (Part 3 of 3)

I/O Standard	Drive Strength	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
Differential SSTL-18 Class I	4 mA	200	150	150	MHz
	6 mA	350	250	200	MHz
	8 mA	450	300	300	MHz
	10 mA	500	400	400	MHz
	12 mA	700	550	400	MHz
Differential SSTL-18 Class II	8 mA	200	200	150	MHz
	16 mA	400	350	350	MHz
	18 mA	450	400	400	MHz
	20 mA	550	500	450	MHz
1.8-V HSTL differential Class I	4 mA	300	300	300	MHz
	6 mA	500	450	450	MHz
	8 mA	650	600	600	MHz
	10 mA	700	650	600	MHz
	12 mA	700	700	650	MHz
1.8-V HSTL differential Class II	16 mA	500	500	450	MHz
	18 mA	550	500	500	MHz
	20 mA	650	550	550	MHz
1.5-V HSTL differential Class I	4 mA	350	300	300	MHz
	6 mA	500	500	450	MHz
	8 mA	700	650	600	MHz
	10 mA	700	700	650	MHz
	12 mA	700	700	700	MHz
1.5-V HSTL differential Class II	16 mA	600	600	550	MHz
	18 mA	650	600	600	MHz
	20 mA	700	650	600	MHz

Note to Table 4–91:
(1) This is the default setting in the Quartus II software.

Table 4–92 shows the maximum output clock toggle rates for Stratix II GX device row pins.

Table 4–92. Stratix II GX Maximum Output Clock Rate for Row Pins (Part 1 of 2)

I/O Standard	Drive Strength	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
LVTTL	4 mA	270	225	210	MHz
	8 mA	435	355	325	MHz
	12 mA *(1)*	580	475	420	MHz
LVCMOS	4 mA	290	250	230	MHz
	8 mA	565	480	440	MHz
	12 mA *(1)*	350	350	297	MHz
2.5 V	4 mA	230	194	180	MHz
	8 mA	430	380	380	MHz
	12 mA *(1)*	630	575	550	MHz
1.8 V	2 mA	120	109	104	MHz
	4 mA	285	250	230	MHz
	6 mA	450	390	360	MHz
	8 mA *(1)*	660	570	520	MHz
1.5 V	2 mA	244	200	180	MHz
	4 mA *(1)*	470	370	325	MHz
SSTL-2 Class I	8 mA	400	300	300	MHz
	12 mA *(1)*	400	400	350	MHz
SSTL-2 Class II	16 mA	350	350	300	MHz
	20 mA *(1)*	350	350	297	MHz
SSTL-18 Class I	4 mA	200	150	150	MHz
	6 mA	350	250	200	MHz
	8 mA	450	300	300	MHz
	10 mA	500	400	400	MHz
	12 mA *(1)*	350	350	297	MHz
1.8-V HSTL Class I	4 mA	300	300	300	MHz
	6 mA	500	450	450	MHz
	8 mA	650	600	600	MHz
	10 mA	700	650	600	MHz
	12 mA *(1)*	700	700	650	MHz
1.5-V HSTL Class I	4 mA	350	300	300	MHz
	6 mA	500	500	450	MHz
	8 mA *(1)*	700	650	600	MHz

Table 4–92. Stratix II GX Maximum Output Clock Rate for Row Pins (Part 2 of 2)

I/O Standard	Drive Strength	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
Differential SSTL-2 Class I	8 mA	400	300	300	MHz
	12 mA	400	400	350	MHz
Differential SSTL-2 Class II	16 mA *(1)*	350	350	300	MHz
Differential SSTL-18 Class I	4 mA	200	150	150	MHz
	6 mA	350	250	200	MHz
	8 mA	450	300	300	MHz
	10 mA *(1)*	500	400	400	MHz
LVDS	-	717	717	640	MHz
HyperTransport	-	717	717	640	MHz

Note to Table 4–92:
(1) This is the default setting in Quartus II software.

Table 4–93 shows the maximum output clock toggle rate for Stratix II GX device dedicated clock pins.

Table 4–93. Stratix II GX Maximum Output Clock Rate for Dedicated Clock Pins (Part 1 of 4)

I/O Standard	Drive Strength	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
LVTTL	4 mA	270	225	210	MHz
	8 mA	435	355	325	MHz
	12 mA	580	475	420	MHz
	16 mA	720	594	520	MHz
	20 mA	875	700	610	MHz
	24 mA *(1)*	1030	794	670	MHz
LVCMOS	4 mA	290	250	230	MHz
	8 mA	565	480	440	MHz
	12 mA	790	710	670	MHz
	16 mA	1020	925	875	MHz
	20 mA	1066	985	935	MHz
	24 mA *(1)*	1100	1040	1000	MHz

Table 4–93. Stratix II GX Maximum Output Clock Rate for Dedicated Clock Pins (Part 2 of 4)

I/O Standard	Drive Strength	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
2.5 V	4 mA	230	194	180	MHz
	8 mA	430	380	380	MHz
	12 mA	630	575	550	MHz
	16 mA *(1)*	930	845	820	MHz
1.8 V	2 mA	120	109	104	MHz
	4 mA	285	250	230	MHz
	6 mA	450	390	360	MHz
	8 mA	660	570	520	MHz
	10 mA	905	805	755	MHz
	12 mA *(1)*	1131	1040	990	MHz
1.5 V	2 mA	244	200	180	MHz
	4 mA	470	370	325	MHz
	6 mA	550	430	375	MHz
	8 mA *(1)*	625	495	420	MHz
SSTL-2 Class I	8 mA	400	300	300	MHz
	12 mA *(1)*	400	400	350	MHz
SSTL-2 Class II	16 mA	350	350	300	MHz
	20 mA	400	350	350	MHz
	24 mA *(1)*	400	400	350	MHz
SSTL-18 Class I	4 mA	200	150	150	MHz
	6 mA	350	250	200	MHz
	8 mA	450	300	300	MHz
	10 mA	500	400	400	MHz
	12 mA *(1)*	650	550	400	MHz
SSTL-18 Class II	8 mA	200	200	150	MHz
	16 mA	400	350	350	MHz
	18 mA	450	400	400	MHz
	20 mA *(1)*	550	500	450	MHz
1.8-V HSTL Class I	4 mA	300	300	300	MHz
	6 mA	500	450	450	MHz
	8 mA	650	600	600	MHz
	10 mA	700	650	600	MHz
	12 mA *(1)*	700	700	650	MHz

Table 4–93. Stratix II GX Maximum Output Clock Rate for Dedicated Clock Pins (Part 3 of 4)

I/O Standard	Drive Strength	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
1.8-V HSTL Class II	16 mA	500	500	450	MHz
	18 mA	550	500	500	MHz
	20 mA *(1)*	550	550	550	MHz
1.5-V HSTL Class I	4 mA	350	300	300	MHz
	6 mA	500	500	450	MHz
	8 mA	700	650	600	MHz
	10 mA	700	700	650	MHz
	12 mA *(1)*	700	700	700	MHz
1.5-V HSTL Class II	16 mA	600	600	550	MHz
	18 mA	650	600	600	MHz
	20 mA *(1)*	700	650	600	MHz
PCI	-	1000	790	670	MHz
PCI-X	-	1000	790	670	MHz
Differential SSTL-2 Class I	8 mA	400	300	300	MHz
	12 mA	400	400	350	MHz
Differential SSTL-2 Class II	16 mA	350	350	300	MHz
	20 mA	400	350	350	MHz
	24 mA	400	400	350	MHz
Differential SSTL-18 Class I	4 mA	200	150	150	MHz
	6 mA	350	250	200	MHz
	8 mA	450	300	300	MHz
	10 mA	500	400	400	MHz
	12 mA	650	550	400	MHz
Differential SSTL-18 Class II	8 mA	200	200	150	MHz
	16 mA	400	350	350	MHz
	18 mA	450	400	400	MHz
	20 mA	550	500	450	MHz
1.8-V differential Class I	4 mA	300	300	300	MHz
	6 mA	500	450	450	MHz
	8 mA	650	600	600	MHz
	10 mA	700	650	600	MHz
	12 mA	700	700	650	MHz

Table 4–93. Stratix II GX Maximum Output Clock Rate for Dedicated Clock Pins (Part 4 of 4)

I/O Standard	Drive Strength	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
1.8-V differential Class II	16 mA	500	500	450	MHz
	18 mA	550	500	500	MHz
	20 mA	550	550	550	MHz
1.5-V differential Class I	4 mA	350	300	300	MHz
	6 mA	500	500	450	MHz
	8 mA	700	650	600	MHz
	10 mA	700	700	650	MHz
	12 mA	700	700	700	MHz
1.5-V differential Class II	16 mA	600	600	550	MHz
	18 mA	650	600	600	MHz
	20 mA	700	650	600	MHz
HyperTransport	-	300	250	125	MHz
LVPECL	-	450	400	300	MHz

Note to Table 4–93:
(1) This is the default setting in Quartus II software.

Table 4–94 shows the maximum output clock toggle rate for Stratix II GX device series-terminated column pins.

Table 4–94. Stratix II GX Maximum Output Clock Rate for Column Pins (Series Termination) (Part 1 of 2)

I/O Standard	Drive Strength	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
LVTTL	OCT_25_OHMS	400	400	350	MHz
	OCT_50_OHMS	400	400	350	MHz
LVCMOS	OCT_25_OHMS	350	350	300	MHz
	OCT_50_OHMS	350	350	300	MHz
2.5 V	OCT_25_OHMS	350	350	300	MHz
	OCT_50_OHMS	350	350	300	MHz
1.8 V	OCT_25_OHMS	700	550	450	MHz
	OCT_50_OHMS	700	550	450	MHz
1.5 V	OCT_50_OHMS	550	450	400	MHz
SSTL-2 Class I	OCT_50_OHMS	600	500	500	MHz
SSTL-2 Class II	OCT_25_OHMS	600	550	500	MHz

Table 4–94. Stratix II GX Maximum Output Clock Rate for Column Pins (Series Termination) (Part 2 of 2)

I/O Standard	Drive Strength	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
SSTL-18 Class I	OCT_50_OHMS	560	400	350	MHz
SSTL-18 Class II	OCT_25_OHMS	550	500	450	MHz
1.5-V HSTL Class I	OCT_50_OHMS	600	550	500	MHz
1.8-V HSTL Class I	OCT_50_OHMS	650	600	600	MHz
1.8-V HSTL Class II	OCT_25_OHMS	500	500	450	MHz
Differential SSTL-2 Class I	OCT_50_OHMS	600	500	500	MHz
Differential SSTL-2 Class II	OCT_25_OHMS	600	550	500	MHz
Differential SSTL-18 Class I	OCT_50_OHMS	560	400	350	MHz
Differential SSTL-18 Class II	OCT_25_OHMS	550	500	450	MHz
1.8-V differential HSTL Class I	OCT_50_OHMS	650	600	600	MHz
1.8-V differential HSTL Class II	OCT_25_OHMS	500	500	450	MHz
1.5-V differential HSTL Class I	OCT_50_OHMS	600	550	500	MHz

Table 4–95 shows the maximum output clock toggle rate for Stratix II GX device series-terminated row pins.

Table 4–95. Stratix II GX Maximum Output Clock Rate for Row Pins (Series Termination) (Part 1 of 2)

I/O Standard	Drive Strength	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
LVTTL	OCT_25_OHMS	400	400	350	MHz
	OCT_50_OHMS	400	400	350	MHz
LVCMOS	OCT_25_OHMS	350	350	300	MHz
	OCT_50_OHMS	350	350	300	MHz
2.5 V	OCT_25_OHMS	350	350	300	MHz
	OCT_50_OHMS	350	350	300	MHz
1.8 V	OCT_50_OHMS	700	550	450	MHz
1.5 V	OCT_50_OHMS	550	450	400	MHz

Table 4–95. Stratix II GX Maximum Output Clock Rate for Row Pins (Series Termination) (Part 2 of 2)

I/O Standard	Drive Strength	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
SSTL-2 Class I	OCT_50_OHMS	600	500	500	MHz
SSTL-2 Class II	OCT_25_OHMS	600	550	500	MHz
SSTL-18 Class I	OCT_50_OHMS	590	400	350	MHz
1.5-V HSTL Class I	OCT_50_OHMS	600	550	500	MHz
1.8-V HSTL Class I	OCT_50_OHMS	650	600	600	MHz
Differential SSTL-2 Class I	OCT_50_OHMS	600	500	500	MHz
Differential SSTL-2 Class II	OCT_25_OHMS	600	550	500	MHz
Differential SSTL-18 Class I	OCT_50_OHMS	590	400	350	MHz
Differential HSTL-18 Class I	OCT_50_OHMS	650	600	600	MHz
Differential HSTL-15 Class I	OCT_50_OHMS	600	550	500	

Table 4–96 shows the maximum output clock toggle rate for Stratix II GX device series-terminated dedicated clock pins.

Table 4–96. Stratix II GX Maximum Output Clock Rate for Dedicated Clock Pins (Series Termination) (Part 1 of 2)

I/O Standard	Drive Strength	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
LVTTL	OCT_25_OHMS	400	400	350	MHz
	OCT_50_OHMS	400	400	350	MHz
LVCMOS	OCT_25_OHMS	350	350	300	MHz
	OCT_50_OHMS	350	350	300	MHz
2.5 V	OCT_25_OHMS	350	350	300	MHz
	OCT_50_OHMS	350	350	300	MHz
1.8 V	OCT_25_OHMS	700	550	450	MHz
	OCT_50_OHMS	700	550	450	MHz
1.5 V	OCT_50_OHMS	550	450	400	MHz
SSTL-2 Class I	OCT_50_OHMS	600	500	500	MHz
SSTL-2 Class II	OCT_25_OHMS	600	550	500	MHz
SSTL-18 Class I	OCT_50_OHMS	450	400	350	MHz

Table 4–96. Stratix II GX Maximum Output Clock Rate for Dedicated Clock Pins (Series Termination) (Part 2 of 2)

I/O Standard	Drive Strength	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
SSTL-18 Class II	OCT_25_OHMS	550	500	450	MHz
1.5-V HSTL Class I	OCT_50_OHMS	600	550	500	MHz
1.8-V HSTL Class I	OCT_50_OHMS	650	600	600	MHz
1.8-V HSTL Class II	OCT_25_OHMS	500	500	450	MHz
DIfferential SSTL-2 Class I	OCT_50_OHMS	600	500	500	MHz
DIfferential SSTL-2 Class II	OCT_25_OHMS	600	550	500	MHz
DIfferential SSTL-18 Class I	OCT_50_OHMS	560	400	350	MHz
DIfferential SSTL-18 Class II	OCT_25_OHMS	550	500	450	MHz
1.8-V differential HSTL Class I	OCT_50_OHMS	650	600	600	MHz
1.8-V differential HSTL Class II	OCT_25_OHMS	500	500	450	MHz
1.5-V differential HSTL Class I	OCT_50_OHMS	600	550	500	MHz

Table 4–97 specifies the derating factors for the output clock toggle rate for a non 0 pF load.

Table 4–97. Maximum Output Clock Toggle Rate Derating Factors (Part 1 of 5)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
3.3-V LVTTL	4 mA	478	510	510	478	510	510	466	510	510
	8 mA	260	333	333	260	333	333	291	333	333
	12 mA	213	247	247	213	247	247	211	247	247
	16 mA	136	197	197	-	-	-	166	197	197
	20 mA	138	187	187	-	-	-	154	187	187
	24 mA	134	177	177	-	-	-	143	177	177

Table 4–97. Maximum Output Clock Toggle Rate Derating Factors (Part 2 of 5)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
3.3-V LVCMOS	4 mA	377	391	391	377	391	391	377	391	391
	8 mA	206	212	212	206	212	212	178	212	212
	12 mA	141	145	145	-	-	-	115	145	145
	16 mA	108	111	111	-	-	-	86	111	111
	20 mA	83	88	88	-	-	-	79	88	88
	24 mA	65	72	72	-	-	-	74	72	72
2.5-V LVTTL/ LVCMOS	4 mA	387	427	427	387	427	427	391	427	427
	8 mA	163	224	224	163	224	224	170	224	224
	12 mA	142	203	203	142	203	203	152	203	203
	16 mA	120	182	182	-	-	-	134	182	182
1.8-V LVTTL/ LVCMOS	2 mA	951	1,421	1,421	951	1,421	1,421	904	1,421	1,421
	4 mA	405	516	516	405	516	516	393	516	516
	6 mA	261	325	325	261	325	325	253	325	325
	8 mA	223	274	274	223	274	274	224	274	274
	10 mA	194	236	236	-	-	-	199	236	236
	12 mA	174	209	209	-	-	-	180	209	209
1.5-V LVTTL/ LVCMOS	2 mA	652	963	963	652	963	963	618	963	963
	4 mA	333	347	347	333	347	347	270	347	347
	6 mA	182	247	247	-	-	-	198	247	247
	8 mA	135	194	194	-	-	-	155	194	194
SSTL-2 Class I	8 mA	364	680	680	364	680	680	350	680	680
	12 mA	163	207	207	163	207	207	188	207	207
SSTL-2 Class II	16 mA	118	147	147	118	147	147	94	147	147
	20 mA	99	122	122	-	-	-	87	122	122
	24 mA	91	116	116	-	-	-	85	116	116
SSTL-18 Class I	4 mA	458	570	570	458	570	570	505	570	570
	6 mA	305	380	380	305	380	380	336	380	380
	8 mA	225	282	282	225	282	282	248	282	282
	10 mA	167	220	220	167	220	220	190	220	220
	12 mA	129	175	175	-	-	-	148	175	175

Table 4–97. Maximum Output Clock Toggle Rate Derating Factors (Part 3 of 5)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
SSTL-18 Class II	8 mA	173	206	206	-	-	-	155	206	206
	16 mA	150	160	160	-	-	-	140	160	160
	18 mA	120	130	130	-	-	-	110	130	130
	20 mA	109	127	127	-	-	-	94	127	127
2.5-V SSTL-2 Class I	8 mA	364	680	680	364	680	680	350	680	680
	12 mA	163	207	207	163	207	207	188	207	207
2.5-V SSTL-2 Class II	16 mA	118	147	147	118	147	147	94	147	147
	20 mA	99	122	122	-	-	-	87	122	122
	24 mA	91	116	116	-	-	-	85	116	116
1.8-V SSTL-18 Class I	4 mA	458	570	570	458	570	570	505	570	570
	6 mA	305	380	380	305	380	380	336	380	380
	8 mA	225	282	282	225	282	282	248	282	282
	10 mA	167	220	220	167	220	220	190	220	220
	12 mA	129	175	175	-	-	-	148	175	175
1.8-V SSTL-18 Class II	8 mA	173	206	206	-	-	-	155	206	206
	16 mA	150	160	160	-	-	-	140	160	160
	18 mA	120	130	130	-	-	-	110	130	130
	20 mA	109	127	127	-	-	-	94	127	127
1.8-V HSTL Class I	4 mA	245	282	282	245	282	282	229	282	282
	6 mA	164	188	188	164	188	188	153	188	188
	8 mA	123	140	140	123	140	140	114	140	140
	10 mA	110	124	124	110	124	124	108	124	124
	12 mA	97	110	110	97	110	110	104	110	110
1.8-V HSTL Class II	16 mA	101	104	104	-	-	-	99	104	104
	18 mA	98	102	102	-	-	-	93	102	102
	20 mA	93	99	99	-	-	-	88	99	99
1.5-V HSTL Class I	4 mA	168	196	196	168	196	196	188	196	196
	6 mA	112	131	131	112	131	131	125	131	131
	8 mA	84	99	99	84	99	99	95	99	99
	10 mA	87	98	98	-	-	-	90	98	98
	12 mA	86	98	98	-	-	-	87	98	98

Table 4–97. Maximum Output Clock Toggle Rate Derating Factors (Part 4 of 5)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
1.5-V HSTL Class II	16 mA	95	101	101	-	-	-	96	101	101
	18 mA	95	100	100	-	-	-	101	100	100
	20 mA	94	101	101	-	-	-	104	101	101
2.5-V differential SSTL Class II *(3)*	8 mA	364	680	680	-	-	-	350	680	680
	12 mA	163	207	207	-	-	-	188	207	207
	16 mA	118	147	147	-	-	-	94	147	147
	20 mA	99	122	122	-	-	-	87	122	122
	24 mA	91	116	116	-	-	-	85	116	116
1.8-V differential SSTL Class I *(3)*	4 mA	458	570	570	-	-	-	505	570	570
	6 mA	305	380	380	-	-	-	336	380	380
	8 mA	225	282	282	-	-	-	248	282	282
	10 mA	167	220	220	-	-	-	190	220	220
	12 mA	129	175	175	-	-	-	148	175	175
1.8-V differential SSTL Class II *(3)*	8 mA	173	206	206	-	-	-	155	206	206
	16 mA	150	160	160	-	-	-	140	160	160
	18 mA	120	130	130	-	-	-	110	130	130
	20 mA	109	127	127	-	-	-	94	127	127
1.8-V differential HSTL Class I *(3)*	4 mA	245	282	282	-	-	-	229	282	282
	6 mA	164	188	188	-	-	-	153	188	188
	8 mA	123	140	140	-	-	-	114	140	140
	10 mA	110	124	124	-	-	-	108	124	124
	12 mA	97	110	110	-	-	-	104	110	110
1.8-V differential HSTL Class II *(3)*	16 mA	101	104	104	-	-	-	99	104	104
	18 mA	98	102	102	-	-	-	93	102	102
	20 mA	93	99	99	-	-	-	88	99	99
1.5-V differential HSTL Class I *(3)*	4 mA	168	196	196	-	-	-	188	196	196
	6 mA	112	131	131	-	-	-	125	131	131
	8 mA	84	99	99	-	-	-	95	99	99
	10 mA	87	98	98	-	-	-	90	98	98
	12 mA	86	98	98	-	-	-	87	98	98

Table 4–97. Maximum Output Clock Toggle Rate Derating Factors (Part 5 of 5)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
1.5-V differential HSTL Class II *(3)*	16 mA	95	101	101	-	-	-	96	101	101
	18 mA	95	100	100	-	-	-	101	100	100
	20 mA	94	101	101	-	-	-	104	101	101
3.3-V PCI		134	177	177	-	-	-	143	177	177
3.3-V PCI-X		134	177	177	-	-	-	143	177	177
LVDS		-	-	-	155 *(1)*	155 *(1)*	155 *(1)*	134	134	134
LVPECL *(4)*		-	-	-	-	-	-	134	134	134
3.3-V LVTTL	OCT 50 Ω	133	152	152	133	152	152	147	152	152
2.5-V LVTTL	OCT 50 Ω	207	274	274	207	274	274	235	274	274
1.8-V LVTTL	OCT 50 Ω	151	165	165	151	165	165	153	165	165
3.3-V LVCMOS	OCT 50 Ω	300	316	316	300	316	316	263	316	316
1.5-V LVCMOS	OCT 50 Ω	157	171	171	157	171	171	174	171	171
SSTL-2 Class I	OCT 50 Ω	121	134	134	121	134	134	77	134	134
SSTL-2 Class II	OCT 25 Ω	56	101	101	56	101	101	58	101	101
SSTL-18 Class I	OCT 50 Ω	100	123	123	100	123	123	106	123	123
SSTL-18 Class II	OCT 25 Ω	61	110	110	-	-	-	59	110	110
1.2-V HSTL *(2)*	OCT 50 Ω	95	-	-	-	-	-	95	-	-

Notes to Table 4–97:

(1) For LVDS output on row I/O pins the toggle rate derating factors apply to loads larger than 5 pF. In the derating calculation, subtract 5 pF from the intended load value in pF for the correct result. For a load less than or equal to 5 pF, refer to Tables 4–91 through 4–95 for output toggle rates.

(2) 1.2-V HSTL is only supported on column I/O pins on -3 devices.

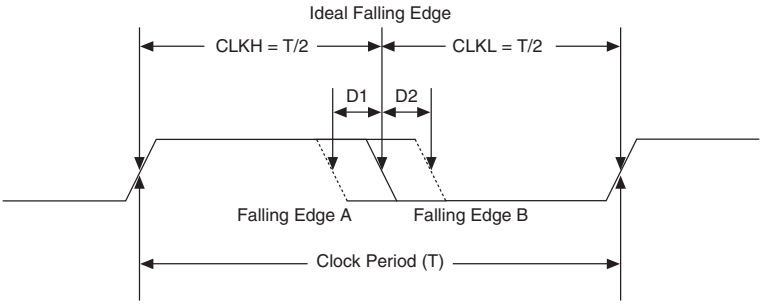
(3) Differential HSTL and SSTL is only supported on column clock and DQS outputs.

(4) LVPECL is only supported on column clock outputs.

Duty Cycle Distortion

Duty cycle distortion (DCD) describes how much the falling edge of a clock is off from its ideal position. The ideal position is when both the clock high time (CLKH) and the clock low time (CLKL) equal half of the clock period (T), as shown in Figure 4–11. DCD is the deviation of the non-ideal falling edge from the ideal falling edge, such as D1 for the falling edge A and D2 for the falling edge B (see Figure 4–11). The maximum DCD for a clock is the larger value of D1 and D2.

Figure 4–11. Duty Cycle Distortion



DCD expressed in absolution derivation, for example, D1 or D2 in Figure 4–11, is clock-period independent. DCD can also be expressed as a percentage, and the percentage number is clock-period dependent. DCD as a percentage is defined as:

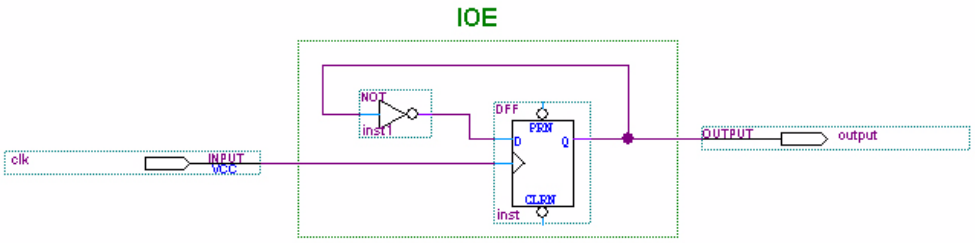
(T/2 – D1) / T (the low percentage boundary)

(T/2 + D2) / T (the high percentage boundary)

DCD Measurement Techniques

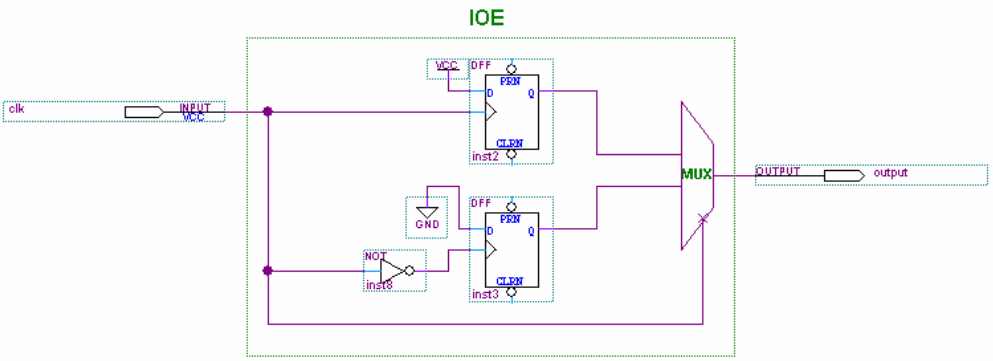
DCD is measured at an FPGA output pin driven by registers inside the corresponding I/O element (IOE) block. When the output is a single data rate signal (non-DDIO), only one edge of the register input clock (positive or negative) triggers output transitions (Figure 4–12). Therefore, any DCD present on the input clock signal or caused by the clock input buffer or different input I/O standard does not transfer to the output signal.

Figure 4–12. DCD Measurement Technique for Non-DDIO (Single-Data Rate) Outputs



However, when the output is a double data rate input/output (DDIO) signal, both edges of the input clock signal (positive and negative) trigger output transitions (Figure 4–13). Therefore, any distortion on the input clock and the input clock buffer affect the output DCD.

Figure 4–13. DCD Measurement Technique for DDIO (Double-Data Rate) Outputs



When an FPGA PLL generates the internal clock, the PLL output clocks the IOE block. As the PLL only monitors the positive edge of the reference clock input and internally re-creates the output clock signal, any DCD present on the reference clock is filtered out. Therefore, the DCD for a DDIO output with PLL in the clock path is better than the DCD for a DDIO output without PLL in the clock path.

Tables 4–98 through 4–105 show the maximum DCD in absolution derivation for different I/O standards on Stratix II GX devices. Examples are also provided that show how to calculate DCD as a percentage.

Table 4–98. Maximum DCD for Non-DDIO Output on Row I/O Pins

Row I/O Output Standard	Maximum DCD (ps) for Non-DDIO Output		
	-3 Devices	-4 and -5 Devices	Unit
3.3-V LVTTTL	245	275	ps
3.3-V LVCMOS	125	155	ps
2.5 V	105	135	ps
1.8 V	180	180	ps
1.5-V LVCMOS	165	195	ps
SSTL-2 Class I	115	145	ps
SSTL-2 Class II	95	125	ps
SSTL-18 Class I	55	85	ps
1.8-V HSTL Class I	80	100	ps
1.5-V HSTL Class I	85	115	ps
LVDS	55	80	ps

Here is an example for calculating the DCD as a percentage for a non-DDIO output on a row I/O on a -3 device:

If the non-DDIO output I/O standard is SSTL-2 Class II, the maximum DCD is 95 ps (see Table 4–99). If the clock frequency is 267 MHz, the clock period T is:

T = 1/ f = 1 / 267 MHz = 3.745 ns = 3,745 ps

To calculate the DCD as a percentage:

(T/2 – DCD) / T = (3,745 ps/2 – 95 ps) / 3,745 ps = 47.5% (for low boundary)

(T/2 + DCD) / T = (3,745 ps/2 + 95 ps) / 3,745 ps = 52.5% (for high boundary)

Therefore, the DCD percentage for the output clock at 267 MHz is from 47.5% to 52.5%.

Table 4–99. Maximum DCD for Non-DDIO Output on Column I/O Pins

Column I/O Output Standard I/O Standard	Maximum DCD (ps) for Non-DDIO Output		Unit
	-3 Devices	-4 and -5 Devices	
3.3-V LVTTL	190	220	ps
3.3-V LVCMOS	140	175	ps
2.5 V	125	155	ps
1.8 V	80	110	ps
1.5-V LVCMOS	185	215	ps
SSTL-2 Class I	105	135	ps
SSTL-2 Class II	100	130	ps
SSTL-18 Class I	90	115	ps
SSTL-18 Class II	70	100	ps
1.8-V HSTL Class I	80	110	ps
1.8-V HSTL Class II	80	110	ps
1.5-V HSTL Class I	85	115	ps
1.5-V HSTL Class II	50	80	ps
1.2-V HSTL-12	170	200	ps
LVPECL	55	80	ps

Table 4–100. Maximum DCD for DDIO Output on Row I/O Pins Without PLL in the Clock Path for -3 Devices *Note (1)*

Maximum DCD (ps) for Row DDIO Output I/O Standard	Input I/O Standard (No PLL in Clock Path)					Unit
	TTL/CMOS		SSTL-2	SSTL/HSTL	LVDS	
	3.3 and 2.5 V	1.8 and 1.5 V	2.5 V	1.8 and 1.5 V	3.3 V	
3.3-V LVTTL	260	380	145	145	110	ps
3.3-V LVCMOS	210	330	100	100	65	ps
2.5 V	195	315	85	85	75	ps
1.8 V	150	265	85	85	120	ps
1.5-V LVCMOS	255	370	140	140	105	ps
SSTL-2 Class I	175	295	65	65	70	ps
SSTL-2 Class II	170	290	60	60	75	ps
SSTL-18 Class I	155	275	55	50	90	ps
1.8-V HSTL Class I	150	270	60	60	95	ps
1.5-V HSTL Class I	150	270	55	55	90	ps
LVDS	180	180	180	180	180	ps

Note to Table 4–100:

(1) The information in Table 4–100 assumes the input clock has zero DCD.

Here is an example for calculating the DCD in percentage for a DDIO output on a row I/O on a -3 device:

If the input I/O standard is 2.5-V SSTL-2 and the DDIO output I/O standard is SSTL-2 Class= II, the maximum DCD is 60 ps (see Table 4–100). If the clock frequency is 267 MHz, the clock period T is:

T = 1/ f = 1 / 267 MHz = 3.745 ns = 3,745 ps

Calculate the DCD as a percentage:

(T/2 – DCD) / T = (3,745 ps/2 – 60 ps) / 3745 ps = 48.4% (for low boundary)

(T/2 + DCD) / T = (3,745 ps/2 + 60 ps) / 3745 ps = 51.6% (for high boundary)

Therefore, the DCD percentage for the output clock is from 48.4% to 51.6%.

Table 4–101. Maximum DCD for DDIO Output on Row I/O Pins Without PLL in the Clock Path for -4 and -5 Devices *Note (1)*

Maximum DCD (ps) for Row DDIO Output I/O Standard	Input I/O Standard (No PLL in the Clock Path)					Unit
	TTL/CMOS		SSTL-2	SSTL/HSTL	LVDS	
	3.3/2.5V	1.8/1.5V	2.5V	1.8/1.5V	3.3V	
3.3-V LVTTL	440	495	170	160	105	ps
3.3-V LVCMOS	390	450	120	110	75	ps
2.5 V	375	430	105	95	90	ps
1.8 V	325	385	90	100	135	ps
1.5-V LVCMOS	430	490	160	155	100	ps
SSTL-2 Class I	355	410	85	75	85	ps
SSTL-2 Class II	350	405	80	70	90	ps
SSTL-18 Class I	335	390	65	65	105	ps
1.8-V HSTL Class I	330	385	60	70	110	ps
1.5-V HSTL Class I	330	390	60	70	105	ps
LVDS	180	180	180	180	180	ps

Note to Table 4–101:

(1) Table 4–101 assumes the input clock has zero DCD.

Table 4–102. Maximum DCD for DDIO Output on Column I/O Pins Without PLL in the Clock Path for -3 Devices (Part 1 of 2) *Note (1)*

Maximum DCD (ps) for DDIO Column Output I/O Standard	Input IO Standard (No PLL in the Clock Path)					Unit
	TTL/CMOS		SSTL-2	SSTL/HSTL	HSTL12	
	3.3/2.5V	1.8/1.5V	2.5V	1.8/1.5V	1.2V	
3.3-V LVTTL	260	380	145	145	145	ps
3.3-V LVCMOS	210	330	100	100	100	ps
2.5 V	195	315	85	85	85	ps
1.8 V	150	265	85	85	85	ps
1.5-V LVCMOS	255	370	140	140	140	ps
SSTL-2 Class I	175	295	65	65	65	ps
SSTL-2 Class II	170	290	60	60	60	ps
SSTL-18 Class I	155	275	55	50	50	ps

Table 4–102. Maximum DCD for DDIO Output on Column I/O Pins Without PLL in the Clock Path for -3 Devices (Part 2 of 2) *Note (1)*

Maximum DCD (ps) for DDIO Column Output I/O Standard	Input IO Standard (No PLL in the Clock Path)					Unit
	TTL/CMOS		SSTL-2	SSTL/HSTL	HSTL12	
	3.3/2.5V	1.8/1.5V	2.5V	1.8/1.5V	1.2V	
SSTL-18 Class II	140	260	70	70	70	ps
1.8-V HSTL Class I	150	270	60	60	60	ps
1.8-V HSTL Class II	150	270	60	60	60	ps
1.5-V HSTL Class I	150	270	55	55	55	ps
1.5-V HSTL Class II	125	240	85	85	85	ps
1.2-V HSTL	240	360	155	155	155	ps
LVPECL	180	180	180	180	180	ps

Note to Table 4–102:
(1) Table 4–102 assumes the input clock has zero DCD.

Table 4–103. Maximum DCD for DDIO Output on Column I/O Pins Without PLL in the Clock Path for -4 and -5 Devices *Note (1)*

Maximum DCD (ps) for DDIO Column Output I/O Standard	Input IO Standard (No PLL in the Clock Path)				Unit
	TTL/CMOS		SSTL-2	SSTL/HSTL	
	3.3/2.5V	1.8/1.5V	2.5V	1.8/1.5V	
3.3-V LVTTL	440	495	170	160	ps
3.3-V LVCMOS	390	450	120	110	ps
2.5 V	375	430	105	95	ps
1.8 V	325	385	90	100	ps
1.5-V LVCMOS	430	490	160	155	ps
SSTL-2 Class I	355	410	85	75	ps
SSTL-2 Class II	350	405	80	70	ps
SSTL-18 Class I	335	390	65	65	ps
SSTL-18 Class II	320	375	70	80	ps
1.8-V HSTL Class I	330	385	60	70	ps
1.8-V HSTL Class II	330	385	60	70	ps
1.5-V HSTL Class I	330	390	60	70	ps
1.5-V HSTL Class II	330	360	90	100	ps
LVPECL	180	180	180	180	ps

Note to Table 4–103:
(1) Table 4–103 assumes the input clock has zero DCD.

Table 4–104. Maximum DCD for DDIO Output on Row I/O Pins With PLL in the Clock Path

Maximum DCD (ps) for Row DDIO Output I/O Standard	Stratix II GX Devices (PLL Output Feeding DDIO)		Unit
	-3 Device	-4 and -5 Device	
3.3-V LVTTL	110	105	ps
3.3-V LVCMOS	65	75	ps
2.5V	75	90	ps
1.8V	85	100	ps
1.5-V LVCMOS	105	100	ps
SSTL-2 Class I	65	75	ps
SSTL-2 Class II	60	70	ps
SSTL-18 Class I	50	65	ps
1.8-V HSTL Class I	50	70	ps
1.5-V HSTL Class I	55	70	ps
LVDS	180	180	ps

Table 4–105. Maximum DCD for DDIO Output on Column I/O Pins With PLL in the Clock Path (Part 1 of 2)

Maximum DCD (ps) for Column DDIO Output I/O Standard	Stratix II GX Devices (PLL Output Feeding DDIO)		Unit
	-3 Device	-4 and -5 Device	
3.3-V LVTTL	145	160	ps
3.3-V LVCMOS	100	110	ps
2.5V	85	95	ps
1.8V	85	100	ps
1.5-V LVCMOS	140	155	ps
SSTL-2 Class I	65	75	ps
SSTL-2 Class II	60	70	ps
SSTL-18 Class I	50	65	ps
SSTL-18 Class II	70	80	ps
1.8-V HSTL Class I	60	70	ps
1.8-V HSTL Class II	60	70	ps
1.5-V HSTL Class I	55	70	ps
1.5-V HSTL Class II	85	100	ps

Table 4–105. Maximum DCD for DDIO Output on Column I/O Pins With PLL in the Clock Path (Part 2 of 2)

Maximum DCD (ps) for Column DDIO Output I/O Standard	Stratix II GX Devices (PLL Output Feeding DDIO)		Unit
	-3 Device	-4 and -5 Device	
1.2-V HSTL	155	155	ps
LVPECL	180	180	ps

High-Speed I/O Specifications

Table 4–106 provides high-speed timing specifications definitions.

Table 4–106. High-Speed Timing Specifications and Definitions

High-Speed Timing Specifications	Definitions
t_C	High-speed receiver/transmitter input and output clock period.
f_{HSCLK}	High-speed receiver/transmitter input and output clock frequency.
J	Deserialization factor (width of parallel data bus).
W	PLL multiplication factor.
t_{RISE}	Low-to-high transmission time.
t_{FALL}	High-to-low transmission time.
Timing unit interval (TUI)	The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency × Multiplication Factor) = t_C/w).
f_{IN}	Fast PLL input clock frequency
f_{HSDR}	Maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
$f_{HSDRDPA}$	Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
Channel-to-channel skew (TCCS)	The timing difference between the fastest and the slowest output edges including t_{CO} variation and clock skew across channels driven by the same fast PLL. The clock is included in the TCCS measurement.
Sampling window (SW)	The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window.
Input jitter	Peak-to-peak input jitter on high-speed PLLs.
Output jitter	Peak-to-peak output jitter on high-speed PLLs.
t_{DUTY}	Duty cycle on high-speed transmitter output clock.
t_{LOCK}	Lock time for high-speed transmitter and receiver PLLs.

Table 4–107 shows the high-speed I/O timing specifications for -3 speed grade Stratix II GX devices.

Table 4–107. High-Speed I/O Specifications for -3 Speed Grade *Notes (1), (2)*

Symbol	Conditions			-3 Speed Grade			Unit
				Min	Typ	Max	
$f_{IN} = f_{HSDR} / W$	W = 2 to 32 (LVDS, HyperTransport technology) *(3)*			16		520	MHz
	W = 1 (SERDES bypass, LVDS only)			16		500	MHz
	W = 1 (SERDES used, LVDS only)			150		717	MHz
f_{HSDR} (data rate)	J = 4 to 10 (LVDS, HyperTransport technology)			150		1,040	Mbps
	J = 2 (LVDS, HyperTransport technology)			*(4)*		760	Mbps
	J = 1 (LVDS only)			*(4)*		500	Mbps
$f_{HSDRDPA}$ (DPA data rate)	J = 4 to 10 (LVDS, HyperTransport technology)			150		1,040	Mbps
TCCS	All differential standards			-		200	ps
SW	All differential standards			330		-	ps
Output jitter						190	ps
Output t_{RISE}	All differential I/O standards					160	ps
Output t_{FALL}	All differential I/O standards					180	ps
t_{DUTY}				45	50	55	%
DPA run length						6,400	UI
DPA jitter tolerance *(5)*	Data channel peak-to-peak jitter			0.44			UI
DPA lock time	**Standard**	**Training Pattern**	**Transition Density**				Number of repetitions
	SPI-4	0000000000 1111111111	10%	256			
	Parallel Rapid I/O	00001111	25%	256			
		10010000	50%	256			
	Miscellaneous	10101010	100%	256			
		01010101		256			

Notes to Table 4–107:

(1) When J = 4 to 10, the SERDES block is used.

(2) When J = 1 or 2, the SERDES block is bypassed.

(3) The input clock frequency and the W factor must satisfy the following fast PLL VCO specification: 150 ≤ input clock frequency × W ≤ 1,040.

(4) The minimum specification is dependent on the clock source (fast PLL, enhanced PLL, clock pin, and so on) and the clock routing resource (global, regional, or local) utilized. The I/O differential buffer and input register do not have a minimum toggle rate.

(5) For setup details, refer to the characterization report.

Table 4–108 shows the high-speed I/O timing specifications for -4 speed grade Stratix II GX devices.

Table 4–108. High-Speed I/O Specifications for -4 Speed Grade *Notes (1), (2)*

Symbol	Conditions			-4 Speed Grade			Unit
				Min	Typ	Max	
$f_{IN} = f_{HSDR} / W$	W = 2 to 32 (LVDS, HyperTransport technology) *(3)*			16		520	MHz
	W = 1 (SERDES bypass, LVDS only)			16		500	MHz
	W = 1 (SERDES used, LVDS only)			150		717	MHz
f_{HSDR} (data rate)	J = 4 to 10 (LVDS, HyperTransport technology)			150		1,040	Mbps
	J = 2 (LVDS, HyperTransport technology)			*(4)*		760	Mbps
	J = 1 (LVDS only)			*(4)*		500	Mbps
$f_{HSDRDPA}$ (DPA data rate)	J = 4 to 10 (LVDS, HyperTransport technology)			150		1,040	Mbps
TCCS	All differential standards			-		200	ps
SW	All differential standards			330		-	ps
Output jitter						190	ps
Output t_{RISE}	All differential I/O standards					160	ps
Output t_{FALL}	All differential I/O standards					180	ps
t_{DUTY}				45	50	55	%
DPA run length						6,400	UI
DPA jitter tolerance	Data channel peak-to-peak jitter			0.44			UI
DPA lock time	**Standard**	**Training Pattern**	**Transition Density**				Number of repetitions
	SPI-4	0000000000 1111111111	10%	256			
	Parallel Rapid I/O	00001111	25%	256			
		10010000	50%	256			
	Miscellaneous	10101010	100%	256			
		01010101		256			

Notes to Table 4–108:

(1) When J = 4 to 10, the SERDES block is used.

(2) When J = 1 or 2, the SERDES block is bypassed.

(3) The input clock frequency and the W factor must satisfy the following fast PLL VCO specification: 150 ≤ input clock frequency × W ≤ 1,040.

(4) The minimum specification is dependent on the clock source (fast PLL, enhanced PLL, clock pin, and so on) and the clock routing resource (global, regional, or local) utilized. The I/O differential buffer and input register do not have a minimum toggle rate.

Table 4–109 shows the high-speed I/O timing specifications for -5 speed grade Stratix II GX devices.

Table 4–109. High-Speed I/O Specifications for -5 Speed Grade *Notes (1), (2)*

Symbol	Conditions			-5 Speed Grade			Unit
				Min	Typ	Max	
$f_{IN} = f_{HSDR} / W$	W = 2 to 32 (LVDS, HyperTransport technology) *(3)*			16		420	MHz
	W = 1 (SERDES bypass, LVDS only)			16		500	MHz
	W = 1 (SERDES used, LVDS only)			150		640	MHz
f_{HSDR} (data rate)	J = 4 to 10 (LVDS, HyperTransport technology)			150		840	Mbps
	J = 2 (LVDS, HyperTransport technology)			*(4)*		700	Mbps
	J = 1 (LVDS only)			*(4)*		500	Mbps
$f_{HSDRDPA}$ (DPA data rate)	J = 4 to 10 (LVDS, HyperTransport technology)			150		840	Mbps
TCCS	All differential I/O standards			-		200	ps
SW	All differential I/O standards			440		-	ps
Output jitter						190	ps
Output t_{RISE}	All differential I/O standards					290	ps
Output t_{FALL}	All differential I/O standards					290	ps
t_{DUTY}				45	50	55	%
DPA run length						6,400	UI
DPA jitter tolerance	Data channel peak-to-peak jitter			0.44			UI
DPA lock time	**Standard**	**Training Pattern**	**Transition Density**				Number of repetitions
	SPI-4	0000000000 1111111111	10%	256			
	Parallel Rapid I/O	00001111	25%	256			
		10010000	50%	256			
	Miscellaneous	10101010	100%	256			
		01010101		256			

Notes to Table 4–109:

(1) When J = 4 to 10, the SERDES block is used.

(2) When J = 1 or 2, the SERDES block is bypassed.

(3) The input clock frequency and the W factor must satisfy the following fast PLL VCO specification: 150 ≤ input clock frequency × W ≤ 840.

(4) The minimum specification is dependent on the clock source (fast PLL, enhanced PLL, clock pin, and so on) and the clock routing resource (global, regional, or local) utilized. The I/O differential buffer and input register do not have a minimum toggle rate.

PLL Timing Specifications

Tables 4–110 and 4–111 describe the Stratix II GX PLL specifications when operating in both the commercial junction temperature range (0 to 85 C) and the industrial junction temperature range (–40 to 100 C), except for the clock switchover and phase-shift stepping features. These two features are only supported from the 0 to 100 C junction temperature range.

Table 4–110. Enhanced PLL Specifications (Part 1 of 2)

Name	Description	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	4		500	MHz
f_{INPFD}	Input frequency to the PFD	4		420	MHz
f_{INDUTY}	Input clock duty cycle	40		60	%
f_{ENDUTY}	External feedback input clock duty cycle	40		60	%
$t_{INJITTER}$	Input or external feedback clock input jitter tolerance in terms of period jitter. Bandwidth ≤0.85 MHz		0.5		ns (peak-to-peak)
	Input or external feedback clock input jitter tolerance in terms of period jitter. Bandwidth > 0.85 MHz		1.0		ns (peak-to-peak)
$t_{OUTJITTER}$	Dedicated clock output period jitter			250 ps for ≥ 100 MHz outclk 25 mUI for < 100 MHz outclk	ps or mUI (p-p)
t_{FCOMP}	External feedback compensation time			10	ns
f_{OUT}	Output frequency for internal global or regional clock	1.5 *(2)*		550	MHz
$f_{OUTDUTY}$	Duty cycle for external clock output	45	50	55	%
$f_{SCANCLK}$	Scanclk frequency			100	MHz
$t_{CONFIGEPLL}$	Time required to reconfigure scan chains for EPLLs		$174/f_{SCANCLK}$		ns
f_{OUT_EXT}	PLL external clock output frequency	1.5 *(2)*		*(1)*	MHz
t_{LOCK}	Time required for the PLL to lock from the time it is enabled or the end of device configuration		0.03	1	ms
t_{DLOCK}	Time required for the PLL to lock dynamically after automatic clock switchover between two identical clock frequencies			1	ms
$f_{SWITCHOVER}$	Frequency range where the clock switchover performs properly	1.5	1	500	MHz
f_{CLBW}	PLL closed-loop bandwidth	0.13	1.2	16.9	MHz

Table 4–110. Enhanced PLL Specifications (Part 2 of 2)

Name	Description	Min	Typ	Max	Unit
f_{VCO}	PLL VCO operating range for –3 and –4 speed grade devices	300		1,040	MHz
	PLL VCO operating range for –5 speed grade devices	300		840	MHz
f_{SS}	Spread-spectrum modulation frequency	100		500	kHz
% spread	Percent down spread for a given clock frequency	0.4	0.5	0.6	%
t_{PLL_PSERR}	Accuracy of PLL phase shift			±30	ps
t_{ARESET}	Minimum pulse width on `areset` signal.	10			ns
$t_{ARESET\_RECONFIG}$	Minimum pulse width on the `areset` signal when using PLL reconfiguration. Reset the PLL after `scandone` goes high.	500			ns
$t_{RECONFIGWAIT}$	The time required for the wait after the reconfiguration is done and the areset is applied.			2	us

Notes to Table 4–110:

(1) This is limited by the I/O f_{MAX}. See Tables 4–91 through 4–95 for the maximum.

(2) If the counter cascading feature of the PLL is utilized, there is no minimum output clock frequency.

Table 4–111. Fast PLL Specifications (Part 1 of 2)

Name	Description	Min	Typ	Max	Unit
f_{IN}	Input clock frequency (for -3 and -4 speed grade devices)	16		717	MHz
	Input clock frequency (for -5 speed grade devices)	16		640	MHz
f_{INPFD}	Input frequency to the PFD	16		500	MHz
f_{INDUTY}	Input clock duty cycle	40		60	%
$t_{INJITTER}$	Input clock jitter tolerance in terms of period jitter. Bandwidth ≤2 MHz		0.5		ns (p-p)
	Input clock jitter tolerance in terms of period jitter. Bandwidth > 0.2 MHz		1.0		ns (p-p)

Table 4–111. Fast PLL Specifications (Part 2 of 2)

Name	Description	Min	Typ	Max	Unit
f_{VCO}	Upper VCO frequency range for –3 and –4 speed grades	300		1,040	MHz
	Upper VCO frequency range for –5 speed grades	300		840	MHz
	Lower VCO frequency range for –3 and –4 speed grades	150		520	MHz
	Lower VCO frequency range for –5 speed grades	150		420	MHz
f_{OUT}	PLL output frequency to GCLK or RCLK	4.6875		550	MHz
	PLL output frequency to LVDS or DPA clock	150		1,040	MHz
f_{OUT_EXT}	PLL clock output frequency to regular I/O	4.6875		*(1)*	MHz
$t_{CONFIGPLL}$	Time required to reconfigure scan chains for fast PLLs		$75/f_{SCANCLK}$		ns
f_{CLBW}	PLL closed-loop bandwidth	1.16	5	28	MHz
t_{LOCK}	Time required for the PLL to lock from the time it is enabled or the end of the device configuration		0.03	1	ms
t_{PLL_PSERR}	Accuracy of PLL phase shift			±30	ps
t_{ARESET}	Minimum pulse width on areset signal.	10			ns
$t_{ARESET\_RECONFIG}$	Minimum pulse width on the areset signal when using PLL reconfiguration. Reset the PLL after scandone goes high.	500			ns

Notes to Table 4–111:
(1) This is limited by the I/O f_{MAX}. See Tables 4–91 through 4–95 for the maximum.

External Memory Interface Specifications

Tables 4–112 through 4–116 contain Stratix II GX device specifications for the dedicated circuitry used for interfacing with external memory devices.

Table 4–112. DLL Frequency Range Specifications (Part 1 of 2)

Frequency Mode	Frequency Range (MHz)	Resolution (Degrees)
0	100 to 175	30
1	150 to 230	22.5
2	200 to 350 (–3 speed grade)	30
	200 to 310 (–4 and –5 speed grade)	30

Table 4–112. DLL Frequency Range Specifications (Part 2 of 2)		
Frequency Mode	**Frequency Range (MHz)**	**Resolution (Degrees)**
3	240 to 400 (–3 speed grade)	36
	240 to 350 (–4 and –5 speed grade)	36

Table 4–113. DQS Jitter Specifications for DLL-Delayed Clock (t_{DQS_JITTER}) Note (1)		
Number of DQS Delay Buffer Stages (2)	**Commercial (ps)**	**Industrial (ps)**
1	80	110
2	110	130
3	130	180
4	160	210

Notes to Table 4–113:

(1) Peak-to-peak period jitter on the phase-shifted DQS clock. For example, jitter on two delay stages under commercial conditions is 200 ps peak-to-peak or 100 ps.

(2) Delay stages used for requested DQS phase shift are reported in a project's Compilation Report in the Quartus II software.

Table 4–114. DQS Phase-Shift Error Specifications for DLL-Delayed Clock (t_{DQS_PSERR})			
Number of DQS Delay Buffer Stages (1)	**–3 Speed Grade (ps)**	**–4 Speed Grade (ps)**	**–5 Speed Grade (ps)**
1	25	30	35
2	50	60	70
3	75	90	105
4	100	120	140

Note to Table 4–114:

(1) Delay stages used for request DQS phase shift are reported in a project's Compilation Report in the Quartus II software. For example, phase-shift error on two delay stages under -3 conditions is 50 ps peak-to-peak or 25 ps.

Table 4–115. DQS Bus Clock Skew Adder Specifications (t_{DQS}_CLOCK_SKEW_ADDER)

Mode	DQS Clock Skew Adder (ps) *(1)*
4 DQ per DQS	40
9 DQ per DQS	70
18 DQ per DQS	75
36 DQ per DQS	95

Note to Table 4–115:
(1) This skew specification is the absolute maximum and minimum skew. For example, skew on a 40 DQ group is 40 ps or 20 ps.

Table 4–116. DQS Phase Offset Delay Per Stage (ps) Notes (1), (2), (3)

Speed Grade	Positive Offset		Negative Offset	
	Min	Max	Min	Max
-3	10	15	8	11
-4	10	15	8	11
-5	10	16	8	12

Notes to Table 4–116:
(1) The delay settings are linear.
(2) The valid settings for phase offset are -32 to +31.
(3) The typical value equals the average of the minimum and maximum values.

JTAG Timing Specifications

Figure 4–14 shows the timing requirements for the JTAG signals

Figure 4–14. Stratix II GX JTAG Waveforms.

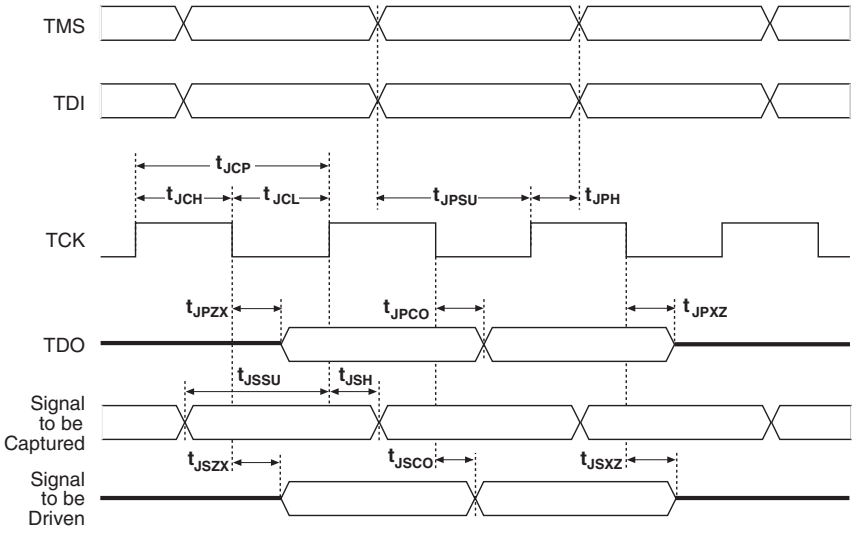


Table 4–117 shows the JTAG timing parameters and values for Stratix II GX devices.

Table 4–117. Stratix II GX JTAG Timing Parameters and Values

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	30		ns
t_{JCH}	TCK clock high time	12		ns
t_{JCL}	TCK clock low time	12		ns
t_{JPSU}	JTAG port setup time	4		ns
t_{JPH}	JTAG port hold time	5		ns
t_{JPCO}	JTAG port clock to output		9	ns
t_{JPZX}	JTAG port high impedance to valid output		9	ns
t_{JPXZ}	JTAG port valid output to high impedance		9	ns
t_{JSSU}	Capture register setup time	4		ns
t_{JSH}	Capture register hold time	5		ns
t_{JSCO}	Update register clock to output		12	ns
t_{JSZX}	Update register high impedance to valid output		12	ns
t_{JSXZ}	Update register valid output to high impedance		12	ns

Referenced Documents

This chapter references the following documents:

- *Operating Requirements for Altera Devices Data Sheet*
- *PowerPlay Power Analyzer* chapter in volume 3 of the *Quartus II Handbook*.
- *PowerPlay Early Power Estimator (EPE) and Power Analyzer*
- *Quartus II PowerPlay Analysis and Optimization Technology*
- *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*
- *Stratix II GX Transceiver Architecture Overview* chapter in volume 2 of the *Stratix II GX Device Handbook*
- Volume 2, *Stratix II GX Device Handbook*

Document Revision History

Table 6–105 shows the revision history for this chapter.

Table 4–118. Document Revision History (Part 1 of 5)

Date and Document Version	Changes Made	Summary of Changes
June 2009 v4.6	Replaced Table 4–31 Updated: • Table 4–5 • Table 4–6 • Table 4–7 • Table 4–8 • Table 4–9 • Table 4–10 • Table 4–11 • Table 4–12 • Table 4–13 • Table 4–14 • Table 4–15 • Table 4–16 • Table 4–17 • Table 4–18 • Table 4–20 • Table 4–50 • Table 4–95 • Table 4–105 • Table 4–110 • Table 4–111	
October 2007 v4.5	Updated: • Table 4–3 • Table 4–6 • Table 4–16 • Table 4–19 • Table 4–20 • Table 4–21 • Table 4–22 • Table 4–55 • Table 4–106 • Table 4–107 • Table 4–108 • Table 4–109 • Table 4–112	
	Updated title only in Tables 4–88 and 4–89.	
	Minor text edits.	

Table 4–118. Document Revision History (Part 2 of 5)

Date and Document Version	Changes Made	Summary of Changes
August 2007 v4.4	Removed note "The data in this table is preliminary. Altera will provide a report upon completion of characterization of the Stratix II GX devices. Conditions for testing the silicon have not been determined." from each table.	
	Removed note "The data in Tables xxx through xxx is preliminary. Altera will provide a report upon completion of characterization of the Stratix II GX devices. Conditions for testing the silicon have not been determined." in the clock timing parameters sections.	
	Updated clock timing parameter Tables 4–63 through 4–78 (Table 4–75 was unchanged).	
	Updated Table 4–21 and added new Table 4–22.	
	Updated: ● Table 4–6 ● Table 4–16 ● Table 4–19 ● Table 4–49 ● Table 4–52 ● Table 4–107	
	Added note to Table 4–50.	
	Added: ● Figure 4–3 ● Figure 4–4 ● Figure 4–5	
	Added the "Referenced Documents" section.	
May 2007 v4.3	Changed 1.875 KHz to 1.875 MHz in Table 4–19, XAUI Receiver Jitter Tolerance section.	

Table 4–118. Document Revision History (Part 3 of 5)

Date and Document Version	Changes Made	Summary of Changes
February 2007 v4.2	Added the "Document Revision History" section to this chapter.	Added support information for the Stratix II GX device.
	Updated Table 4–5: • Removed last three lines • Removed note 1 • Added new note 4	
	Deleted table 6-6.	
	Replaced Table 4–6 with all new information.	
	Added Figures 4–1 and 4–2.	
	Added Tables 4–7 through 4–19.	
	Removed Figures 6-1 through 6-4.	
	Updated Table 4–22: • Changed R_{CONF} information.	
	Updated Table 4–52 • SSTL-18 Class I, column 1: changed 25 to 50.	
	Updated: • Table 4–54 • Table 4–87 • Table 4–91 • Table 4–94	
	Updated Tables 4–62 through 4–77	
	Updated Tables 4–79 and 4–80 • Added "units" column	
	Updated Tables 4–83 through 4–86 • Changed column title to "Fast Corner Industrial/Commercial".	
	Updated Table 4–109. • Added a new line to the bottom of the table.	
August 2006 v4.1	Update Table 6–75, Table 6–84, and Table 6–90.	

Table 4–118. Document Revision History (Part 4 of 5)

Date and Document Version	Changes Made	Summary of Changes
June 2006, v4.0	• Updated Table 6–5. • Updated Table 6–6. • Updated all values in Table 6–7. • Added Tables 6–8 and 6–9. • Added Figures 6–1 through 6–4. • Updated Table 6–18. • Updated Tables 6–85 through 6–96. • Added Table 6–80, Stratix II GX Maximum Output Clock Rate for Dedicated Clock Pins. • Updated Table 6–100. • In "I/O Timing Measurement Methodology" section, updated Table 6–42. • In "Internal Timing Parameters" section, updated Tables 6–43 through 6–48. • In "Stratix II GX Clock Timing Parameters" section, updated Tables 6–50 through 6–65. • In "IOE Programmable Delay" section, updated Tables 6–67 and 6–68. • In "I/O Delays" section, updated Tables 6–71 through 6–74. • In "Maximum Input & Output Clock Toggle Rate" section, updated Tables 6–75 through 6–83. • In "DCD Measurement Techniques" section, updated Tables 6–85 through 6–92. • In "High-Speed I/O Specifications" section, updated Tables 6–94 through 6–96. • In "External Memory Interface Specifications" section, updated Table 6–100.	• Removed rows for V_{ID}, V_{OD}, V_{ICM}, and V_{OCM} from Table 6–5. • Updated values for rx, tx, and `refclkb` in Table 6–6. • Removed table containing 1.2-V PCML I/O information. That information is in Table 6–7. • Added values to Table 6–100.

Table 4–118. Document Revision History (Part 5 of 5)

Date and Document Version	Changes Made	Summary of Changes
April 2006, v3.0	• Updated Table 6–3. • Updated Table 6–5. • Updated Table 6–7. • Added Table 6–42. • Updated "Internal Timing Parameters" section (Tables 6–43 through 6–48). • Updated "Stratix II GX Clock Timing Parameters" section (Tables 6–49 through 6–65). • Updated "IOE Programmable Delay" section (Tables 6–67 and 6–68) • Updated "I/O Delays" section (Tables 6–71 through 6–74. • Updated "Maximum Input & Output Clock Toggle Rate" section. Replaced tables 6-73 and 6-74 with Tables 6–75 through 6–83. Input and output clock rates for row, column, and dedicated clock pins are now in separate tables.	
February 2006, v2.1	• Updated Tables 6–4 and 6–5. • Updated Tables 6–49 through 6–65 (removed column designations for industrial/commercial and removed industrial numbers).	
December 2005, v2.0	Updated timing numbers.	
October 2005 v1.1	• Updated Table 6–7. • Updated Table 6–38. • Updated 3.3-V PCML information and notes to Tables 6–73 through 6–76. • Minor textual changes throughout the document.	
October 2005 v1.0	Added chapter to the *Stratix II GX Device Handbook*.	