



# CAM3908 CMOS Mini Color Camera Head User Manual

***Dr Robot®***

Version: 1.0.0  
APRIL 2005

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## Related Document:

WiRobot PMB5010 Multimedia Controller User Manual

## 1. Overview

This camera Module is designed for Mobile communication tools, which consists of CIF CMOS sensor and Digital signal processor to convert input video signal(digital) of CIF CMOS sensor to CIF/QCIF/QQCIF/QVGA/QQVGA formats.

### 1-1. Feature

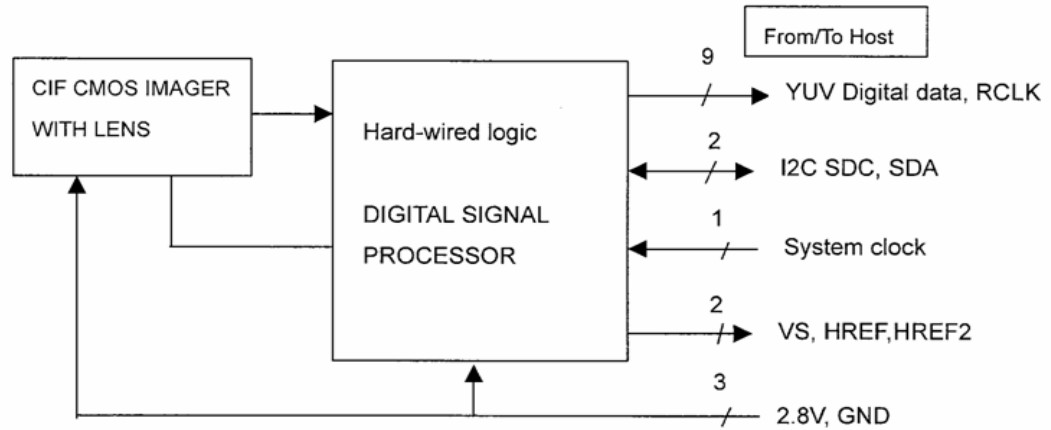
- Thinner built-in lens CMOS imager with CIF resolution
  - Dedicated DSP by hard-wired logic with operating voltage of  $+2.5V \pm 10\%$
  - Supply voltage  $+2.80V \pm 0.2V$
- Power consumption: typ. 45 mW at 15 fps
- Smaller and thinner size for built-in camera inside Mobile phone

### 1-2. Function

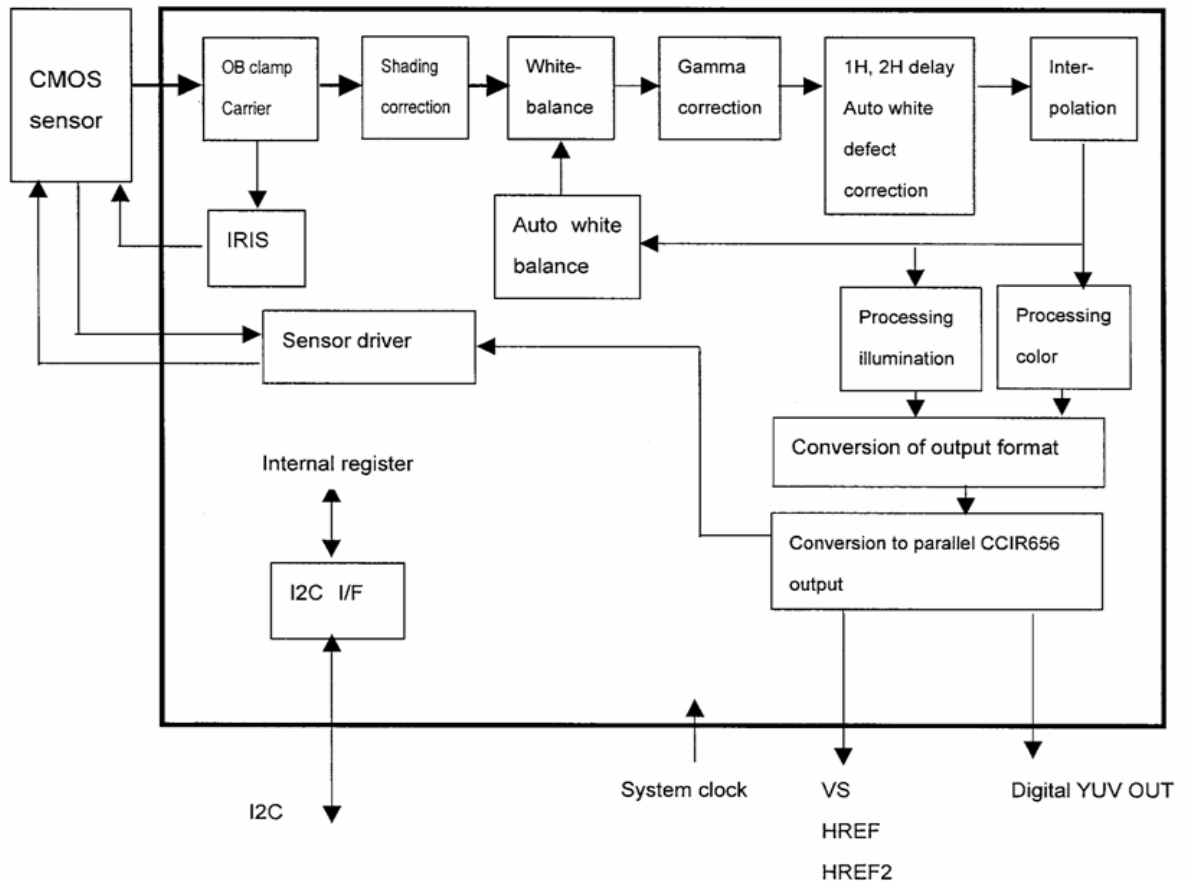
- With CIF CMOS sensor, digital parallel output in CIF/QCIF/QQCIF/ QVGA/QQVGA format is available.
- UYVY digital parallel output is available.
- Includes the function of generating sync signal of CIF CMOS sensor.
- It is able to construct video camera only from this LSI and CIF CMOS sensor.
- It is able to change parameters, which is necessary for video signal processing.
- Auto exposure control is included.
- Auto white-balance control is included.
- Auto carrier-balance control is included..
- Auto correction of white defects is included.
- Shading correction control is included.

## 2. CAMERA MODULE BLOCK DIAGRAM

Below shows block diagram of the CIF camera module .



### 2-1. Block diagram of DSP



## 2-2. Pin assignment

| NO | NAME    | I/O | CONTENTS                                      |
|----|---------|-----|-----------------------------------------------|
| 1  | GND     | -   | Ground                                        |
| 2  | SCL     | I/O | I2C Serial Clock                              |
| 3  | SDA     | I/O | I2C Data                                      |
| 4  | STDBY   | I   | Stand -by input                               |
| 5  | VS      | OUT | Digital image vertical blank pulse output     |
| 6  | NC      | -   | Non connection                                |
| 7  | NC      | -   | Non connection                                |
| 8  | AVDD    | I   | DC2.8V for CMOS sensor                        |
| 9  | NC      | -   | Non connection                                |
| 10 | NC      | -   | Non connection                                |
| 11 | RCLK2   | OUT | Digital YUV signal separation signal output   |
| 12 | NC      | -   | Non connection                                |
| 13 | NC      | -   | Non connection                                |
| 14 | CKI     | I   | System clock input (9MHz)                     |
| 15 | MITYPEZ | I   | Camera serial device address select input     |
| 16 | DAS     | I   | Camera serial DAS device address input        |
| 17 | TEST4   | I   | Camera self-test input (Normal : Open)        |
| 18 | VDD2    | I   | DC 2.8V for I/O pin                           |
| 19 | GND     | -   | Ground                                        |
| 20 | RSTN    | I   | Camera reset input (Low active)               |
| 21 | EEPINIT | I   | EEPROM data auto loading enable/disable input |
| 22 | RCLK    | O   | Digital YUV signal synchronized clock output  |
| 23 | HREF2   | OUT | Digital image horizontal blank pulse output 2 |
| 24 | HREF    | OUT | Digital image horizontal blank pulse output   |
| 25 | GND     | -   | Ground                                        |
| 26 | OD0     | OUT | Digital YUV-signal output(LSB)                |
| 27 | OD1     | OUT | Digital YUV-signal output                     |
| 28 | OD2     | OUT | Digital YUV-signal output                     |
| 29 | OD3     | OUT | Digital YUV-signal output                     |
| 30 | OD4     | OUT | Digital YUV-signal output                     |
| 31 | OD5     | OUT | Digital YUV-signal output                     |
| 32 | OD6     | OUT | Digital YUV-signal output                     |
| 33 | OD7     | OUT | Digital YUV-signal output ( MSB )             |
| 34 | NC      | -   | Non connection                                |
| 35 | NC      | -   | Non connection                                |
| 36 | VDD1    | I   | DC2.8V for DSP                                |

### 3. SIGNAL INTERFACE FORMATS

#### 3-1 CAMERA CLOCK

Available input clock to this module is System\_clk.

MODE1(clock selector) allows to select the clock to use.

##### 3-1-1 SYSTEM CLK: 9MHz input

Input clock from outside is supplied to CMOS sensor through SCKO of DSP after dividing according to DSP\_CTRL1[7:5](CLK\_MODE). Examples are described in Table 3-1.

Table 3-1: Operation examples

| CMOS Sensor | System_clk frequency | DSP_CTRL1[7:5] (CLK_MODE) | CMOS sensor Clock frequency | Operation frame rate |
|-------------|----------------------|---------------------------|-----------------------------|----------------------|
| CIF         | 9MHz                 | 30fps(000): 1/1 clock     | 9MHz                        | 30fps (NOTE)         |
|             |                      | 15fps(001): 1/2 clock     | 4.5MHz                      | 15fps                |
|             |                      | 10fps(010): 1/3 clock     | 3MHz                        | 10fps                |
|             |                      | 6fps(011): 1/5 clock      | 6MHz                        | 6fps                 |
|             |                      | 5fps(100): 1/6 clock      | 6MHz                        | 5fps                 |
|             |                      | 3fps(101): 1/10 clock     | 3MHz                        | 3fps                 |
|             |                      | 2fps(110): 1/15 clock     | 2MHz                        | 2fps                 |
|             |                      | 1fps(111): 1/30 clock     | 1MHz                        | 1fps                 |

(NOTE) Camera performance can not be guaranteed at 30 fps.

#### 3-2 Digital Image output

##### 3-2-1 Image format

In addition to CIF, shrink or cut out to QVGA/QQVGA/QCIF/QQCIF formats can be applied. Capture image size can be changed by capture start position(HCAPS, VCAPS) and capture end position(HCAPE, VCAPE). It is able to adapt to CIF sensor/CIF mode by setting of register MOS\_CTRL1[7:6](MOS\_TYPE).

Available settings are described table 3-2.

| Processing image size |                 |               | Image parameter<br>DSP_CTRL1[2:0]<br>(RESIZE) | Output image size |                 |               |
|-----------------------|-----------------|---------------|-----------------------------------------------|-------------------|-----------------|---------------|
|                       | Horizontal size | Vertical size |                                               |                   | Horizontal size | Vertical size |
| CIF                   | 352             | 288           | X 1 (000)                                     | CIF               | 352             | 288           |
| CIF                   | 352             | 288           | X 1/2 (001)                                   | QCIF              | 176             | 144           |
| CIF                   | 352             | 288           | X 1/4 (010)                                   | QQCIF             | 88              | 72            |
| QCIF                  | 176             | 144           | X 1 (000)                                     | QCIF              | 176             | 144           |
| QCIF                  | 176             | 144           | X 1/2 (001)                                   | QQCIF             | 88              | 72            |
| QVGA                  | 320             | 240           | X 1 (000)                                     | QVGA              | 320             | 240           |
| QVGA                  | 320             | 240           | X 1/2 (001)                                   | QQVGA             | 160             | 120           |

Table 3-2: Output conversion in using CIF sensor

### 3-2-2 Parallel data output

Parallel output from data output pin with basically-complied CCIR=656 is available.

It is able to adapt to CIF sensor/CIF mode by setting to the register MOS\_CTRL1[7:6] (MOS\_TYPE). And also adapt to YUV (each component is 8bits, YUV output: OUT\_SEL = "00"), UYVY (each component is 8bits, UYVY output: OUT\_SEL = "01"), RGB (each component 8bits, RGB output: OUT\_SEL = "10") by setting to the register DSP\_CTRL3[5:4] (OUT\_SEL). Maximum frame rate is 15fps.

### 3-3 I2C interface

I2C interface of this LSI has the functions that can be read/written from external hosts.

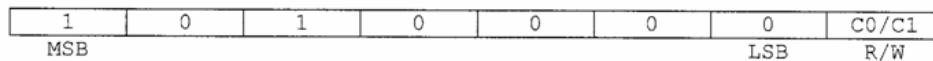
After power-on, the LSI waits for register written from external hosts (WFLG=1).

SDA: Data I/O port from external hosts

SDC: Clock input from external hosts

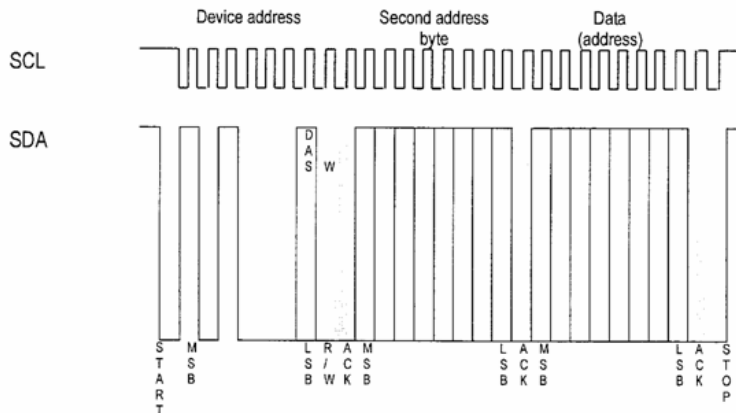
### 3-3-1 Camera module address

Device address from external hosts is shown in following.

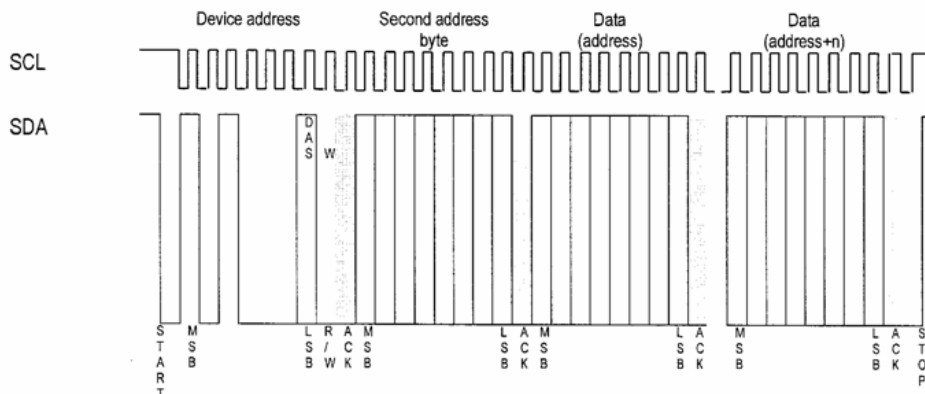


### 3-3-2 Write from external hosts

(1) Writing one Byte register ( example )

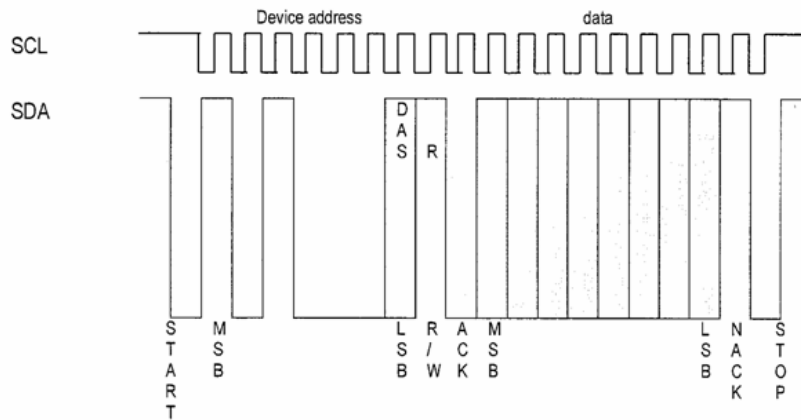


(2) Writing Block registers ( example )

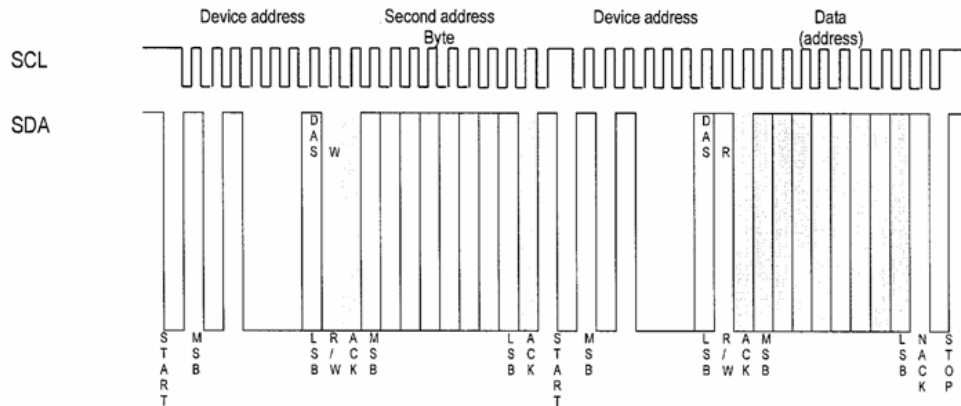


### 3-3-3 Read to external hosts

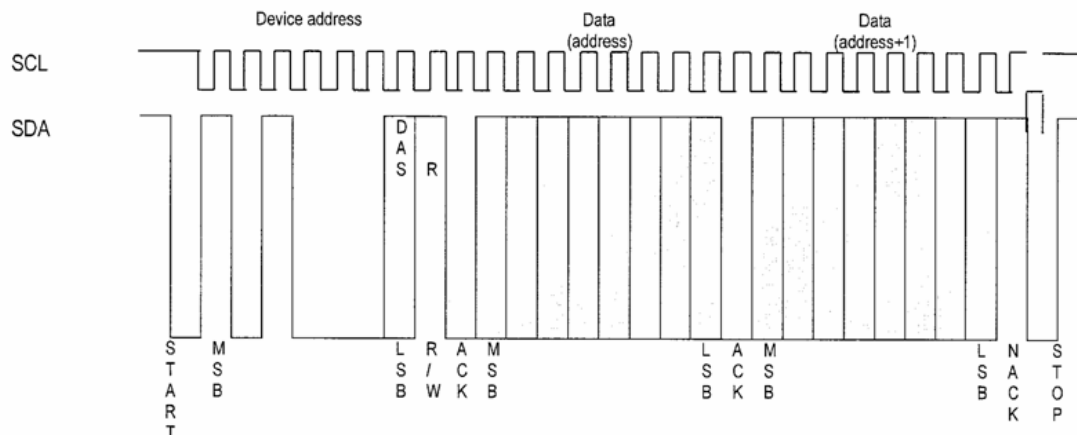
#### (1) Reading Current address register (example )



#### (2) Reading Random registers ( example )



#### (3) Reading Sequential register ( example )



#### ( NOTE )

Below addresses range is not available to read with "Reading Sequential register".

RANGE 0X00EFh ~ 0X00FFh

Either "Reading Current register" or "Reading Random registers" is available to read out a data for addresses of 0X00EFh ~ 0X00FFh.

## 4. CAMERA SYSTEM SPECIFICATIONS

### 4-1. Absolute Maximum Rating

| Item                 | Symbol          | Rated value  | Unit | Note                     |
|----------------------|-----------------|--------------|------|--------------------------|
| Power supply voltage | 2.8V            | -0.3~4.3     | V    | AVDD, VDD1, VDD2         |
| Input voltage        | V <sub>I2</sub> | -0.3~VDD+0.3 | V    | System_clk, SDA, SDC     |
| Output voltage       | V <sub>O1</sub> | -0.3~VDD+0.3 | V    | YUVDData, RCLK, VS, HREF |

### 4-2. RECOMMENDED OPERATING CONDITION

| Item                      | Symbol           | MIN. | TYP. | MAX. | Unit | Note                    |
|---------------------------|------------------|------|------|------|------|-------------------------|
| Power supply voltage      | 2.8V             | 2.60 | 2.80 | 3.0  | V    | VDD                     |
| Operating temperature     | T <sub>OPR</sub> | -20  | 25   | 60   | °C   |                         |
| Storage temperature       | T <sub>STG</sub> | -20  | 25   | 70   | °C   |                         |
| Operating frequency       | f <sub>OPR</sub> | 1.0  | 9.0  | -    | MHz  | System_clk              |
| Power consumption         |                  |      | 45   |      | mW   | CIF at 15 fps           |
| Standby Power consumption |                  |      | TBD  |      | mW   | CIF at 15 fps           |
| Operating humidity        | H <sub>OPR</sub> |      |      | TBD  | %    | never condense into dew |

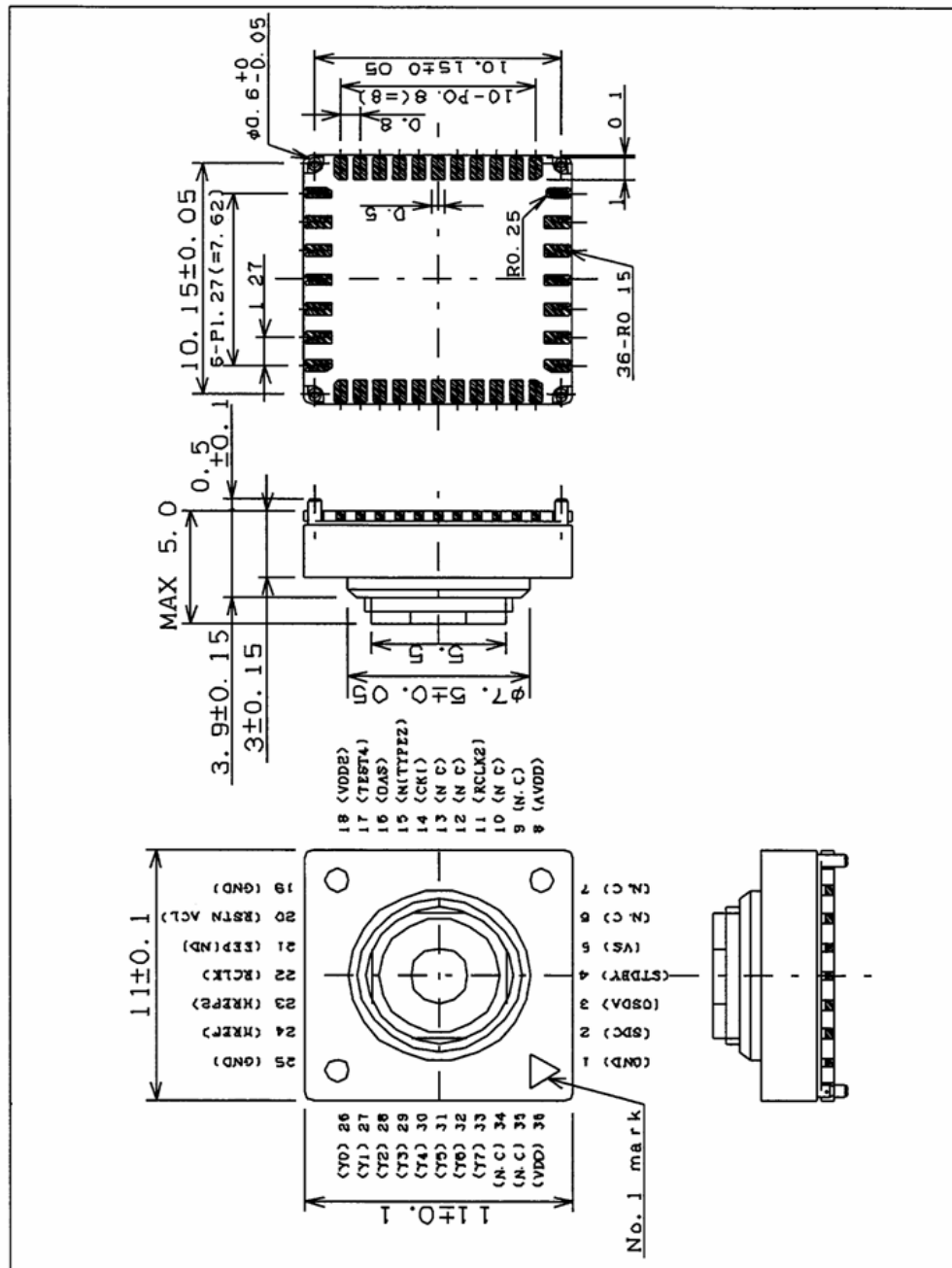
### 4-3. CAMERA PERFORMANCE

| Items                              | Specification |          |      |          |                   |
|------------------------------------|---------------|----------|------|----------|-------------------|
|                                    | Min.          | Typ.     | Max. | Unit     | Others            |
| Horizontal Resolution              | 150           |          |      | TV-line  | Image center      |
| γ correction                       |               | 0.45     |      | —        | Adjustable by I2C |
| Fastest Electronic shutter speed   |               | 1/9,900  |      | sec      |                   |
| Slowest Electronic shutter speed   |               | 1        |      | sec      |                   |
| Image SN                           | 43 (TBD)      |          |      | dB       | Adjustable by I2C |
| Image Dynamic range                | 57 (TBD)      |          |      | dB       | Adjustable by I2C |
| Minimum object illumination (25°C) |               |          | 10   | lux      | at 15 fps         |
| Low object illumination (40°C)     |               |          | 100  | lux      | at 15 fps         |
| Maximum object illumination (25°C) | 50,000        |          |      | lux      | at 15 fps         |
| AGC maximum gain                   |               | 20 (TBD) |      | dB       | Adjustable by I2C |
| AGC minimum gain                   |               | 3 (TBD)  |      | dB       | Adjustable by I2C |
| Maximum color temperature by AWB   |               | 100000   |      | degree K | Adjustable by I2C |
| Minimum color temperature by AWB   |               | 2500     |      | degree K | Adjustable by I2C |
| Maximum Frame rate                 |               | 15       |      | fps      |                   |
| Minimum Frame rate                 |               | 1        |      | fps      |                   |

#### 4-4. OPTICAL PERFORMANCE

| ITEM                            | CHARACTERISTICS                             | OTHERS                                                  |
|---------------------------------|---------------------------------------------|---------------------------------------------------------|
| Number of Lens elements         | Aspheric single lens                        | for 1/7"                                                |
| Material of Lens element        | Higher heat-proof plastic                   |                                                         |
| View angle in Horizontal        | typ. 58deg.                                 | for the image area of<br>H2.06mm x V1.63mm<br>(D2.63mm) |
| View angle in Vertical          | typ. 46 deg.                                |                                                         |
| View angle in Diagonal          | typ. 73 deg.                                |                                                         |
| Image circle                    | Approx. Ø2.63mm<br>Effective circle Ø2.63mm |                                                         |
| Focal length                    | 2.0 mm $\pm$ 5 %                            |                                                         |
| F number                        | 2.8 $\pm$ 5 %                               |                                                         |
| Image distortion                | Approx. -4.0 % at the edge of Image         | TV distortion                                           |
| Focus range                     | 20 cm – Infinity                            |                                                         |
| MTF center                      | 80 LP/mm                                    | at MTF 30%                                              |
| circumference (70%)             | 45 LP/mm                                    | at MTF 30%                                              |
| Material of Lens holder         | Plastic PPS (GF30%)                         |                                                         |
| Material to support Lens Barrel | Plastic PC (GF20%)                          |                                                         |
| IR cut filter                   | Spattered on glass lid                      |                                                         |
| Optical LPF                     | not built-in                                |                                                         |

#### 4-5-1. Dimensions



## 5. ELECTRICAL CHARACTERISTICS

### 5-1. DC Characteristics

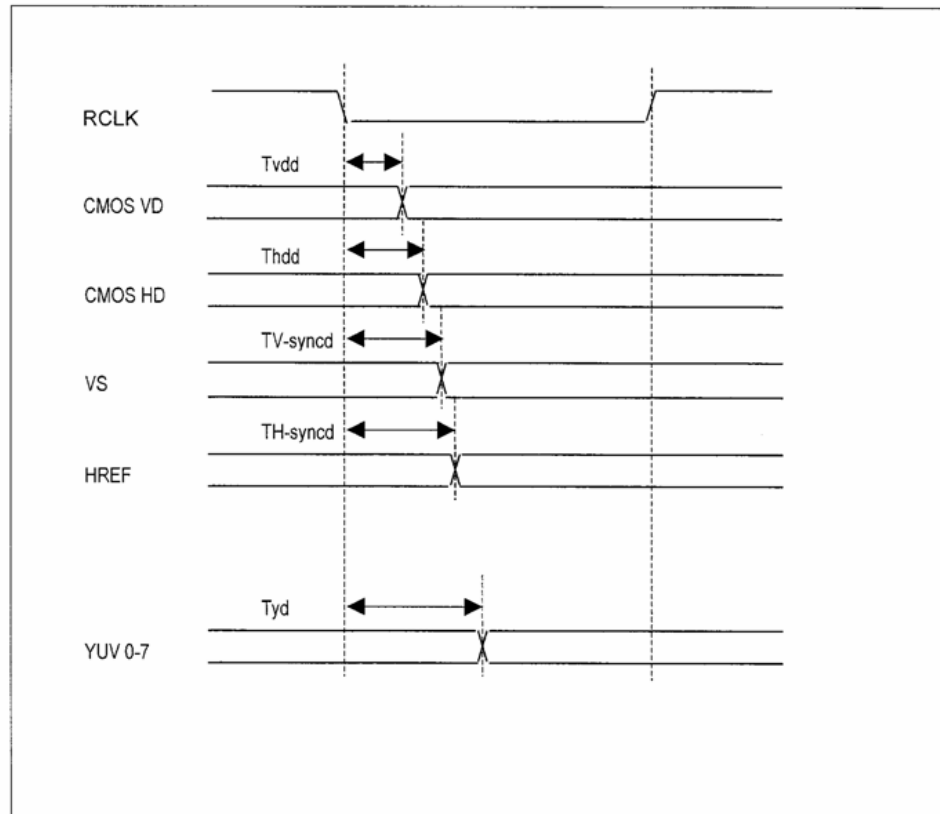
(VDD = +2.80V Ta = -10°C ~ 60°C)

| Item                       | Symbol          | Test condition            | MIN.    | TYP. | MAX.   | Unit    | Note |
|----------------------------|-----------------|---------------------------|---------|------|--------|---------|------|
| Low level input voltage1   | $V_{IL1}$       |                           |         |      | 0.3VDD | V       | 1    |
| High level input voltage1  | $V_{IH1}$       |                           | 0.7VDD  |      |        | V       |      |
| Low level input voltage2   | $V_{IL2}$       |                           |         |      | 0.2VDD | V       | 2    |
| High level input voltage2  | $V_{IH2}$       |                           | 0.8VDD  |      |        | V       |      |
| Hysteresis voltage         | $V_{HYS}$       |                           | 0.1VDD  |      |        | V       | 3    |
| Input leak current 1       | $I_{I1}$        | $V_{IN} = 0V \sim V_{DD}$ | -1.0    |      | +1.0   | $\mu A$ | 4    |
| Input leak current 2       | $I_{I2}$        | $V_{IN} = 0V \sim V_{DD}$ | -1.0    |      | +1.0   | $\mu A$ | 5    |
| Low level output voltage1  | $V_{OL1}$       | $I_{OL} = 3mA$            |         |      | 0.2VDD | V       | 6    |
| Low level output voltage1  | $V_{OL2}$       | $I_{OL} = 3mA$            |         |      | 0.5    | V       | 7    |
| High level output voltage1 | $V_{OH2}$       | $I_{OL} = -3mA$           | VDD-0.5 |      |        | V       |      |
| Clock frequency            | $F_{Sync\ clk}$ |                           | 1       | 9    | 10     | MHz     | 8    |
| Clock input voltage        | $V_{Sync\ clk}$ |                           |         | 2.8  |        | Vp-p    |      |

| NOTE | COMMENT                                       |
|------|-----------------------------------------------|
| 1    | Applicable to pin SDA, SDC                    |
| 2    | Applicable to pin YUVData 0-7                 |
| 3    | Applicable to pin SDA, SDC                    |
| 4    | Applicable to pin SDA, SDC                    |
| 5    | Applicable to pin YUVData 0-7                 |
| 6    | Applicable to pin SDA, SDC                    |
| 7    | Applicable to pin YUVData 0-7, RCLK, VS, HREF |
| 8    | Applicable to pin System_clock                |

## 5-2. AC Characteristics

### 5-2-1. Digital parallel output timing



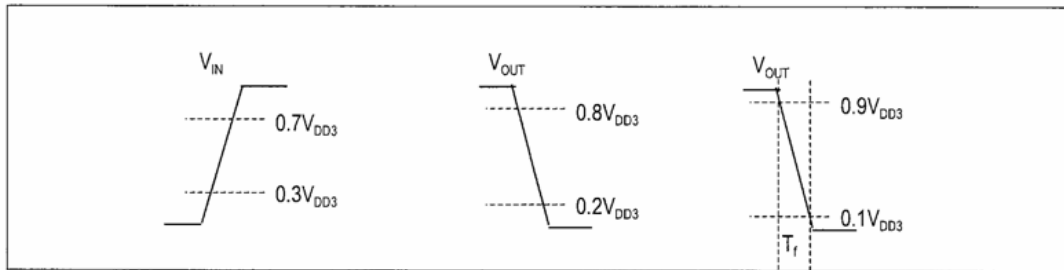
( $V_{DD} = +2.78V$   $T_a = -10^{\circ}C \sim 60^{\circ}C$ )

| Item                        | Symbol  | Condition |     | Unit | Note |
|-----------------------------|---------|-----------|-----|------|------|
|                             |         | MIN       | MAX |      |      |
| CMOS imager VD output delay | Tvdd    | -15       | 15  | ns   | 1    |
| CMOS imager HD output delay | Thdd    | -15       | 15  | ns   | 1    |
| VS output delay             | TV-sync | -15       | 15  | ns   | 1    |
| HREF output delay           | TH-sync | -15       | 15  | ns   | 1    |
| YUVDData 0-7 output delay   | Tyd     | -15       | 15  | ns   | 1    |

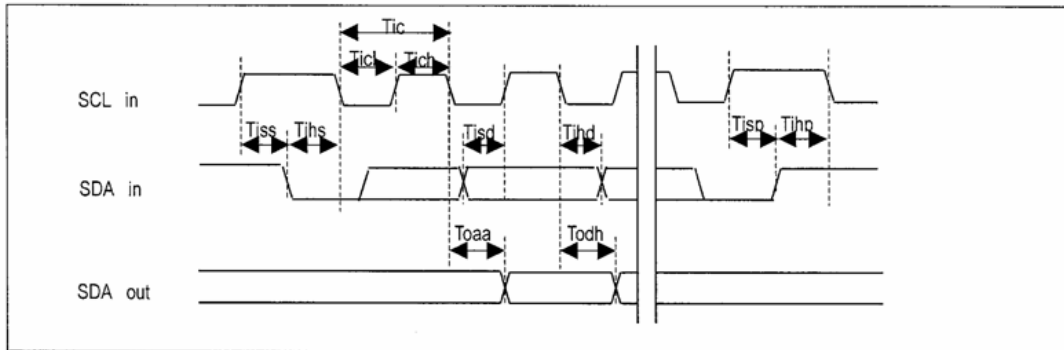
(Note 1) Output load capacitance  $CL = 15pF$

## 5-2-2. I2C interface timing

### I/O level, rising time



### Host I/F timing



(VDD= +2.78V Ta = -10°C ~ 60°C)

| Item                           | Symbol | MIN | MAX | UNIT | Note |
|--------------------------------|--------|-----|-----|------|------|
| Operating clock frequency      | Tic    |     | 400 | kHz  |      |
| Period that clock is High.     | Tich   | 0.1 |     | μs   |      |
| Period that clock is Low.      | Ticl   | 0.2 |     | μs   |      |
| Setup time of start condition. | Tiss   | 0.1 |     | μs   |      |
| Hold time of start condition.  | Tihs   | 0.1 |     | μs   |      |
| Setup time of input data.      | Tisd   | 0.1 |     | μs   |      |
| Hold time of input data.       | Tihd   | 0   |     | μs   |      |
| Output delay                   | Toaa   | 0   |     | μs   | 1    |
| Hold time of output data.      | Todh   | 0   |     | μs   | 1    |
| Setup time of stop condition.  | Tisp   | 0.1 |     | μs   |      |
| Hold time of stop condition.   | Tihp   | 0.1 |     | μs   |      |
| Period of rising               | Tf     |     | 300 | ns   | 1    |

(Note 1) Output load capacitance CL = 15pF.

## 6. Function guide

### 6-1-1. Auto exposure control

Control variable speed electronic shutter and gain of AGC (Auto Gain Control), so that exposure data can converge in standard. When the exposure data converge in error range of exposure control, shutter control and gain control of AGC will halt, until they exceed the range. When the exposure data exceed error range of exposure control, shutter control and gain control of AGC will be continued, until they converge in the range. And this LSI also has "Back light correction", "variable exposure weight control", "switching auto/fixed exposure control", "variable speed of exposure control", "variable max shutter speed in auto exposure control", "variable LPF used in auto exposure control loops".

### 6-1-2. Auto optical black level adjustments

It is able to switch auto/fixed control of auto optical black level, and LPF used in control loops.

### 6-1-3. Auto carrier balance control

Automatic carrier balance correction is available. It is able to select "auto control + correction by fixed value" or "correction by fixed value".

### 6-1-4. Auto white balance control

R and B signal are multiplied by each factor to control white balance. When white balanced data converge in defined range 1, control would halt, until they exceed defined range 2. When white balanced data exceed defined range 2, control would be continued until they converge in defined range 1. It is able to switch to fast white balance mode and change LPF of white balance, too.

### 6-1-5 Color suppression

This function can suppress false color seen at the edge of luminance signals and at high luminance level areas, and suppress color signals at low luminance level areas. And color signal is suppressed synchronized with change of AGC gain.

### 6-1-6. AGC aperture suppression

It is able to suppress aperture signal synchronized with change of AGC gain.

#### 6-1-7. Property of gamma

Gamma correction can be applied by the curve approximated to 10 line graphs.

Slope and offset of line graphs can be configured.

#### 6-1-8 White defect correction

Fixed white defect correction (less than 32 points) and auto white defect correction can be applied. It is able to switch to use auto and fixed correction, or use only fixed correction.

#### 6-1-9 Shading correction

It is able to correct the shading at corner of the image, which is caused by optical characteristics of lens. It is able to select using shading correction or not.

#### 6-1-10. Procedure for setting parameters on booting

After Power-on, this Camera module will have booted as "slave mode", and parameter will be set by host connected to SDC ( clock for I<sup>2</sup>C ), SDA( data for I<sup>2</sup>C).

#### 6-1-11. About standby mode

Standby mode means the status that MOS\_CTRL2[3](MOS\_STDBY) is '1'.

In this status, the internal LSI halts all function, except I<sup>2</sup>C interface control, and CSTDBYO goes High level in order to let CMOS sensor go standby. Not in standby mode, CSTDBYO is Low level.

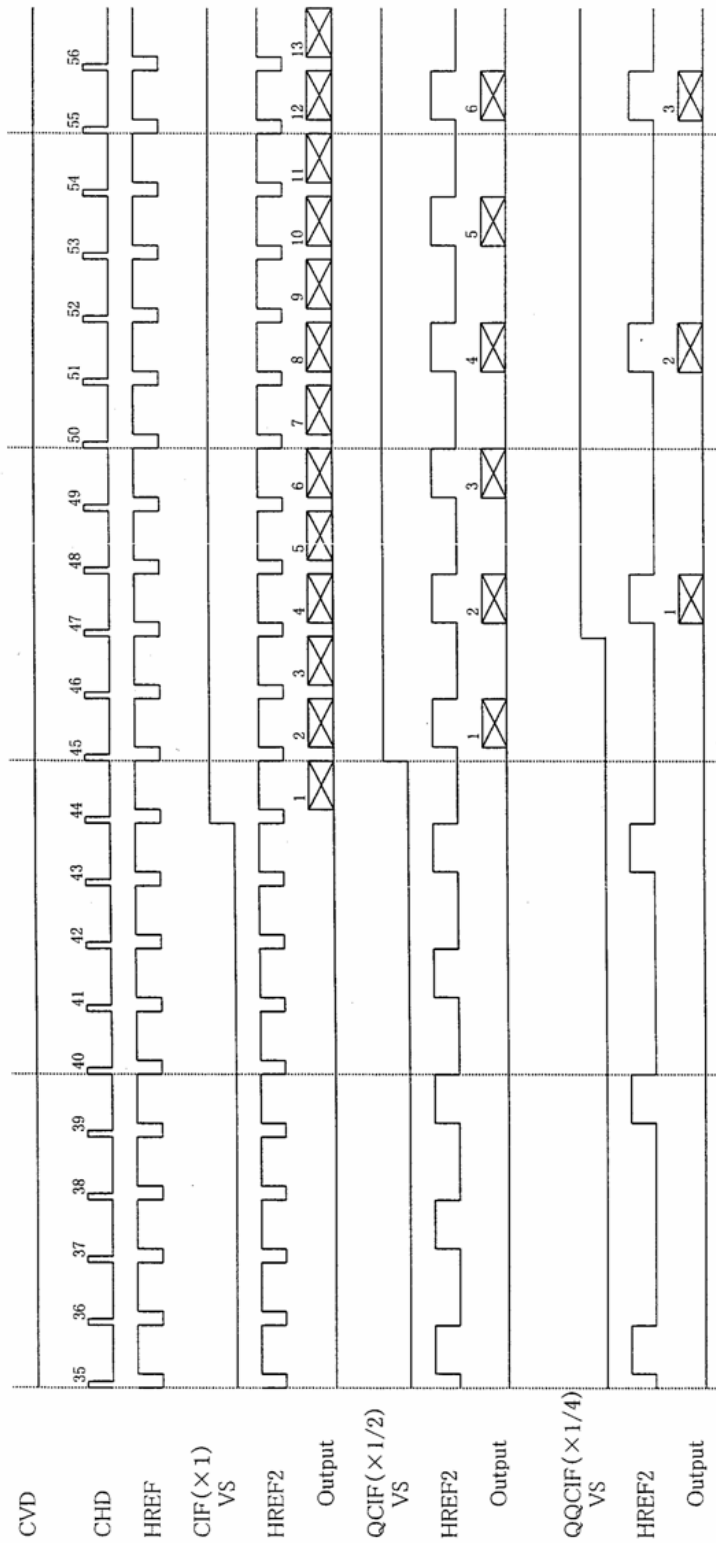
Return procedures from standby mode to normal mode are described below.

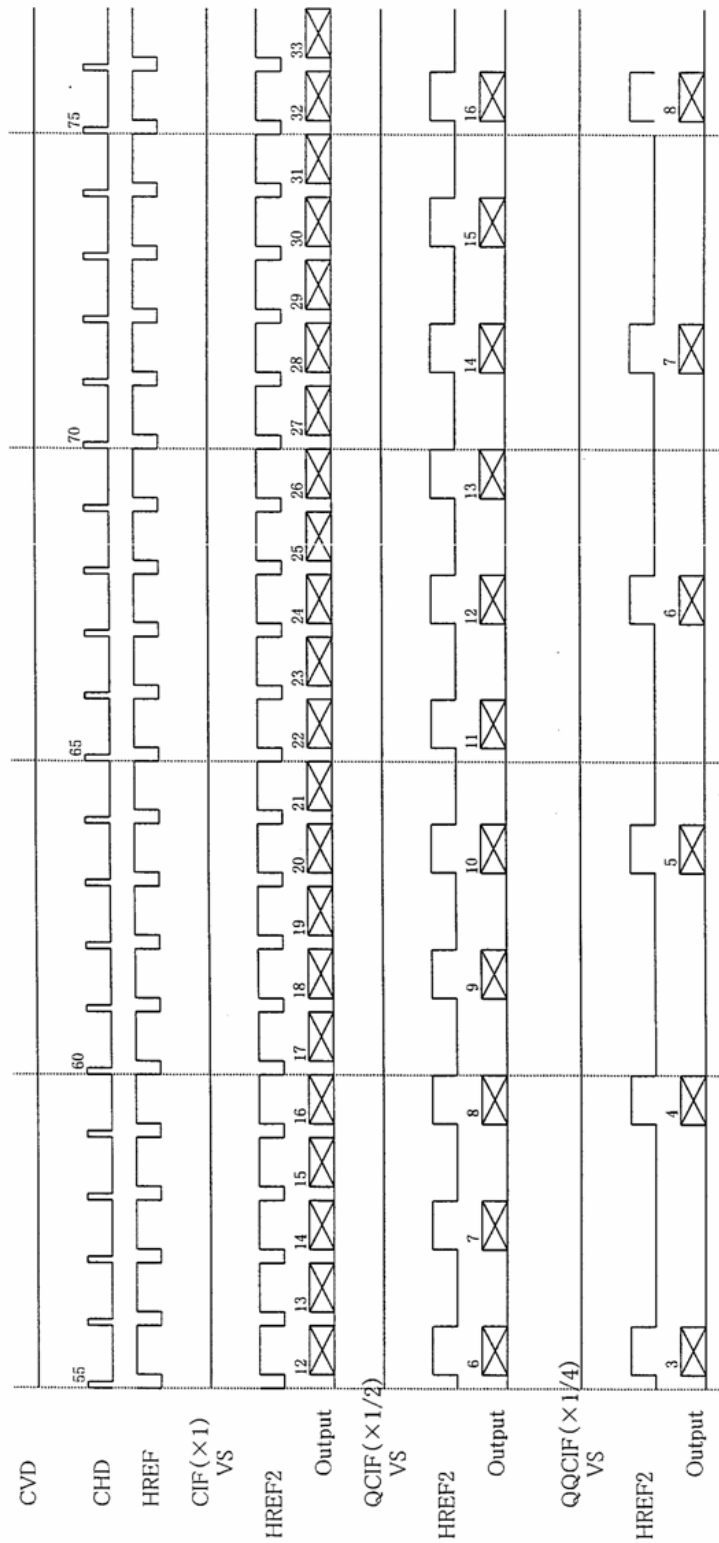
Procedure 1: When MOS\_CTRL2[3] is '1'.

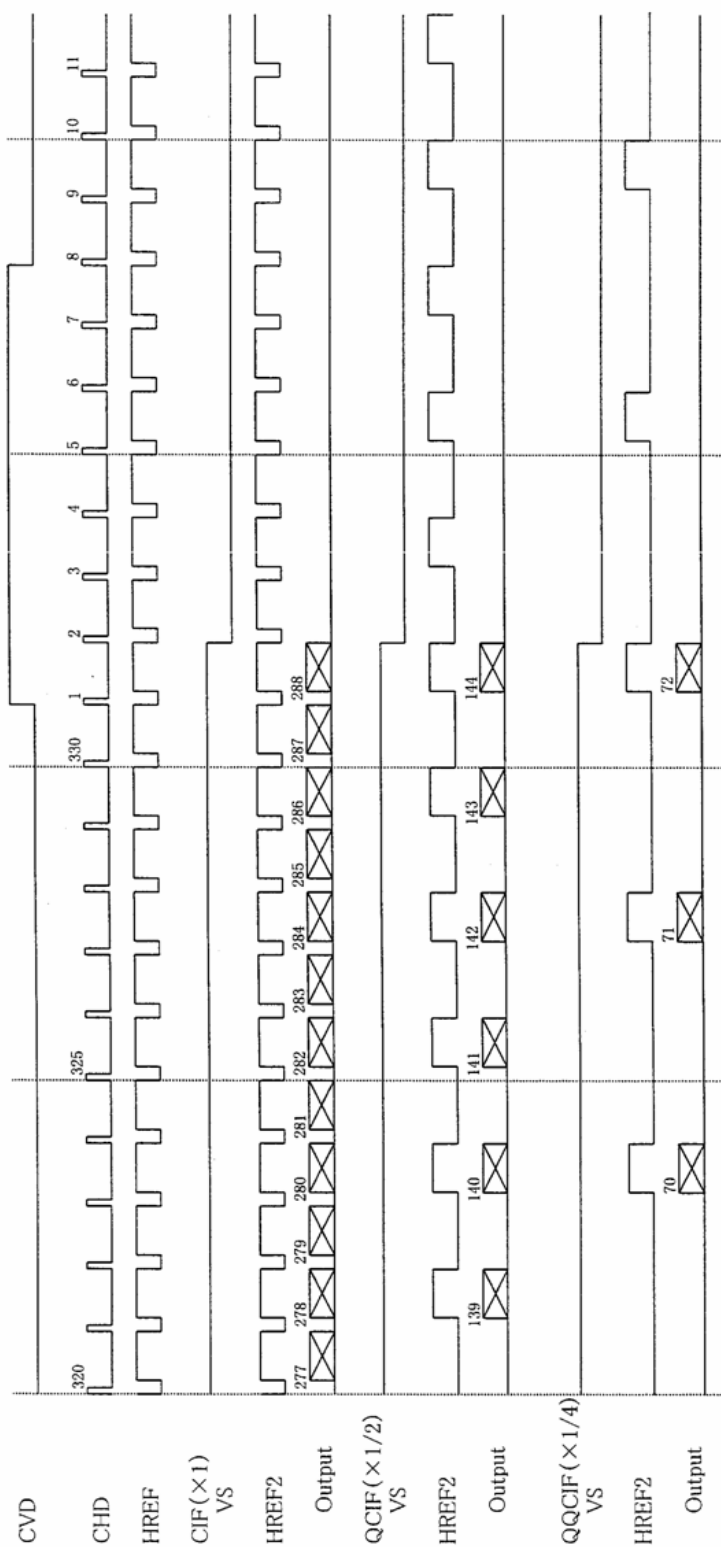
- 1 Set DSP\_ENB[1](FWFLG) to '0' and DSP\_ENB[0](WFLG) to '0'.
- 2 Set MOS\_CTRL2[3] to '0'.
- 3 Set DSP\_ENB[1] to '0' and DSP\_ENB[0] to '1'.
- 4 Camera returns to normal mode after the time configured in STDBY\_TIM.

Procedure 2: When MOS\_CTRL2[3] is '1'.

- 1 Set MOS\_CTRL2[3] to '0'.
- 2 Set DSP\_ENB[1] to '1'.
- 3 Camera returns to normal mode after the time configured in STDBY\_TIM.







**UYVY output**

HREF, HREF2

| Y | 80 | 01 | 80 | 01 | 80 | 01 | u | v | u | v | u | v | u | v | u | v |
|---|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 7 |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| 6 |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| 5 |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| 4 |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| 3 |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| 2 |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| 1 |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

RCLK

RCLK2

UV[0]

The diagram shows a sequence of data bytes from 348 to 352. The signals are:

- VY output**: A signal that transitions from low to high at the start of the sequence.
- HREF, HREF2**: A signal that transitions from low to high at the start of the sequence and remains high.
- Y**: A signal that transitions from low to high at the start of the sequence and remains high.
- RCLK**: A clock signal that transitions from low to high at the start of the sequence and remains high.
- RCLK2**: A clock signal that transitions from low to high at the start of the sequence and remains high.
- UV[0]**: A signal that transitions from low to high at the start of the sequence and remains high.

The data bytes are:

| Byte  | 348 | 349 | 350 | 351 | 352 |
|-------|-----|-----|-----|-----|-----|
| Y     | v   | y   | u   | y   | v   |
| RCLK  | v   | y   | u   | y   | v   |
| RCLK2 | v   | y   | u   | y   | v   |
| UV[0] | v   | y   | u   | y   | v   |