DALLAS SEMICONDUCTOR

DS1065
EconOscillator/Divider

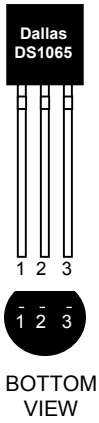
FEATURES

- 30 kHz to 100 MHz output frequencies
- User-programmable on-chip dividers (from 1-513)
- User-programmable on-chip prescaler (1, 2, 4)
- No external components
- ±0.5% initial tolerance
- ±3% variation over temperature and voltage
- Single 5V supply

FREQUENCY OPTIONS

Part No.	Max O/P freq.
DS1065-100	100.000 MHz
DS1065-80	80.000 MHz
DS1065-66	66.667 MHz
DS1065-60	60.000 MHz

PIN ASSIGNMENT



BOTTOM VIEW

PIN DESCRIPTION

TO-92

1 I/O	- Input/Output
2 V_{CC}	- Power Supply
3 GND	- Ground

DESCRIPTION

The DS1065 is a fixed frequency oscillator requiring no external components for operation. Numerous operating frequencies are possible in the range of approximately 30 kHz to 100 MHz through the use of an on-chip programmable prescaler and divider.

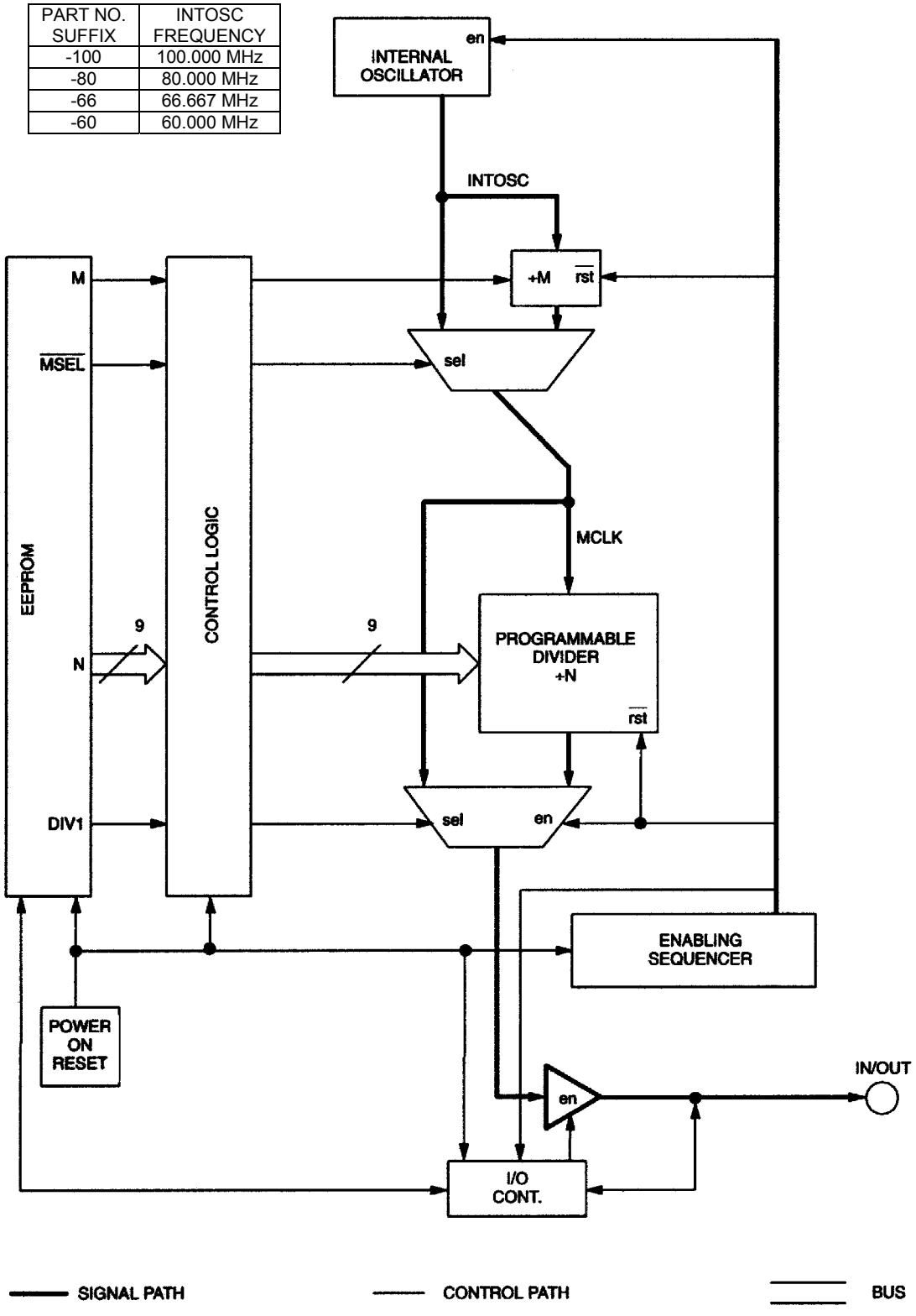
The DS1065 features a master oscillator followed by a prescaler and then a programmable divider. The prescaler and programmable divider are user-programmable with the desired values being stored in nonvolatile memory. This allows the user to buy an off the shelf component and program it on site prior to board production. Design changes can be accommodated easily by simply programming different values into the device (or reprogramming previously programmed devices). The DS1065 is shipped from the factory configured for half the maximum operating frequency. Contact the factory for specially programmed devices.

The DS1065 features a dual-purpose Input/Output pin. If the device is powered up in Program mode this pin can be used to input serial data to the on-chip registers. After a write command this data is stored in nonvolatile memory. When the chip is subsequently powered up in operating mode these values are automatically restored to the on-chip registers and the Input/Output pin becomes the oscillator output.

The DS1065 is available in TO-92 (3 LEAD) package, allowing the generation of a clock signal easily, economically and using minimal board area.

BLOCK DIAGRAM Figure 1

PART NO. SUFFIX	INTOSC FREQUENCY
-100	100.000 MHz
-80	80.000 MHz
-66	66.667 MHz
-60	60.000 MHz



PIN DESCRIPTIONS

Input/Output Pin (IN/OUT): This pin is the main oscillator output, with a frequency determined by clock reference, M and N dividers. Except in programming mode this pin is always an output and will be referred to as "OUT". In programming mode this pin will be referred to as "IN".

USER-PROGRAMMABLE REGISTERS

The following registers can be programmed by the user to determine device operating frequency and mode of operation. Details of how these registers are programmed can be found in a later section; in this section the function of the registers are described. The register settings are nonvolatile, the values being stored automatically in EEPROM when the registers are programmed.

NOTE: The register bits cannot be used to make frequency changes on the fly. Changes can only be made by powering the device up in "Programming" mode. For them to be become effective the device must then be powered down and powered up again in "Operation" mode.

For programming purposes the register bits are divided into two 9-bit words; the "MUX" word determines mode prescaler values and the "DIV" word sets the value of the programmable divider.

MUX WORD Figure 2

(MSB)								(LSB)
0*	0*	0*	1*	1*	M	$\overline{\text{MSEL}}$	DIV1	0*

*These bits must be set to the indicated values

DIV1

This bit allows the master clock to be routed directly to the output (DIV1=1). The N programmable divider is bypassed so the programmed value of N is ignored. The frequency of the output (f_{OUT}) will be INTCLK or EXTCLK depending on which reference has been selected. If the Internal clock is selected the M prescaler is also bypassed (the bit values of MSEL and M are ignored), so in this case f_{OUT} = INTOSC (which also equals MCLK and INTCLK). If DIV1=0 the prescaler and programmable divider function normally.

$\overline{\text{MSEL}}$

This bit determines whether or not the M prescaler is bypassed. $\overline{\text{MSEL}}$ =1 will bypass the prescaler. $\overline{\text{MSEL}}$ =0 will switch in the prescaler (unless overridden by DIV1=1), with a divide-by number determined by the M bit.

M

This bit sets the divide-by number for the prescaler. M = 0 results in divide-by-4, M=1 results in divide-by-2. The setting of this bit is irrelevant if either DIV1=1 or $\overline{\text{MSEL}}$ =1.

Table 2

DIV1 BIT	$\overline{\text{MSEL}}$ BIT	M BIT	OPERATION
0	0	0	INTERNAL OSCILLATOR DIVIDED BY 4*N
0	0	1	INTERNAL OSCILLATOR DIVIDED BY 2*N
0	1	X	INTERNAL OSCILLATOR DIVIDED BY N

1	X	X	INTERNAL OSCILLATOR DIVIDED BY 1

DIV WORD Figure 3

(MSB)									**(LSB)**
N (9-BITS)									

N

These 9 bits determine the value of the programmable divider. The range of divisor values is from 2 to 513, and is equal to the programmed value of N plus 2:

Table 3

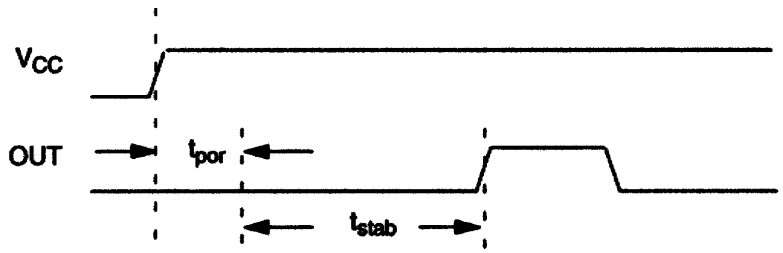
BIT VALUES	DIVISOR (N) VALUE
000000000	2
000000001	3
.	.
.	.
.	.
.	.
.	.
111111111	513

POWER-ON RESET

When power is initially applied to the device supply pin, a power-on reset sequence is executed, similar to that which occurs when the device is restored from a power-down condition. This sequence comprises two stages, first a conventional POR to initialize all on-chip circuitry, followed by a stabilization period to allow the oscillator to reach a stable frequency before enabling the output:

1. Initialize internal circuitry.
2. Enable internal oscillator.
3. Set M and N to maximum values.
4. Wait approximately 1024 cycles of INTOSC for the oscillator to stabilize.
5. Load M and N programmed values from EEPROM.
6. Enable OUT.

Figure 10



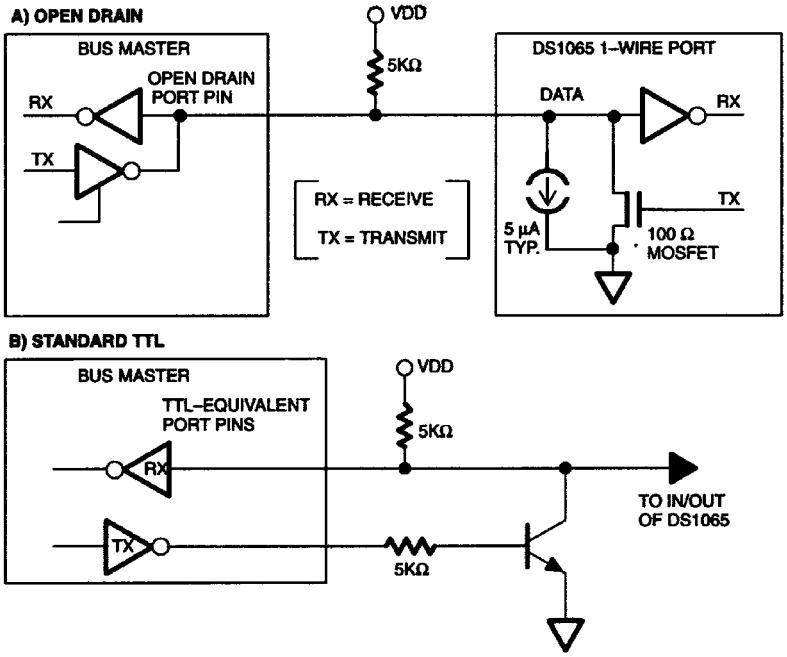
PROGRAMMING

Normally when power is applied to the supply voltage pin the device will enter its normal operating mode, following the power-on reset sequence. However the device can be made to enter a programming mode if a pullup resistor is connected between IN/OUT and the supply voltage pin prior to power-up. The method used for programming is a variant of the 1-Wire™ protocol used on a number of Dallas Semiconductor products.

HARDWARE

The hardware configuration is shown in the diagram. A bus master is used to read and write data to the DS1065's internal registers. The bus master may have either an open-drain or TTL-type architecture.

Figure 11

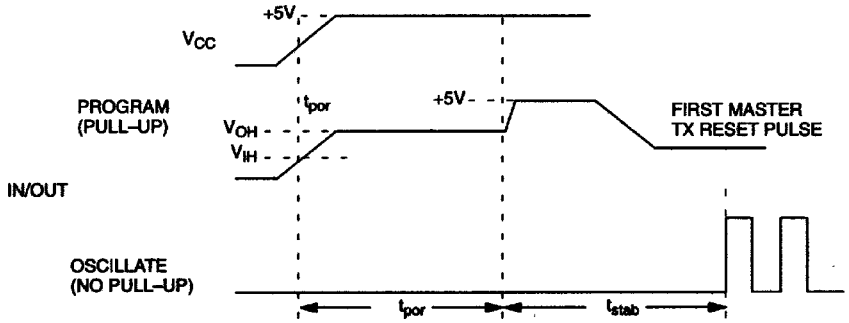


Programming mode is entered by simply powering up the DS1065 with a pullup of approximately 5kΩ. This will pull the IN/OUT pin above V_{IH} on power-up and initiate the programming mode, causing the DS1065 to internally release the IN/OUT pin after t_{STAB} and allow the pullup resistor to pull up the pin to the supply rail and await the Master Tx Reset pulse (see diagram).

NOTE:

To ensure normal operation any external pullup applied to IN/OUT must be greater than 20 kΩ in value. This will cause the IN/OUT pin to remain below V_{IH} on power-up, resulting in normal operation at the end of t_{STAB}.

Figure 12



TRANSACTION SEQUENCE

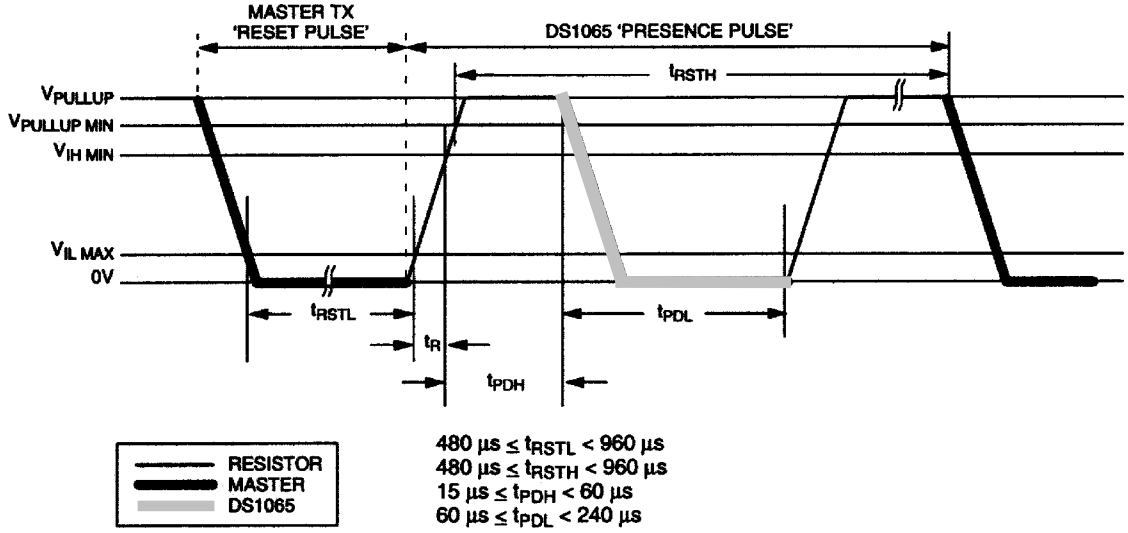
The sequence for accessing the DS1065 via the 1-Wire port is as follows:

Initialization
Function Command
Transaction/Data

INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by a presence pulse(s) transmitted by the DS1065. The presence pulse lets the bus master know that the DS1065 is present and is ready to operate.

Figure 13



FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the four function commands. All Function Commands are 8 bits long, and are written lsb first. A list of these commands follows:

Write DIV Register [01H]
This command allows the bus master to write to the DS1065's DIV register.

Read DIV Register [A1H]
This command allows the bus master to read the DS1065's DIV register.

Write MUX Register [02H]
This command allows the bus master to write to the DS1065's MUX register.

Read MUX Register [A2H]
This command allows the bus master to read the DS1065's MUX register.

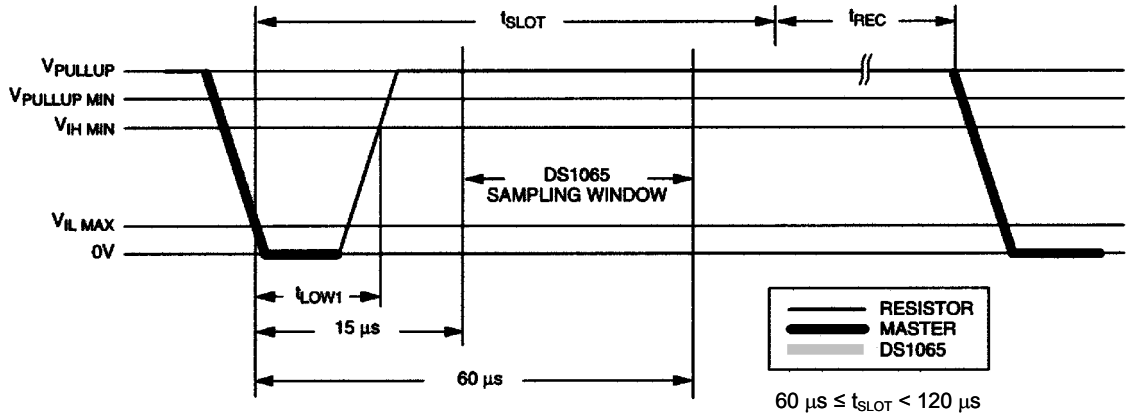
TRANSACTION/DATA

Immediately following the Function Command, the 9 data bits are written to or read from the DS1065. This data is written/read lsb first. The following diagrams illustrate the timing. Once data transfer is complete a new transaction sequence can be started by re-initializing the device. Therefore to program both the DIV and MUX registers two complete transaction sequences are required.

READ/WRITE TIME SLOTS

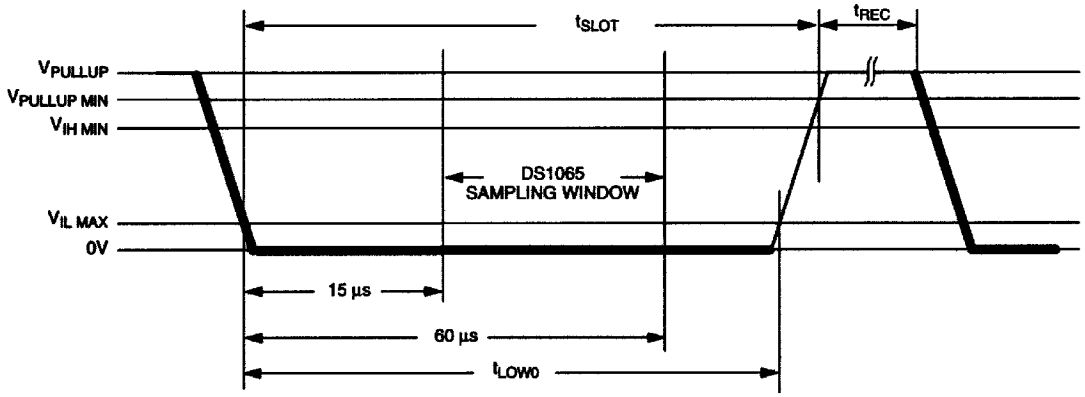
The definitions of write and read time slots are illustrated below. All time slots are initiated by the master driving the data line low. The falling edge of the data line synchronizes the DS1065 to the master by triggering a delay circuit in the DS1065. During write time slots, the delay circuit determines when the DS1065 will sample the data line. For a read data time slot, if a 0 is to be transmitted, the delay circuit determines how long the DS1065 will hold the data line low overriding the 1 generated by the master. If the data bit is a 1, the DS1065 will leave the read data time slot unchanged.

WRITE 1 TIME SLOT Figure 14



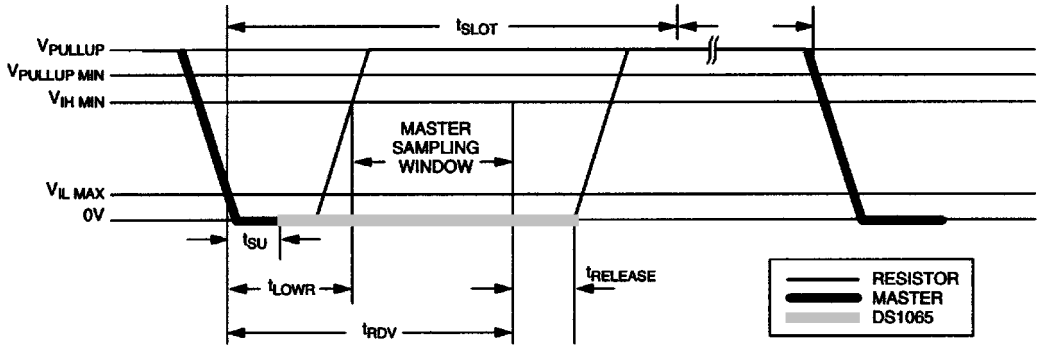
60 µs ≤ t_{SLOT} < 120 µs
1 µs ≤ t_{LOW1} < 15 µs
1 µs ≤ t_{REC} < ∞

WRITE 0 TIME SLOT Figure 15



60 µs ≤ t_{LOW0} < t_{SLOT} < 120 µs
1 µs ≤ t_{REC} < ∞

READ DATA TIME SLOT Figure 16



60 µs ≤ t_{SLOT} < 120 µs
1 µs ≤ t_{LOWR} < 15 µs
0 µs ≤ $t_{RELEASE}$ < 45 µs
1 µs ≤ t_{REC} < ∞
t_{RDV} = 15 µs
t_{SU} < 1 µs

RETURN TO NORMAL OPERATION

When programming is complete, the DS1065 should be powered down. If the pullup resistor on the IN/OUT pin is removed, normal device operation will be restored next time power is applied.

DEFAULT REGISTER VALUES

Unless ordered from the factory with specific register program values, the DS1065 is shipped with the following default register values:

DIV = 0 0000 0000 (Programmable divider will divide by two)
MUX = 0 0011 0100
M = 4 (Ignored, see $\overline{\text{MSEL}}$)
$\overline{\text{MSEL}}$ = 1 (M prescaler bypassed)
DIV1 = 0 (N Dividers enabled)

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5	5.25	V	
High-level Output Voltage (IN/OUT)	V_{OH}	I_{OH} = -4 mA, V_{CC} = MIN	2.4			V	
Low-level Output Voltage (IN/OUT)	V_{OL}	I_{OL} = 4 mA			0.4	V	
High-level Input Voltage (IN/OUT)	V_{IH}		2			V	
Low-level Input Voltage(IN/OUT)	V_{IL}				0.8	V	
High-level Input Current	I_{IH}	V_{IH} =2.4V, V_{CC} = 5.25V			1	uA	
Low-level Input Current	I_{IL}	V_{IL} =0,V_{CC} =5.25V	-1			uA	
Supply Current (Active) DS1065-100 DS1065-80 DS1065-66 DS1065-60	I_{CC}	C_L= 15 pF		35	50	 mA mA mA mA	

AC ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Output Frequency Tolerance	Δf_O	V_{CC} = 5V, T_A =25°C	-0.5	0	+0.5	%	
Combined Frequency Variation	Δf_O	Over temp and voltage	-3		+3	%	
Power-Up Time	$t_{por} + t_{stab}$			0.1	1	ms	1
Load Capacitance (IN/OUT)	C_L			15	2	pF	2
Output Duty Cycle IN/OUT OUT0			 40 40		 60 60	 % %	
Jitter	J				100	pS	3

NOTES:

1. This is the time from when V_{CC} is applied until the output starts oscillating.

2. Operation with higher capacitance loads may result in reduced output voltage and maximum operating frequency.

3. Parameter given is a typical max.