

QED & Symbolic QED

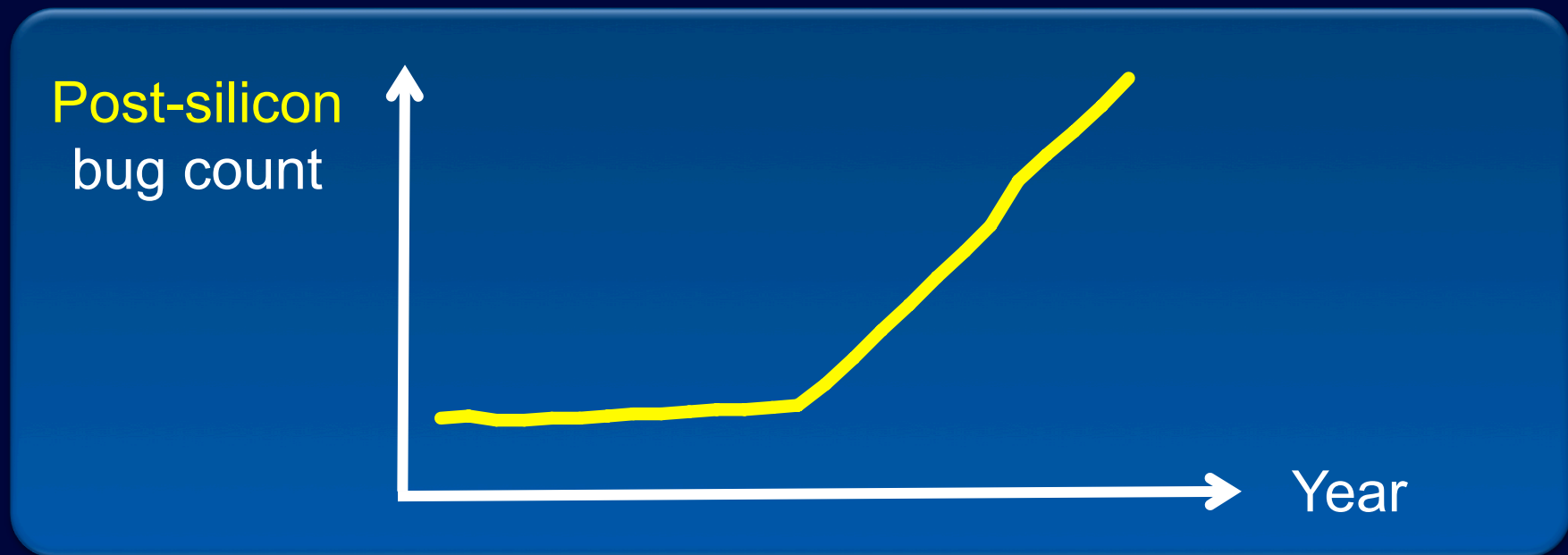
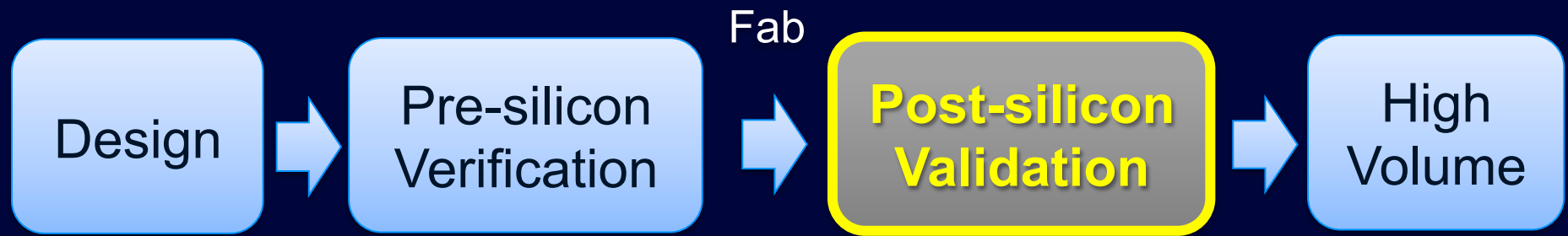
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Acknowledgment: Students & Collaborators

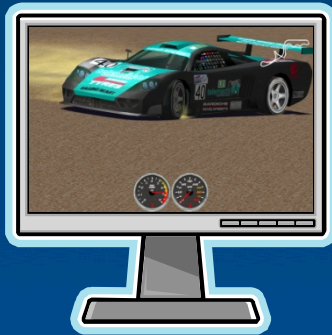
Pre-Silicon Verification Inadequate



New architectural features limited by validation

Post-Silicon Validation Difficult

System tests



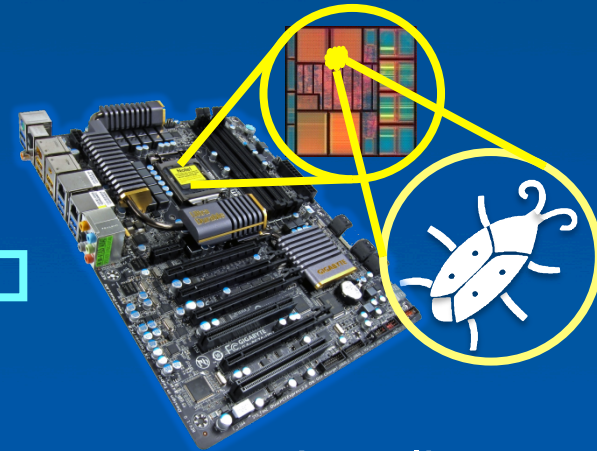
Detect



Weeks or months of manual work



Root-cause & fix



Localize

Scalability Barriers

- System-level failure reproduction
- Full system simulation

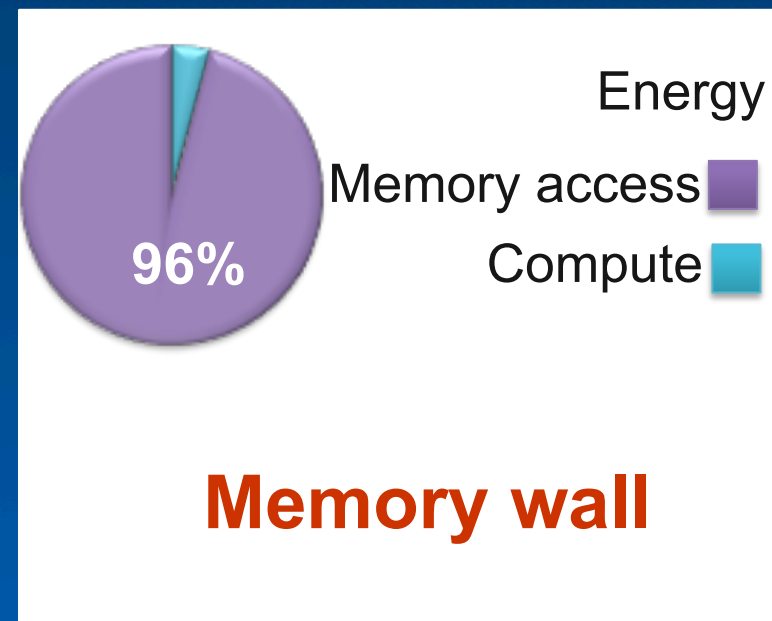
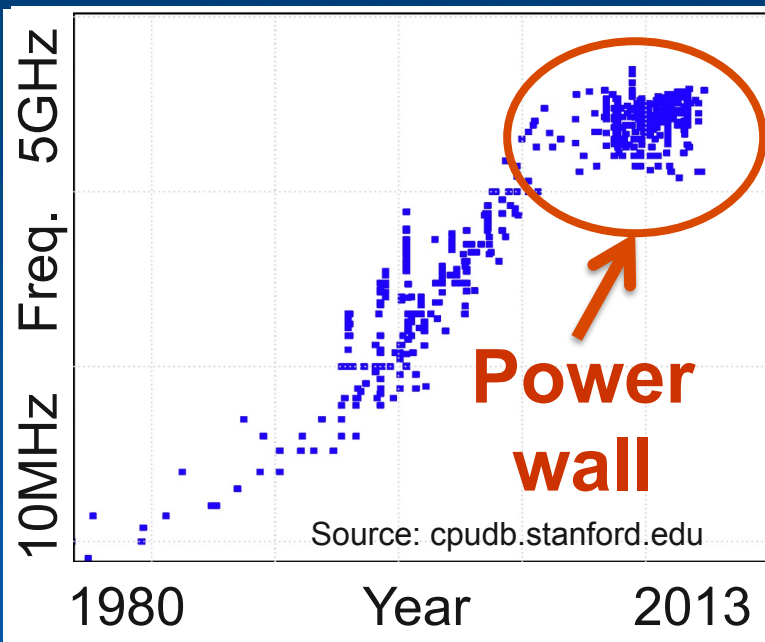


J. Stinson (ex-Intel)

Post-silicon costs rising faster than design cost

It's Only Getting Worse

Many walls simultaneously

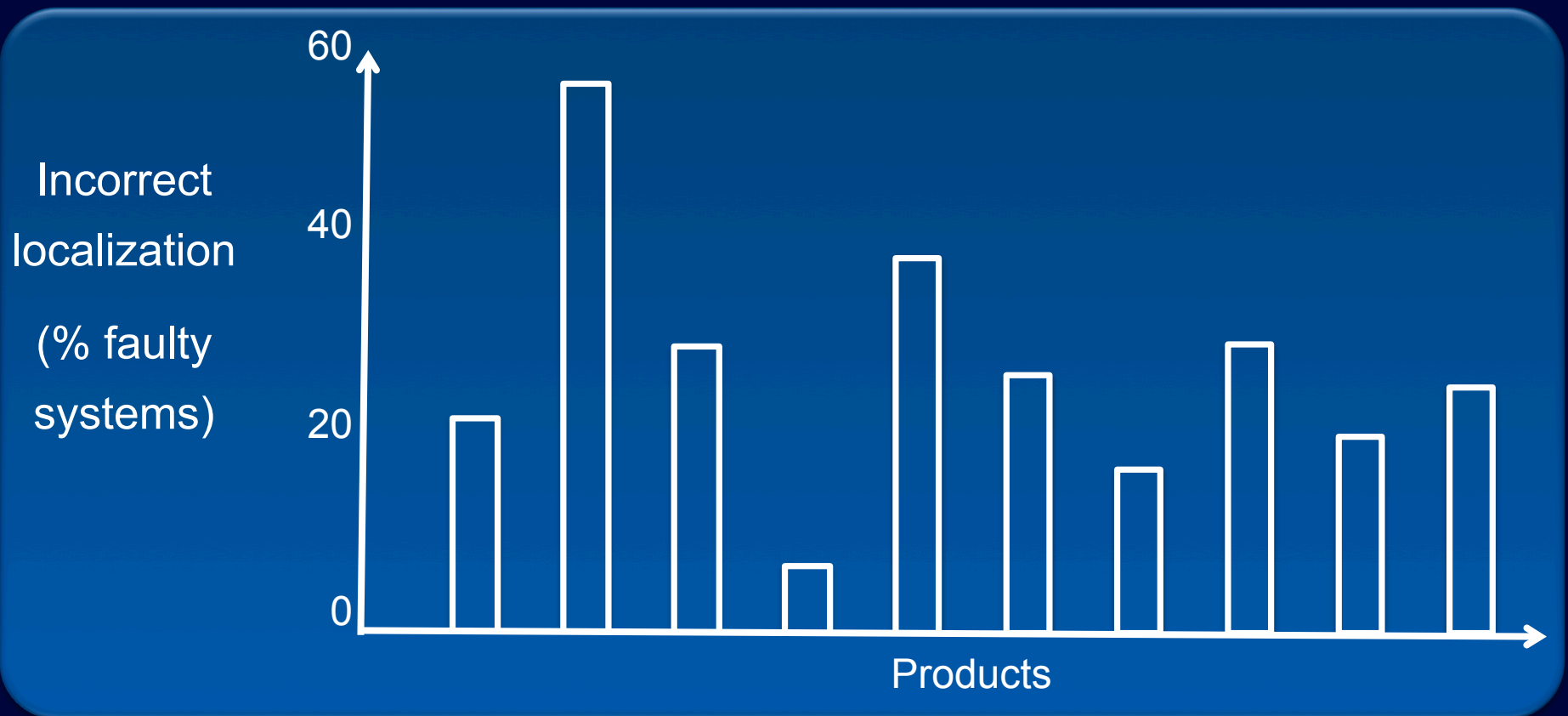


Also: interconnect wall, cooling wall, resilience wall, ...

Bigger Obstacles at System Level

1. Localize faulty IC
2. No Trouble Found

Incorrect localization: up to 60%



QED & Symbolic QED Results

- Pre-silicon formal verification

Few minutes to 7 hours

Automatic: no manual properties, constraints

Billion-transistor designs:

Processor cores, uncore, accelerators

QED & Symbolic QED Results

- Post-silicon validation & debug

20 flip-flops (out of 1 Million)

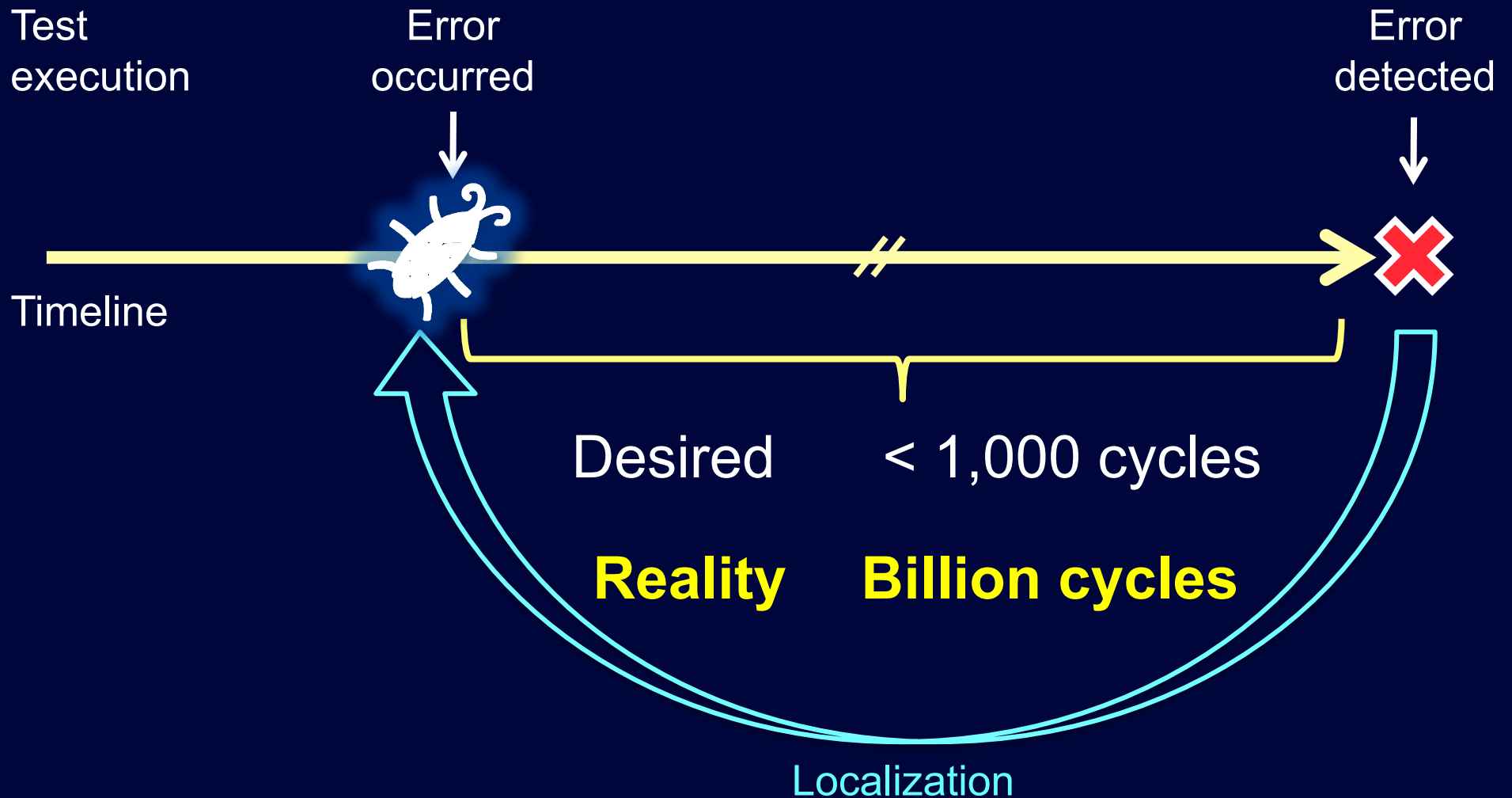
9 instructions (out of billions)

Automatic

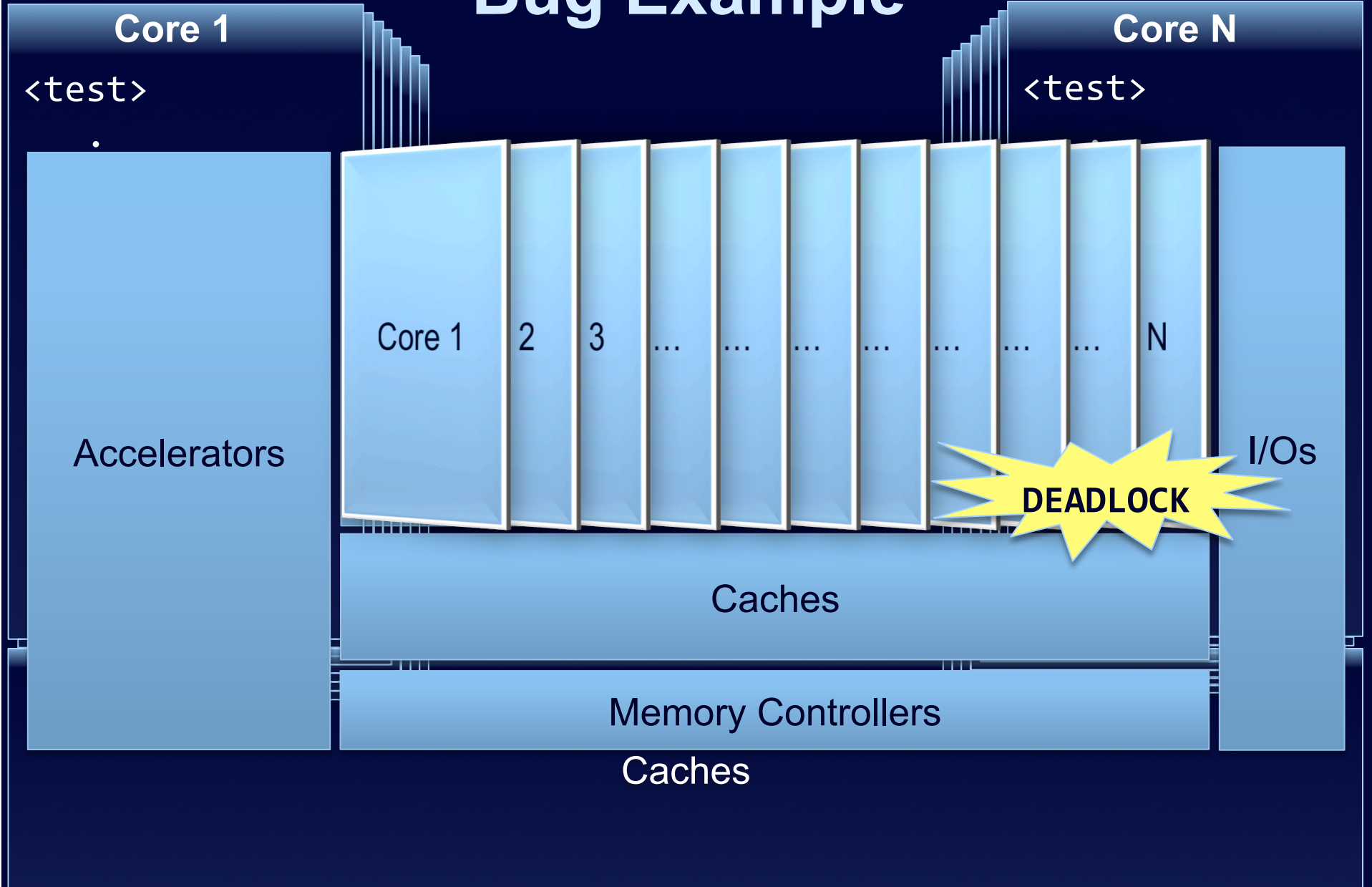
Few seconds to 9 hours

Billion-transistor designs

Error Detection Latency



Bug Example



Bug Example



Existing Techniques Inadequate

- **Very long** error detection latencies

Deadlock detection

Design-specific assertions

Self-checking tests

Store readback tests

Checkpointing

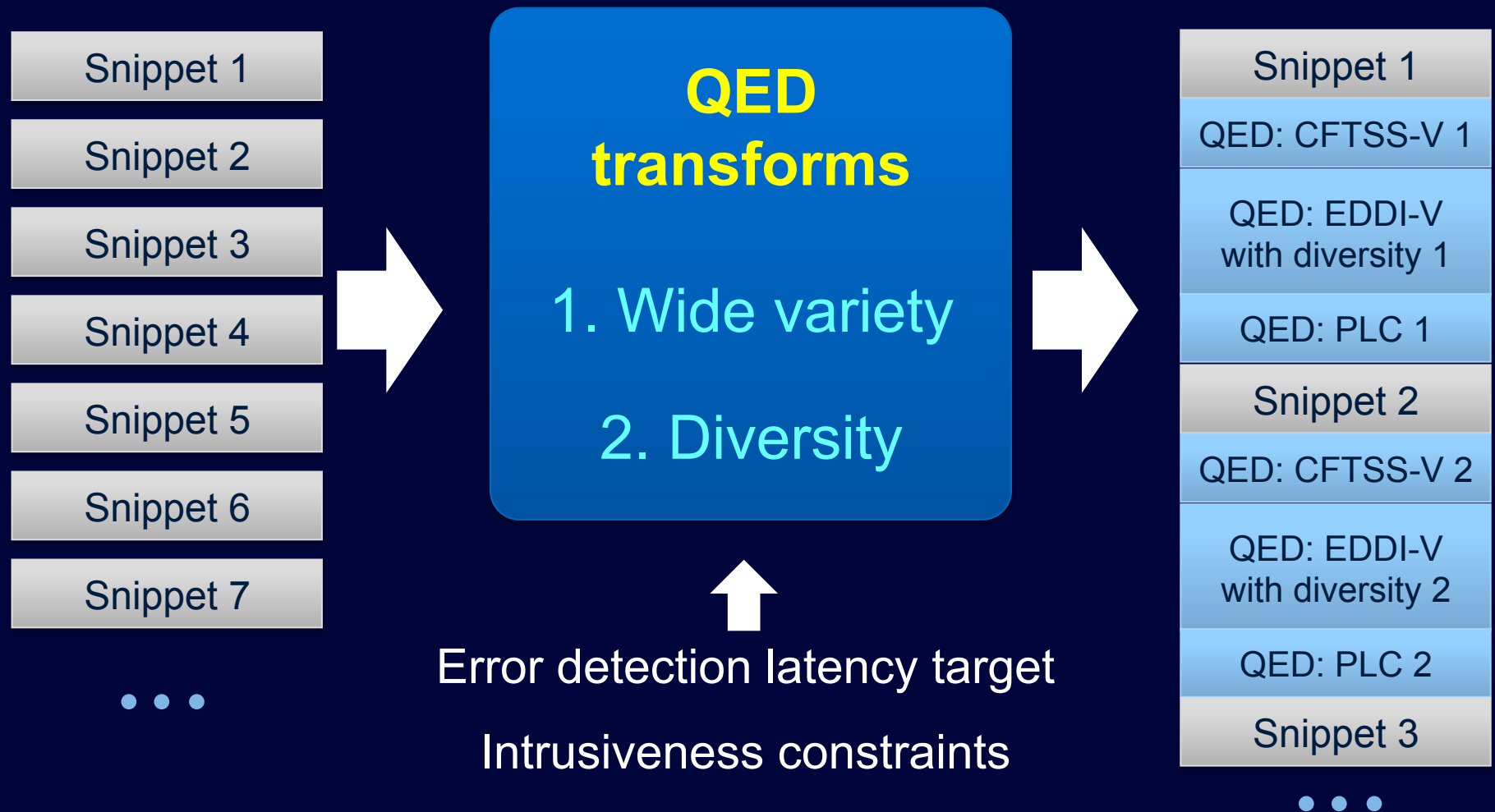
etc...

Quick Error Detection

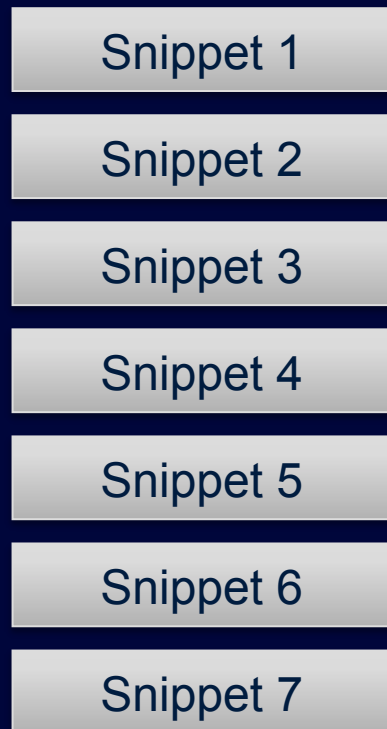


- Error detection latency: **guaranteed short**
- Coverage: **improved**
- Software-only: **readily applicable**

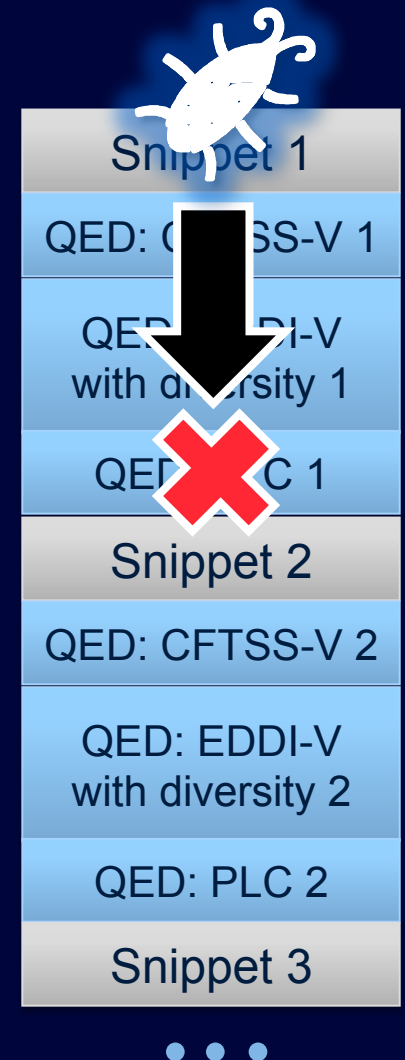
Quick Error Detection



Quick Error Detection

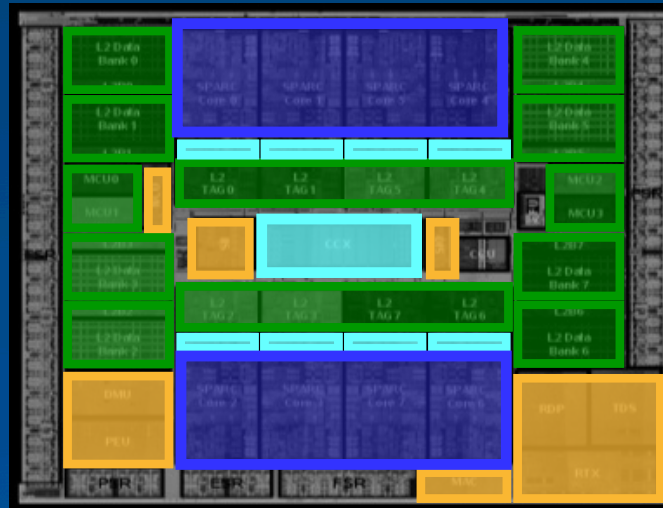


Error detection latency target
Intrusiveness constraints



QED Transforms

System on Chip



■ Processor cores

■ ■ ■ Uncore, accelerators

EDDI-V

PLC

CFTSS-V

Fast QED

CFCSS-V

Hybrid QED

QED Example: Duplicate & Check

Validation program

```
void matgen (REAL a[], int lda, int n, REAL b[], REAL *norma)
{
    int i,j;
    int m = 3333;
    *norma = 0.0;
    for (i = 0; i < n; i++) {
        for (j = 0; j < n; j++) {
            init = 3125*init % 0x100000000;
            a[lda*i+j] = (init - 32768.0)/16384.0;
            *norma = (a[lda*i+j] > *norma) ? a[lda*i+j] : *norma;
        }
    }
    for (i = 0; i < n; i++) {
        b[i] = 0.0;
    }
    for (i = 0; i < n; i++) {
        for (j = 0; j < n; j++) {
            b[i] = b[i] + a[lda*j+i];
        }
    }
    return;
}

void dgefa(REAL a[], int lda, int n, int ipvt[], int *info)
/*
   internal variables
*/
REAL t;
int j,k,kpl,lm1;

/*
   gaussian elimination with partial pivoting
*/

*info = 0;
nm1 = n - 1;
if (nm1 <= 0) {
    for (k = 0; k < nm1; k++) {
        kpl = k + 1;

        /* find l = pivot index */
        l = ldmax(n-k, &a[lda*k+k], 1) + k;
        ipvt[k] = l;

        /* zero pivot implies this column already
           triangularized */

        if (a[lda*k+l] != ZERO) {
            /* interchange if necessary */

            if (l != k) {
                t = a[lda*k+l];
                a[lda*k+l] = a[lda*k+k];
                a[lda*k+k] = t;
            }

            /* compute multipliers */
            t = -a[lda*k+l];
            dscal(n-(k+1), t, &a[lda*k+k+1], 1);

            /* row elimination with column indexing */
            for (j = kpl; j <= n; j++) {
                t = a[lda*j+l];
                if (l != k) {
                    a[lda*j+l] = a[lda*j+k];
                    a[lda*j+k] = t;
                }
                daxpy(n-(k+1), t, &a[lda*k+k+1], 1,
                    &a[lda*j+k+1], 1);
            }
        }
        else {
            *info = k;
        }
    }
}

ipvt[n-1] = n-1;
if (a[lda*(n-1)*(n-1)] == ZERO) *info = n-1;
checkbse(a, ipvt, info);
return;
}

void dgesl(REAL a[], int lda, int n, int ipvt[], REAL b[], int job)
{
    REAL t;
    int k,kb,lm1;

    nm1 = n - 1;
    if (job == 0) {
        /* solve a * x = b */
        first solve l*y = b
        if (nm1 >= 1) {
            for (k = 0; k < nm1; k++) {
                l = ipvt[k];
                t = b[l];
                if (l != k) {
                    b[l] = b[k];
                    b[k] = t;
                }
                daxpy(n-(k+1), t, &a[lda*k+k+1], 1, &b[k+1], 1);
            }
        }

        /* now solve u*x = y */
        for (kb = 0; kb < n; kb++) {
            k = n - (kb + 1);
            b[k] = b[k]/a[lda*k+k];
            t = -b[k];
            daxpy(k, t, &a[lda*k+0], 1, &b[0], 1);
        }
    }
    else {

```

Trace

...

R1	←	R1	+	5
R2	←	R2	-	R1
R3	←	R1	*	R2



Very Long!

...

Check end_result



QED Example: Duplicate & Check

Validation program

```
void matgen (REAL a[], int lda, int n, REAL b[], REAL *norma)
{
    int i,j;
    int m=1;
    *norma = 0.0;
    for (i = 0; i < n; i++) {
        for (j = 0; j < n; j++) {
            init = 3125*init % 0x100000000;
            a[lda*j+i] = (init - 32768.0)/16384.0;
            *norma = (a[lda*j+i] > *norma) ? a[lda*j+i] : *norma;
        }
    }
    for (i = 0; i < n; i++) {
        b[i] = 0.0;
    }
    for (i = 0; i < n; i++) {
        for (j = 0; j < n; j++) {
            b[i] = b[i] + a[lda*j+i];
        }
    }
    return;
}

void dgefa (REAL a[], int lda, int n, int ipvt[], int *info)
/*
   internal variables
*/
REAL t;
int j,k,kpl,lm1;

/* gaussian elimination with partial pivoting */

*info = 0;
m1 = n - 1;
if (m1 <= 0) {
    for (k = 0; k < m1; k++) {
        kpl = k + 1;

        /* find l = pivot index */
        l = idamax(n-k, &a[lda*k+k], 1) + k;
        ipvt[k] = l;

        /* zero pivot implies this column already
           triangularized */
        if (a[lda*k+l] != ZERO) {
            /* interchange if necessary */
            if (l != k) {
                t = a[lda*k+l];
                a[lda*k+l] = a[lda*k+k];
                a[lda*k+k] = t;
            }

            /* compute multipliers */
            t = -ONE/a[lda*k+k];
            dscal(n-k+1, t, &a[lda*k+k+1], 1);

            /* row elimination with column indexing */
            for (j = kpl; j < n; j++) {
                t = a[lda*j+l];
                if (l != k) {
                    a[lda*j+l] = a[lda*j+k];
                    a[lda*j+k] = t;
                }
                daxpy(n-k+1, t, &a[lda*k+k+1], 1,
                    &a[lda*j+k+1], 1);
            }
        }
        else {
            *info = k;
        }
    }
}

ipvt[m1] = m1;
if (a[lda*(m1-1)] != ZERO) *info = m1;
checkbipped(a, ipvt, info);
return;
}

void dgesl (REAL a[], int lda, int n, int ipvt[], REAL b[], int job)
{
    REAL t;
    int k,kb,lm1;

    m1 = n - 1;
    if (job == 0) {
        /* job == 0, solve a * x = b
           first solve l'y = b */
        if (m1 >= 1) {
            for (k = 0; k < m1; k++) {
                l = ipvt[k];
                t = b[l];
                if (l != k) {
                    b[l] = b[k];
                    b[k] = t;
                }
                daxpy(n-k+1, t, &a[lda*k+k+1], 1, &b[k+1], 1);
            }
        }

        /* now solve u*x = y */
        for (kb = 0; kb < n; kb++) {
            k = n - (kb + 1);
            b[k] = b[k]/a[lda*k+k];
            t = -b[k];
            daxpy(k, t, &a[lda*k+0], 1, &b[0], 1);
        }
    }
    else {

```

QED Trace

R16 ← R1; R18 ← R2; R19 ← R3

...

R1 ← R1 + 5

R16 ← R16 + 5

R1 == R16

R2 ← R2 - R1

R18 ← R18 - R16

R2 == R18

R3 ← R1 * R2

R19 ← R16 * R18

R3 == R19

...

Check end_result



Quick!

QED Improves Coverage

Validation program

```
void matgen (REAL a[], int lda, int n, REAL b[], REAL *norma)
{
    int i,j;
    int m = 3333;
    *norma = 0.0;
    for (i = 0; i < n; i++) {
        for (j = 0; j < n; j++) {
            init = 3125*init % 0x100000000;
            a[lda*i+j] = (init - 32768.0)/65536.0;
            *norma = (a[lda*i+j] > *norma) ? a[lda*i+j] : *norma;
        }
    }
    for (i = 0; i < n; i++) {
        b[i] = 0.0;
    }
    for (i = 0; i < n; i++) {
        for (j = 0; j < n; j++) {
            b[i] = b[i] + a[lda*j+i];
        }
    }
    return;
}

void dgefa (REAL a[], int lda, int n, int ipvt[], int *info)
/*
   internal variables
*/
REAL t;
int j,k,kp1,l,nml;

/*
   gaussian elimination with partial pivoting
*/

*info = 0;
nml = n - 1;
if (nml <= 0) {
    for (k = 0; k < nml; k++) {
        kp1 = k + 1;

        /* find l = pivot index */
        l = idamax(n-k, &a[lda*k+k], 1) + k;
        ipvt[k] = l;

        /* zero pivot implies this column already
           triangularized */

        if (a[lda*k+l] != ZERO) {
            /* interchange if necessary */

            if (l != k) {
                t = a[lda*k+l];
                a[lda*k+l] = a[lda*k+k];
                a[lda*k+k] = t;
            }

            /* compute multipliers */
            t = -ONE/a[lda*k+l];
            dscal(n-(k+1), t, &a[lda*k+k+1], 1);

            /* row elimination with column indexing */
            for (j = kp1; j <= n; j++) {
                t = a[lda*j+l];
                if (l != k) {
                    a[lda*j+l] = a[lda*j+k];
                    a[lda*j+k] = t;
                }
                dcopy(n-(k+1), t, &a[lda*k+k+1], 1,
                    &a[lda*j+k+1], 1);
            }
        }
        else {
            *info = k;
        }
    }
}

ipvt[n-1] = n-1;
if (a[lda*(n-1)*(n-1)] == ZERO) *info = n-1;
checkbanded(a, ipvt, info);
return;
}

void dgesl (REAL a[], int lda, int n, int ipvt[], REAL b[], int job)
{
    REAL t;
    int kb,kb1,nml;

    nml = n - 1;
    if (job == 0) {
        /* solve a * x = b
           first solve l * y = b
        */
        if (nml >= 1) {
            for (k = 0; k < nml; k++) {
                l = ipvt[k];
                t = b[l];
                if (l != k) {
                    b[l] = b[k];
                    b[k] = t;
                }
                dcopy(n-(k+1), t, &a[lda*k+k+1], 1, &b[k+1], 1);
            }
        }

        /* now solve u * x = y */
        for (kb = 0; kb < n; kb++) {
            k = n - (kb + 1);
            b[k] = b[k]/a[lda*k+k];
            t = -b[k];
            dcopy(k, t, &a[lda*k+0], 1, &b[0], 1);
        }
    }
    else {

```

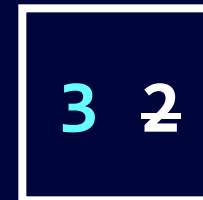
Trace

• • •

R1 ← R1 + 1



R1



• • •

R1 ← 0

• • •

Check R1 == 0

**Error
masked!**

QED Improves Coverage

Validation program

```
void matgen (REAL a[], int lda, int n, REAL b[], REAL *norma)
{
    int i, j;
    int m = 32768;
    *norma = 0.0;
    for (i = 0; i < n; i++) {
        for (j = 0; j < n; j++) {
            init = 3125*init % 0x100000000;
            a[lda*i+j] = (init - 32768.0)/6384.0;
            *norma = (a[lda*i+j] > *norma) ? a[lda*i+j] : *norma;
        }
    }
    for (i = 0; i < n; i++) {
        b[i] = 0.0;
    }
    for (i = 0; i < n; i++) {
        for (j = 0; j < n; j++) {
            b[i] = b[i] + a[lda*j+i];
        }
    }
    return;
}

void dgefa (REAL a[], int lda, int n, int ipvt[], int *info)
/* internal variables */
REAL t;
int j, k, kpl, l, mml;

/* gaussian elimination with partial pivoting */

*info = 0;
mml = n - 1;
if (mml <= 0) {
    for (k = 0; k < mml; k++) {
        kpl = k + 1;

        /* find l = pivot index */
        l = idamax(mml-k+1, &a[lda*k+k], 1) + k;
        ipvt[k] = l;

        /* zero pivot implies this column already
        triangularized */

        if (a[lda*k+k] != ZERO) {
            /* interchange if necessary */

            if (l != k) {
                t = a[lda*k+k];
                a[lda*k+k] = a[lda*k+l];
                a[lda*k+l] = t;
            }

            /* compute multipliers */
            t = -a[lda*k+k];
            dscal(mml-k+1, t, &a[lda*k+k+1], 1);

            /* row elimination with column indexing */
            for (j = kpl; j <= n; j++) {
                t = a[lda*j+k];
                if (l != k) {
                    a[lda*j+k] = a[lda*j+l];
                    a[lda*j+l] = t;
                }
                daxpy(n-(k+1), t, &a[lda*k+k+1], 1,
                    &a[lda*j+k+1], 1);
            }
        }
        else {
            *info = k;
        }
    }
}

ipvt[mml] = mml;
if (a[lda*mml](mml) == ZERO) *info = mml;
checkbipped(a, ipvt, info);
return;
}

void dgesl (REAL a[], int lda, int n, int ipvt[], REAL b[], int job)
{
    REAL t;
    int k, kb, l, mml;

    mml = n - 1;
    if (job == 0) {
        /* solve a * x = b */
        first solve l * y = b
        if (mml >= 1) {
            for (k = 0; k < mml; k++) {
                l = ipvt[k];
                t = b[k];
                if (l != k) {
                    b[k] = b[l];
                    b[l] = t;
                }
                daxpy(n-(k+1), t, &a[lda*k+k+1], 1, &b[k+1], 1);
            }
        }

        /* now solve u * x = y */
        for (kb = 0; kb < n; kb++) {
            k = n - (kb + 1);
            b[k] = b[k]/a[lda*k+k];
            t = -b[k];
            daxpy(k, t, &a[lda*k+0], 1, &b[0], 1);
        }
    }
    else {

```

QED Trace

• • •

R1 ← R1 + 1

R18 ← R18 + 1

R1 == R18

• • •

R1 ← 0

• • •

Check R1 == 0 masked!



Error

No QED: bug escape

QED: quick detection

R1

R18

3	2
2	2

Diversity-Enhanced QED

Validation program

```
void matgen (REAL a[], int lda, int n, REAL b[], REAL *norma)
{
    int i, j;
    int m = 1;
    *norma = 0.0;
    for (i = 0; i < n; i++) {
        for (j = 0; j < n; j++) {
            init = 3125*init % 0x100000000;
            a[lda*i+j] = (init - 32768.0)/65536.0;
            *norma = (a[lda*i+j] > *norma) ? a[lda*i+j] : *norma;
        }
    }
    for (i = 0; i < n; i++) {
        b[i] = 0.0;
    }
    for (i = 0; i < n; i++) {
        for (j = 0; j < n; j++) {
            b[i] = b[i] + a[lda*i+j];
        }
    }
    return;
}

void dgefa(REAL a[], int lda, int n, int ipvt[], int *info)
/*
   internal variables
*/
REAL t;
int j,k,kp1,l,nml;

/* gaussian elimination with partial pivoting */

*info = 0;
nml = n - 1;
if (nml <= 0) {
    for (k = 0; k < nml; k++) {
        kp1 = k + 1;

        /* find l = pivot index */
        l = idamax(n-k, &a[lda*k+k], 1) + k;
        ipvt[k] = l;

        /* zero pivot implies this column already
           triangularized */
        if (a[lda*k+k] != ZERO) {
            /* interchange if necessary */
            if (l != k) {
                t = a[lda*k+k];
                a[lda*k+k] = a[lda*k+l];
                a[lda*k+l] = t;
            }

            /* compute multipliers */
            t = -a[lda*k+k];
            dscal(n-k+1, t, &a[lda*k+k+1], 1);

            /* row elimination with column indexing */
            for (j = kp1; j < n; j++) {
                t = a[lda*k+j];
                if (l != k) {
                    a[lda*k+j] = a[lda*j+k];
                    a[lda*j+k] = t;
                }
                daxpy(n-(k+1), t, &a[lda*k+k+1], 1,
                    &a[lda*j+k+1], 1);
            }
        }
        else {
            *info = k;
        }
    }
}

ipvt[n-1] = n-1;
if (a[lda*(n-1)*(n-1)] == ZERO) *info = n-1;
checkiopted(a, ipvt, info);
return;
}

void dgesl(REAL a[], int lda, int n, int ipvt[], REAL b[], int job)
{
    REAL t;
    int k,kb,l,nml;

    nml = n - 1;
    if (job == 0) {
        /* solve a * x = b
           first solve l*y = b */
        if (nml >= 1) {
            for (k = 0; k < nml; k++) {
                l = ipvt[k];
                t = b[l];
                if (l != k) {
                    b[l] = b[k];
                    b[k] = t;
                }
                daxpy(n-(k+1), t, &a[lda*k+k+1], 1, &b[k+1], 1);
            }
        }

        /* now solve u*x = y */
        for (kb = 0; kb < n; kb++) {
            k = n - (kb + 1);
            b[k] = b[k]/a[lda*k+k];
            t = -b[k];
            daxpy(k, t, &a[lda*k+0], 1, &b[0], 1);
        }
    }
    else {

```

QED Trace

$$a \leftarrow 1; a' \leftarrow a; b \leftarrow 1, b' \leftarrow b$$

$$R1 \leftarrow a + b$$

$$R18 \leftarrow 5a' + 5b'$$

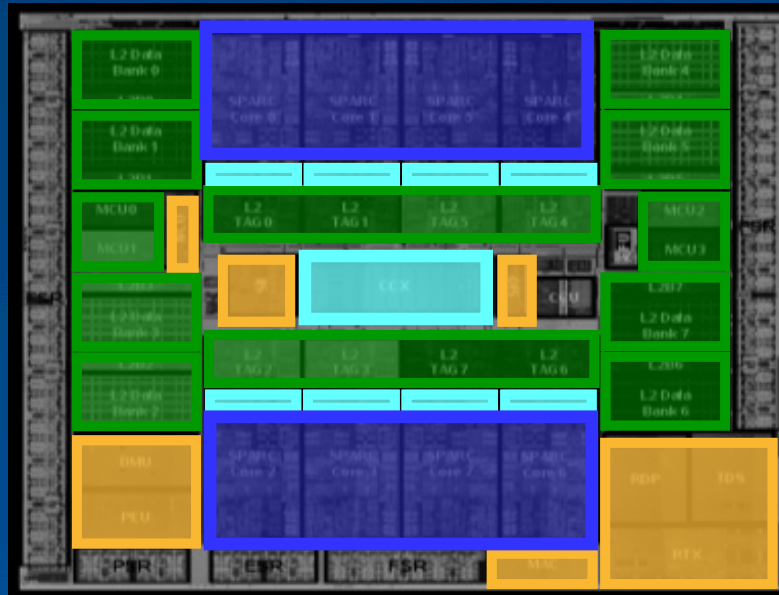
$$5 \times R1 == R18$$

	R1 62	R1
	R18 1410	R18

Many diversity techniques

e.g., ED⁴I [Oh IEEE Trans. Comp. 02]

QED Transforms



■ Processor cores

■ ■ ■ Uncore, accelerators

EDDI-V

PLC

CFTSS-V

Fast QED

CFCSS-V

Hybrid QED

Original Test

Core 1

$A = B * 2$

Store $\text{mem}[1] \leftarrow C$

Core 2

$E = F * G$

$H = D + E$

Store $\text{mem}[5] \leftarrow H$

...

Core N

$I = E / 2$

Load $J \leftarrow \text{mem}[7]$

$K = J + 1$

QED: Duplicate & Check

Core 1

$A' = A \quad B' = B \quad C' = C$

$A = B * 2 \quad B = 2$

$A' = B' * 2 \quad B' = 2$

check(A==A')

Store mem[1] ← C

Store mem[1'] ← C'

Core 2

$D' = D \quad E' = E \quad F' = F$

$G' = G \quad H' = H$

$E = F * G \quad F = G$

$E' = F' * G' \quad F' = G'$

check(E==E')

$H = D + E \quad D = E$

$H' = D' + E' \quad D' = E'$

check(H==H')

Store mem[5] ← H

Store mem[5'] ← H'

Core N

$E' = E \quad I' = E$

$J' = J \quad K' = K$

$I = E / 2 \quad E = 2$

$I' = E' / 2 \quad E' = 2$

check(I==I')

Load J ← mem[7]

Load J' ← mem[7']

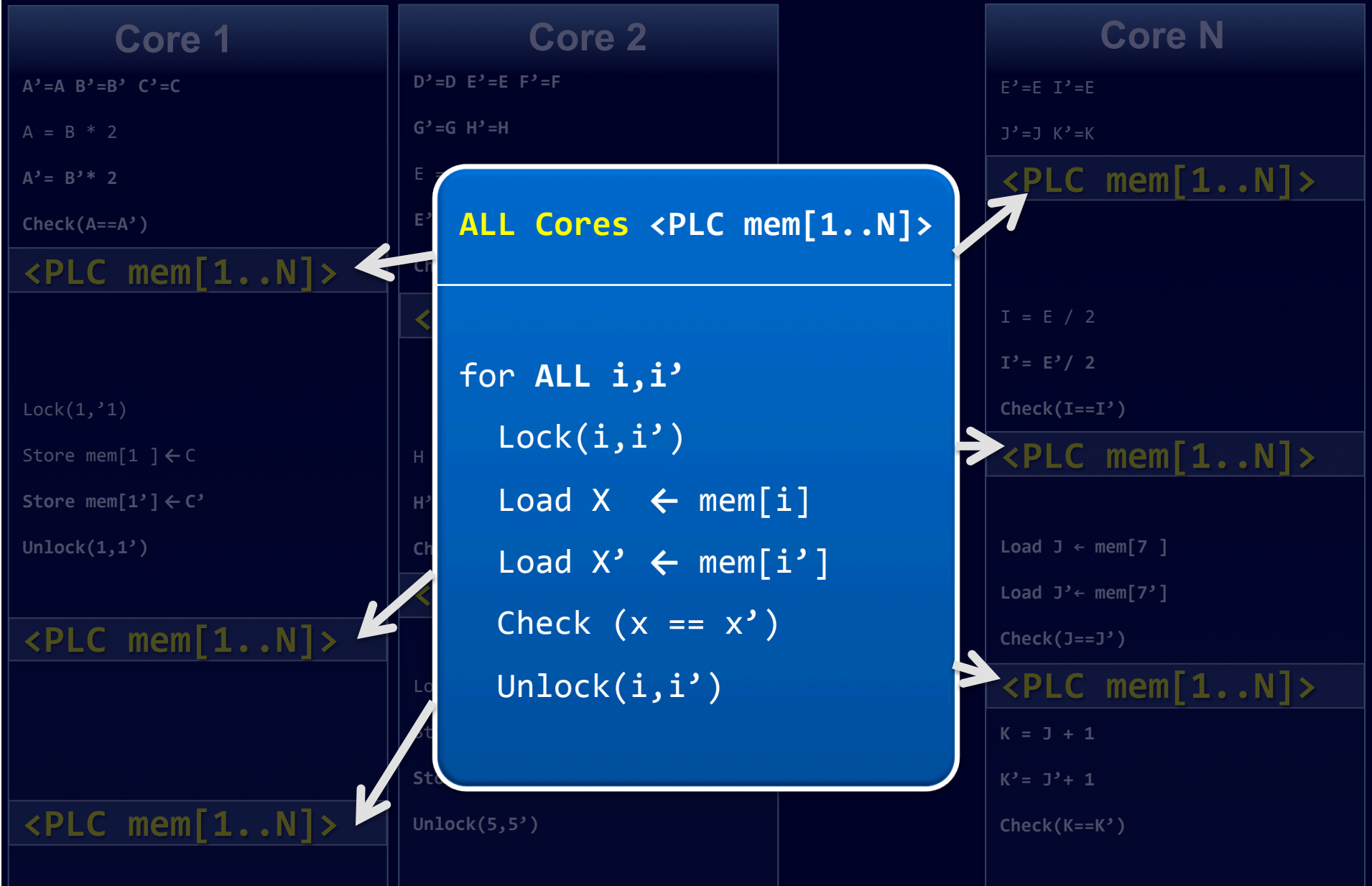
check(J==J')

$K = J + 1 \quad J = 1$

$K' = J' + 1 \quad J' = 1$

check(K==K')

QED: Proactive Load & Check



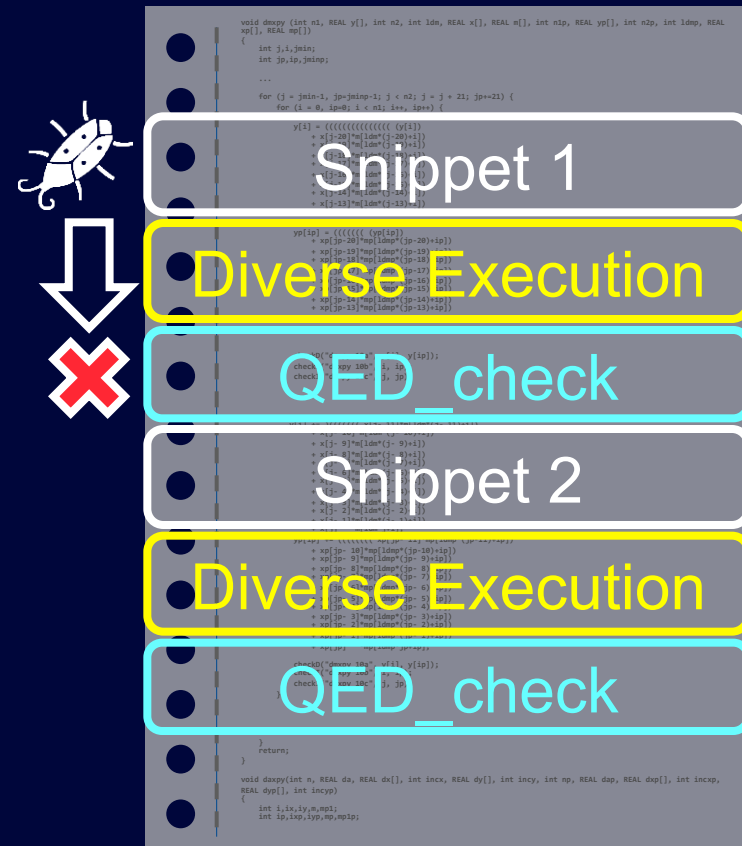
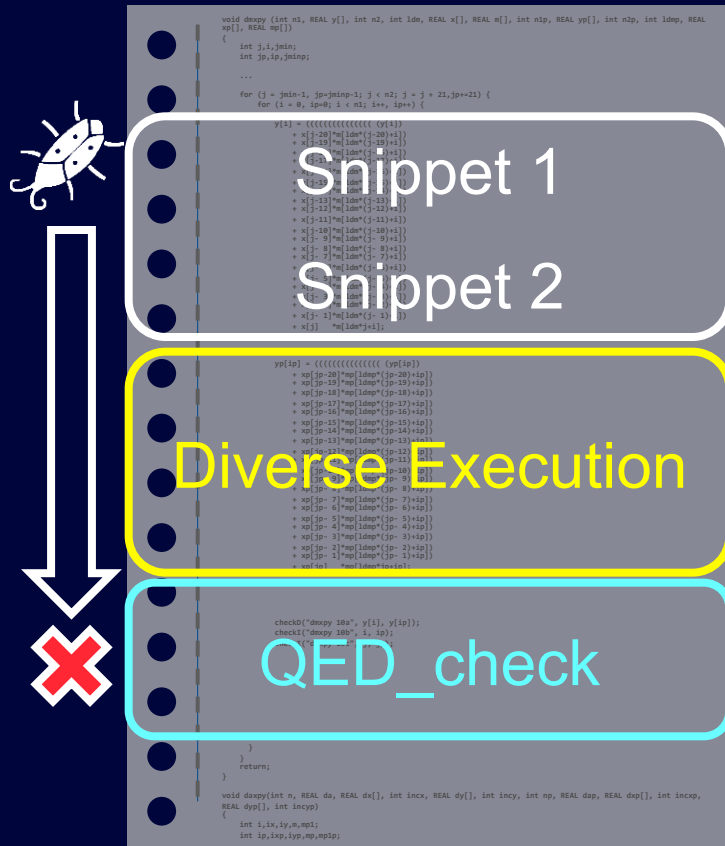
QED Coverage Considerations

- Challenge
 - Intrusiveness: coverage impact ?
- Systematic solutions
 - QED family tests
 - Hardware-enhanced QED

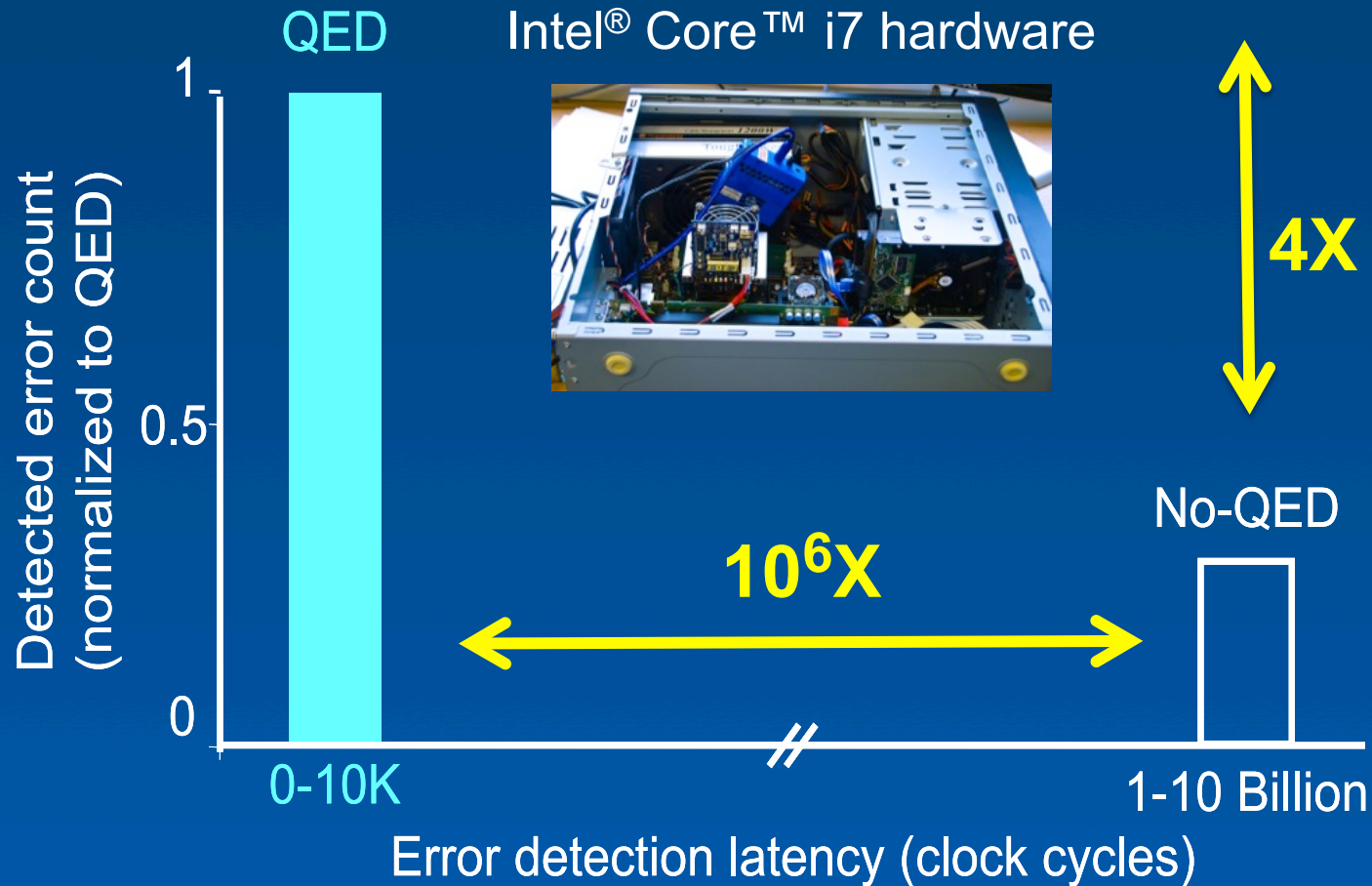
Error Detection Latency vs. Intrusiveness

😊 Improved error detection latency

😞 Increased intrusiveness?



QED Effective for Electrical Bugs



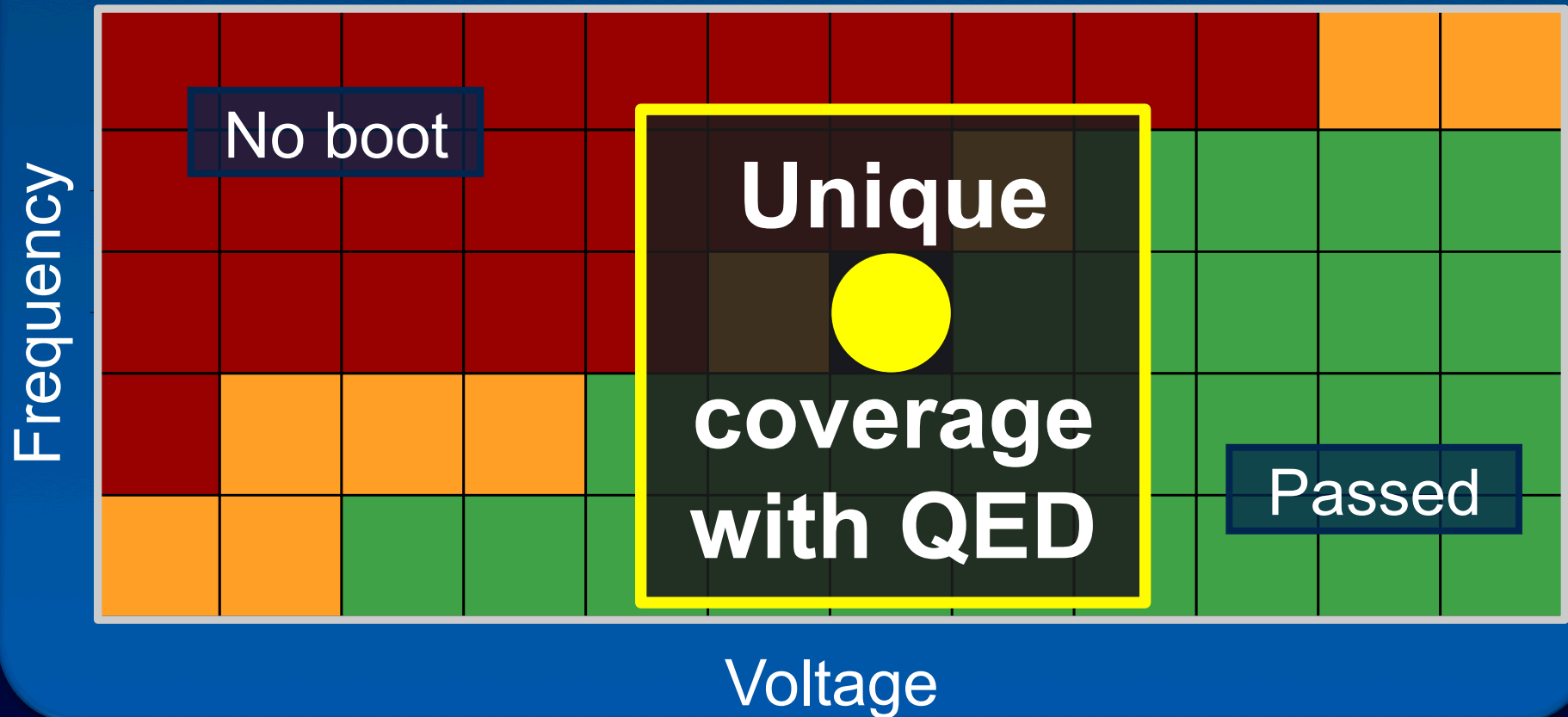
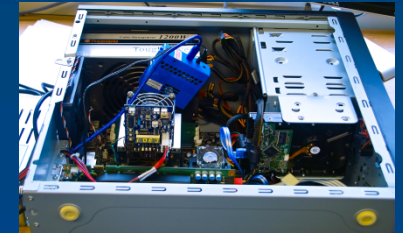
Intel® Core™ i7 Hardware



Error detected (QED and no-QED)



Error detected (QED only)



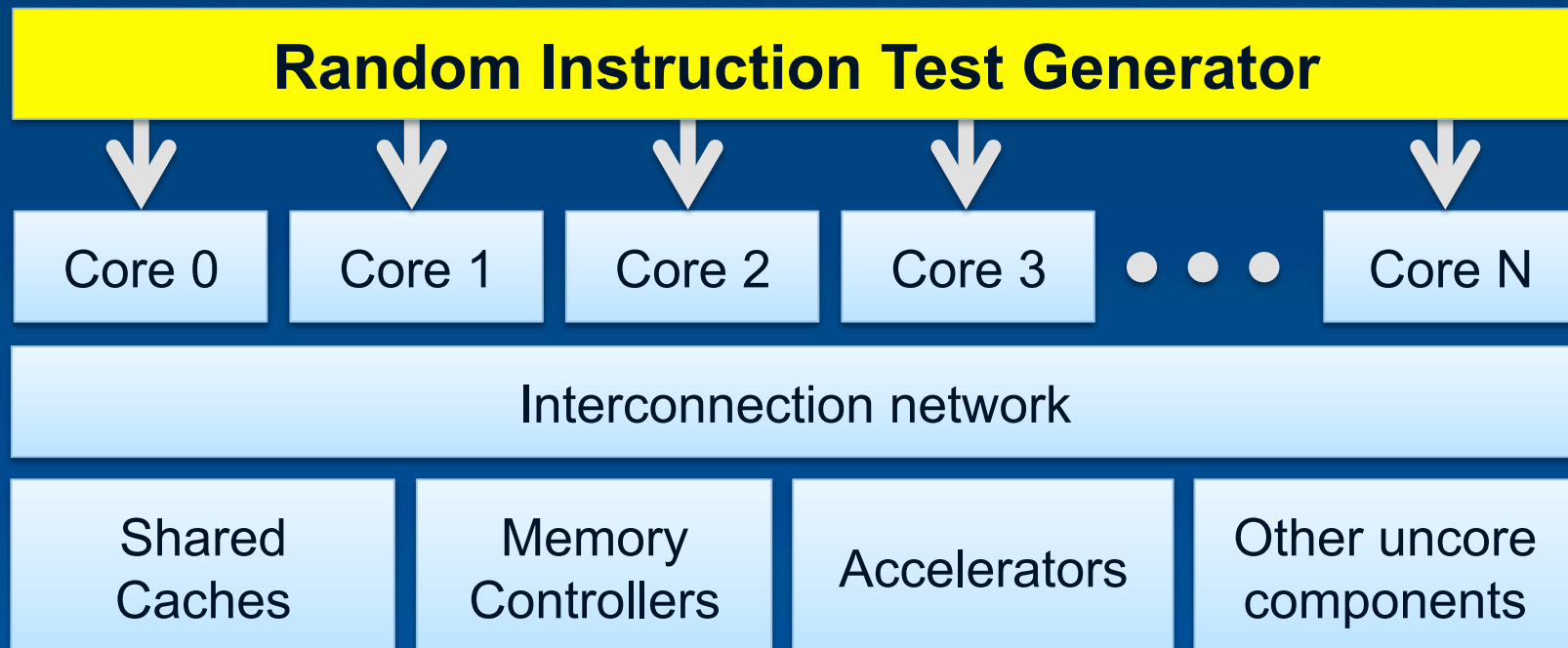
QED Effective for Logic Bugs

- “Difficult” logic bugs
 - Industrial bug databases
- Processor cores, accelerators, uncore, power management



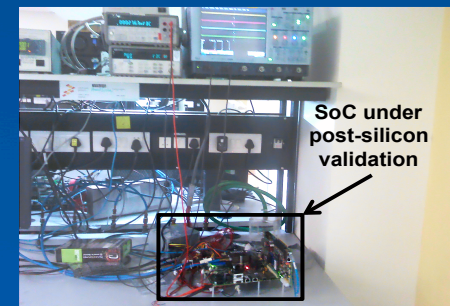
QED Logic Bugs

Freescale SoC hardware



Error detection latency (cycles)

No QED	QED
15 Billion	9



Symbolic QED

- Logic bugs: pre-silicon & post-silicon

	Traditional	Symbolic QED
Pre-silicon	Doesn't scale	20 mins to 7 hrs, automatic
Post-silicon	Weeks, months (Manual)	Overnight, automatic
	Million cycle traces	3 to 22-cycle traces

OpenSPARC T2 SoC (500M transistors): difficult bugs inserted

Traditional Bounded Model Checking

Property

Model



If property violated



Counter-example = bug trace

Traditional BMC vs. Symbolic QED

	Traditional BMC	Symbolic QED
Properties	Manual	Automatic QED checks
Design size	Small blocks	Large SoCs
False positives	Possible	None
Input constraints	Manual	QED module

Traditional BMC Challenges

1. What property ?

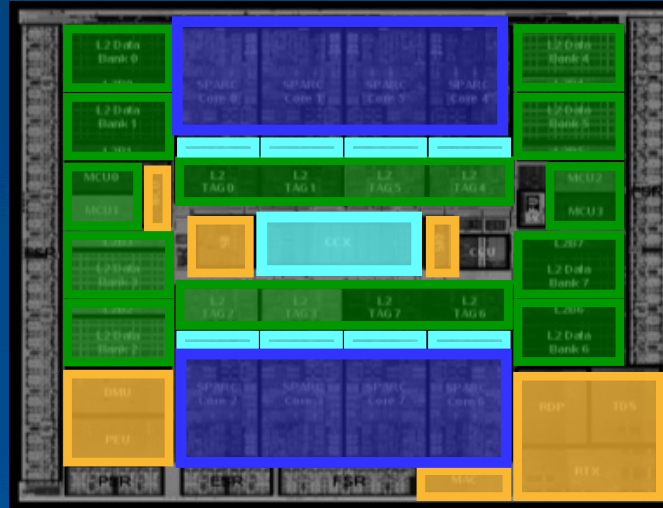
- Bugs not known *a priori*

2. Design size ?

- Big designs, cannot load

QED Transforms

System on Chip



■ Processor cores

■ ■ ■ Uncore, accelerators

EDDI-V

PLC

CFTSS-V

Fast QED

CFCSS-V

Hybrid QED

QED: Duplicate & Check

Input

$R16 \leftarrow R1; R18 \leftarrow R2; R19 \leftarrow R3$

...

$R1 \leftarrow R1 + 5$

$R2 \leftarrow R2 - R1$

$R3 \leftarrow R1 * R2$

$R16 \leftarrow R16 + 5$

$R18 \leftarrow R18 - R16$

$R19 \leftarrow R16 * R18$

$\text{CMP } R1 == R16$

$\text{CMP } R2 == R18$

$\text{CMP } R3 == R19$

...



Quick!



“Universal” Property: QED Check

CMP Ra == Ra'

- Ra – original register
- Ra' – corresponding duplicated register
- $Ra \neq Ra'$ – error detected

BMC Symbolic QED

“Universal” Property

Model



If property violated



Counter-example = bug trace

Need Input Constraints

- If unconstrained, BMC may choose any inputs

$Ra \leftarrow 1$

$Ra' \leftarrow 2$

CMP $Ra == Ra'$

- False fail – not a bug

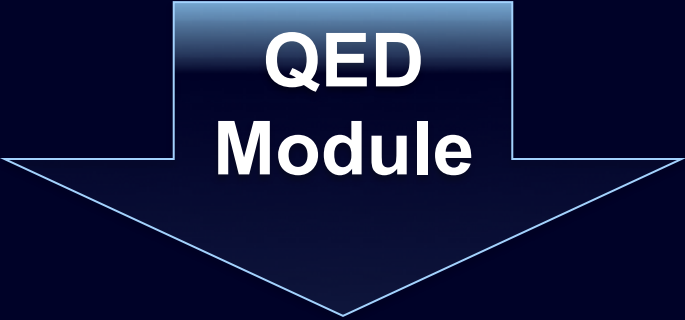
Solution: QED Module

Only during BMC, not in fabricated chip

Input
(Chosen by BMC)

```
ST [0x10000], Ra  
ST [0x10040], Rb  
LD Rc, [0x10000]
```

**QED
Module**

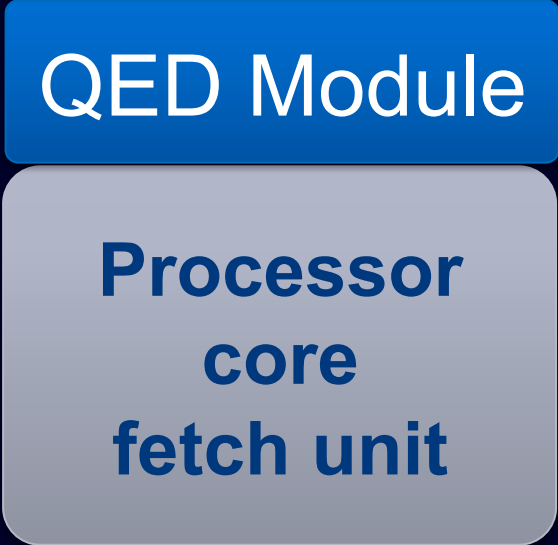


Output

```
ST [0x10000], Ra  
ST [0x10040], Rb  
LD Rc, [0x10000]  
ST [0x20000], Ra'  
ST [0x20040], Rb'  
LD Rc', [0x20000]  
<COMPARES>
```


Solution: QED Module

Only during BMC, not in fabricated chip



QED Module

Processor
core
fetch unit

- Automatically duplicates instructions
- Determines when QED checks happen

BMC Symbolic QED

“Universal” Property

Model + QED Module
(no hardware overhead)



If property violated



Counter-example = bug trace

Initial State Important

- If unconstrained, BMC may choose any initial state

$Ra = 1$ $Ra' = 2$ // initial state

$Ra = Ra + 1; Ra' = Ra' + 1; \text{CMP } Ra == Ra'$

- QED-consistent initial state
 - Run “simple” QED test
- More sophisticated [Fadiheh DATE 2018]

BMC Symbolic QED

“Universal” Property +
QED-consistent initial state

Model + QED Module
(no hardware overhead)



If property violated



Counter-example = bug trace

Symbolic QED Results

RIDECORE: RISC-V super-scalar core

3 new bugs: previously unknown

Difficult & complex corner cases

~ 1 minute Symbolic QED run

Automatic: no manual properties, constraints, etc.

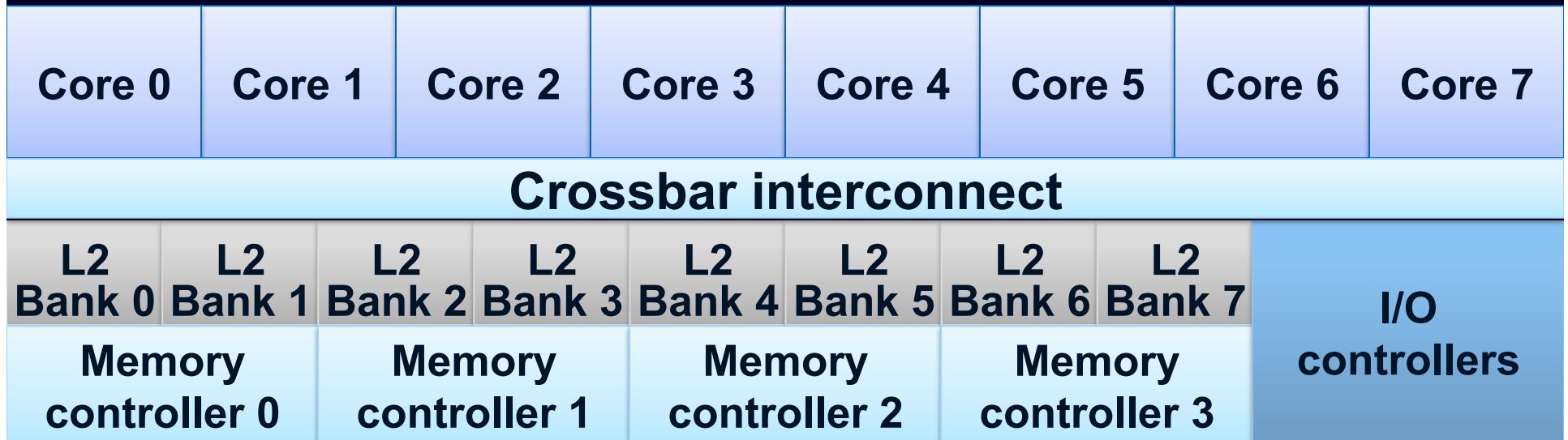
Confirmed & fixed by designers

(<https://github.com/ridecore/ridecore/issues/4>)

BUT...

- Big designs ?
- **Solution: QED checks compositional**
 - Preserved across partial instances
 - Not design- / implementation-specific

Solution: Partial Instantiation

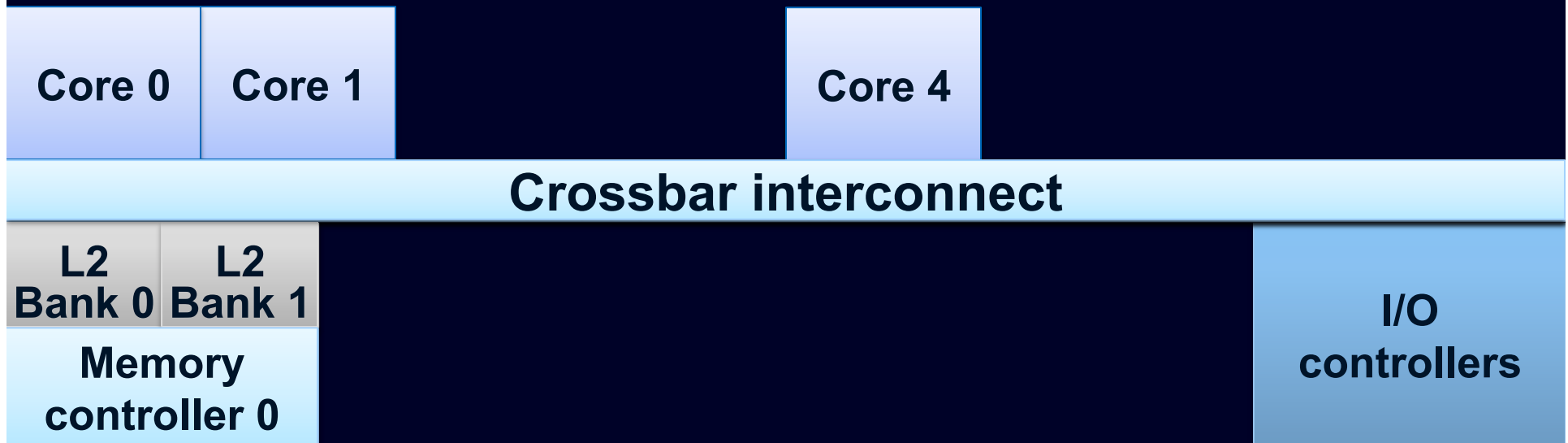


Solution: Partial Instantiation

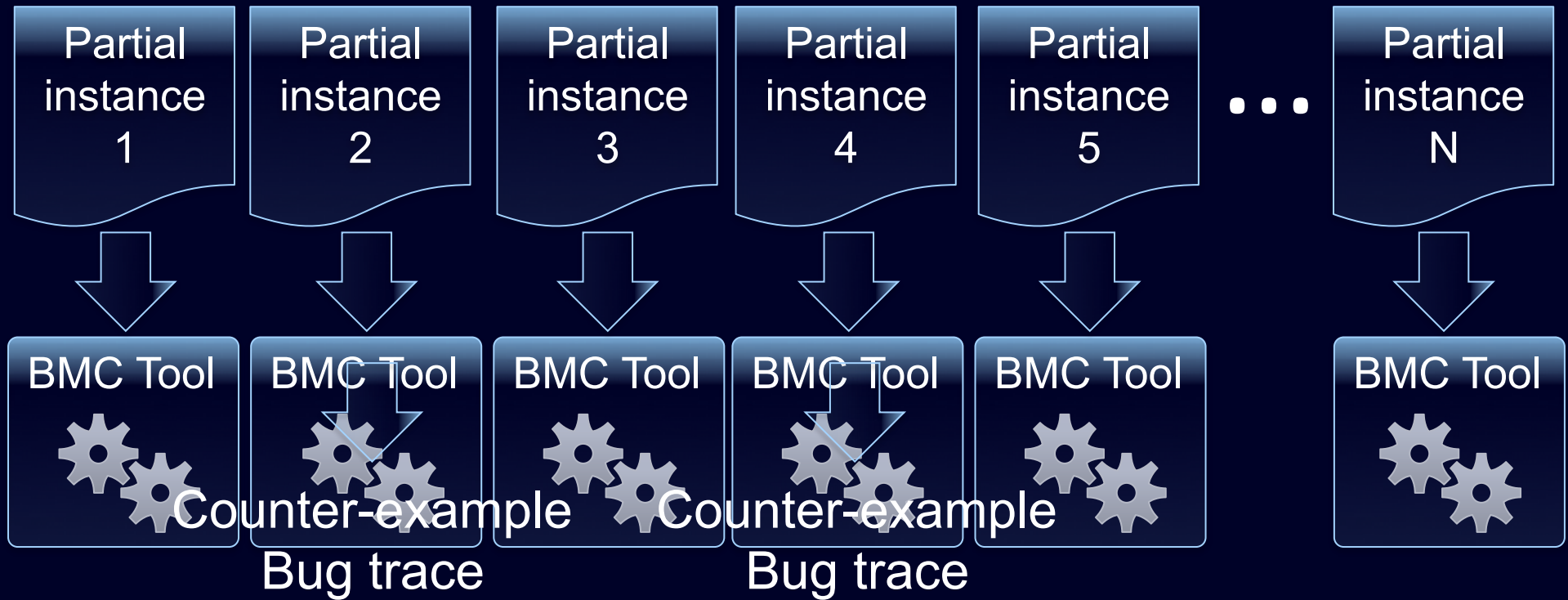


**Partial
instances**

- At least 1 processor core per partial instance



BMC on Partial Instances



Symbolic QED Results

	Traditional	Symbolic QED
Pre-silicon	BMC doesn't scale	20 mins to 7 hrs, automatic
Post-silicon	Weeks, months (Manual)	Overnight, automatic
	Million cycle traces	3 to 22-cycle traces

OpenSPARC T2 SoC (500M transistors): difficult bugs inserted

E-QED

- Electrical bugs: post-silicon debug

Design RTL

```
// Memory Write Block
// Write Operation : When we_0 = 1,
cs_0 = 1
always @ (address_0 or cs_0 or we_0
or data_0 47 or address_1 or cs_1 or
we_1 or data_1)
begin : MEM_WRITE
if ( cs_0 && we_0 ) begin
mem[address_0] <= data_0;
end else if (cs_1 && we_1) begin
mem[address_1] <= data_1;
end end
```

Record
test inputs

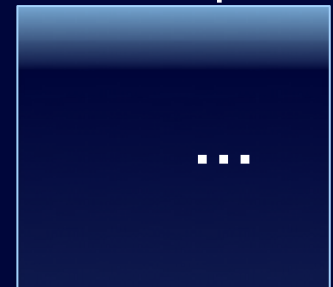
0	1	1	1
0	0	1	0
1	1	0	...
0	1	1	1

Chip



Electrical bug

Record
test outputs



Find
inconsistencies

Electrical bug candidates (e.g., flip-flops)

E-QED

Design phase: E-QED signature blocks



QED post-silicon validation tests



Localize error: formal methods

E-QED

- Electrical bugs: post-silicon debug

	E-QED
Flip-flop candidates (~1 million total)	18 flip-flops (50,000× localization)
Area impact	2.5% (actually 0%)
Debug effort	Automatic
Runtime	~ 9 hours

OpenSPARC T2 SoC (500M transistors)

Thanks to Students & Collaborators



Thanks to Sponsors



QED & Symbolic QED

- Pre-silicon verification, post-silicon debug
- Billion-transistor SoCs
- Overnight (vs. weeks or months)
- Automatic (vs. manual)
- Broadly applicable
 - Core, uncore, accelerator, logic & electrical bugs