

Embedded Development Platform



EDP System Manual

This document contains information on the structure
and features of the EDP system phase 1

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1. The EDP System

1.1 Introduction

1.1.1 EDP Baseboard

The EDP Baseboard (or “motherboard”) consists of 4 ‘stations’ with the minimum configuration of the motherboard with a single plug-in processor module. All 4 stations are identical, and there are many permutations of CPU modules and Application modules possible. Even with just the minimum configuration of Motherboard and CPU module for example, you can easily run a web-server through the standard onboard Ethernet connection. There are various application modules; we have introduced an initial starter range consisting of basic digital and analogue I/O, a motor control module and a communications module. The more advanced user will discover that it is possible to run more than one processor module on the motherboard in a Master and Slave configuration.

The motherboard is an Extended Euro card size (220 x 100 mm) fitted with rubber feet to lay flat on the bench, but able to be used in a standard rack system. Add a 64-way DIN (RS 381-8696) connector and you can plug the EDP into a backplane. Connectors for four module stations are supplied, arranged to ensure correct module fitting. There are also fitted +3.3V and +5V voltage regulators, a back-up battery, an RJ45 Ethernet connector, a mini-USB connector, +12 volt power-supply jack, I/O breakout header and eight DIP switches ported onto the system I2C bus.

The DIP switches allow the user software running on a processor module to read a configuration setting, enabling I/O ports to be set up correctly, for example, or for CAN or TCP/IP addresses to be set. Depending on the capability of the particular processor module in use, up to three I2C buses and two CAN networks are available. Many of the application modules use an I2C bus for primary communication with the processor providing maximum flexibility. Some processor chips will require +5 volts, others +3.3 volts. A factory link on the module selects the correct supply from the connector. This supply is linked to a further connector pin on all the other module stations providing a correct voltage reference or bus pull-up for the application modules. There is also duplication of an analogue input unit, to give a very large number of inputs.

1.1.2 Reusable Components

The EDP baseboard is designed to be used and reused with new CPU and application modules being introduced on a regular basis. Its robust design has been rigorously tested, and every effort has been made at the design stage to protect the EDP from the most common human errors: the motherboard will have a significantly longer life than the average development board and is suitable for use in specialist one-off and low-volume products. Typical applications might be industrial controllers, scientific instrument controllers, datalogging and remote monitoring. For these reasons the EDP will prove attractive to all design engineers looking for a cost effective solution which allows them to significantly improve their development process and thus deliver products in reduced time. Design engineers, consultants, educators and trainers will quickly realise the benefits and recognise the potential of the development platform modules system as an effective solution.

1.1.3 Bread-Boarding Platform

With the difficulty in applying traditional “bread-boarding” techniques to today’s tiny SMT components, evaluating new active devices has become major problem. There is usually no alternative to creating a special “try-out” PCB using rapid PCB production houses just to get a new device up and running. The EDP has been designed to host such experimental and trial designs, providing “clean” 5 and 3V3 supplies and instant access to a range of standard microcontrollers and IO blocks and devices. The design information necessary to allow you to create your own module for experimenting with new devices is available free of charge but in many cases, RS will already have such a module available to save you the effort.

The EDP represents the start of a continuous launch process which will see the introduction of new processor and application modules on a monthly basis.

1.2 EDP Modules Available Now

Processor Module: ST Microelectronics STR912

Processor Module: Infineon XC167

Application Module: Analogue Input

Application Module: Digital Input/Output

Application Module: Brushed DC Motor Control

Application Module: Basic Communications

1.3 Basic EDP Concepts

The EDP allows microcontrollers and IO devices to communicate through a standardised interface. To some extent this interface is analogous to PC104 or STE busses where a connector pinout is defined that allows the interconnection of address and data-bus connected devices. Such busses tend to include only power line, data and address busses plus control signals such as chipselects and interrupt request lines.

Pin	A	B
1	IOCHCK#	GND
2	D7	RSTDRV
3	D6	+5V
4	D5	IRQ9
5	D4	+5V
6	D3	DRQ2
7	D2	-12V
8	D1	ENDXFR#
9	D0	+12V
10	IOCHRDY	GND/KEY
11	AEN	SMEMW#
12	A19	SMEMR#
13	A18	IOW#
14	A17	IOR#
15	A16	DACK3#
16	A15	DRQ3
17	A14	DACK1#
18	A13	DRQ1
19	A12	REFRESH#
20	A11	SYSCLK
21	A10	IRQ7
22	A9	IRQ6
23	A8	IRQ5
24	A7	IRQ4
25	A6	IRQ3
26	A5	DACK2#
27	A4	TC
28	A3	BALE
29	A2	+5V
30	A1	OSC
31	A0	GND
32	GND	GND

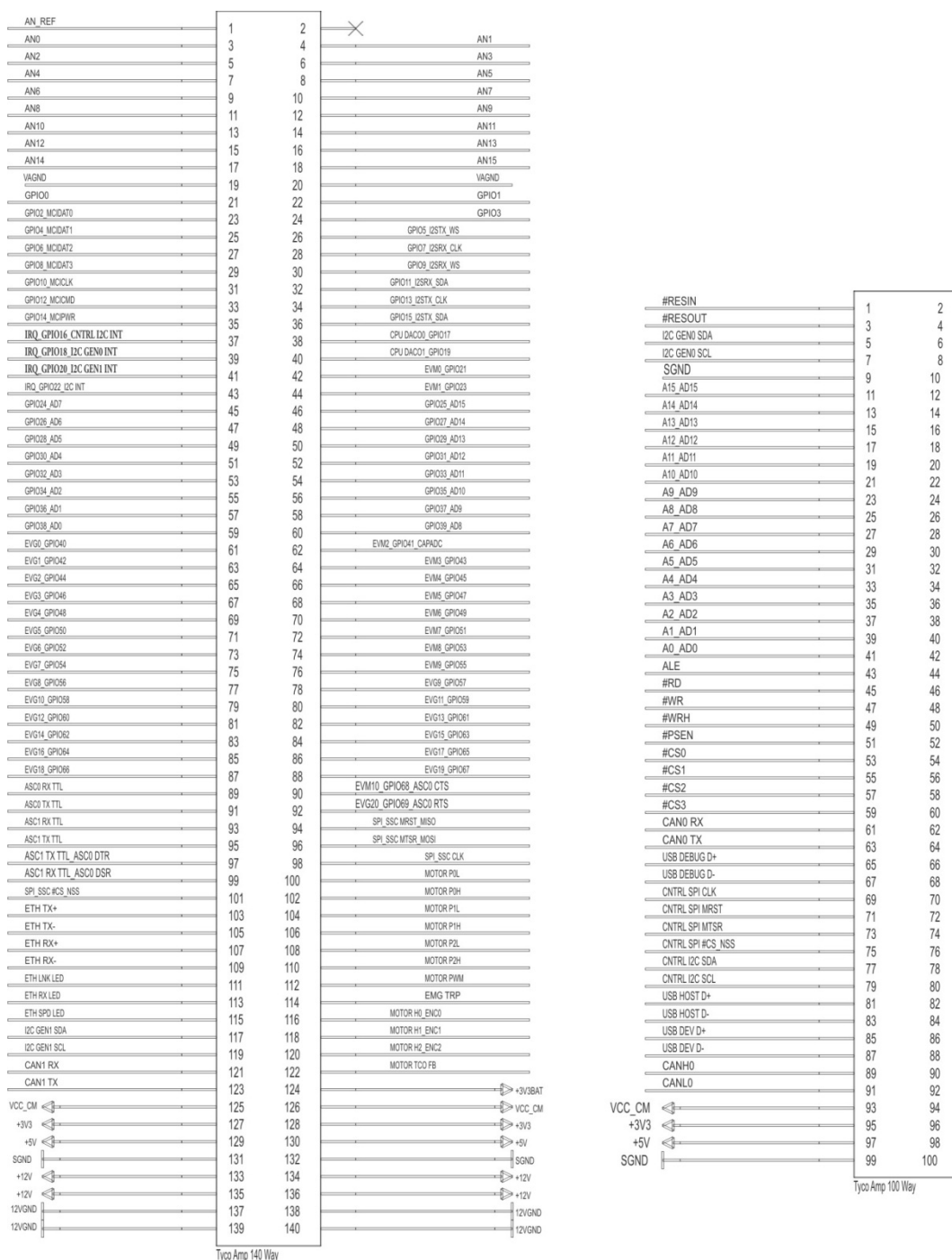
Pin	D	C
0	GND	GND
1	MEMCS16#	SBHE#
2	IOCS16#	LA23
3	IRQ10	LA22
4	IRQ11	LA21
5	IRQ12	LA20
6	IRQ15	LA19
7	IRQ14	LA18
8	DACK0#	LA17
9	DRQ0	MEMR#
10	DACK5#	MEMW#
11	DRQ5	SD8
12	DACK6#	SD9
13	DRQ6	SD10
14	DACK7#	SD11
15	DRQ7	SD12
16	+5V	SD13
17	MASTER#	SD14
18	GND	SD15
19	GND	GND/KEY

For microcontroller systems, such a collection of signals is of very limited use, especially for single-chip CPUs that use no external bus. It also takes no account of the specialist pin functions available on microcontrollers such as CAN, I2C, SPI, signal measurement and signal generation peripherals.

1.3.1 Standardised Signal Set For Embedded Microcontrollers

The EDPCON1 and 2 connectors thus defines a set of signals on a standardised format that are relevant to typical 8, 16 and 32-bit microcontrollers. In addition to address bus, data bus and chip select signals, they include 3 I2C channels, 2 CAN channels, groups of pins able to create interrupts in response to external events, groups of pins able to create pulsetrains, others dedicated to motor control, I2S, memory cards and many other common microcontroller IO types.

All of these signals are contained within two 0.8mm dual-row connectors of 140 and 100 pins each.

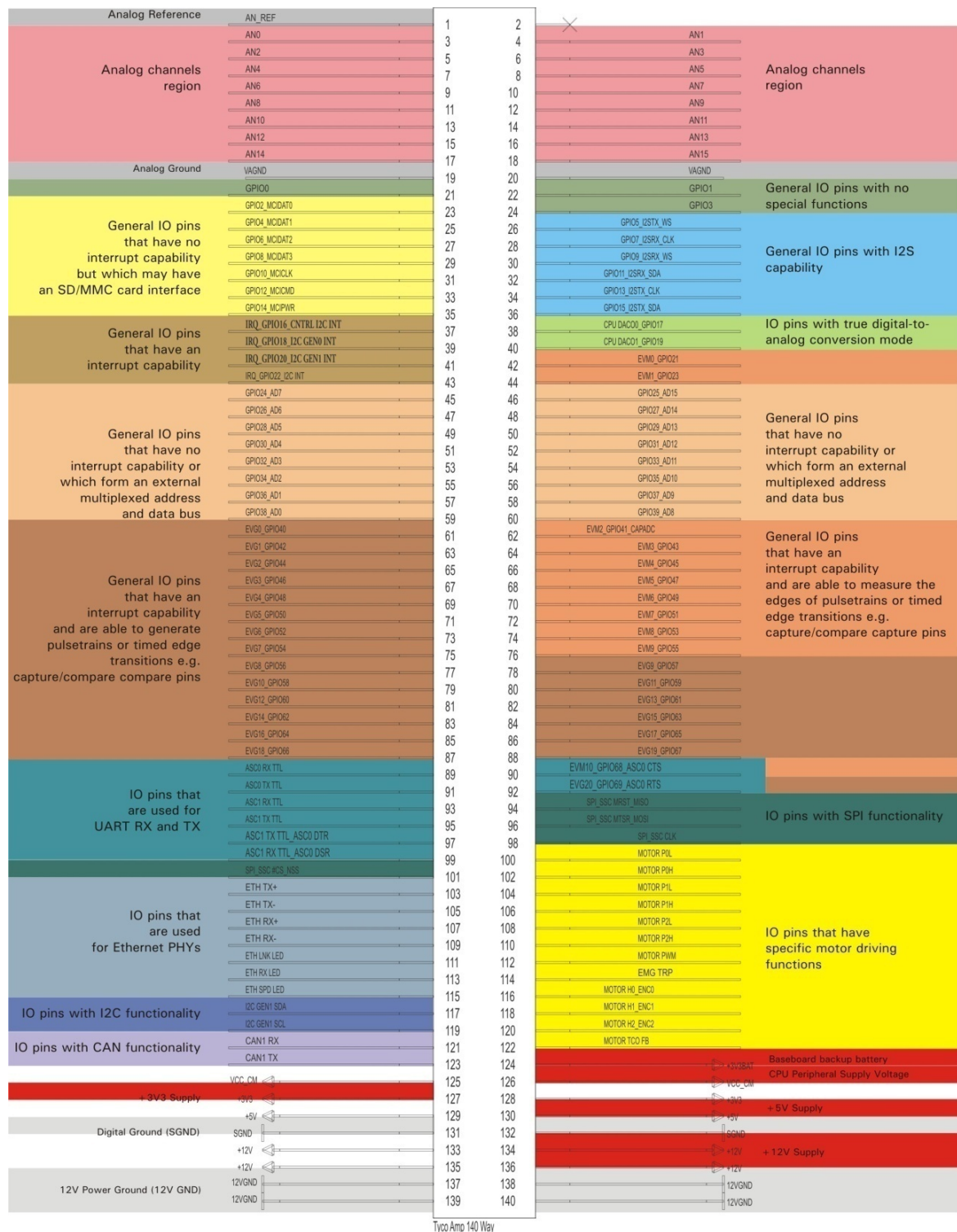


1.3.2 Grouping Of Signals On The EDP Connectors

The EDPCON1 and 2 connector specification divide the total available 240 pins into groups or regions of similar characteristics, as shown below:

1.3.2.1 EDPCON1 Connector IO Regions

EDPCON1 carries both analog and digital signals. The analog signals are grouped together in a “quiet zone”.



1.3.2.2 EDPCON2 Connector Regions

EDPCON2 carries mainly bus signals such as I2C, SPI, CAN and the multiplexed 16-bit external bus from the CPU module.

CPU Reset IN & OUT	#RESIN	1	2
	#RESOUT	3	4
IO pins with I2C capability	I2C GEN0 SDA	5	6
	I2C GEN0 SCL	7	8
	SGND	9	10
16 bit address and databus	A15_AD15	11	12
	A14_AD14	13	14
	A13_AD13	15	16
	A12_AD12	17	18
	A11_AD11	19	20
	A10_AD10	21	22
	A9_AD9	23	24
	A8_AD8	25	26
	A7_AD7	27	28
	A6_AD6	29	30
	A5_AD5	31	32
	A4_AD4	33	34
	A3_AD3	35	36
	A2_AD2	37	38
	A1_AD1	39	40
	A0_AD0	41	42
Address and databus control lines	ALE	43	44
	#RD	45	46
	#WR	47	48
	#WRH	49	50
Address and databus chip selects	#PSEN	51	52
	#CS0	53	54
	#CS1	55	56
	#CS2	57	58
CAN RX/TX	CAN0 RX	59	60
	CAN0 TX	61	62
USB interface to USB-JTAG debug	USB DEBUG D+	63	64
	USB DEBUG D-	65	66
SPI pins	CNTRL SPI CLK	67	68
	CNTRL SPI MRST	69	70
	CNTRL SPI MTSR	71	72
	CNTRL SPI #CS_NSS	73	74
I2C pins	CNTRL I2C SDA	75	76
	CNTRL I2C SCL	77	78
IO pins with USB and/or USB device capabilities	USB HOST D+	79	80
	USB HOST D-	81	82
	USB DEV D+	83	84
	USB DEV D-	85	86
CAN physical layer	CANH0	87	88
	CANL0	89	90
VCC_CM	+3V3	91	92
	+5V	93	94
	SGND	95	96
		97	98
		99	100

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1.3.3 EDP Signal Names

The generic signals present on the connectors have names which indicate their primary and secondary functions.

1.3.3.1 EDPCON1 Signal Description

ANx:	Analog signals
VAGND:	Analog ground, referenced to CPU and Analog application analog signal grounds
GPIOx:	Pins that can only be set to 1 or 0 by a CPU instruction. It has no special or alternate function.
GPIOx_MCIxxx:	Pins that have basic IO function like "GPIOx" but which also form an SM/MMC card interface
GPIOx_I2S_XXX:	Pins that have basic IO function like "GPIOx" but which also form an I2S interface.
IRQx_GPIOx_X_I2C_INT:	Pins that are used by the three I2C busses to request a CPU interrupt. Note: IRQ_GPIO16_CNTRL_I2C_INT should always be reserved for use by the I2C CNTRL I2C bus.
CPU_DACx_GPIOx:	Pins where CPUs with true digital to analog converter outputs are always connected. Alternatively, PWM will be available if there is no DAC.
EVMx_GPIOx:	Pins which have basic IO function but which also can measure timed events, pulse times and durations e.g. CAPCOM input.
GPIOx_ADx:	Pins with basic IO function but which also can form a multiplexed address and data bus.
EVGx_GPIOx:	Pins which have basic IO function but which also can generate events like timed pulses and transitions e.g. CAPCOM output.
EVM2_GPIO41_CAPADC:	Pins which have basic IO function but which also can measure pulse times and durations e.g. CAPCOM input. If the CPU supports the triggering of ADC readings on an edge, the function will be on this pin.
ASC0_RX_TTL:	Logic level connection to CPU module's serial port 0 receive pin.
ASC0_TX_TTL:	Logic level connection to CPU module's serial port 0 transmit pin.
ASC1_RX_TTL:	Logic level connection to CPU module's serial port 1 receive pin.
ASC1_TX_TTL:	Logic level connection to CPU module's serial port 1 transmit pin.
ASC1_TX_TTL_ASC0_DTR:	If CPU supports DTR function on ASC0, the function is available here.
ASC1_RX_TTL_ASC0_DSR:	If CPU supports DSR function on ASC0, the function is available here.
EVM_GPIOx_ASC0_xTS:	Event measurement, general IO and ASC0 RTS and CTS functions, where available.
SPI_XXXX:	Pins associated with SPI function, where supported by CPU module.
ETH_xxx:	Pins connected to an Ethernet PHY on CPU module, where available.
I2C_GEN1_SDA/SCL:	Pins connected to CPU's I2c channel 1
MOTOR_XXXX:	Pins required for driving three-phase AC and DC brushless motors, including inputs for Hall sensors and tachometers or other speed-related signals.
EMRG_TRP:	Emergency stop/trip function for motor control.
CAN1_RX/TX:	Logic level connection to CPU module's second CAN module (where fitted).
VCC_CM:	Peripheral operating voltage of CPU module currently fitted.
+3V3:	+3V3 supply from baseboard voltage regulator
+5V:	+5V supply from baseboard voltage regulator

+12V:	Raw 12V from power input to baseboard
12VGND:	Ground connection to power supply.
SGND:	Digital logic ground (connects to 12VGND at star point in baseboard)
3V3 Vbatt:	Permanent 3V3 supply from Lithium cell on baseboard (where fitted)

1.3.3.2 EDPCON2 Signal Description

#RESIN:	Reset input to CPU module
#RESEOUT:	Reset out signal from CPU module (where available)
I2C_GEN0_SDA/SCL:	Secondary I2C bus data and clock (where available)
SGND:	Digital logic ground (connects to 12VGND at star point in baseboard)
Axx_ADxx:	16 bit multiplexed address/data bus when enabled by jumpers on CPU module.
ALE:	CPU module's address latch enable signal
#RD:	CPU module's READ signal
#WR:	CPU module's WRITE (or WRITELOW) signal
#WRH:	CPU module's WRITE (or WRITEHIGH) signal
#PSEN_A16:	CPU module's PSEN signal (8051) or A16, where available
#CS0:	CPU module's first chipselect signal
#CS1:	CPU module's second chipselect signal
#CS2:	CPU module's third chipselect signal
#CS3:	CPU module's fourth chipselect signal
CAN0_RX/TX:	Logic level connection to CPU module's first CAN module (where fitted).
USB-DEBUG +/-	USB signals connected to FTDI USB-JTAG device on CPU module
CNTRL_SPI_XX:	Signals connected to CPU module's first SPI peripheral
CNTRL_I2C_SDA/SCL:	Signals connected to CPU module's first or primary I2C channel. (This is the I2C control backbone for the EDP baseboard).
CANH0/CANL0:	CPU module's first CAN module via physical layer drivers.
VCC_CM:	Peripheral operating voltage of CPU module currently fitted.
+3V3:	+3V3 supply from baseboard voltage regulator
+5V:	+5V supply from baseboard voltage regulator
SGND:	Digital logic ground (connects to 12VGND at star point in baseboard)

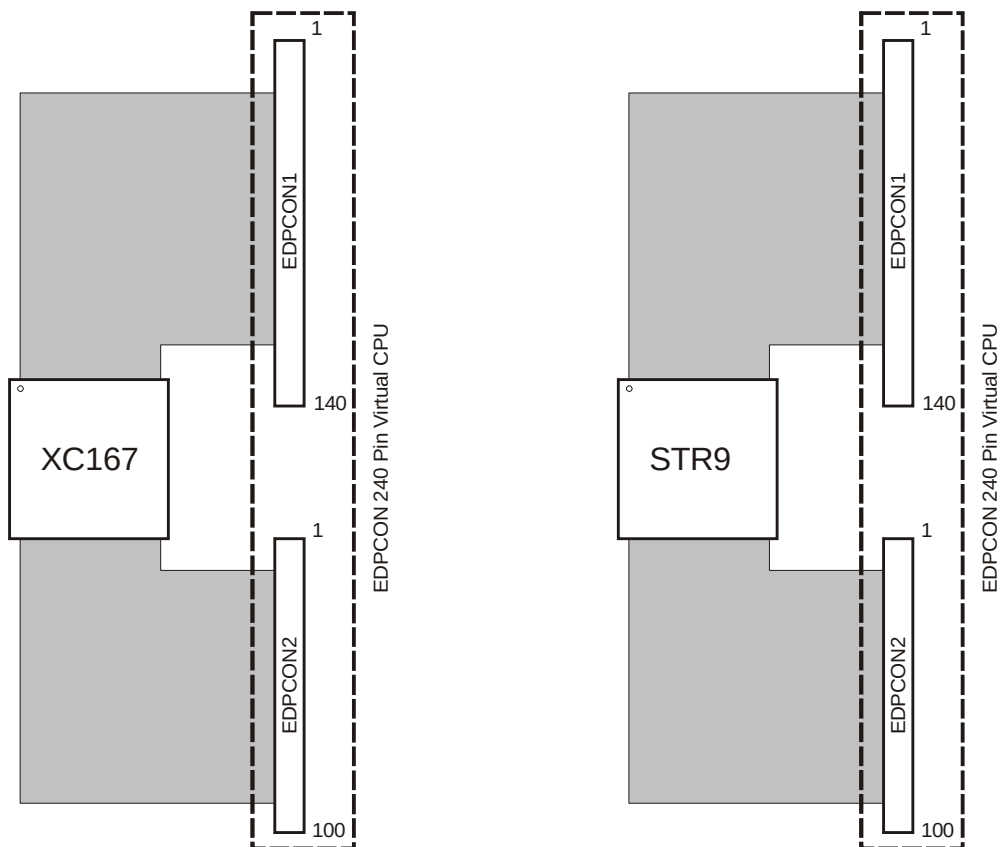
1.4 The EDP Virtual CPU Concept

A microcontroller that has its IO pins mapped appropriately onto the EDPCON1 and EDPCON2 connectors appears to be a virtual CPU to other IO devices fitted on the bus. Thus for example, a 14-bit ADC device on the EDPCON baseboard will see a CPU module also on the bus, as a virtual CPU whose pinout is defined by the EDP bus. Currently two popular microcontrollers (Infineon XC167 and ST STR9) have had their IO pins mapped onto the EDPCON system. These two devices have some features in common -UARTs, capture and compare pins, ADC, CAN but the STR9 also has USB device. Thus the pin mapping to the EDPCON is not 100% in that on the XC167 version, the USB device pins are unused. Both devices have dedicated motor control peripherals which although they have different pin names, have virtually the same functionality.

Hence for example, a brushless DC motor control module with half-bridges can be designed to interface to the motor control region of the EDPCON bus without any regard for the CPU type to be ultimately used.

The net result is that subject some limitations, a range of modules bearing different CPUs can be freely connected to a range of IO modules.

The EDPCON has been designed to accommodate all the common peripherals found on current microcontrollers, including advanced interfaces like SD/MMC and I2S. Thus it is possible to map almost any microcontroller to this format.



1.4.1 Example Of Real CPU To EDPCON Mapping

This is the mapping developed for the Infineon XC167 and used on the RS-EDP-CM-XC167 module.

1.4.1.1 Infineon XC167 – EDPCON1 Mapping

This mapping assigns the XC167 pins (and hence peripherals) into the appropriate regions on the EDPCON1 connector.

XC167 Pin
And Function

41 VAREF	AN_REF	1	2
29 AN0	AN0	3	4
31 AN2	AN2	5	6
33 AN4	AN4	7	8
39 AN6	AN6	9	10
37 AN8	AN8	11	12
35 AN10	AN10	13	14
43 AN12	AN12	15	16
45 AN14	AN14	17	18
42 GUARD/AN GND	VAGND	19	20
92 P20.2	GPIO0	21	22
128 MRST1	GPIO2_MCIDAT0	23	24
62 P3.3	GPIO4_MCIDAT1	25	26
63 P3.4	GPIO6_MCIDAT2	27	28
129 MTSR1	GPIO8_MCIDAT3	29	30
130 SCLK1	GPIO10_MCIDAT4	31	32
77 P3.15	GPIO12_MCIDAT5	33	34
83 P4.3	GPIO14_MCIDAT6	35	36
P3.2	IRQ_GPIO16_CNTRL2C_INT	37	38
P3.5	IRQ_GPIO18_I2C_GEN0_INT	39	40
P3.6	IRQ_GPIO20_I2C_GEN1_INT	41	42
P3.7	IRQ_GPIO22_I2C_INT	43	44
P0L.7	GPIO24_AD7	45	46
P0L.6	GPIO26_AD6	47	48
P0L.5	GPIO28_AD5	49	50
P0L.4	GPIO30_AD4	51	52
P0L.3	GPIO32_AD3	53	54
P0L.2	GPIO34_AD2	55	56
P0L.1	GPIO36_AD1	57	58
P0L.0	GPIO38_AD0	59	60
49 CC8IO	EVM0_GPIO40	61	62
50 CC9IO	EVM1_GPIO42	63	64
51 CC10IO	EVM2_GPIO44	65	66
52 CC11IO	EVM3_GPIO46	67	68
53 CC12IO	EVM4_GPIO48	69	70
54 CC13IO	EVM5_GPIO50	71	72
55 CC14IO	EVM6_GPIO52	73	74
56 CC15IO	EVM7_GPIO54	75	76
8 CC1IO	EVM8_GPIO56	77	78
9 CC2IO	EVM9_GPIO58	79	80
10 CC3IO	EVM10_GPIO60	81	82
11 CC4IO	EVM11_GPIO62	83	84
12 CC5IO	EVM12_GPIO64	85	86
13 CC6IO	EVM13_GPIO66	87	88
70 RxD0	ASC0_RX_TTL	89	90
69 TxD0	ASC0_TX_TTL	91	92
60 RxD1	ASC1_RX_TTL	93	94
59 TxD1	ASC1_TX_TTL	95	96
NC	ASC1_TX_TTL_ASC0_DTR	97	98
P20.2	ASC1_RX_TTL_ASC0_DSR	99	100
83 P4.3	SPI_SSC_ACS_NSS	101	102
Ethernet TX+ (CS8900)	ETH_TX+	103	104
Ethernet TX-	ETH_TX-	105	106
Ethernet RX+	ETH_RX+	107	108
Ethernet RX-	ETH_RX-	109	110
Ethernet LINK LED	ETH_LINK_LED	111	112
Ethernet RX LED	ETH_RX_LED	113	114
NC	ETH_SPD_LED	115	116
NC	I2C_GEN1_SDA	117	118
NC	I2C_GEN1_SCL	119	120
85 CAN0 RX	CAN1_RX	121	122
86 CAN0 TX	CAN1_TX	123	124
Vcc to BB	VCC_CM	125	126
Vcc 3V3 from reg	+3V3	127	128
Vcc 5V from reg	+5V	129	130
Digital GND	SGND	131	132
+12V 2A	+12V	133	134
+12V 2A	+12V	135	136
12V Power GND	12VGND	137	138
12V Power GND	12VGND	139	140

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XC167 Pin
And Function

NC	30 AN1
	32 AN3
	34 AN5
	40 AN7
	38 AN9
	36 AN11
	44 AN13
	46 AN15
	GUARD/AN GND
	80 P4.0
	81 P4.1
	64 P3.5
	65 P3.6
	66 P3.7
	12 CC5IO
	13 CC6IO
	14 CC7IO
	25 CC20IO
	26 CC21IO
	127 CC23IO
	124 CC22IO
	P0H.7
	P0H.6
	P0H.5
	P0H.4
	P0H.3
	P0H.2
	P0H.1
	P0H.0
	18 CC31IO (CS8900A INT)
	17 CC30IO
	16 CC29IO
	15 CC28IO
	134 CC27IO
	133 CC26IO
	132 CC25IO
	131 CC24IO
	24 CC19IO
	23 CC18IO
	22 CC17IO
	21 CC16IO
	56 CC15IO
	55 CC14IO
	124 CC22IO
	121 CC62
	128 MRST1
	129 MTSR1
	130 SCLK1
	117 CC60
	118 COUT60
	119 CC61
	120 COUT61
	121 CC62
	122 COUT62
	123 COUT63
	124 CTRAP
	127 #C6POS0
	128 #C6POS1
	129 #C6POS2
	61 CAPIN
	3V3 Vbatt
	Vcc to BB
	Vcc 3V3 from reg
	Vcc 5V from reg
	Digital GND
	+12V 2A
	+12V 2A
	12V Power GND
	12V Power GND

1.4.1.2. Infineon XC167 – EDPCON2 Mapping

142 #RSTIN	#RESIN	1	2
3 #RSTOUT	#RESOUT	3	4
23 SDA1	I2C GEN0 SDA	5	6
24 SCL1	I2C GEN0 SCL	7	8
Digital GND	SGND	9	10
116 AD15	A15_AD15	11	12
115 AD14	A14_AD14	13	14
114 AD13	A13_AD13	15	16
113 AD12	A12_AD12	17	18
112 AD11	A11_AD11	19	20
111 AD10	A10_AD10	21	22
106 AD9	A9_AD9	23	24
105 AD8	A8_AD8	25	26
102 AD7	A7_AD7	27	28
101 AD6	A6_AD6	29	30
100 AD5	A5_AD5	31	32
99 AD4	A4_AD4	33	34
98 AD3	A3_AD3	35	36
97 AD2	A2_AD2	37	38
96 AD1	A1_AD1	39	40
95 AD0	A0_AD0	41	42
93 #ALE	ALE	43	44
90 #RD	#RD	45	46
91 #WRL	#WR	47	48
75 #WRH	#WRH	49	50
A16	#PSEN	51	52
7 #CS0 (SRAM)	#CS0	53	54
8 #CS1 (CS8900)	#CS1	55	56
9 #CS2	#CS2	57	58
10 #CS3	#CS3	59	60
84 CAN1 RX	CAN0 RX	61	62
87 CAN1 TX	CAN0 TX	63	64
USB DEBUG D+	USB DEBUG D+	65	66
USB DEBUG D-	USB DEBUG D-	67	68
76 SCLK0	CNTRL SPI CLK	69	70
67 MRST0	CNTRL SPI MRST	71	72
68 MTSR0	CNTRL SPI MTSR	73	74
82 P4.2	CNTRL SPI #CS, NSS	75	76
25 SDA2	CNTRL I2C SDA	77	78
26 SCL2	CNTRL I2C SCL	79	80
NC	USB HOST D+	81	82
NC	USB HOST D-	83	84
NC	USB DEV D+	85	86
NC	USB DEV D-	87	88
CANH control physical layer (CAN1)	CANH0	89	90
CANL control physical layer (CAN1)	CANL0	91	92
CPU's Vcc 3V3 or 5V	VCC_CM	93	94
Vcc 3V3 from reg	+3V3	95	96
Vcc 5V from reg	+5V	97	98
Digital GND	SGND	99	100

Tyco Amp 100 Way

1.5 Inter-Module Communication

With up to 4 modules on the EDPCON bus, some form of communication is required. With a limited number of CPU pins available, it is necessary to use a serial communications protocol for example, take readings from a high-precision ADC that might be present on an IO module at the same time as read a serial EEPROM on another module. The I2C protocol is used as the main communication channel for such actions, although provision is made for SPI or even a CAN physical layer.

Module	I2C Device	Possible Range	Actual 7-bit Address	I2C channel	Actual 7-bit Address	I2C channel	Comment
			Module 1		Module 2		
Analog Module	MAX1138 address	0x35	0x35	CNTRL	0x35	Gen0	MAX1138 has no address pin so only one can be present per I2C channel
	MAX1038 address	0x65	0x65	CNTRL	0x65	Gen0	
	AD5263 BRU50 address	0x2C-0x2F	0x2C	CNTRL	0x2C	Gen0	
	PCA8575 address	0x20-0x27	0x21	CNTRL	0x21	Gen0	
Baseboard	PCF8575 24C32 (Rev B Only)	0x20-0x27	0x20	CNTRL	XXXXX	XXXXX X	0x50 is occupied by PCA8583
		0x50-0x57	0x51	CNTRL	0x52	CNTRL	
Comms AM	RTC PCA8583	0x50-0x51	0x50	CNTRL	XXXXX	XXXXX X	
Digital AM	PCF8575 IN address	0x20-0x27	0x22	CNTRL	0x24	CNTRL	
	PCF8575 OUT address	0x20-0x27	0x23	CNTRL	0x25	CNTRL	

Default I2C Addresses Used In The EDP System

There are three possible I2C channels available although in most cases the default one (I2C_CTRL) will be sufficient. EDP modules that carry I2C device do, where possible, allow the user to configure the I2C addresses. This allows for example, up to three digital IO modules to be fitted, with the GPIO devices on each module given an unique address. Where the address space of a particular I2C channel becomes full, devices can be connected to an alternative channel to get access to a completely new address space.

1.6 Inter-EDP System Communications

In a situation where there are multiple EDP baseboards, each with their own CPU modules in a complete system, I2C can still be used to allow the CPUs to communicate but it is strongly recommended to use CAN. EDP IO signals that are intended to be taken off-board are brought out on a standard DIN414162 64-way connector.

2. Using The EDP Baseboard

This section gives information on the features of the EDP baseboard, its connectors and the overall structure of the EDP system.

2.1 EDP Connectors

The EDP bus contained in the EDP baseboard is accessed through two Tyco-AMP .8mm pitch connectors. The signal names are intended to convey something of the capabilities of that signal. For example signal EVGO_GPIO40 is a pin that can generate timed events (i.e. pulses and pulse trains) as well as performing simple on/off pin control.

EDPCON1 IO Connector			
J101			
AN REF	1	2	AN1
AN0	3	4	AN3
AN2	5	6	AN5
AN4	7	8	AN7
AN6	9	10	AN9
AN10	11	12	AN11
AN12	13	14	AN13
AN14	15	16	AN15
VAGND	17	18	
GPIO0	19	20	GPIO1
GPIO2 MCIDAT0	21	22	GPIO3
GPIO4 MCIDAT1	23	24	GPIO5 I2STX_WS
GPIO6 MCIDAT2	25	26	GPIO7 I2SRX_CLK
GPIO8 MCIDAT3	27	28	GPIO9 I2SRX_WS
GPIO10 MCICLK	29	30	GPIO11 I2SRX_SDA
GPIO12 MCICMD	31	32	GPIO13 I2STX_CLK
GPIO14 MCIPWR	33	34	GPIO15 I2STX_SDA
IRQ_GPIO16 CNTRL I2C INT	35	36	CPU DAC00 GPIO17
IRQ_GPIO18 I2C GEN0 INT	37	38	CPU DAC01 GPIO19
IRQ_GPIO20 I2C GEN1 INT	39	40	EVM0 GPIO21
IRQ_GPIO22 I2C INT	41	42	EVM1 GPIO23
GPIO24 AD7	43	44	GPIO25 AD15
GPIO28 AD5	45	46	GPIO27 AD14
GPIO28 AD5	47	48	GPIO29 AD13
GPIO30 AD4	49	50	GPIO31 AD12
GPIO32 AD3	51	52	GPIO33 AD11
GPIO34 AD2	53	54	GPIO35 AD10
GPIO36 AD1	55	56	GPIO37 AD9
GPIO38 AD0	57	58	GPIO39 AD8
EVGO_GPIO40	59	60	EVM2 GPIO41 CAPADC
EVG1 GPIO42	61	62	EVM3 GPIO43
EVG2 GPIO44	63	64	EVM4 GPIO45
EVG3 GPIO46	65	66	EVM5 GPIO47
EVG4 GPIO48	67	68	EVM6 GPIO49
EVG5 GPIO50	69	70	EVM7 GPIO51
EVG6 GPIO52	71	72	EVM8 GPIO53
EVG7 GPIO54	73	74	EVM9 GPIO55
EVG8 GPIO56	75	76	EVM9 GPIO57
EVG10 GPIO58	77	78	EVG11 GPIO59
EVG12 GPIO60	79	80	EVG13 GPIO61
EVG14 GPIO62	81	82	EVG15 GPIO63
EVG16 GPIO64	83	84	EVG17 GPIO65
EVG18 GPIO66	85	86	EVG19 GPIO67
ASC0 RX TTL	87	88	EVM10 GPIO68 ASC0 CTS
ASC0 TX TTL	89	90	EVG20 GPIO69 ASC0 RTS
ASC1 RX TTL	91	92	SPI SSC MRST MISO
ASC1 TX TTL	93	94	SPI SSC MTSR MOSI
SPI SSC #CS_NSS	95	96	SPI SSC CLK
ETH TX+	97	98	MOTOR_P0H
ETH TX-	101	102	MOTOR_P0L
ETH RX+	103	104	MOTOR_P1H
ETH RX-	105	106	MOTOR_P1L
ETH RX+	107	108	MOTOR_P2H
ETH RX-	109	110	MOTOR_P2L
ETH LNK LED	111	112	MOTOR_PWM
ETH RX LED	113	114	EMG TRP
ETH SPD LED	115	116	MOTOR_H0_ENC0
I2C GEN1_SDA	117	118	MOTOR_H1_ENC1
I2C GEN1_SCL	119	120	MOTOR_H2_ENC2
CAN1 RX	121	122	MOTOR_TCO_FB
CAN1 TX	123	124	
VCC_CM	125	126	→ +3VBAT
+3V3	127	128	→ VCC_CM
+5V	129	130	→ +3V3
SGND	131	132	→ +5V
+12V	133	134	→ SGND
+12V	135	136	→ +12V
12V_GND	137	138	→ +12V
12V_GND	139	140	→ 12V_GND

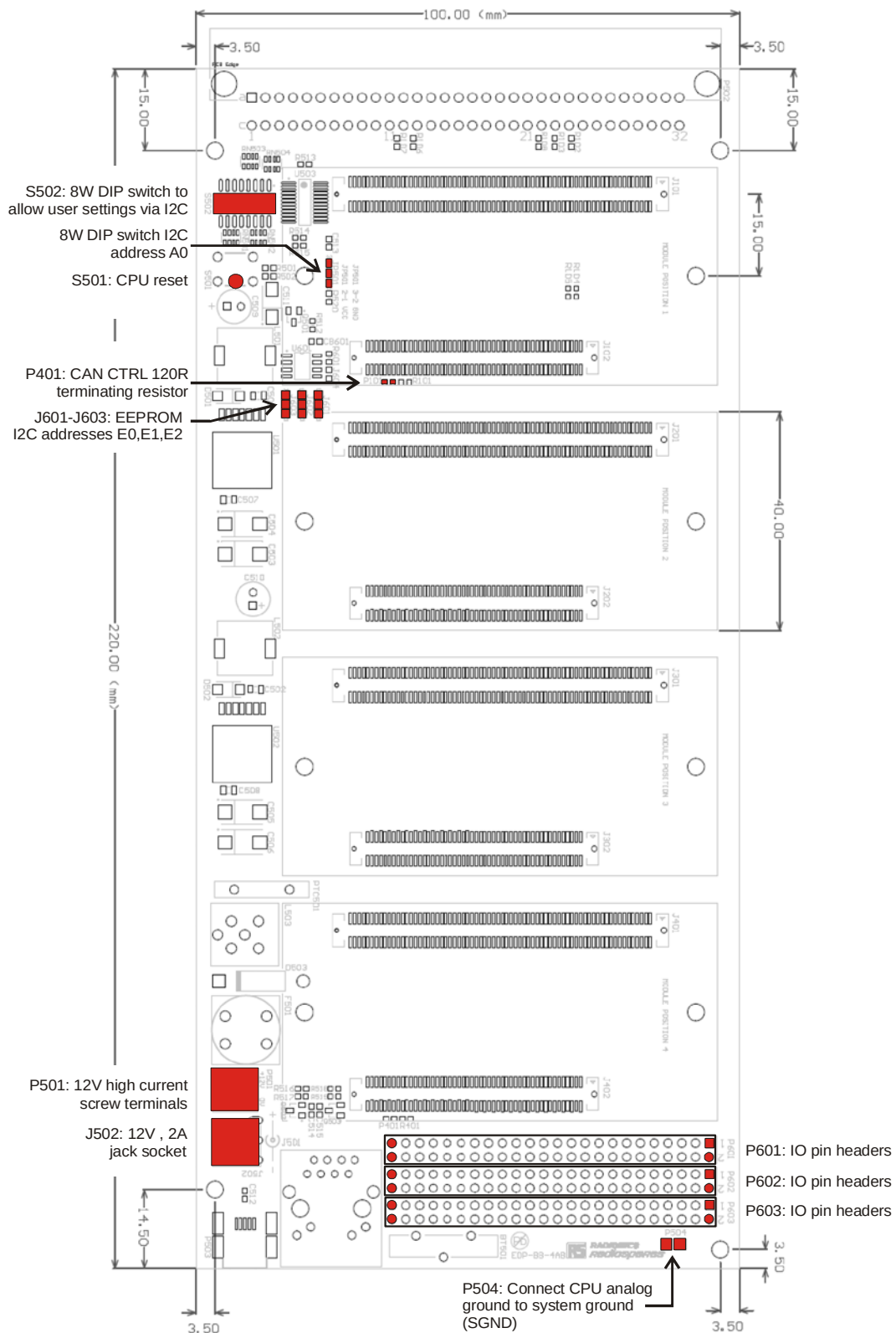
EDPCON1 Connector

EDPCON2 Bus/Control Connector			
J102			
#RESN	1	2	#RESN
#RESOUT	3	4	#RESOUT
I2C GEN0_SDA	5	6	I2C GEN0_SDA
I2C GEN0_SCL	7	8	I2C GEN0_SCL
SGND	9	10	
A15_AD15	11	12	A15_AD15
A14_AD14	13	14	A14_AD14
A13_AD13	15	16	A13_AD13
A12_AD12	17	18	A12_AD12
A11_AD11	19	20	A11_AD11
A10_AD10	21	22	A10_AD10
A9_AD9	23	24	A9_AD9
A8_AD8	25	26	A8_AD8
A7_AD7	27	28	A7_AD7
A6_AD6	29	30	A6_AD6
A5_AD5	31	32	A5_AD5
A4_AD4	33	34	A4_AD4
A3_AD3	35	36	A3_AD3
A2_AD2	37	38	A2_AD2
A1_AD1	39	40	A1_AD1
A0_AD0	41	42	A0_AD0
ALE	43	44	ALE
#RD	45	46	#RD
#WR	47	48	#WR
#PSEN	49	50	#PSEN
#CS0	51	52	#CS0
#CS1	53	54	#CS1
#CS2	55	56	#CS2
#CS3	57	58	#CS3
CAN0_RX	59	60	CAN0_RX
CAN0_TX	61	62	CAN0_TX
USB_DEBUG_D+	63	64	USB_DEBUG_D+
USB_DEBUG_D-	65	66	USB_DEBUG_D-
CNTRL_SPI_CLK	67	68	CNTRL_SPI_CLK
CNTRL_SPI_MRST	69	70	CNTRL_SPI_MRST
CNTRL_SPI_MTSR	71	72	CNTRL_SPI_MTSR
CNTRL_SPI_CS_NSS	73	74	CNTRL_SPI_CS_NSS
CNTRL_I2C_SDA	75	76	CNTRL_I2C_SDA
CNTRL_I2C_SCL	77	78	CNTRL_I2C_SCL
USB_HOST_D+	79	80	USB_HOST_D+
USB_HOST_D-	81	82	USB_HOST_D-
USB_DEV_D+	83	84	USB_DEV_D+
USB_DEV_D-	85	86	USB_DEV_D-
CANH0	87	88	CANH0
CANL0	89	90	CANL0
VCC_CM	91	92	→ VCC_CM
+3V3	93	94	→ +3V3
+5V	95	96	→ +5V
SGND	97	98	→ SGND
	99	100	→ +12V

EDPCON2 Connector

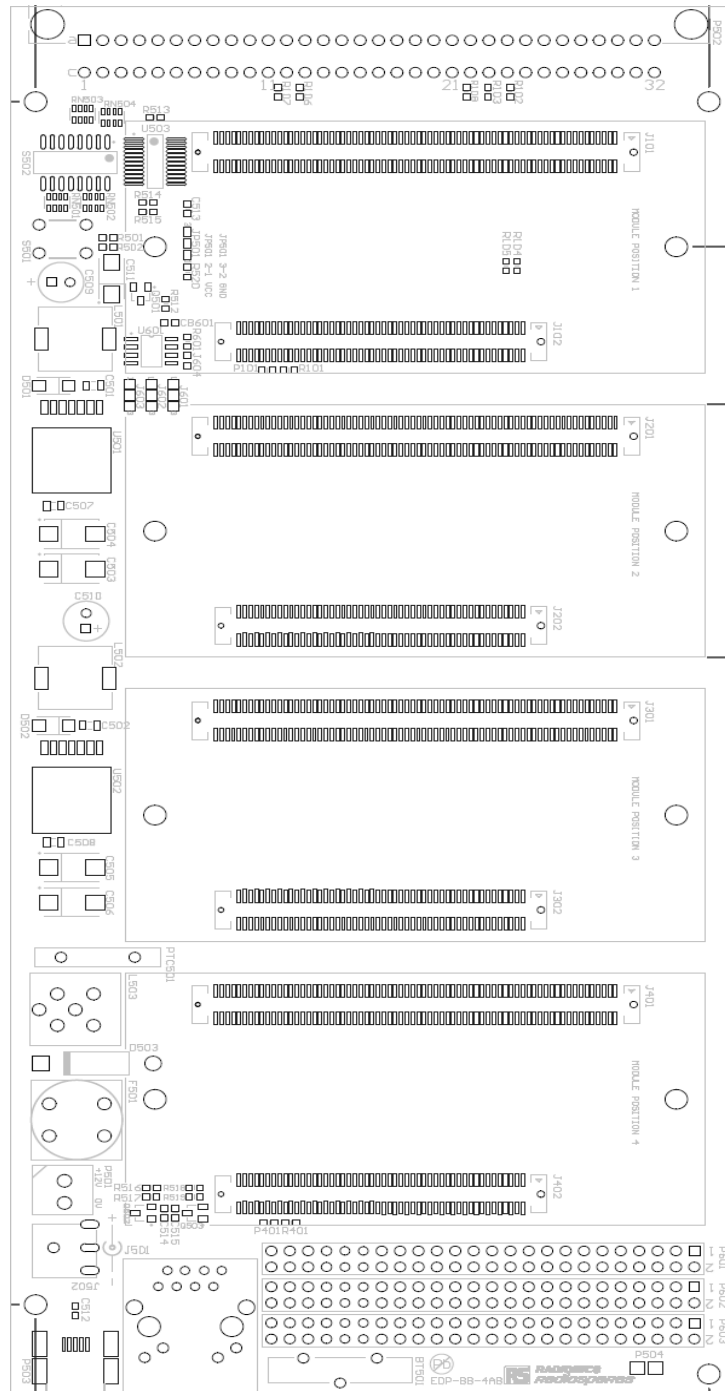
2.2 EDP Baseboard User Options Placement

There are a number of user-selectable functions on the baseboard, as shown below:



2.3 EDP Baseboard Component Placement

The location of the major items on the EDP baseboard is shown below.



2.4 EDP IO Pin Headers

All the signals in the EDP backplane are available here on 0.1" pin headers for sampling by 'scopes etc.



P601				P602				P603			
AN10	1	2	AN8	AN6	1	2	AN4	AN2	1	2	AN0
AN11	3	4	AN9	AN7	3	4	AN3	AN14	3	4	AN12
VAGND	5	6	AN REF	AN15	5	6	AN13	AN3	5	6	AN1
CPUDAC00_GPIO19	7	8	EVM0_GPIO21	IRQ_GPIO22_I2C INT	7	8	GPIO24_AD7	CPUDAC00_GPIO17	7	8	GPIO15_I2STX_SDA
EVM1_GPIO23	9	10	GPIO25_AD15	GPIO26_AD6	9	10	GPIO28_AD5	IRQ_GPIO20_I2C GEN1 INT	9	10	GPIO18_I2C GEN0 INT
GPIO27_AD14	11	12	GPIO29_AD13	GPIO30_AD4	11	12	GPIO32_AD3	IRQ_GPIO16_CNTRL I2C INT	11	12	GPIO14_MCIPWR
GPIO31_AD12	13	14	GPIO33_AD11	GPIO34_AD2	13	14	GPIO36_AD1	GPIO0	13	14	GPIO2_MCIDAT0
GPIO35_AD10	15	16	GPIO37_AD9	GPIO38_AD0	15	16	EVG0_GPIO40	GPIO1	15	16	GPIO3
GPIO39_AD8	17	18	EVM2_GPIO41_CAPADC	EVG1_GPIO42	17	18	EVG2_GPIO44	GPIO4_MCIDAT1	17	18	GPIO6_MCIDAT2
EVM3_GPIO43	19	20	EVM4_GPIO45	EVG3_GPIO46	19	20	EVG4_GPIO48	GPIO5_I2STX_WS	19	20	GPIO7_I2SRX_CLK
EVM5_GPIO47	21	22	EVM6_GPIO49	EVG5_GPIO50	21	22	EVG6_GPIO52	GPIO9_I2SRX_WS	21	22	GPIO8_MCIDAT3
EVM7_GPIO51	23	24	EVM8_GPIO53	EVG7_GPIO54	23	24	EVG8_GPIO56	GPIO10_MCICLK	23	24	GPIO11_I2SRX_SDA
EVM9_GPIO55	25	26	EVG9_GPIO57	EVG10_GPIO58	25	26	EVG12_GPIO60	GPIO13_I2STX_CLK	25	26	#RESIN
EVG11_GPIO59	27	28	EVG13_GPIO61	EVG14_GPIO62	27	28	EVG16_GPIO64	#RESOUT	27	28	I2C GEN0 SDA
EVG15_GPIO63	29	30	EVG17_GPIO65	EVG18_GPIO66	29	30	ASCO_RX_TTL	I2C GEN0_SCL	29	30	CNTRL SPI_CLK
EVG19_GPIO67	31	32	EVM10_GPIO68_ASC0CTS	ASCO_TX_TTL	31	32	ASCO_RX_TTL	CNTRL SPI_MST	31	32	CNTRL SPI_MTSR
EVG20_GPIO69_ASC0RTS	33	34	SPI_SSC_MST_MISO	ASCO_TX_TTL	33	34	ASCO_TX_TTL_ASC0DTR	CNTRL SPI_MCS_NSS	33	34	CNTRL I2C_SDA
SPI_SSC_MTSR_MOSI	35	36	SPI_SSC_CLK	ASCO_RX_TTL_ASC0DSR	35	36	SPI_SSC_MCS_NSS	CNTRL I2C_SCL	35	36	USB HOST D+
MOTOR_P1L	37	38	MOTOR_P0H	ETH_TX-	37	38	ETH_TX-	USB HOST D-	37	38	USB DEV D+
MOTOR_P1L	39	40	MOTOR_P1H	ETH_RX-	39	40	ETH_RX-	USB DEV D-	39	40	CAN0
MOTOR_PWM	41	42	EMG_TRP	ETH_LNK_LED	41	42	ETH_RX_LED	CAN0	41	42	>+3VBAT
MOTOR_H0_ENC0	43	44	MOTOR_H1_ENC1	ETH_SPD_LED	43	44	I2C GEN1_SDA	VCC_CM<	43	44	>+3V3
MOTOR_H2_ENC2	45	46	MOTOR_TCO_FB	I2C GEN1_SCL	45	46	CAN1_RX	+5V<	45	46	SGND
	47	48		CAN1_TX	47	48		+12V<	47	48	12V GND

2.4.1 Relating The Pin Headers To The CPU Pins

The pins of the CPU on the CM correspond to the pin headers according to the following tables, starting with P601.

XC167 Pin Allocation	STR9 Pin Allocation	EDPCON1 Signal Name	Connector	Pin No.
35 AN10	NC	AN10	P601	1
37 AN8	NC	AN8	P601	2
36 AN11	NC	AN11	P601	3
38 AN9	NC	AN9	P601	4
42 GUARD/AN GND	AVSS Analog GND	VAGND	P601	5
GUARD/AN GND	AVSS Analog GND	VAGND	P601	5
41 VAREF	AVREF - Analog	AN_REF	P601	6
26 P9.5/CC21IO	P6.2	CPU DAC01_GPIO19	P601	7
127 P1H.0/CC23IO	P0.4 (PHY disabled)	EVM0_GPIO21	P601	8
124 P1L.7/CC22IO	P0.5 (PHY disabled)	EVM1_GPIO23	P601	9
P0H.0	P9.0	GPIO25_AD15	P601	10
P0H.1	P9.1	GPIO27_AD14	P601	11
P0H.2	P9.2	GPIO29_AD13	P601	12
P0H.3	P9.3	GPIO31_AD12	P601	13
P0H.4	P9.4	GPIO33_AD11	P601	14
P0H.5	P9.5	GPIO35_AD10	P601	15
P0H.6	P9.6	GPIO37_AD9	P601	16
P0H.7	P9.7	GPIO39_AD8	P601	17
P7.7/CC31IO (CS8900A INT)	P7.0	EVM2_GPIO41_CAPADC	P601	18
17 P7.6/CC30IO	P7.1 (PHY disabled)	EVM3_GPIO43	P601	19
16 P7.5/CC29IO	P7.2	EVM4_GPIO45	P601	20
15 P7.4/CC28IO	P7.3	EVM5_GPIO47	P601	21
134 P1H.7/CC27IO	P7.6	EVM6_GPIO49	P601	22
133 P1H.6/CC26IO	P7.7	EVM7_GPIO51	P601	23
132 P1H.5/CC25IO	P6.6	EVM8_GPIO53	P601	24
131 P1H.4/CC24IO	P6.7	EVM9_GPIO55	P601	25
24 P9.3/CC19IO	P4.0	EVG9_GPIO57	P601	26
23 P9.2/CC18IO	P4.2	EVG11_GPIO59	P601	27
22 P9.1/CC17IO	P4.4	EVG13_GPIO61	P601	28
21 P9.0/CC16IO	P4.6	EVG15_GPIO63	P601	29
56 P2.15/CC15IO	P6.5	EVG17_GPIO65	P601	30
55 P2.14/CC14IO	P0.1	EVG19_GPIO67	P601	31
124 P1L.7/CC22IO	P0.6 (PHY disabled)	EVM10_GPIO68_ASC0 CTS	P601	32
121 P1L.4/CC62	P0.7 (PHY disabled)	EVG20_GPIO69_ASC0 RTS	P601	33
128 MRST1	P3.5	SPI_SSC MRST_MISO	P601	34
129 MTSR1	P3.6	SPI_SSC MTSR_MOSI	P601	35
130 SCLK1	P3.4	SPI_SSC CLK	P601	36
117 P1L.0/CC60	P6.1	MOTOR P0L	P601	37
118 P1L.1/COU60	P6.0	MOTOR P0H	P601	38
119 P1L.2/CC61	P6.3	MOTOR P1L	P601	39
120 P1L.3/COU61	P6.2	MOTOR P1H	P601	40
121 P1L.4/CC62	P6.5	MOTOR P2L	P601	41
122 P1L.5/COU62	P6.4	MOTOR P2H	P601	42
123 P1L.6/COU63	NC	MOTOR PWM	P601	43
124 P1L.7/CTRAP	P6.7	EMG TRP	P601	44
127 P1H.0/#C6POS0	P7.0	MOTOR H0_ENC0	P601	45
128 P1H.1/#C6POS1	P7.1	MOTOR H1_ENC1	P601	46
129 P1H.2/#C6POS2	P7.2	MOTOR H2_ENC2	P601	47
61 P3.2/CAPIN	P6.6	MOTOR TCO FB	P601	48

XC167 Pin Allocation	STR9 Pin Allocation	EDPCON1 Signal Name	Connector	Pin No.
39 AN6	P4.6	AN6	P602	1
33 AN4	P4.4	AN4	P602	2
40 AN7	P4.7	AN7	P602	3
34 AN5	P4.5	AN5	P602	4
46 AN15	NC	AN15	P602	5
44 AN13	NC	AN13	P602	6
P3.7	P7.4	IRQ_GPIO22_I2C INT	P602	7
P0L.7	P8.7	GPIO24_AD7	P602	8
P0L.0	P8.0	GPIO26_AD6	P602	9
P0L.5	P8.5	GPIO36_AD1	P602	10
P0L.2	P8.2	GPIO30_AD4	P602	11
P0L.3	P8.3	GPIO32_AD3	P602	12
P0L.4	P8.4	GPIO34_AD2	P602	13
P0L.1	P8.1	GPIO28_AD5	P602	14
P0L.6	P8.6	GPIO38_AD0	P602	15
49 P2.8/CC8IO	P4.0	EVG0_GPIO40	P602	16
50 P2.9/CC9IO	P4.1	EVG1_GPIO42	P602	17
51 P2.10/CC10IO	P4.0	EVG2_GPIO44	P602	18
52 P2.11/CC11IO	P4.2	EVG3_GPIO46	P602	19
53 P2.12/CC12IO	P4.3	EVG4_GPIO48	P602	20
54 P2.13/CC13IO	P4.4	EVG5_GPIO50	P602	21
55 P2.14/CC14IO	P4.5	EVG6_GPIO52	P602	22
56 P2.15/CC15IO	P4.6	EVG7_GPIO54	P602	23
8 P6.1/CC1IO	P4.7	EVG8_GPIO56	P602	24
9 P6.2/CC2IO	P6.0	EVG10_GPIO58	P602	25
10 P6.3/CC3IO	P6.1	EVG12_GPIO60	P602	26
11 P6.3/CC4IO	P6.2	EVG14_GPIO62	P602	27
12 P6.5/CC5IO	P6.3	EVG16_GPIO64	P602	28
13 P6.6/CC6IO	P6.4	EVG18_GPIO66	P602	29
70 P3.11/RxD0	P5.1	ASC0 RX TTL	P602	30
69 P3.10/TxD0	P5.0	ASC0 TX TTL	P602	31
59 P3.0/TxD1	P1.0 (PHY Disabled)	ASC1 RX TTL	P602	32
60 P3.1/RxD1	P1.1 (PHY Disabled)	ASC1 TX TTL	P602	33
NC	P3.0	ASC1 TX TTL_ASC0 DTR	P602	34
P20.2	P3.1	ASC1 RX TTL_ASC0 DSR	P602	35
83 P4.3	P3.7	SPI_SSC #CS_NSS	P602	36
Ethernet TX+ (CS8900)		ETH TX+	P602	37
Ethernet TX-		ETH TX-	P602	38
Ethernet RX+		ETH RX+	P602	39
Ethernet RX-		ETH RX-	P602	40
Ethernet LINK LED		ETH LNK LED	P602	41
Ethernet RX LED		ETH RX LED	P602	42
NC		ETH SPD LED	P602	43
NC	P2.1	I2C GEN1 SDA	P602	44
NC	P2.0	I2C GEN1 SCL	P602	45
85 P4.5/CAN0 RX	NC	CAN1 RX	P602	46
86 P4.6/CAN0 TX	NC	CAN1 TX	P602	47

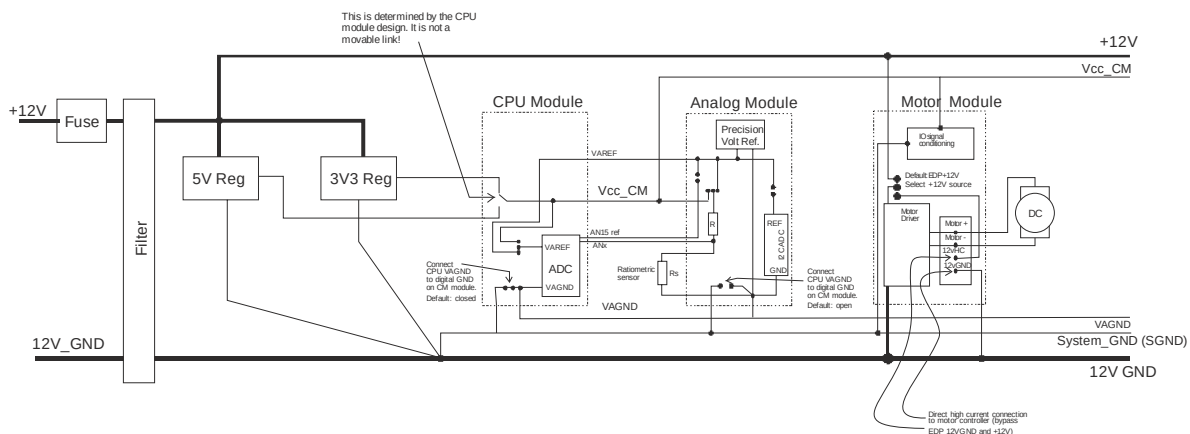
XC167 Pin Allocation	STR9 Pin Allocation	EDPCON1 Signal Name	Connector	Pin No.
31 AN2	P4.2	AN2	P603	1
29 AN0	P4.0	AN0	P603	2
45 AN14	NC	AN14	P603	3
43 AN12	NC	AN12	P603	4
32 AN3	P4.3	AN3	P603	5
30 AN1	P4.1	AN1	P603	6
25 P9.4/CC20IO	P6.0	CPU DAC00_GPIO17	P603	7
14 P6.7/CC7IO	NC	GPIO15_I2STX_SDA	P603	8
P3.2	P5.6	IRQ_GPIO16_CNTRL I2C INT	P603	9
P3.5	P5.7	IRQ_GPIO18_I2C GEN0 INT	P603	10
P3.6	P7.5	IRQ_GPIO20_I2C GEN1 INT	P603	11
83 P4.3	P0.7 (PHY disabled)	GPIO14_MCIPWR	P603	12
92 P20.2	P8.0	GPIO0	P603	13
128 MRST1	P3.5	GPIO2_MCIDAT0	P603	14
80 P4.0	P8.1	GPIO1	P603	15
81 P4.1	P8.2	GPIO3	P603	16
62 P3.3	P8.4	GPIO4_MCIDAT1	P603	17
63 P3.4	P8.3	GPIO6_MCIDAT2	P603	18
64 P3.5	TAMPER_IN	GPIO5_I2STX_WS	P603	19
65 P3.6	NC	GPIO7_I2SRX_CLK	P603	20
66 P3.7	NC	GPIO9_I2SRX_WS	P603	21
129 P1H.2/MTSR1	P3.7	GPIO8_MCIDAT3	P603	22
13 P6.6/CC6IO	NC	GPIO13_I2STX_CLK	P603	23
12 P6.5/CC5IO	NC	GPIO11_I2SRX_SDA	P603	24
130 P1H.3/SCLK1	P3.4	GPIO10_MCICLK	P603	25
3V3 Vbatt	3V3 Vbatt	+3VBAT	P603	42
Vcc to BB	Vcc 3V3 or 5V, supplied by CM	VCC_CM	P603	43
Vcc to BB	Vcc 3V3 or 5V, supplied by CM	VCC_CM	P603	43
Vcc 3V3 from reg	3V3 from baseboard regulator	+3V3	P603	44
Vcc 3V3 from reg	3V3 from baseboard regulator	+3V3	P603	44
Vcc 5V from reg	5V from baseboard regulator	+5V	P603	45
Vcc 5V from reg	5V from baseboard regulator	+5V	P603	45
Digital GND	Digital GND	SGND	P603	46
Digital GND	Digital GND	SGND	P603	46
+12V 2A	+12V 2A	+12V	P603	47
+12V 2A	+12V 2A	+12V	P603	47
+12V 2A	+12V 2A	+12V	P603	47
+12V 2A	+12V 2A	+12V	P603	47
12V Power GND	12V Power GND	12VGND	P603	48
12V Power GND	12V Power GND	12VGND	P603	48
12V Power GND	12V Power GND	12VGND	P603	48
12V Power GND	12V Power GND	12VGND	P603	48
77 P3.15	P3.6	Not Used		

XC167 Pin Allocation	STR9 Pin Allocation	EDPCON1 Signal Name	Connector	Pin No.
142 #RSTIN	RESET_INn	#RESIN	P603	26
3 #RSTOUT	RESET_OUTn	#RESOUT	P603	27
23 SDA1	P2.3	I2C GEN0 SDA	P603	28
24 SCL1	P2.2	I2C GEN0 SCL	P603	29
76 SCLK0	P2.4	CNTRL SPI CLK	P603	30
67 MRST0	P2.6	CNTRL SPI MRST	P603	31
68 MTSR0	P2.5	CNTRL SPI MTSR	P603	32
82 P4.2	P2.7	CNTRL SPI #CS_NSS	P603	33
25 SDA2	P2.1	CNTRL I2C SDA	P603	34
26 SCL2	P2.0	CNTRL I2C SCL	P603	35
NC	USBDN	USB HOST D+	P603	36
NC	USBDP	USB HOST D-	P603	37
USB DEBUG D+	USB debug D+	USB DEV D+	P603	38
USB DEBUG D-	USB debug D-	USB DEV D-	P603	39
CANH0	CANH0	CANH0	P603	40
CANL0	CANL0	CANL0	P603	41

2.5 Grounding Arrangements

The system ground (SGND) and 12V GND are connected together at a star point on the baseboard. The 12V GND is used for high current devices like the motor controller and the ULN2003 output drivers on the digital IO AM. System ground is used for all returns on logic devices on all modules. It can be used for analog returns but there is a risk of noise (ground bounce).

Analog ground (VAGND) by default is an offshoot of the system ground which occurs only on the CM. It is routed to the VAGND pins of the CPU and also acts as a return for filter circuits used for analog inputs. It is optionally possible to connect the SGND to the Analog ground on the analog module, although this should not be necessary unless there are a large number of resistive sensors being used. In this case, the link connecting VAGND and SGND on the CM must be opened to avoid ground loops.



2.6 Positive Supplies

The +12V line comes via the screw terminals on the baseboard or the mini-jack. It is fused and filtered before entering the EDP backplane. The 3V3 and 5V voltage regulators are driven from the +12V.

2.6.1 Logic Supplies

Both 3V3 and 5V are available on the EDP CON to support both 5V and 3V3 processors and devices. To allow the interfacing of IO devices at the required voltage, the positive supply to the CPU IO domain is routed into the EDP CON through Vcc_CM. It is intended to be used for pull-ups on IO pins and powering small active components that connect directly to the CPU such as discrete logic, op-amps etc.. Vcc_CM is limited to 500mA total current draw from other modules and the baseboard.

Vcc_CM is connected inside the CM to the voltage used by the CPU's IO domain.

2.6.2 Analog Supply

The Analog supply to the CPU ADC may be derived from the local Vcc or from a precision reference located on the Analog AM. Ideally the Analog AM and CM should be in adjacent positions on the baseboard to keep the signal length to a minimum if the latter is chosen.

The I2C ADC on the analog module can use the Vcc_CM or the local precision voltage references, either 3V3 or 5V. The 5V reference is driven from the 12V to guarantee no drop-out problems.

As the anti-aliasing filters are run at 5V, the local ADC is not tied to the same voltage range as the CPU's ADC. It is the user's responsibility to make sure that the input does not exceed the permissible input voltage range of the CPU ADC. Protection resistors are provided to prevent damage.

2.7 Limits And Restrictions

Vcc_CM max current	500mA
3V3 max current	2000mA
5V max current	2000mA
Sum of 3V3 current + 5V current + Vcc_CM = 2000mA	
SGND max current	2000mA
12VGND max current	2000mA

Warning: do not attempt to fit two CPU modules to the baseboard at the same time. If they have different peripheral supply voltages then damage is likely to occur.

2.8 EDP Control Busses

2.8.1 I2C Busses

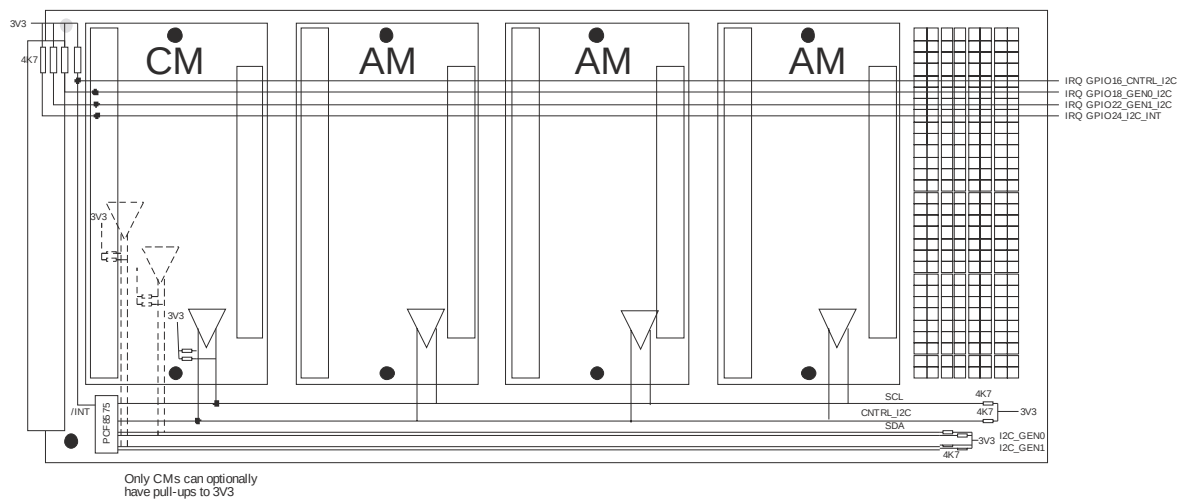
The EDP uses I2C as the data and control backbone. Depending on the capabilities of the CM fitted, up to three independent I2C busses are available. I2C channel "CNTRL_I2C" is the primary I2C device bus and is used by default to communicate with I2C devices on the baseboard and application modules.

The I2C address space is based on the 7-bit addressing scheme. I2C devices that are able to generate an interrupt request by default use the IRQ_GPIO16_CNTRL_I2C_INT line, with the option of using up to another three interrupt-capable lines. A pull-up resistor is provided on IRQ_GPIO16_CNTRL_I2C_INT so that the open collector /INT outputs on I2C devices can signal an interrupt by pulling this line down.

The I2C bus runs at 3V3 so any 5V devices must be connected via a level shifting mechanism.

The I2C bus devices require pull-up resistors on the SDA and SCL lines and these are incorporated on the baseboard.

There are three possible I2C channels available although in most cases the default one (I2C_CTRL) will be sufficient. EDP modules that carry I2C device do, where possible, allow the user to configure the I2C addresses. This allows for example, up to three digital IO modules to be fitted, with the GPIO devices on each module given a unique address. Where the address space of a particular I2C channel becomes full, devices can be connected to an alternative channel to get access to a completely new address space.



2.8.1.1 Default I2C Addresses

At the time of writing, the default addresses for the I2C devices on the existing modules are:

Module	I2C Device	Possible Range	Actual 7-bit Address Module 1	I2C channel	Actual 7-bit Address Module 2	I2C channel
Analog Module	MAX1138 address	0x35	0x35	CNTRL	0x35	Gen0
	MAX1038 address	0x65	0x65	CNTRL	0x65	Gen0
	AD5263 BRU50 address	0x2C-0x2F	0x2C	CNTRL	0x2C	Gen0
	PCA8575 address	0x20-0x27	0x21	CNTRL	0x21	Gen0
Baseboard	PCF8575	0x20-0x27	0x20	CNTRL	XXXXX	XXXXXX
Comms AM	RTC PCA8583	0x50-0x51	0x50	CNTRL	XXXXX	XXXXXX
Digital AM	PCF8575 IN address	0x20-0x27	0x22	CNTRL	0x24	CNTRL
	PCF8575 OUT address	0x20-0x27	0x23	CNTRL	0x25	CNTRL
	24C32	0x50-0x57	0x51	CNTRL	0x52	CNTRL

2.8.1.2 Available I2C Interrupt Request Lines

Each of the three potential I2C channels has a dedicated interrupt request line into the CM. A spare interrupt line is provided that can be allocated to any channel, as defined by the user. However it is up to user to make sure that the software is able to determine the I2C device that requested the interrupt.

I2C_CTRL	IRQ GPIO16_CNTRL_I2C	(integral pull-ups)
I2C_GEN0	IRQ GPIO18_GEN0_I2C	(integral pull-ups)
I2C_GEN1	IRQ GPIO22_GEN1_I2C	(integral pull-ups)
Uncommitted	IRQ GPIO24_I2C_INT	(integral pull-ups)

2.8.1.3 EDP Baseboard Jumper Settings

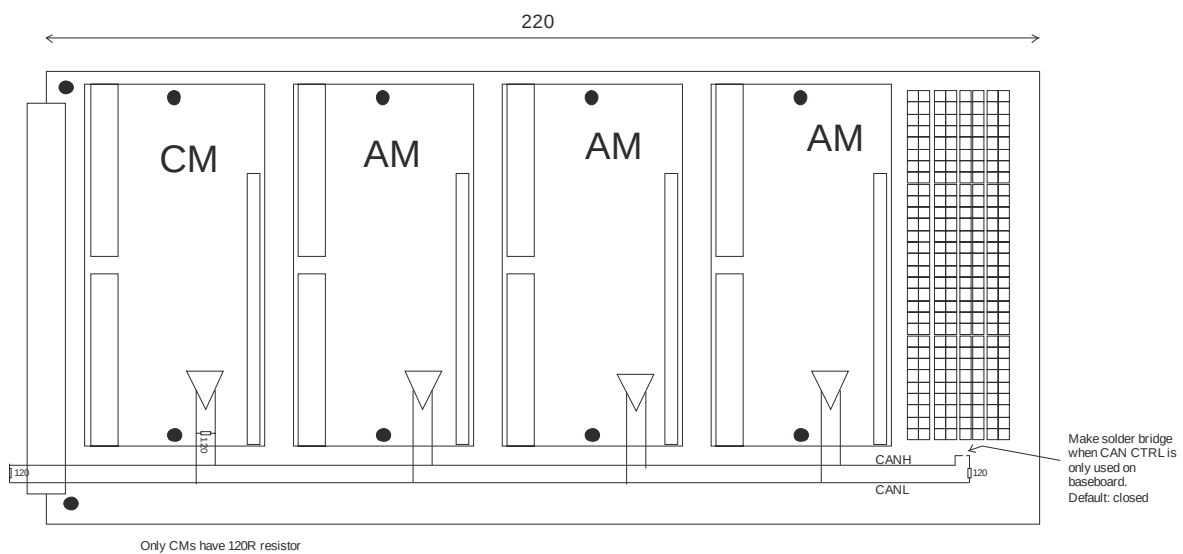
There are a number of user-definable jumpers on the baseboard. Their significance is given below.

Jumper	Type	Purpose	Default
P401	Solder	Apply 120R terminating resistor to on-board CAN	Closed
P101	Solder	Apply 120R terminating resistor to on-board CAN	Closed
JP501	Solder	Set address pin A0 for I2C GPIO	2-3
P504	Solder	Select source for motor direction control	Open
J601	Solder	Set address pin A0 for I2C EEPROM	1-2
J602	Solder	Set address pin A1 for I2C EEPROM	2-3
J603	Solder	Set address pin A2 for I2C EEPROM	2-3
J604	Solder	Enable write control /WC for EEPROM	Open

2.9 CAN

The on-board CAN network "CAN CNTRL" is intended to allow the interconnection of modules and other EDP systems via CAN. The first CAN module on any CPU is by default allocated to the CANH0 and CANL0 bus. This is the CAN physical layer (i.e. after the CAN transceivers) and can run at up to 1MB/s. The 120R termination resistors at the ends of the network are located on the CM and at the end of the baseboard that carries the Ethernet and USB connectors. If the CAN CNTRL bus is taken off-board via the DIN14162 expansion connector then the 120R resistor on the baseboard must be disconnected via the P201 link.

The CAN CNTRL bus is available through a 9D connector on the optional EDP-AM-CO1-A communications module.



3. Basic EDP Application Modules

3.1 Communications Module EDP-AM-C01

This module allows the easy interfacing to the following communication devices present on the CM:

Comms Type	Channel No.	Connector	Name	Comment
RS232	ASC0	9D Male	J305	
	ASC0	5x2 Header	P302	
RS232	ASC1	5x2 Header	P301	p3 = RX, p5 = TX
RS485	ASC1	5x2 Header	P301	p3 = RX, p5 = TX
USB		USB mini		
device	USB DEV	socket	P303	Where available on CM
CAN	CAN CNTRL	9D Female	P201	120R on baseboard
CAN	CAN CNTRL	5x2 Header	P204	Opto-isolated CAN
CAN	CAN1	5x2 Header	P204	Opto-isolated CAN

It also carries a PCF8583 real time clock device on the I2C bus and 240 bytes of non-volatile data storage, powered from the optional lithium battery on the EDP baseboard.

Note: Only one communications module may be fitted to a baseboard at any one time.

3.1.1 Controller Area Network Interfaces - CAN

The first CAN channel (CAN0) from the CM (where available) is routed through the 9-D female connector as CAN-High and CAN-Low signals, ready for interfacing to an existing CAN network. CAN0 may also be routed through a galvanically isolated CAN physical layer, emerging on P204 and selectable via P205. If this is required, CAN0 TX and RX connections to the CPU on the CM must be isolated via jumpers on the CM itself (please refer to the user manual for the CM fitted). The isolated physical layer has its own 5V DC-DC convertor so that the EDP system can float relative to other CAN devices.

If the CM has a second CAN channel (CAN1), this can also be routed through the galvanically isolated CAN physical layer via P205.

An optional 120R CAN terminating resistor can be added via solder bridge J203.

3.1.2 Serial Interfaces

3.1.2.1 RS232 Interfaces

Asynchronous serial channel 0 from the CPU appears as RS232-level signals on the J305 9-D connector. To allow the RS232 connector be mounted away from the EDP hardware, the same signals are available on P302. A simple PC-style IDC 9D connector on a ribbon cable can be used.

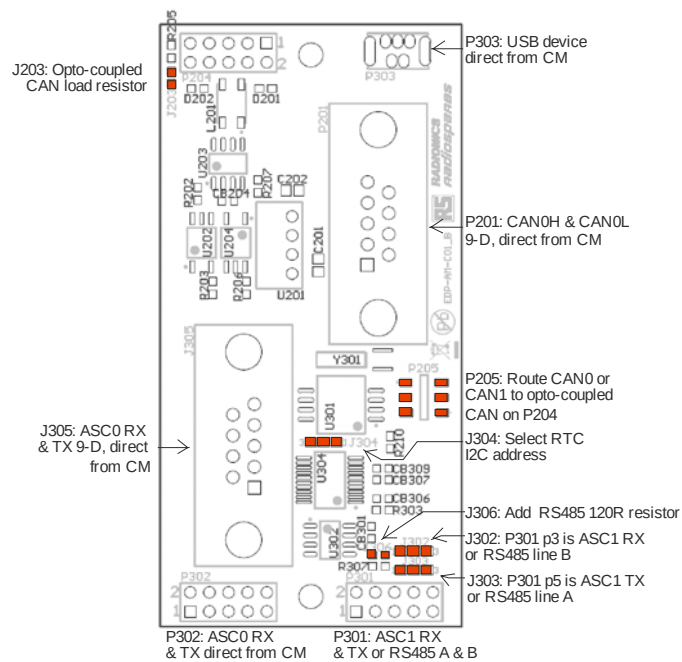
For CMs that have a second asynchronous port, it can be routed to P301 where a PC-style IDC 9-D with ribbon cable can be used. Alternatively it can be connected to an RS485 transceiver via jumpers J302 and J303.

3.1.2.2 RS485

RS485 communications are supported using a Linear Technology LTC485. To make use of this option, the CM software must operate the Receive Enable/Data Enable control line. In RS485 installations where no load resistor is present, J306 allows a default one to be made available.

3.2 User Jumpers And Connectors

User-configurable jumpers



3.2.1 Mapping Of CPU Pins To The Communications Module

The connectors on the communications module are connected to the CPU module as shown below.

Please note that the USB device connector is inactive when the XC167 module is fitted and that the second serial port is not available when the Ethernet PHY is enabled on the STR9 module. Finally, there is no second CAN channel available with the STR9.

XC167 Pin Allocation	STR9 Pin Allocation	EDP-AM-CO1 Allocation
Vcc to BB	Vcc 3V3 or 5V, supplied by CM	Vcc 3V3 or 5V, supplied by CM
P3.2 Digital GND	P5.6 Digital GND	IRQ_GPIO16_CNTRL I2C INT Digital GND
86 CAN0 TX	NC	CAN1 TX
85 CAN0 RX	NC	CAN1 RX
60 RxD1	P1.1 (PHY Disabled)	ASC1 TX TTL
P20.2	P3.1	ASC1 RX TTL_ASC0 DSR
59 TxD1	P1.0 (PHY Disabled)	ASC1 RX TTL
69 TxD0	P5.0	ASC0 TX TTL
70 RxD0	P5.1	ASC0 RX TTL
Vcc 5V from reg	5V from baseboard regulator	5V from baseboard regulator
Vcc 3V3 from reg	3V3 from baseboard regulator	3V3 from baseboard regulator

XC167 Pin Allocation	STR9 Pin Allocation	EDP-AM-CO1 Allocation
Vcc to BB	Vcc 3V3 or 5V, supplied by CM	Vcc 3V3 or 5V, supplied by CM
Digital GND	Digital GND	Digital GND
Vcc 5V from reg	5V from baseboard regulator	5V from baseboard regulator
3V3 Vbatt	3V3 Vbatt	3V3 Vbatt
Vcc 3V3 from reg	3V3 from baseboard regulator	3V3 from baseboard regulator

XC167 Pin Allocation	STR9 Pin Allocation	EDP-AM-CO1 Allocation
Vcc 5V from reg	Vcc 5V from reg	Vcc 5V from reg
Vcc 3V3 or 5V, supplied by CPU	Vcc 3V3 or 5V, supplied by CPU	Vcc 3V3 or 5V, supplied by CPU
Vcc 3V3 from reg	Vcc 3V3 from reg	Vcc 3V3 from reg
NC	USBDN	USB DEV D+
NC	USBDP	USB DEV D-
Digital GND	Digital GND	Digital GND
25 SDA2	P2.1	CNTRL I2C SDA
26 SCL2	P2.0	CNTRL I2C SCL
CANL0	CANL0	CANL0
CANH0	CANH0	CANH0
87 CAN1 TX	P3.2	CAN0 TX
84 CAN1 RX	P3.3	CAN0 RX

3.3 Analog Input Module

The EDP-AM-AN16-A analog module allows up to 32 analog channels to be interfaced to the CM. It has a mix of filtered and unfiltered inputs and two precision voltage sources for accurate absolute measurements.

The on-board MAX1138 ADC is accessible via I2C CNTRL bus and gives up to an extra 12 channels of 10-bit analog to digital conversion. Each of the first 12 channels can be routed via jumpers to either the CM's own ADC or to the on-board ADC. In addition, any unused channels on the on-board ADC is available on a connector, meaning up to 28 channels are possible.

Two analog modules may be fitted simultaneously so that up to 40 channels are possible. If a second module is fitted, the channels belonging to the CM remain the same, although the user can specify which channel will be routed through which analog module. The second analog module must use the second I2C channel, I2C_GEN0 as the MAX1138 ADC has a fixed I2C address. An alternative version of this device (MAX1138KEE+) has a different I2C address and can be fitted to the second module.

The on-board ADC is by default the MAX1138 5V, 10-bit ADC but the alternative MAX1139 3V3 device can be fitted. The CM analog channels have a voltage range determined by the CPU fitted. The analog module inputs are able to cope with a 0-5V range, regardless of the CM type fitted. It is therefore up to the user to ensure that the voltage applied to the inputs does not exceed that required by the CM. A series protection resistor may optionally be fitted to reduce the chance of damaging a 3V3 ADC if 5V is applied.

The 5V and 3V3 precision references can be applied to the CM's ADC and the on-board ADC, although the latter will sacrifice one channel if this is used. They can also be fed back to the CM via the VAREF EDP signal.

Ratiometric conversions are possible using a special output pin on connector P201 pin1 for driving resistive sensors.

Quantity	Type
2	2 pole filters with digitally controlled cut-off
6	2-pole active filters with fixed cut-off
8	1-pole passive filters with fixed cut-off
12	Unfiltered channels
1	5V reference
1	3V3 reference

3.3.1 Anti-Aliasing Filters

Channels AN0 to AN7 are equipped with 2-pole, Sallen-Key anti-aliasing filters, configured in a Butterworth mode. The active filters are unity gain so they can be used for DC voltage measurements as well as for sampling rapidly changing signals. Channels AN0 and AN1 optionally have I2C-controlled 256 step digital potentiometers which allow the filter characteristics to be altered under software control. They can also be cascaded to yield a single 4-pole filter on channel AN0. The remaining active filters have a cut-off frequency of 12kHz.

By fitting the appropriate resistors to the potential dividers on the filter inputs (R301, R304 etc.), the input voltage range can be extended to suit the user's application on a channel-by-channel basis.

AN8-AN15 have simple low-pass filter inputs. All inputs are protected against over-voltage conditions.

3.3.2 Additional Items

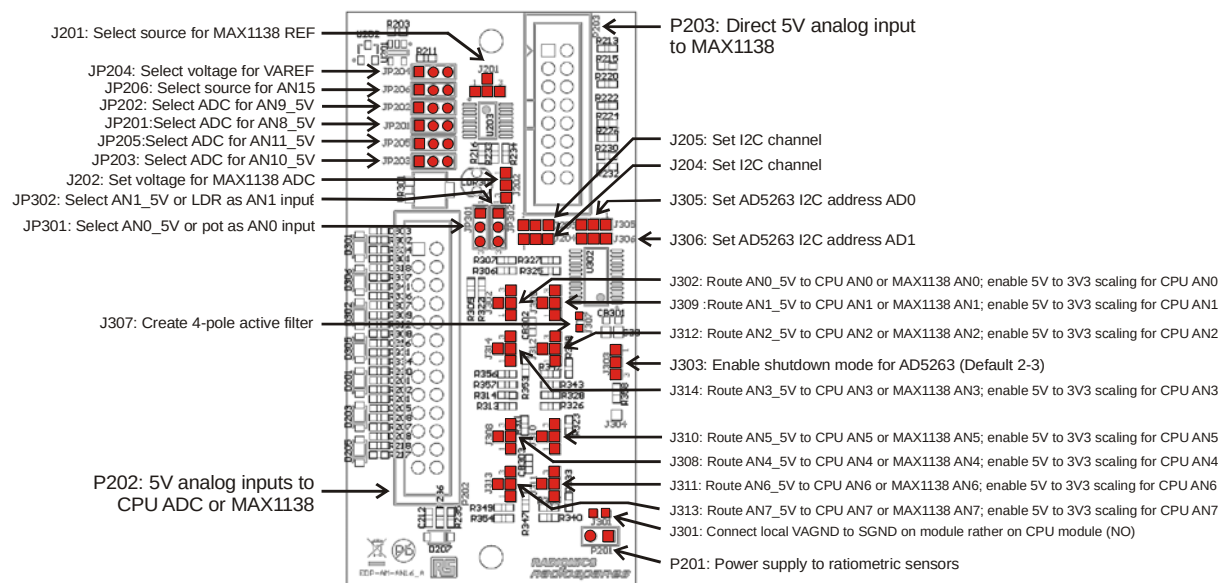
A trimmer potentiometer and light-dependent resistor and are fitted to channels AN0 and AN1 respectively for educational purposes.

3.3.3 Setting Jumper Options

Some options are made using black 2mm links. These are available from RS under part number 180-9353. The possible user settings are listed below, along with their default configurations.

Jumper	Type	Purpose	Default
J202	Solder	Set voltage for MAX1138 ADC	1-2
J204	Solder	Set I2C channel	1-2
J205	Solder	Set I2C channel	1-2
J301	Solder	Connect local VAGND to SGND on module rather on CPU module (NO)	1-2
J302	Solder	Route AN0_5V to CPU AN0 or MAX1138 AN0; enable 5V to 3V3 scaling for CPU AN0	1-2
J303	Solder	Enable shutdown mode for AD5263 (Default 2-3)	2-3
J305	Solder	Set AD5263 I2C address AD0	2-3
J306	Solder	Set AD5263 I2C address AD1	2-3
J307	Solder	Create 4-pole active filter from U301A and U301B	Open
J308	Solder	Route AN4_5V to CPU AN4 or MAX1138 AN4; enable 5V to 3V3 scaling for CPU AN4	1-2
J309	Solder	Route AN1_5V to CPU AN1 or MAX1138 AN1; enable 5V to 3V3 scaling for CPU AN1	1-2
J310	Solder	Route AN5_5V to CPU AN5 or MAX1138 AN5; enable 5V to 3V3 scaling for CPU AN5	1-2
J311	Solder	Route AN6_5V to CPU AN6 or MAX1138 AN6; enable 5V to 3V3 scaling for CPU AN6	1-2
J312	Solder	Route AN2_5V to CPU AN2 or MAX1138 AN2; enable 5V to 3V3 scaling for CPU AN2	1-2
J313	Solder	Route AN7_5V to CPU AN7 or MAX1138 AN7; enable 5V to 3V3 scaling for CPU AN7	1-2
J314	Solder	Route AN3_5V to CPU AN3 or MAX1138 AN3; enable 5V to 3V3 scaling for CPU AN3	1-2
J201	4W Link	Select source for MAX1138 REF	Open
JP201	Link	Select ADC for AN8_5V input	1-2
JP202	Link	Select ADC for AN9_5V input	1-2
JP203	Link	Select ADC for AN10_5V input	1-2
JP204	Link	Select voltage for VAREF	1-2
JP205	Link	Select ADC for AN11_5V input	1-2
JP206	Link	Select source for AN15 input	2-3
JP301	Link	Select AN0_5V or pot as AN0 input	1-2
JP302	Link	Select AN1_5V or LDR as AN1 input	1-2
P201	2-way	Power supply to ratiometric sensors	NC

The locations of the most important user-selectable items are shown below.



3.3.4 Software Drivers For Analog Module

The module has two I2C devices, both of which require special software drivers to access. These are currently in preparation and will be made available on the EDP website.

3.3.5 Mapping Of CPU Peripheral Pins To The Analog Module

The analog inputs on connector P202 on the analog IO module are connected to the CPU module as shown below. There is a 1-to-1 correspondence between the analog channel numbers on the P202 connector and the physical analog channels on the CPU.

XC167 Pin Allocation	STR9 Pin Allocation	EDP-AM-AN16 Allocation
Vcc to BB	Vcc 3V3 or 5V, supplied by CM	Vcc 3V3 or 5V, supplied by CM
42 GUARD/AN GND	AVSS Analog GND	VAGND
P3.5	P5.7	IRQ_GPIO18_I2C GEN0 INT
P3.2	P5.6	IRQ_GPIO16_CNTRL I2C INT
Digital GND	Digital GND	Digital GND
37 AN8	NC	AN8
39 AN6	P4.6	AN6
33 AN4	P4.4	AN4
31 AN2	P4.2	AN2
45 AN14	NC	AN14
43 AN12	NC	AN12
35 AN10	NC	AN10
29 AN0	P4.0	AN0
41 VAREF	AVREF - Analog	AN_REF
Vcc 5V from reg	5V from baseboard regulator	5V from baseboard regulator
Vcc 3V3 from reg	3V3 from baseboard regulator	3V3 from baseboard regulator

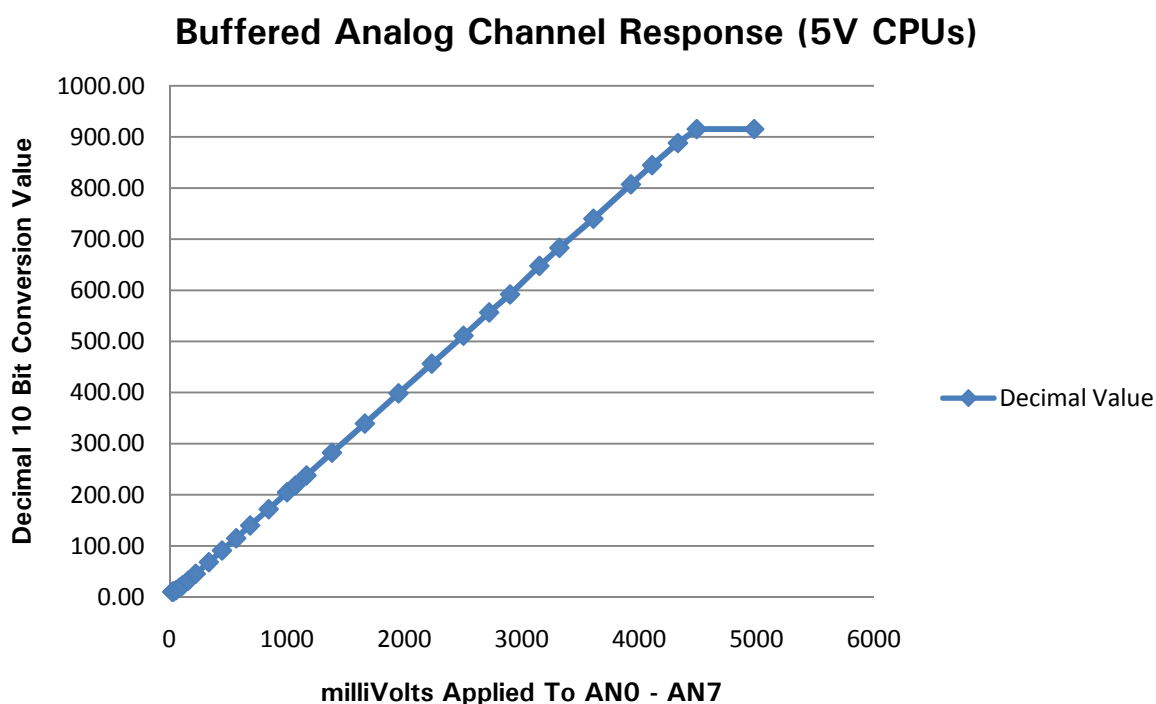
Pin	XC167 Pin Allocation	STR9 Pin Allocation	EDP-AM-AN16 Allocation
126	Vcc to BB	Vcc 3V3 or 5V, supplied by CM	Vcc 3V3 or 5V, supplied by CM
20	GUARD/AN GND	AVSS Analog GND	VAGND
132	Digital GND	Digital GND	Digital GND
12	38 AN9	NC	AN9
10	40 AN7	P4.7	AN7
8	34 AN5	P4.5	AN5
6	32 AN3	P4.3	AN3
18	46 AN15	NC	AN15
16	44 AN13	NC	AN13
14	36 AN11	NC	AN11
4	30 AN1	P4.1	AN1
130	Vcc 5V from reg	5V from baseboard regulator	5V from baseboard regulator
128	Vcc 3V3 from reg	3V3 from baseboard regulator	3V3 from baseboard regulator
2	NC		
22	80 P4.0	P8.1	
24	81 P4.1	P8.2	

XC167 Pin Allocation	STR9 Pin Allocation	EDP-AM-AN16 Allocation
Vcc 5V from reg	Vcc 5V from reg	Vcc 5V from reg
Vcc 3V3 or 5V, supplied by CPU	Vcc 3V3 or 5V, supplied by CPU	Vcc 3V3 or 5V, supplied by CPU
Vcc 3V3 from reg	Vcc 3V3 from reg	Vcc 3V3 from reg
23 SDA1	P2.3	I2C GEN0 SDA
24 SCL1	P2.2	I2C GEN0 SCL
Digital GND	Digital GND	Digital GND
25 SDA2	P2.1	CNTRL I2C SDA
26 SCL2	P2.0	CNTRL I2C SCL

3.3.6 Analog Module Input Characteristics

3.3.6.1 Channels AN0-AN7

These are over-voltage protected and buffered with unity gain, 2nd order filters. The characteristics of the OP amps fitted mean that the usable voltage input range is 24mV to 4.49V, with a linear and monotonic response. With a 5V, 10-bit ADC the decimal value range is from 9 to 804 bits. With a 3V3, 10-bit ADC, the upper value is 1023 bits.



3.3.6.2 Channels AN8- AN15

These are unbuffered but still have over-voltage protection. The usable range is determined entirely by the characteristics of the ADC used.

3.3.7 Analog Module Hints

For best performance when using the CPU's own ADC, i.e. least noise and greatest conversion accuracy, ensure that the analog module is placed in the EDP baseboard position immediately adjacent to the CPU module. Also, solder bridge J301 can be closed to ensure that the analog ground is connected to the system ground (SGND) on the analog module rather than on the CPU module. However to avoid ground loops though, the link on the CPU module that connects these two grounds must be opened (XC167 only).

3.4 Digital IO Module

The digital module provides a means to apply digital signals to the CM and drive world devices from it. There are 12 input channels with overvoltage protection and optional pull-ups, plus another 16 TTL inputs accessible only via I2C. 16 outputs are present each with a current drive capability of 500mA, plus another 16, 25mA logic outputs.

The first 12 inputs and 16 outputs are derived from the CM (where possible), although the protected input stages and high-current output stages can be connected to the I2C IO expander also.

The input I2C ports can generate an interrupt request. This is disabled by default as it could result in a high CPU interrupt loading.

An RGB colour LED may be fitted for experimental purposes

3.4.1 Digital Outputs

The 500mA outputs are simple low-side drives and are in the OFF state at power-up. They are designed to drive relays and solenoids and in fact can sink up to 1A but the user may need to attach a mini-heatsink to the driver IC if high duty ratios are expected.

It is up to the user to program the digital output pins of the CPU to a logic '1' to turn the outputs on. There is a net inversion through the drivers so that a logic '1' at the CPU output pin will result in a low (i.e. current sink enabled) at the output connector.

If any of the I2C GPIO device (PCA9555)'s pins are connected to the 500mA drivers then it is again up to the user to use a suitable I2C command to switch the output ON.

Depending on the CPU module being used, not all of the 12 inputs and 16 outputs can be controlled independently. This is due to a potential shortage of IO pins on the CPU itself. In such cases, the duplicated or unavailable channels should be routed to one of the two I2C GPIO devices to make up the shortfall.

3.4.2 Using Multiple Digital IO Modules

Up to 3 digital IO modules may be fitted to a single baseboard (4 if not CPU is fitted). Typically, the first module would make use of the CPU module's own port pins. Other modules would rely on the I2C GPIO devices for their connection to the CPU. The full address range of 8 is available to all these devices so the user can make sure that there are no conflicts. Alternatively, all digital IO modules could use I2C, freeing up CPU pins for other purposes.

Where a second EDP baseboard is available, the I2C_GEN_0 I2C bus can be used to connect further digital IO modules.

3.4.3 Software Drivers For Digital Module

The module has two I2C GPIO devices, both of which require special software drivers to access. These are currently in preparation and will be made available on the EDP website.

3.4.4 Digital IO Module Connectors

3.4.4.1 500mA Outputs

X202	Description	X202	Description
1	DO0 1A output	2	DO8 1A output
3	DO1 1A output	4	DO9 1A output
5	DO2 1A output	6	DO10 1A output
7	DO3 1A output	8	DO11 1A output
9	DO4 1A output	10	DO12 500mA output
11	DO5 1A output	12	DO13 500mA output
13	DO6 1A output	14	DO14 500mA output
15	DO7 1A output	16	DO15 500mA output
17	DO16 L logic output	18	DO17 L logic output
19	DO18 L logic output	20	DO15 500mA output
21	CPU Vcc	22	12V GND
23	CPU Vcc	24	+12V

Note: Although the outputs DO0 – DO11 are rated at 1 Amp you should take care that the maximum total ULN2003 power dissipation is not exceeded.

3.4.4.2 I2C GPIO Outputs (25mA)

X203	Description	X203	Description
1	GPIO OUT P00	2	GPIO OUT P10
3	GPIO OUT P01	4	GPIO OUT P11
5	GPIO OUT P02	6	GPIO OUT P12
7	GPIO OUT P03	8	GPIO OUT P13
9	GPIO OUT P04	10	GPIO OUT P14
11	GPIO OUT P05	12	GPIO OUT P15
13	GPIO OUT P06	14	GPIO OUT P16
15	GPIO OUT P07	16	GPIO OUT 17
17	CPU Vcc	18	+3V3
19	+5V	20	SGND

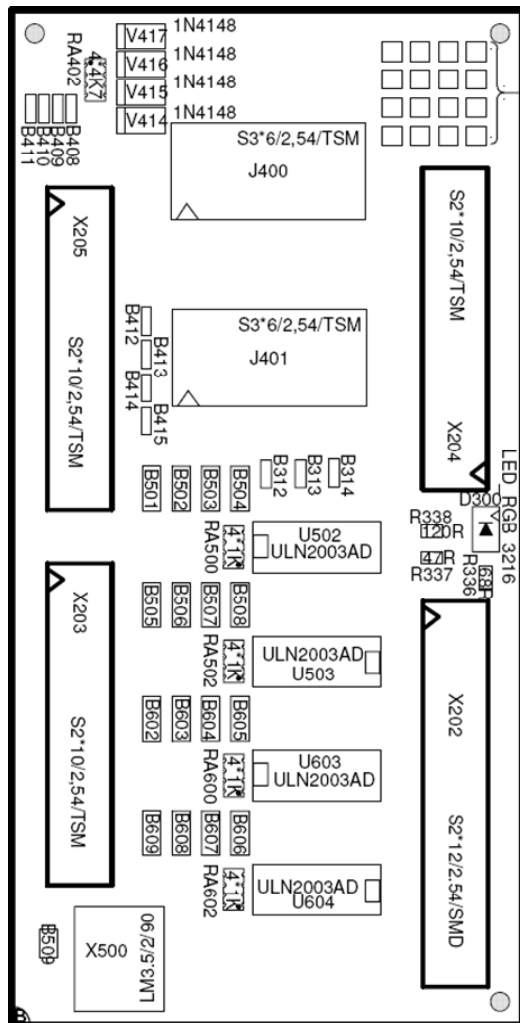
3.4.4.3 I2C GPIO Inputs (unprotected)

X204	Description	X204	Description
1	GPIO IN P00	2	GPIO IN P10
3	GPIO IN P01	4	GPIO IN P11
5	GPIO IN P02	6	GPIO IN P12
7	GPIO IN P03	8	GPIO IN P13
9	GPIO IN P04	10	GPIO IN P14
11	GPIO IN P05	12	GPIO IN P15
13	GPIO IN P06	14	GPIO IN P16
15	GPIO IN P07	16	GPIO IN P17
17	CPU Vcc	18	+3V3
19	+5V	20	SGND

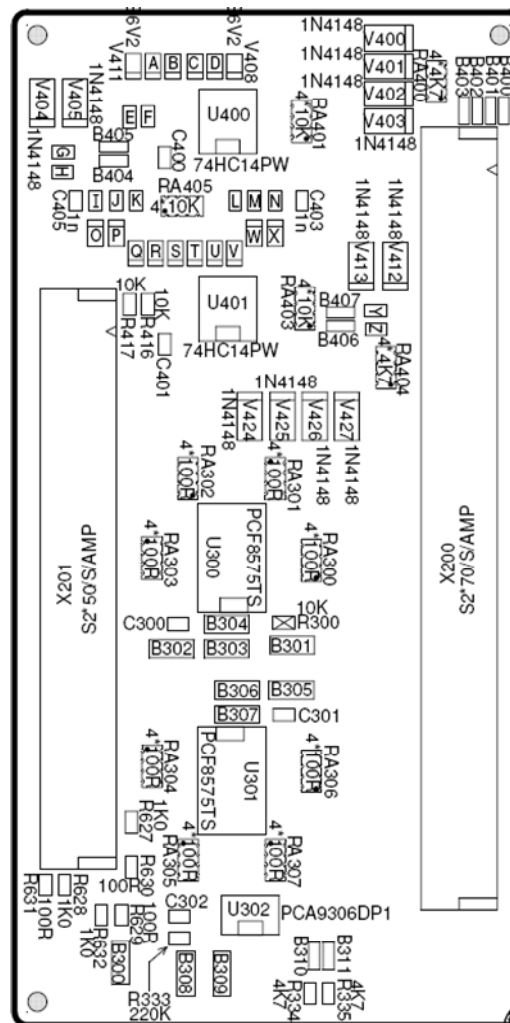
3.4.4.4 Protected Digital Inputs

X205	Description	X205	Description
1	DI0 input	2	DI8 input
3	DI1 input	4	DI9 input
5	DI2 input	6	DI10 input
7	DI3 input	8	DI11 input
9	DI4 input	10	DI12 input
11	DI5 input	12	DI13 input
13	DI6 input	14	DI14 input
15	DI7 input	16	DI15 input
17	CPU Vcc	18	+3V3
19	+5V	20	SGND

3.4.4.5 Location Of Module Jumpers And Connectors



Top View



Bottom View

3.4.5 Detailed Notes On Configuring The DIO54 Module For Use

3.4.5.1 DIO54 Compatibility

The DIO54 module has been designed as a universal module which can accept any processor modules designed for the EDP system. As such it is important to note that there are a few limitations which the user needs to be aware of. You must check that the DIO54 is correctly configured for your CPU before fitting it to the EDP baseboard!

3.4.5.2 Controlling The DIO54 Digital I/O Module

This module can be controlled by the CPU in several ways. On board the module are two independent serial I/O latch devices. Each of these devices has an input mode and an output mode function. The PCB has been designed such that one device is dedicated to output mode and the other device is dedicated for input mode. The chip used is the NXP PCA9555 device.

The PCA9555 device can be controlled via the I2C0 channel on the CPU via the back plane. This I2C0 channel is referred to as the CNTRL I2C channel on the Baseboard. Each of the two PCA9555 devices has its own unique I2C address to communicate on.

3.4.5.3 Digital Outputs

The PCA9555A device can be used to output data, the raw logic level output signals for this are referred to as OUT_P0(x) and OUT_P1(x) where $x = 0$ to 7. These signals are available to probe on connector X203, and there are 16 logic level outputs in total. These raw logic level outputs **can** be fed into a high current Darlington driver of the type ULN2003. This however is a board option and the user has to configure the board to do this via a series of solder bridges. These bridges are B501-B508 and B602-B609. Check the board to ensure they are configured how you want them.

The Darlington drive output from the ULN2003 appears on another connector X202, as signal DO(y) where $y = 0$ to 15. Note the output drive of DO(0)-DO(11) is double that of DO(12)-DO(15), due to the way the hardware has been implemented.

The CPU also has some direct I/O capability and this feature is bought out onto the Baseboard. The Digital I/O Module has access to these signals and the user can use these rather than the signals produced by the I2C PCA9555 digital latches. On the Digital I/O Module these signals are referred to as EDP_DO(y) where $y = 0$ to 15.

The mapping between the CPU's port pins and the Output on the DO(y) pins is given later.

3.4.5.4 Digital Inputs

The Digital I/O Module can also read in external input signals via an input buffer. The real world signals are referred to as DI(y) where $y = 0$ to 15. Signals DI(0) to DI(11) have an input protection stage and hex Schmitt trigger inverting buffer input whilst signals DI(12) to DI(15) have a different input protection arrangement. There are no buffers or inversion of these signals. The input signals after the protection stage can be routed via jumper links to either the serial input latches or to the STR9 MCU I/O pins. Jumpers J400 and J401 provide routing for 12 inputs DI(0) to DI(11) whilst input DI(12) to DI(15) have no routing capability and are fed directly into one of the PCA9555 serial latch device. The signals which are passed into the latches are referred to as IN_P0(x) and IN_P1(x) where $x = 0$ to 7, whilst the signals which pass directly into the MCU pins are referred to as EDP_DI(z) where $z = 0$ to 11.

There is no problems at all when the devices are configured as serial latch input device, although it's worth noting that the same logic level when presented to DI(0) to DI(11) will read differently when presented to DI(12) to DI(15). This is because the DI(0) to DI(11) inputs have the Schmitt inverter in series with them.

When the link options are organised for direct input digital reading it's worth noting that there may be a share conflict with other modules that may require these I/O pins as output pins.

3.4.5.5 Mapping Of CPU Peripheral Pins To The Digital Module

XC167 Pin Allocation	STR9 Pin Allocation	EDP-AM-DIO54 Allocation
Vcc to BB	Vcc 3V3 or 5V, supplied by CM	Vcc 3V3 or 5V, supplied by CM
P3.5	P5.7	IRQ_GPIO18_I2C GEN0 INT
P3.2	P5.6	IRQ_GPIO16_CNTRL I2C INT
9 P6.2/CC2IO	P6.0	EDP_DO9
8 P6.1/CC1IO	P4.7	EDP_DO8
56 P2.15/CC15IO	P4.6	EDP_DO7
55 P2.14/CC14IO	P4.5	EDP_DO6
54 P2.13/CC13IO	P4.4	EDP_DO5
53 P2.12/CC12IO	P4.3	EDP_DO4
52 P2.11/CC11IO	P4.2	EDP_DO3
51 P2.10/CC10IO	P4.0	EDP_DO2
13 P6.6/CC6IO	P6.4	EDP_DO13
12 P6.5/CC5IO	P6.3	EDP_DO12
11 P6.3/CC4IO	P6.2	EDP_DO11
10 P6.3/CC3IO	P6.1	EDP_DO10
50 P2.9/CC9IO	P4.1	EDP_DO1
49 P2.8/CC8IO	P4.0	EDP_DO0
P3.7	P7.4	EDP_DI11
Digital GND	Digital GND	Digital GND
Vcc 5V from reg	5V from baseboard regulator	5V from baseboard regulator
Vcc 3V3 from reg	3V3 from baseboard regulator	3V3 from baseboard regulator
12V Power GND	12V Power GND	12V Power GND
12V Power GND	12V Power GND	12V Power GND
+12V 2A	+12V 2A	+12V 2A
+12V 2A	+12V 2A	+12V 2A

XC167 Pin Allocation	STR9 Pin Allocation	EDP-AM-DIO54 Allocation
Vcc to BB	Vcc 3V3 or 5V, supplied by CM	Vcc 3V3 or 5V, supplied by CM
24 P9.3/CC19IO	P4.0	NC
55 P2.14/CC14IO	P0.1	EDP_DO18
56 P2.15/CC15IO	P6.5	EDP_DO17
21 P9.0/CC16IO	P4.6	EDP_DO16
22 P9.1/CC17IO	P4.4	EDP_DO15
23 P9./2CC18IO	P4.2	EDP_DO14
131 P1H.4/CC24IO	P6.7	EDP_DI9
132 P1H.5/CC25IO	P6.6	EDP_DI8
133 P1H.6/CC26IO	P7.7	EDP_DI7
134 P1H.7/CC27IO	P7.6	EDP_DI6
15 P7.4/CC28IO	P7.3	EDP_DI5
16 P7.5/CC29IO	P7.2	EDP_DI4
17 P7.6/CC30IO	P7.1 (PHY disabled)	EDP_DI3
P7.7/CC31IO (CS8900A INT)	P7.0	EDP_DI2
124 P1L.7/CC22IO	P0.6 (PHY disabled)	EDP_DI10
124 P1L.7/CC22IO	P0.5 (PHY disabled)	EDP_DI1
127 P1H.0/CC23IO	P0.4 (PHY disabled)	EDP_DI0
Digital GND	Digital GND	Digital GND
Vcc 5V from reg	5V from baseboard regulator	5V from baseboard regulator
Vcc 3V3 from reg	3V3 from baseboard regulator	3V3 from baseboard regulator
12V Power GND	12V Power GND	12V Power GND
12V Power GND	12V Power GND	12V Power GND
+12V 2A	+12V 2A	+12V 2A
+12V 2A	+12V 2A	+12V 2A

XC167 Pin Allocation	STR9 Pin Allocation	EDP-AM-DIO54 Allocation
Vcc 5V from reg	Vcc 5V from reg	Vcc 5V from reg
Vcc 3V3 or 5V, supplied by CPU	Vcc 3V3 or 5V, supplied by CPU	Vcc 3V3 or 5V, supplied by CPU
Vcc 3V3 from reg	Vcc 3V3 from reg	Vcc 3V3 from reg
26 SCL2	P2.0	EDPCON2.79
25 SDA2	P2.1	EDPCON2.77
24 SCL1	P2.2	EDPCON2.7
23 SDA1	P2.3	EDPCON2.5
Digital GND	Digital GND	Digital GND

Note: The shaded signals are not available with certain CPU modules. These inputs and outputs are recommended to be connected to the appropriate I2C GPIO device rather than relying on the CPU's own port pins.

3.4.6 Setting The Jumpers And Solder Bridges

To make the Digital I/O Module compatible with direct MCU drive from the I/O pins the solder jumpers mentioned above, B501-B508 and B602-B609 need to be set accordingly. This means the user has the option to drive the output directly from the MCU's or via the PCA9555 serial latch depending on the jumper options.

In terms of compatibility with other modules it is worth noting that the STR9 has on board ADC. These ADC channels are on Port4, so there is a potentially conflicting situation when used with the Analogue Module. I.e. The analogue module will present analogue values to Port4 whilst

Port4 is trying to drive the Digital Module outputs. It is therefore prudent to reserve the Port4 pins for analogue input whilst using the Port6 pins for digital output. This means having some idea of what MCU system resources you will require in your design and modifying both the source code and the hardware to suite.

The low level hardware drivers may therefore need to be modified when mixing modules to avoid this potential conflict.

The Digital I/O Module can also read in external input signals via an input buffer. The real world signals are referred to as DI(y) where $y = 0$ to 15. Signals DI(0) to DI(11) have an input protection stage and hex Schmitt trigger inverting buffer input whilst signals DI(12) to DI(15) have a different input protection arrangement. There are no buffers or inversion of these signals. The input signals after the protection stage can be routed via jumper links to either the serial input latches or to the STR9 MCU I/O pins. Jumpers J400 and J401 provide routing for 12 inputs DI(0) to DI(11) whilst input DI(12) to DI(15) have no routing capability and are fed directly into one of the PCA9555 serial latch device. The signals which are passed into the latches are referred to as IN_P0(x) and IN_P1(x) where $x = 0$ to 7, whilst the signals which pass directly into the MCU pins are referred to as EDP_DI(z) where $z = 0$ to 11.

There is no problems at all when the devices are configured as serial latch input device, although it's worth noting that the same logic level when presented to DI(0) to DI(11) will read differently when presented to DI(12) to DI(15). This is because the DI(0) to DI(11) inputs have the Schmitt inverter in series with them.

When the link options are organised for direct input digital reading it's worth noting that there may be a share conflict with other modules that may require these I/O pins as output pins.

3.4.7 Digital IO Module Jumper Settings

Before fitting the DIO54 module to your EDP baseboard, you must configure the jumpers and solder bridges to suit the CPU module you are intending to use. The possible settings are given in the following table.

Jumper	Type	Purpose	Default State	Default
B300	Cut & Solder	Set operating voltage of I2C GPIO devices	Use CPU's Vcc	1-2
B301	Cut & Solder	Select which I2C channel interrupt to use with both I2C GPIO devices	I2C_CTRL INT	1-2
B302	Cut & Solder	Set address bit A0 for U300 (input) I2C GPIO device	A0 = 0	1-2
B303	Cut & Solder	Set address bit A1 for U300 (input) I2C GPIO device	A1 = 1	2-3
B304	Cut & Solder	Set address bit A2 for U300 (input) I2C GPIO device	A2 = 0	1-2
B305	Cut & Solder	Set address bit A0 for U301 (output) I2C GPIO device	A0 = 1	2-3
B306	Cut & Solder	Set address bit A1 for U301 (output) I2C GPIO device	A1 = 1	2-3
B307	Cut & Solder	Set address bit A2 for U301 (output) I2C GPIO device	A2 = 0	1-2
B308	Cut & Solder	Select I2C_CTRL bus or I2C_GEN0 bus	I2C_CTRL	1-2
B309	Cut & Solder	Select I2C_CTRL bus or I2C_GEN0 bus	I2C_CTRL	1-2
B310	Solder	Bypass PCA9306	Not Bypassed	Open
B311	Solder	Bypass PCA9306	Not Bypassed	Open
B312	Solder	Connect blue LED in RGB array to D00	Not connected	Open
B313	Solder	Connect green LED in RGB array to D00	Not connected	Open
B314	Solder	Connect red LED in RGB array to D00	Not connected	Open
B400	Cut	Pull up DI0 digital input to DIO54 module	Pulled-up	Closed
B401	Cut	Pull up DI1 digital input to DIO54 module	Pulled-up	Closed
B402	Cut	Pull up DI2 digital input to DIO54 module	Pulled-up	Closed
B403	Cut	Pull up DI3 digital input to DIO54 module	Pulled-up	Closed
B404	Cut	Pull up DI4 digital input to DIO54 module	Pulled-up	Closed
B405	Cut	Pull up DI5 digital input to DIO54 module	Pulled-up	Closed
B406	Cut	Pull up DI6 digital input to DIO54 module	Pulled-up	Closed
B407	Cut	Pull up DI7 digital input to DIO54 module	Pulled-up	Closed
B408	Cut	Pull up DI8 digital input to DIO54 module	Pulled-up	Closed
B409	Cut	Pull up DI9 digital input to DIO54 module	Pulled-up	Closed
B410	Cut	Pull up DI10 digital input to DIO54 module	Pulled-up	Closed
B411	Cut	Pull up DI11 digital input to DIO54 module	Pulled-up	Closed
B412	Cut	Pull up DI12 digital input to DIO54 module	Pulled-up	Closed
B413	Cut	Pull up DI13 digital input to DIO54 module	Pulled-up	Closed
B414	Cut	Pull up DI14 digital input to DIO54 module	Pulled-up	Closed
B415	Cut	Pull up DI15 digital input to DIO54 module	Pulled-up	Closed



= CPU output option may not be available with all EDP CPU modules

Jumper	Type	Purpose	Default State	Default
B501	Cut & Solder	Connect ULN2003 input to either CPU output pin or U301 I2C GPIO device	CPU output	1-2
B502	Cut & Solder	Connect ULN2003 input to either CPU output pin or U301 I2C GPIO device	CPU output	1-2
B503	Cut & Solder	Connect ULN2003 input to either CPU output pin or U301 I2C GPIO device	CPU output	1-2
B504	Cut & Solder	Connect ULN2003 input to either CPU output pin or U301 I2C GPIO device	CPU output	1-2
B505	Cut & Solder	Connect ULN2003 input to either CPU output pin or U301 I2C GPIO device	CPU output	1-2
B506	Cut & Solder	Connect ULN2003 input to either CPU output pin or U301 I2C GPIO device	CPU output	1-2
B507	Cut & Solder	Connect ULN2003 input to either CPU output pin or U301 I2C GPIO device	CPU output	1-2
B508	Cut & Solder	Connect ULN2003 input to either CPU output pin or U301 I2C GPIO device	CPU output	1-2
B602	Cut & Solder	Connect ULN2003 input to either CPU output pin or U301 I2C GPIO device	CPU output	1-2
B603	Cut & Solder	Connect ULN2003 input to either CPU output pin or U301 I2C GPIO device	CPU output	1-2
B604	Cut & Solder	Connect ULN2003 input to either CPU output pin or U301 I2C GPIO device	CPU output	1-2
B605	Cut & Solder	Connect ULN2003 input to either CPU output pin or U301 I2C GPIO device	CPU output	1-2
B606	Cut & Solder	Connect ULN2003 input to either CPU output pin or U301 I2C GPIO device	CPU output	1-2
B607	Cut & Solder	Connect ULN2003 input to either CPU output pin or U301 I2C GPIO device	CPU output	1-2
B608	Cut & Solder	Connect ULN2003 input to either CPU output pin or U301 I2C GPIO device	CPU output	1-2
B609	Cut & Solder	Connect ULN2003 input to either CPU output pin or U301 I2C GPIO device	CPU output	1-2
J400A	Jumper	Route DIO input to CPU digital input pin via EDP or to I2C GPIO U300	Use CPU input	1-2
J400B	Jumper	Route DIO input to CPU digital input pin via EDP or to I2C GPIO U300	Use CPU input	1-2
J400C	Jumper	Route DIO input to CPU digital input pin via EDP or to I2C GPIO U300	Use CPU input	1-2
J400D	Jumper	Route DIO input to CPU digital input pin via EDP or to I2C GPIO U300	Use CPU input	1-2
J400E	Jumper	Route DIO input to CPU digital input pin via EDP or to I2C GPIO U300	Use CPU input	1-2
J400F	Jumper	Route DIO input to CPU digital input pin via EDP or to I2C GPIO U300	Use CPU input	1-2
J401A	Jumper	Route DIO input to CPU digital input pin via EDP or to I2C GPIO U300	Not fitted	Open
J401B	Jumper	Route DIO input to CPU digital input pin via EDP or to I2C GPIO U300	Not fitted	Open
J401C	Jumper	Route DIO input to CPU digital input pin via EDP or to I2C GPIO U300	Not fitted	Open
J401D	Jumper	Route DIO input to CPU digital input pin via EDP or to I2C GPIO U300	Not fitted	Open
J401E	Jumper	Route DIO input to CPU digital input pin via EDP or to I2C GPIO U300	Not fitted	Open
J401F	Jumper	Route DIO input to CPU digital input pin via EDP or to I2C GPIO U300	Not fitted	Open

= CPU output option may not be available with all EDP CPU modules

3.5 DC Brushed Motor Controller

The motor controller module is designed to drive 12V DC brushed motors of up to 2A with 3A being permitted when the auxiliary power connector is used. Up to two motor control modules may be fitted to a single baseboard (see section on configuring module for use as a secondary drive). There is no intelligence contained within the module and software running on a CPU module is required to realise an useful motor drive.

It is based on the LM18200 full DMOS bridge controller and can be used in a variety of ways to realise different levels of current and speed control strategy. Current monitoring is possible via the CM's ADC and the device itself is protected by an over-temperature output which allows the drive to be deactivated under software control to prevent damage.

Warning: it is the user's responsibility to provide such software.

To allow the creation of a motor controller with practical applications, inputs are provided for the following:

Input Name	Default Input Type	Alternate Input Type	Comment
Open limit switch	Voltless contact to ground (1MOhm pull-up)	4K7 pull-up to VCC_CM	Extreme of travel if used as a servo
Closed limit switch	Voltless contact to ground (1MOhm pull-up)	4K7 pull-up to VCC_CM	Extreme of travel if used as a servo
Tachogenerator	0-10V	0-ADC VAREF voltage	Speed feedback as a voltage
Quadrature encoder/Hall sensor	1K pull-up to VCC_CM	None	Speed and direction feedback
Tacho pulses	4K7 pull-up to VCC_CM	None	Speed feedback
External fault	4K7 pull-up to VCC_CM	None	Emergency stop request from controlled plant
Fault reset	Voltless contact to ground (1MOhm pull-up)	4K7 pull-up to VCC_CM	Clear any faults and restart motor
Motor run/stop	Voltless contact to ground (1MOhm pull-up)	4K7 pull-up to VCC_CM	Start or stop motor
Motor direction	Voltless contact to ground (1MOhm pull-up)	4K7 pull-up to VCC_CM	Change motor direction of running
Vdclink	Analog 0-VCC_CM	None	Allows the motor drive voltage to be measured
Vsense	Analog 0-VCC_CM	None	Allows the motor current to be measured as a voltage ($R_{sense} * 377\mu A$ per Amp)
Target current reached	Digital, 0-3V3	None	Interrupt request to CM when motor current reached target level set by CPU DAC00_GPIO17 during last chopping period

Software is required for the CM fitted to make full use of these inputs.

3.5.1 Mapping Of CPU Peripherals To Motor Control Module

The CPU peripheral pins on the CPU module are connected to the motor control module as shown below. The mapping shows the connections for the situation where two motor control modules are present.

XC167 Pin Allocation	STR9 Pin Allocation	EDP-AM-MC1 Allocation
Vcc to BB	Vcc 3V3 or 5V, supplied by CM	Vcc 3V3 or 5V, supplied by CM
42 GUARD/AN GND	AVSS Analog GND	VAGND
92 P20.2	P8.0	GPIO0
8 P6.1/CC1IO	P4.7	EVG8_GPIO56
56 P2.15/CC15IO	P4.6	EVG7_GPIO54
55 P2.14/CC14IO	P4.5	EVG6_GPIO52
54 P2.13/CC13IO	P4.4	EVG5_GPIO50
53 P2.12/CC12IO	P4.3	EVG4_GPIO48
52 P2.11/CC11IO	P4.2	EVG3_GPIO46
51 P2.10/CC10IO	P4.0	EVG2_GPIO44
13 P6.6/CC6IO	P6.4	EVG18_GPIO66
12 P6.5/CC5IO	P6.3	EVG16_GPIO64
10 P6.3/CC3IO	P6.1	EVG12_GPIO60
50 P2.9/CC9IO	P4.1	EVG1_GPIO42
49 P2.8/CC8IO	P4.0	EVG0_GPIO40
Digital GND	Digital GND	Digital GND
37 AN8	NC	AN8
39 AN6	P4.6	AN6
33 AN4	P4.4	AN4
31 AN2	P4.2	AN2
45 AN14	NC	AN14
43 AN12	NC	AN12
35 AN10	NC	AN10
29 AN0	P4.0	AN0
Vcc 5V from reg	5V from baseboard regulator	5V from baseboard regulator
Vcc 3V3 from reg	3V3 from baseboard regulator	3V3 from baseboard regulator
12V Power GND	12V Power GND	12V Power GND
12V Power GND	12V Power GND	12V Power GND
+12V 2A	+12V 2A	+12V 2A
+12V 2A	+12V 2A	+12V 2A

XC167 Pin Allocation	STR9 Pin Allocation	EDP-AM-MC1 Allocation
Vcc to BB	Vcc 3V3 or 5V, supplied by CM	Vcc 3V3 or 5V, supplied by CM
GUARD/AN GND	AVSS Analog GND	VAGND
80 P4.0	P8.1	GPIO1
131 P1H.4/CC24IO	P6.7	EVM9_GPIO55
132 P1H.5/CC25IO	P6.6	EVM8_GPIO53
133 P1H.6/CC26IO	P7.7	EVM7_GPIO51
134 P1H.7/CC27IO	P7.6	EVM6_GPIO49
15 P7.4/CC28IO	P7.3	EVM5_GPIO47
16 P7.5/CC29IO	P7.2	EVM4_GPIO45
P7.7/CC31IO (CS8900A INT)	P7.0	EVM2_GPIO41_CAPADC
124 P1L.7/CTRAP	P6.7	EMG TRP
Digital GND	Digital GND	Digital GND
26 P9.5/CC21IO	P6.2	CPU DACO1_GPIO19
25 P9.4/CC20IO	P6.0	CPU DACO0_GPIO17
Vcc 5V from reg	5V from baseboard regulator	5V from baseboard regulator
Vcc 3V3 from reg	3V3 from baseboard regulator	3V3 from baseboard regulator
12V Power GND	12V Power GND	12V Power GND
12V Power GND	12V Power GND	12V Power GND
+12V 2A	+12V 2A	+12V 2A
+12V 2A	+12V 2A	+12V 2A

3.5.2 Characteristics Of Motor Controller

The LM18200 as deployed on the module can handle 12V - 24V motors at up to 3A continuous or 6A peak. However the EDP baseboard only allows a maximum of 2A. Therefore if your application is likely to require more than 2A, you must power the motor module directly through the screw terminals P302 – see below.

3.5.2.1 High Current Applications

If a motor of above 2A current rating is used, the auxiliary high current connector P302 must be used to supply 12V and ground otherwise the current limit of the EDP baseboard module connectors will be exceeded. You must also set jumper JP301 to position 2-3.

3.5.3 Controlling The DC Motor

There are two basic approaches to regulating motor torque and hence for a given load, its speed.

3.5.3.1 Simple Fixed-On Time Mode

The simplest way to configure the module is to set jumpers JP203 to 1-2, JP205 to 2-3 JP207 to 1-2. In this mode, the voltage applied to CPU DACO0_GPIO17 will set the maximum current in the motor windings. For a given load, the motor speed can therefore be controlled. The chopping frequency will be approximately 25kHz, as determined by the LM555 C204 and R204..

A pulse-width modulated (PWM) or true digital-to-analog conversion channel from the CM can be used to provide a DC level that is compared with the voltage level achieved across the current sense resistor (R219).

This strategy provides only a crude control over motor current and should only be used with CMs that have limited PWM capabilities.

3.5.3.2 Full PWM Control Mode

This mode allows the current in the motor to be controlled directly and allows a precise control of motor speed. The default jumper settings are intended for this mode of operation.

3.5.4 Hardware Protection

The LM18200T over current output is connected to the EDPCON EMGTRP line to allow software on the CM to switch the motor off.

3.5.5 Motor Controller User Options

There are a large number of user options for this module. The default settings assume the module will be used in a single motor system or as the first controller in a dual motor arrangement.

3.5.5.1 Default (First Motor Controller)

Jumper	Type	Purpose	Default	Notes
JP201	3-way	Select CPU interrupt for current threshold reached	2-3	
JP202	3-way	Select source of current control voltage	1-2	
JP203	3-way	Enable LM555 control of motor current	2-3	LM555 disabled
JP204	3-way	Select source of PWM for direct motor current control	1-2	
JP205	3-way	Enable LM555 control of motor current	1-2	LM555 disabled
JP206	3-way	Select source for motor direction control	1-2	
JP207	3-way	Motor direction set by CPU pin or from P301 motor direction input	2-3	CPU controls direction
JP208	3-way	Select CPU input for P301 motor direction input	1-2	
JP209	3-way	Select CPU pin motor brake control	2-3	
JP210	2-way	Add 4K7 pull-up to Vcc_CM to motor direction input	Open	No pull-up
JP301	3-way	Allow LM18200 driver to be powered from external high current 12V supply	1-2	Motors > 2A must use 2-3
JP302	3-way	Select CPU pin for encoder0/tacho pulses input	1-2	
JP303	3-way	Enable tacho pulse input or encoder input 0	1-2	
JP304	3-way	Select CPU analog channel for Tacho voltage input	1-2	
JP305	2-way	Add 4K7 pull-up to Vcc_CM for P301 fault reset input	Open	Assume voltless contact to GND
JP306	3-way	Select CPU pin for encoder1 input	1-2	
JP307	3-way	Select CPU analog channel for motor current sense resistor voltage input	1-2	
JP308	2-way	Add 4K7 pull-up to Vcc_CM for P301 closed limit switch input	Open	Assume voltless contact to GND
JP309	3-way	Select CPU pin for P301 closed limit switch input	1-2	
JP310	2-way	Add 4K7 pull-up to Vcc_CM for P301 motor run/stop input	Open	Assume voltless contact to GND
JP311	3-way	Select CPU pin for motor run/stop input	1-2	
JP312	3-way	Select CPU analog channel for Tacho voltage input	1-2	
JP313	2-way	Add 4K7 pull-up to Vcc_CM for P301 open limit switch input	Open	Assume voltless contact to GND
JP314	3-way	Select CPU pin for P301 open limit switch input	1-2	
J301	solder	Connect pot VR301 to CPU ADC	closed	
J302	solder	Connect pot VR302 to CPU ADC	closed	

3.5.5.2 Jumper Settings As A Second Motor Controller

Jumper	Type	Purpose	Motor 2	Notes
JP201	3-way	Select CPU interrupt for current threshold reached	1-2	
JP202	3-way	Select source of current control voltage	2-3	
JP203	3-way	Enable LM555 control of motor current	2-3	LM555 disabled
JP204	3-way	Select source of PWM for direct motor current control	2-3	
JP205	3-way	Enable LM555 control of motor current	1-2	LM555 disabled
JP206	3-way	Select source for motor direction control	2-3	
JP207	3-way	Motor direction set by CPU pin or from P301 motor direction input	2-3	CPU controls direction
JP208	3-way	Select CPU input for P301 motor direction input	2-3	
JP209	3-way	Select CPU pin motor brake control	1-2	
JP210	2-way	Add 4K7 pull-up to Vcc_CM to motor direction input	Open	No pull-up
JP301	3-way	Allow LM18200 driver to be powered from external high current 12V supply	1-2	Motors > 2A must use 2-3
JP302	3-way	Select CPU pin for encoder0/tacho pulses input	2-3	
JP303	3-way	Enable tacho pulse input or encoder input 0	2-3	
JP304	3-way	Select CPU analog channel for Tacho voltage input	2-3	
JP305	2-way	Add 4K7 pull-up to Vcc_CM for P301 fault reset input	Open	Assume voltless contact to GND
JP306	3-way	Select CPU pin for encoder1 input	2-3	
JP307	3-way	Select CPU analog channel for motor current sense resistor voltage input	2-3	
JP308	2-way	Add 4K7 pull-up to Vcc_CM for P301 closed limit switch input	Open	Assume voltless contact to GND
JP309	3-way	Select CPU pin for P301 closed limit switch input	2-3	
JP310	2-way	Add 4K7 pull-up to Vcc_CM for P301 motor run/stop input	Open	Assume voltless contact to GND
JP311	3-way	Select CPU pin for motor run/stop input	2-3	
JP312	3-way	Select CPU analog channel for Tacho voltage input	2-3	
JP313	2-way	Add 4K7 pull-up to Vcc_CM for P301 open limit switch input	Open	Assume voltless contact to GND
JP314	3-way	Select CPU pin for P301 open limit switch input	2-3	
J301	solder	Connect pot VR301 to CPU ADC	open	Not for motor 2
J302	solder	Connect pot VR302 to CPU ADC	open	Not for motor 2

3.5.6 Using The Motor Control Module

3.5.6.1 Connecting The DC Motor

The connection example here is based on the 12A Crouzet motor (RS part no. 715-106) with optional 1 pulse-per-rev encoder kit (RS part no. 715-134). An example program is provided that allows a simple proportional-integral-derivative (PID) speed controller to be demonstrated.



3.5.6.2 Motor Controller Connectors

The 4-way miniature screw connector terminal P302 is used to connect the DC motor armature.

P302	Description
1	Motor +
2	Motor -
3	12V high current
4	12V ground

The 16-way pin header P301 is used to connect encoders, tachometers, limit switches, run/stop and direction inputs.

P301	Description	P301	Description
1	NC	2	Open limit switch
3	CPU Vcc	4	Closed limit switch
5	+3V3	6	Tacho pulses
7	+5V	8	Encoder 0
9	Motor Run/Stop	10	Encoder 1
11	Motor Direction	12	Fault reset in
13	Tacho Voltage	14	External fault in
15	Digital Ground	16	Digital Ground

3.5.6.3 Connecting The Crouzet Motor And Encoder

The encoder module requires a 5V supply which is derived from pin 7 of the 16-way pin header P301. The open collector output is connected to P302 pin 6 – R306 on the motor control module provides the necessary pull-up resistor to the positive supply rail.

P301	Encoder Connector	P301	Encoder Connector
1		2	
3		4	
5		6	4
7	2	8	
9		10	
11		12	
13		14	
15	3	16	

As the duty cycle of the encoder output is not guaranteed to be 50%, only one edge should be used to detect the motor speed. The example application supplied uses only the negative edge.

3.5.7 Using Two EDP-AM-MC1 Modules To Drive Two Motors

A second motor module can be added. This requires the jumpers to be changed from the default 1-2 position to 2-3, as shown below. Note: The CM must have sufficient IO to support two motors.

Jumper	Type	Purpose	Default	Notes
JP201	3-way	Select CPU interrupt for current threshold reached	1-2	
JP202	3-way	Select source of current control voltage	2-3	
JP204	3-way	Select source of PWM for direct motor current control	2-3	
JP206	3-way	Select source for motor direction control	2-3	
JP208	3-way	Select CPU input for P301 motor direction input	2-3	
JP209	3-way	Select CPU pin motor brake control	1-2	
JP302	3-way	Select CPU pin for encoder0/tacho pulses input	2-3	
JP304	3-way	Select CPU analog channel for Tacho voltage input	2-3	
JP306	3-way	Select CPU pin for encoder1 input	2-3	
JP307	3-way	Select CPU analog channel for motor current sense resistor voltage input	2-3	
JP309	3-way	Select CPU pin for P301 closed limit switch input	2-3	
JP311	3-way	Select CPU pin for motor run/stop input	2-3	
JP312	3-way	Select CPU analog channel for Tacho voltage input	2-3	
JP314	3-way	Select CPU pin for P301 open limit switch input	2-3	

4. EDP CPU Modules

4.1 EDP-CM-XC167 CPU Module

The XC167 module uses development tools for C166/XC166 CPUs. The recommended toolchains are the Keil uVISION166 and the HitopXC. Other toolchains may be used such as Tasking but there are no specific examples provided for them.

4.1.1 Get The Latest Versions

It is recommended to always visit the EDP support website for the latest versions of the tools and examples. This is frequently updated and contains huge amount of useful information.

4.1.2 Module Features

XC167 CPU Module	Part Number EDP-CM-XC167
Features	Comment
140way TycoAMP FH series connector	
100way TycoAMP FH series connector	
SAF-XC167CI-32F40F, 256k FLASH, 40MHz, 5V	144TQFP, 256k on-chip FLASH
Singe-chip boot but with optional 16 bit external bus	16-bit mux bus
64kx16, <25ns, 5V SRAM	Chipselect = CS1
1x CAN transceiver with PESD2CAN protection	CAN_CTRL
8MHz XTAL	PLL multiplies to 40MHz
CS8900 ethernet controller	Easyweb stack.
2.5V core regulator	
32kHz XTAL for RTC	
I2C 3V3 to 5V level shifter	EDP I2C bus is 3V3
FTDI USB-JTAG and ASC1 interface	ASC1 may be connected to a virtual USB COM port via FT232L
Raw JTAG connector (0.05" socket)	Samtec FTSH
4-DIL switch	Bootstrap, bootmode and other configurations
User LED	Yellow (Port 4.3)
Power LED	Blue
ResetIN LED	Orange
ResetOUT LED	Red

4.1.3 XC167 To EDP Baseboard Connector Pin Mapping

The peripheral pins on the XC167 are mapped onto the EDP CON 1 & 2 connectors as show below. In the “Pin Function” column, the XC167 pin number and name is given.

4.1.3.1 EDP Connector 1

Pin	Pin Function	Pin	Pin Function	Pin	Pin Function	Pin	Pin Function
1	41 VAREF	2	NC	71	54 CC13IO	72	133 CC26IO
3	29 AN0	4	37 AN8	73	55 CC14IO	74	132 CC25IO
5	30 AN1	6	38 AN9	75	56 CC15IO	76	131 CC24IO
7	31 AN2	8	35 AN10	77	8 CC1IO	78	24 CC19IO
9	32 AN3	10	36 AN11	79	9 CC2IO	80	23 CC18IO
11	33 AN4	12	43 AN12	81	10 CC3IO	82	22 CC17IO
13	34 AN5	14	44 AN13	83	11 CC4IO	84	21 CC16IO
15	39 AN6	16	45 AN14	85	12 CC5IO	86	56 CC15IO
17	40 AN7	18	46 AN15	87	13 CC6IO	88	55 CC14IO
19	42 GUARD/AN GND	20	GUARD/AN GND	89	70 RxD0	90	124 CC22IO
21	92 P20.2	22	80 P4.0	91	69 TxD0	92	121 CC62
23	128 MRST1	24	81 P4.1	93	60 RxD1	94	128 MRST1
25	62 P3.3	26	64 P3.5	95	59 TxD1	96	129 MTSR1
27	63 P3.4	28	65 P3.6	97	NC	98	130 SCLK1
29	129 MTSR1	30	66 P3.7	99	P20.2	100	117 CC60
31	130 SCLK1	32	12 CC5IO	101	83 P4.3	102	118 COUT60
33	77 P3.15	34	13 CC6IO	103	Ethernet TX+ (CS8900)	104	119 CC61
35	83 P4.3	36	14 CC7IO	105	Ethernet TX-	106	120 COUT61
37	P3.2	38	25 CC20IO	107	Ethernet RX+	108	121 CC62
39	P3.5	40	26 CC21IO	109	Ethernet RX-	110	122 COUT62
41	P3.6	42	127 CC23IO	111	Ethernet LINK LED	112	123 COUT63
43	P3.7	44	124 CC22IO	113	Ethernet RX LED	114	124 CTRAP
45	POL.7	46	POH.7	115	NC	116	127 #C6POS0
47	POL.6	48	POH.6	117	NC	118	128 #C6POS1
49	POL.5	50	POH.5	119	NC	120	129 #C6POS2
51	POL.4	52	POH.4	121	85 CAN0 RX	122	61 CAPIN
53	POL.3	54	POH.3	123	86 CAN0 TX	124	3V3 Vbatt
55	POL.2	56	POH.2	125	Vcc to BB	126	Vcc to BB
57	POL.1	58	POH.1	127	Vcc 3V3 from reg	128	Vcc 3V3 from reg
59	POL.0	60	POH.0	129	Vcc 5V from reg	130	Vcc 5V from reg
61	49 CC8IO	62	18 CC31IO (CS8900A INT)	131	Digital GND	132	Digital GND
63	50 CC9IO	64	17 CC30IO	133	+12V 2A	134	+12V 2A
65	51 CC10IO	66	16 CC29IO	135	+12V 2A	136	+12V 2A
67	52 CC11IO	68	15 CC28IO	137	12V Power GND	138	12V Power GND
69	53 CC12IO	70	134 CC27IO	139	12V Power GND	140	12V Power GND

4.1.3.2 EDP Connector 2

Pin	Pin Function		Pin Function	Pin	Pin Function		Pin Function
1	142 #RSTIN	2	142 #RSTIN	51	A16	52	A16
3	3 #RSTOUT	4	3 #RSTOUT	53	7 #CS0 (SRAM)	54	7 #CS0 (SRAM)
5	23 SDA1	6	23 SDA1	55	8 #CS1 (CS8900)	56	8 #CS1 (CS8900)
7	24 SCL1	8	24 SCL1	57	9 #CS2	58	9 #CS2
9	Digital GND	10	Digital GND	59	10 #CS3	60	10 #CS3
11	116 AD15	12	116 AD15	61	84 CAN1 RX	62	84 CAN1 RX
13	115 AD14	14	115 AD14	63	87 CAN1 TX	64	87 CAN1 TX
15	114 AD13	16	114 AD13	65	USB DEBUG D+	66	USB DEBUG D+
17	113 AD12	18	113 AD12	67	USB DEBUG D-	68	USB DEBUG D-
19	112 AD11	20	112 AD11	69	76 SCLK0	70	76 SCLK0
21	111 AD10	22	111 AD10	71	67 MRST0	72	67 MRST0
23	106 AD9	24	106 AD9	73	68 MTSR0	74	68 MTSR0
25	105 AD8	26	105 AD8	75	82 P4.2	76	82 P4.2
27	102 AD7	28	102 AD7	77	25 SDA2	78	25 SDA2
29	101 AD6	30	101 AD6	79	26 SCL2	80	26 SCL2
31	100 AD5	32	100 AD5	81	NC	82	NC
33	99 AD4	34	99 AD4	83	NC	84	NC
35	98 AD3	36	98 AD3	85	NC	86	NC
37	97 AD2	38	97 AD2	87	NC	88	NC
39	96 AD1	40	96 AD1	89	CANH control physical layer (CAN1)	90	CANH control physical layer (CAN1)
41	95 AD0	42	95 AD0	91	CANL control physical layer (CAN1)	92	CANL control physical layer (CAN1)
43	93 #ALE	44	93 #ALE	93	Vcc 3V3 or 5V, supplied by CPU	94	Vcc 3V3 or 5V, supplied by CPU
45	90 #RD	46	90 #RD	95	Vcc 3V3 from reg	96	Vcc 3V3 from reg
47	91 #WRL	48	91 #WRL	97	Vcc 5V from reg	98	Vcc 5V from reg
49	75 #WRH	50	75 #WRH	99	Digital GND	100	Digital GND

4.1.4 XC167 Module Selectable Jumpers

The XC167 module has the following selectable options:

Option	Type	Purpose	Default	Notes
B200-B215	Solder bridge	Connect CPU P9 & P8 multiplexed address bus to EDPCON2 or EDPCON1	Connect to EDPCON1 for IO use (XC167 bus isolated from backplane)	
B300-B301	Solder bridge	Connect ASC1 to USB virtual COMport	Connect ASC1 to EDPCON1	Allows XC167 ASC1 to be routed to a COMport on PC without using RS232
X300	Jumper	Select source of analog reference voltage	Reference derived from local 5V	EDP-AM-AN16 module required to use external reference
SW400	DIL Switch	Select XC167 boot configuration	Set internal FLASH boot	See XC167 manual for details
X500	Jumper	Enable local CAN transceiver on CAN0	Enabled	Disable if opto-isolated CAN channel is to be used for CAN0

The default jumper settings will cover most situations.

4.1.5 XC167 Module DIL Switch Settings

The XC167 has 4 DIL switches (SW400) which are used to configure the startup of the XC167 CPU. The switches are by default set to standard internal FLASH start mode (#EA = 1) and it is likely that this would ever need to be changed. The most important is switch is "1" which when set to ON will enable the built-in serial bootstrap mode via ASC0. Setting switch "3" to on as well will cause the CAN bootstrap loader to be enabled.

4.1.5.1 Entering The Special Bootstrap Modes

To enter bootstrap mode, set the switch 1 to ON and then power up the EDP baseboard or press the RESET button. Tools such as the Infineon MEMTOOL can then be used to program the on-chip FLASH.

4.2 EDP-CM-STR9 CPU Module

The STR9 module uses development tools for ARM CPUs. The recommended toolchains are the Keil uVISION, based on the ARM RealView compiler and the HitopARM, based on the GNU-C compiler. Other toolchains may be used but there are no specific examples provided for them.

4.2.1 Get The Latest Versions

Always visit the EDP support website for the latest versions of the tools and examples. This is frequently updated and contains huge amount of useful information.

4.2.2 Module Features

STR912 CPU Module	Part Number EDP-CM-STR9
Features	Comment
140way TycoAMP FH series connector	128TQFP, 512k on-chip FLASH, 96k SRAM Chipselect = CS0
100way TycoAMP FH series connector	
ARM966 CPU at 48MHz, 3V3	
64kx16, <25ns, 3V SRAM to be specified	CPU Runs at 96MHz
1x CAN transceiver with PESD2CAN protection	
25MHz XTAL	
USB ESD protection on USB +/- pins	Ethernet
STE100P PHY	
1.8V core regulator	
32kHz XTAL for RTC	Samtec FTSH. 0.1" JTAG adaptor available
FTDI USB-JTAG and ASC1 interface	
Raw JTAG connector (0.05" socket)	
Raw ETM trace connector (Mictor socket)	Optional part
User LED	Yellow (Port 7.0)
Power LED	Blue
ResetIN LED	Orange
ResetOUT LED	Red

4.2.2.1 EDP Connector 1

Pin	STR9 Pin	Pin	STR9 Pin
1	AVREF - Analog	2	
3	P4.0	4	NC
5	P4.1	6	NC
7	P4.2	8	NC
9	P4.3	10	NC
11	P4.4	12	NC
13	P4.5	14	NC
15	P4.6	16	NC
17	P4.7	18	NC
19	AVSS Analog GND	20	AVSS Analog GND
21	P8.0	22	P8.1
23	P3.5	24	P8.2
25	P8.4	26	TAMPER_IN
27	P8.3	28	NC
29	P3.7	30	NC
31	P3.4	32	NC
33	P3.6	34	NC
35	P0.7 (PHY disabled)	36	NC
37	P5.6	38	P6.0
39	P5.7	40	P6.2
41	P7.5	42	P0.4 (PHY disabled)
43	P7.4	44	P0.5 (PHY disabled)
45	P8.7	46	P9.7
47	P8.6	48	P9.6
49	P8.5	50	P9.5
51	P8.4	52	P9.4
53	P8.3	54	P9.3
55	P8.2	56	P9.2
57	P8.1	58	P9.1
59	P8.0	60	P9.0
61	P4.0	62	P7.0
63	P4.1	64	P7.1 (PHY disabled)
65	P4.0	66	P7.2
67	P4.2	68	P7.3
69	P4.3	70	P7.6

Pin	STR9 Pin	Pin	STR9 Pin
71	P4.4	72	P7.7
73	P4.5	74	6.6
75	P4.6	76	6.7
77	P4.7	78	P4.0
79	P6.0	80	P4.2
81	6.1	82	P4.4
83	6.2	84	P4.6
85	6.3	86	P6.5
87	P6.4	88	P0.1
89	P5.1	90	P0.6 (PHY disabled)
91	P5.0	92	P0.7 (PHY disabled)
93	P1.1 (PHY Disabled)	94	P3.5
95	P1.0 (PHY Disabled)	96	P3.6
97	P3.0	98	P3.4
99	P3.1	100	P6.1
101	P3.7	102	P6.0
103		104	P6.3
105		106	P6.2
107		108	P6.5
109		110	P6.4
111		112	NC
113		114	P6.7
115		116	P7.0
117	P2.1	118	P7.1
119	P2.0	120	P7.2
121	NC	122	P6.6
123	NC	124	3V3 Vbatt
125	Vcc 3V3 or 5V, supplied by CM	126	Vcc 3V3 or 5V, supplied by CM
127	3V3 from baseboard regulator	128	3V3 from baseboard regulator
129	5V from baseboard regulator	130	5V from baseboard regulator
131	Digital GND	132	Digital GND
133	+12V 2A	134	+12V 2A
135	+12V 2A	136	+12V 2A
137	12V Power GND	138	12V Power GND
139	12V Power GND	140	12V Power GND

4.2.2.2 EDP Connector 2

Pin	STR9 Pin	Pin	STR9 Pin
1	RESET_INn	2	RESET_INn
3	RESET_OUTn	4	RESET_OUTn
5	P2.3	6	P2.3
7	P2.2	8	P2.2
9	Digital GND	10	Digital GND
11	P9.7	12	P9.7
13	P9.6	14	P9.6
15	P9.5	16	P9.5
17	P9.4	18	P9.4
19	P9.3	20	P9.3
21	P9.2	22	P9.2
23	P9.1	24	P9.1
25	P9.0	26	P9.0
27	P8.7	28	P8.7
29	P8.6	30	P8.6
31	P8.5	32	P8.5
33	P8.4	34	P8.4
35	P8.3	36	P8.3
37	P8.2	38	P8.2
39	P8.1	40	P8.1
41	P8.0	42	P8.0
43	EMI_ALE	44	EMI_ALE
45	EMI_RD	46	EMI_RD
47	EMI_BWR_WRL	48	EMI_BWR_WRL
49	EMI_BWR_WRH	50	EMI_BWR_WRH

Pin	STR9 Pin	Pin	STR9 Pin
51	NC	52	NC
53	P5.4	54	P5.4
55	P5.5	56	P5.5
57	P5.6	58	P5.6
59	P5.7	60	P5.7
61	P3.3	62	P3.3
63	P3.2	64	P3.2
65	USB debug D+	66	USB debug D+
67	USB debug D-	68	USB debug D-
69	P2.4	70	P2.4
71	P2.6	72	P2.6
73	P2.5	74	P2.5
75	P2.7	76	P2.7
77	P2.1	78	P2.1
79	P2.0	80	P2.0
81	USB Host D+	82	USB Host D+
83	USB Host D-	84	USB Host D-
85	USBDP	86	USBDP
87	USBDN	88	USBDN
89	CANH0 control (physical layer)	90	CANH0 control (physical layer)
91	CANL0 control (physical layer)	92	CANL0 control (physical layer)
93	Vcc 3V3 or 5V, supplied by CM	94	Vcc 3V3 or 5V, supplied by CM
95	3V3 from baseboard regulator	96	3V3 from baseboard regulator
97	5V from baseboard regulator	98	5V from baseboard regulator
99	Digital GND	100	Digital GND

4.2.3 STR9 Module Selectable Jumpers

The STR9 module has the following selectable options:

Option	Type	Purpose	Default	Notes
B200-B215	Solder bridge	Connect CPU P0 multiplexed address bus to EDPCON2 or EDPCON1	Connect to EDPCON1 for IO use (ST912 bus isolated from backplane)	
B300-B301	Solder bridge	Connect UART1 RX & TX to USB virtual COMport	Connect UART1 to EDPCON1	Allows STR912 UART1 to be routed to a COMport on PC without using RS232
X300	Jumper	Select source of analog reference voltage	Reference derived from local 3V3	EDP-AM-AN16 module required to use external reference
X401	Jumper	Enable/disable STE100 Ethernet PHY	Closed = Ethernet enabled	Note: UART1 & 2 lost
X402	Jumper	Enable/disable local CAN transceiver	Closed = use local transceiver	Open if opto-isolated CAN is used on EDP-AM-CO1 module

4.2.4 STR9 Analog Grounding Arrangements

The analog ground (Avss) pin on the STR9 CPU is not connected to the digital ground on the module itself. This connection must be made via solder bridge P504 on the baseboard. By default, this is open so that the Avss is independent. This means that the user must ensure that either P504 is closed or that the Avss pin is not subjected to voltages that will cause internal damage to the STR9.

