EDP-AM-DIO54 Digital IO Module User Manual

This document contains information on the DIO54 digital IO module for the RS EDP system.

Version v5.0, 10/06/2010

Contents

1. Digital IO Module

The digital module provides a means to apply digital signals to the CM and drive world devices from it. There are 12 input channels with overvoltage protection and optional pull-ups, plus another 16 TTL inputs accessible only via I2C. 16 outputs are present each with a current drive capability of 500mA, plus another 16, 25mA logic outputs.

The first 12 inputs and 16 outputs are derived from the CM (where possible), although the protected input stages and high-current output stages can be connected to the I2C IO expander also.

The input I2C ports can generate an interrupt request. This is disabled by default as it could result in a high CPU interrupt loading.

An RGB colour LED may be fitted for experimental purposes

1.1 Digital Outputs

The 500mA outputs are simple low-side drives and are in the OFF state at power-up. They are designed to drive relays and solenoids and in fact can sink up to 1A but the user may need to attach a mini-heatsink to the driver IC if high duty ratios are expected.

It is up to the user to program the digital output pins of the CPU to a logic ‘1’ to turn the outputs on. There is a net inversion through the drivers so that a logic ‘1’ at the CPU output pin will result in a low (i.e. current sink enabled) at the output connector.

The user is provided with a software suite of drivers to allow the pins of the IO module to be controlled both by I2C and also via direct port manipulation of the MCU’s IO pins. All of the CMs provided by Hitex provide software support for the Digital IO Module

Depending on the CPU module being used, not all of the 12 inputs and 16 outputs can be controlled independently. This is due to a potential shortage of IO pins on the CPU itself. In such cases, the duplicated or unavailable channels should be routed to one of the two I2C GPIO devices to make up the shortfall.

1.2 Using Multiple Digital IO Modules

Up to 3 Digital IO Modules may be fitted to a single baseboard (4 if no CPU is fitted). Typically, the first module would make use of the CPU module’s own port pins. Other modules would rely on the I2C GPIO devices for their connection to the CPU. The full 8 I2C slave address variations is available to all these devices (via solder links on the AM). The user must make sure that there are no conflicts on IO pins on the backplane when more than one module is fitted. Alternatively, all digital IO modules could use I2C, freeing up CPU pins for other purposes.

Where a second EDP baseboard is available, the I2C_GEN_0 I2C bus can be used to connect further digital IO modules.

1.3 Software Drivers For Digital Module

The module has two I2C GPIO devices, both of which require special software drivers to access. These are provided for each of the CPU Modules. The software allows for control from both I2C bus commands and also via direct port control from the CPU.

1.4 Digital IO Module Connectors

1.4.1 500mA Outputs

X202	Description	X202	Description
1	DO0 1A output	2	DO8 1A output
3	DO1 1A output	4	DO9 1A output
5	DO2 1A output	6	DO10 1A output
7	DO3 1A output	8	DO11 1A output
9	DO4 1A output	10	DO12 500mA output
11	DO5 1A output	12	DO13 500mA output
13	DO6 1A output	14	DO14 500mA output
15	DO7 1A output	16	DO15 500mA output
17	DO16_L logic output	18	DO17_L logic output
19	DO18_L logic output	20	DO15 500mA output
21	CPU Vcc	22	12V GND
23	CPU Vcc	24	+12V

Note: Although the outputs DO0 – DO11 are rated at 1 Amp you should take care that the maximum total ULN2003 power dissipation is not exceeded.

1.4.2 I2C GPIO Outputs (25mA)

X203	Description	X203	Description
1	GPIO OUT_P00	2	GPIO OUT_P10
3	GPIO OUT_P01	4	GPIO OUT_P11
5	GPIO OUT_P02	6	GPIO OUT_P12
7	GPIO OUT_P03	8	GPIO OUT_P13
9	GPIO OUT_P04	10	GPIO OUT_P14
11	GPIO OUT_P05	12	GPIO OUT_P15
13	GPIO OUT_P06	14	GPIO OUT_P16
15	GPIO OUT_P07	16	GPIO OUT_17
17	CPU Vcc	18	+3V3
19	+5V	20	SGND

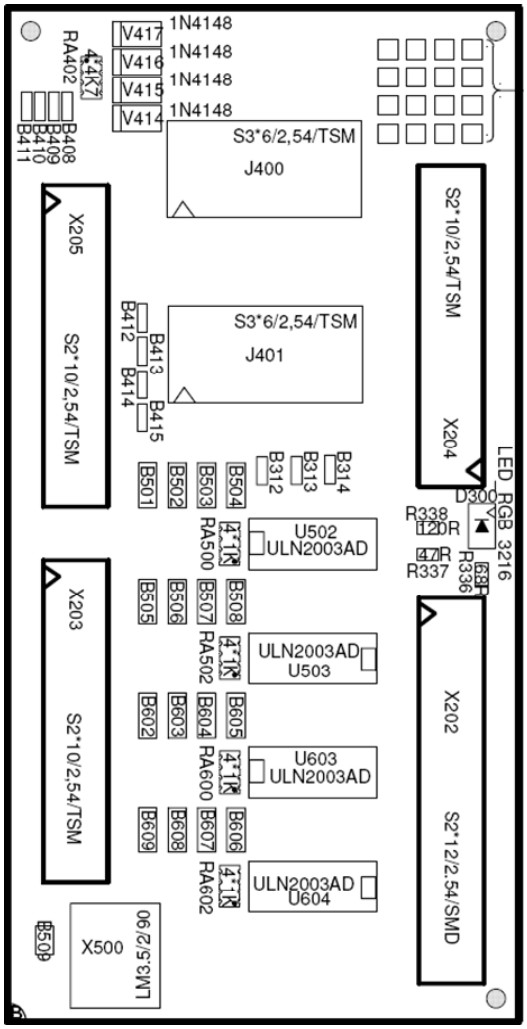
1.4.3 I2C GPIO Inputs (unprotected)

X204	Description	X204	Description
1	GPIO IN_P00	2	GPIO IN_P10
3	GPIO IN_P01	4	GPIO IN_P11
5	GPIO IN_P02	6	GPIO IN_P12
7	GPIO IN_P03	8	GPIO IN_P13
9	GPIO IN_P04	10	GPIO IN_P14
11	GPIO IN_P05	12	GPIO IN_P15
13	GPIO IN_P06	14	GPIO IN_P16
15	GPIO IN_P07	16	GPIO IN_P17
17	CPU Vcc	18	+3V3
19	+5V	20	SGND

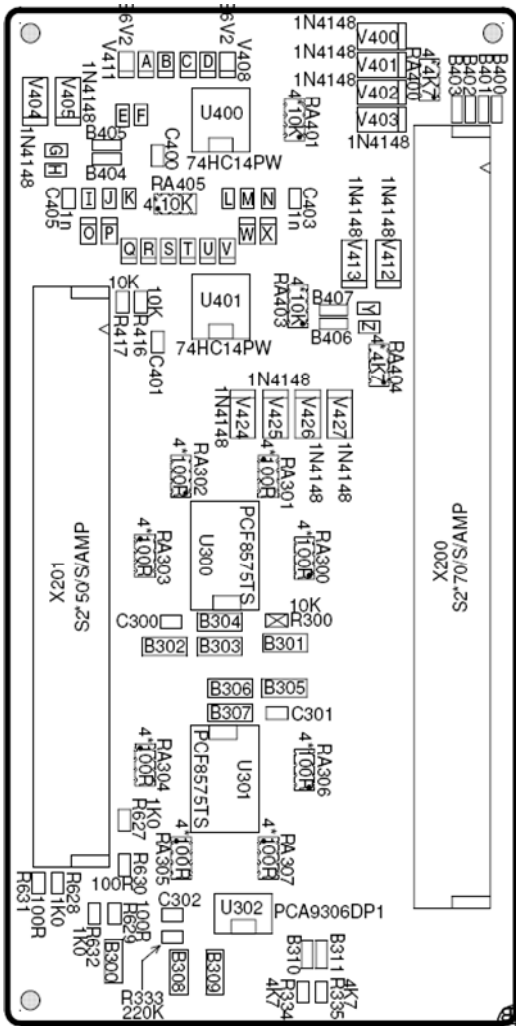
1.4.4 Protected Digital Inputs

X205	Description	X205	Description
1	DI0 input	2	DI8 input
3	DI1 input	4	DI9 input
5	DI2 input	6	DI10 input
7	DI3 input	8	DI11 input
9	DI4 input	10	DI12 input
11	DI5 input	12	DI13 input
13	DI6 input	14	DI14 input
15	DI7 input	16	DI15 input
17	CPU Vcc	18	+3V3
19	+5V	20	SGND

1.4.5 Location Of Module Jumpers And Connectors



Top View



Bottom View

1.5 Detailed Notes On Configuring The DIO54 Module For Use

1.5.1 DIO54 Compatibility

The DIO54 module has been designed as a universal module which can accept any processor modules designed for the EDP system. As such it is important to note that there are a few limitations which the user needs to be aware of. You must check that the DIO54 is correctly configured for your CPU before fitting it to the EDP baseboard!

1.5.2 Controlling The DIO54 Digital I/O Module

This module can be controlled by the CPU in several ways. On board the module are two independent serial I/O latch devices. Each of these devices has an input mode and an output mode function. The PCB has been designed such that one device is dedicated to output mode and the other device is dedicated for input mode. The chip used is the NXP PCA9555 device.

The PCA9555 device can be controlled via the I2C0 channel on the CPU via the back plane. This I2C0 channel is referred to as the CNTRL I2C channel on the Baseboard. Each of the two PCA9555 devices has its own unique I2C address to communicate on.

1.5.3 Digital Outputs

The PCA9555A device can be used to output data, the raw logic level output signals for this are referred to as OUT_P0(x) and OUT_P1(x) where x = 0 to7. These signals are available to probe on connector X203, and there are 16 logic level outputs in total. These raw logic level outputs **can** be fed into a high current Darlington driver of the type ULN2003. This however is a board option and the user has to configure the board to do this via a series of solder bridges. These bridges are B501-B508 and B602-B609. Check the board to ensure they are configured how you want them.

The Darlington drive output from the ULN2003 appears on another connector X202, as signal DO(y) where y = 0 to 15. Note the output drive of DO(0)-DO(11) is double that of DO(12)-DO(15), due to the way the hardware has been implemented.

The CPU also has some direct I/O capability and this feature is bought out onto the Baseboard. The Digital I/O Module has access to these signals and the user can use these rather than the signals produced by the I2C PCA9555 digital latches. On the Digital I/O Module these signals are referred to as EDP_DO(y) where y = 0 to 15.

The mapping between the CPU's port pins and the Output on the D0(y) pins is given later.

1.5.4 Digital Inputs

The Digital I/O Module can also read in external input signals via an input buffer. The real world signals are referred to as DI(y) where y = 0 to 15. Signals DI(0) to DI(11) have an input protection stage and hex Schmitt trigger inverting buffer input whilst signals DI(12) to DI(15) have a different input protection arrangement. There are no buffers or inversion of these signals.
The input signals after the protection stage can be routed via jumper links to either the serial input latches or to the STR9 MCU I/O pins. Jumpers J400 and J401 provide routing for 12 inputs DI(0) to DI(11) whilst input DI(12) to DI(15) have no routing capability and are fed directly into one of the PCA9555 serial latch device. The signals which are passed into the latches are referred to as IN_P0(x) and IN_P1(x) where x = 0 to 7, whilst the signals which pass directly into the MCU pins are referred to as EDP_DI(z) where z=0 to 11.

There is no problems at all when the devices are configured as serial latch input device, although it's worth noting that the same logic level when presented to DI(0) to DI(11) will read differently when presented to DI(12) to DI(15). This is because the DI(0) to DI(11) inputs have the Schmitt inverter in series with them.

When the link options are organised for direct input digital reading it's worth noting that there may be a share conflict with other modules that may require these I/O pins as output pins.

1.5.5 Mapping Of CPU Peripheral Pins To The Digital Module

The mapping of the various CPU modules to the backplane is different for each CPU Module. This means the digital IO Module appears slightly differently for each CM that is fitted. An example of the mapping is shown below for two CPU modules. The provided software allows for easy reading and writing of values to the Digital IO Module. The software is different for each Command Module.

XC167 Pin Allocation	STR9 Pin Allocation	EDP-AM-DIO54 Allocation
Vcc to BB	Vcc 3V3 or 5V, supplied by CM	Vcc 3V3 or 5V, supplied by CM
P3.5	P5.7	IRQ_GPIO18_I2C GEN0 INT
P3.2	P5.6	IRQ_GPIO16_CNTRL I2C INT
9 P6.2/CC2IO	P6.0	EDP_DO9
8 P6.1/CC1IO	P4.7	EDP_DO8
56 P2.15/CC15IO	P4.6	EDP_DO7
55 P2.14/CC14IO	P4.5	EDP_DO6
54 P2.13/CC13IO	P4.4	EDP_DO5
53 P2.12/CC12IO	P4.3	EDP_DO4
52 P2.11/CC11IO	P4.2	EDP_DO3
51 P2.10/CC10IO	P4.0	EDP_DO2
13 P6.6/CC6IO	P6.4	EDP_DO13
12 P6.5/CC5IO	P6.3	EDP_DO12
11 P6.3/CC4IO	P6.2	EDP_DO11
10 P6.3/CC3IO	P6.1	EDP_DO10
50 P2.9/CC9IO	P4.1	EDP_DO1
49 P2.8/CC8IO	P4.0	EDP_DO0
P3.7	P7.4	EDP_DI11
Digital GND	Digital GND	Digital GND
Vcc 5V from reg	5V from baseboard regulator	5V from baseboard regulator
Vcc 3V3 from reg	3V3 from baseboard regulator	3V3 from baseboard regulator
12V Power GND	12V Power GND	12V Power GND
12V Power GND	12V Power GND	12V Power GND
+12V 2A	+12V 2A	+12V 2A
+12V 2A	+12V 2A	+12V 2A

XC167 Pin Allocation	STR9 Pin Allocation	EDP-AM-DIO54 Allocation
Vcc to BB	Vcc 3V3 or 5V, supplied by CM	Vcc 3V3 or 5V, supplied by CM
24 P9.3/CC19IO	P4.0	NC
55 P2.14/CC14IO	P0.1	EDP_DO18
56 P2.15/CC15IO	P6.5	EDP_DO17
21 P9.0/CC16IO	P4.6	EDP_DO16
22 P9.1/CC17IO	P4.4	EDP_DO15
23 P9./2CC18IO	P4.2	EDP_DO14
131 P1H.4/CC24IO	P6.7	EDP_DI9
132 P1H.5/CC25IO	P6.6	EDP_DI8
133 P1H.6/CC26IO	P7.7	EDP_DI7
134 P1H.7/CC27IO	P7.6	EDP_DI6
15 P7.4/CC28IO	P7.3	EDP_DI5
16 P7.5/CC29IO	P7.2	EDP_DI4
17 P7.6/CC30IO	P7.1 (PHY disabled)	EDP_DI3
P7.7/CC31IO (CS8900A INT)	P7.0	EDP_DI2
124 P1L.7/CC22IO	P0.6 (PHY disabled)	EDP_DI10
124 P1L.7/CC22IO	P0.5 (PHY disabled)	EDP_DI1
127 P1H.0/CC23IO	P0.4 (PHY disabled)	EDP_DI0
Digital GND	Digital GND	Digital GND
Vcc 5V from reg	5V from baseboard regulator	5V from baseboard regulator
Vcc 3V3 from reg	3V3 from baseboard regulator	3V3 from baseboard regulator
12V Power GND	12V Power GND	12V Power GND
12V Power GND	12V Power GND	12V Power GND
+12V 2A	+12V 2A	+12V 2A
+12V 2A	+12V 2A	+12V 2A

XC167 Pin Allocation	STR9 Pin Allocation	EDP-AM-DIO54 Allocation
Vcc 5V from reg	Vcc 5V from reg	Vcc 5V from reg
Vcc 3V3 or 5V, supplied by CPU	Vcc 3V3 or 5V, supplied by CPU	Vcc 3V3 or 5V, supplied by CPU
Vcc 3V3 from reg	Vcc 3V3 from reg	Vcc 3V3 from reg
26 SCL2	P2.0	EDPCON2.79
25 SDA2	P2.1	EDPCON2.77
24 SCL1	P2.2	EDPCON2.7
23 SDA1	P2.3	EDPCON2.5
Digital GND	Digital GND	Digital GND

Note: The shaded signals are not available with certain CPU modules. These inputs and outputs are recommended to be connected to the appropriate I2C GPIO device rather than relying on the CPU's own port pins.

1.6 Setting The Jumpers And Solder Bridges

To make the Digital I/O Module compatible with direct MCU drive from the I/O pins the solder jumpers mentioned above, B501-B508 and B602-B609 need to be set accordingly. This means the user has the option to drive the output directly from the MCU's or via the PCA9555 serial latch depending on the jumper options.
In terms of compatibility with other modules it is worth noting that the STR9 has on board ADC. These ADC channels are on Port4, so there is a potentially conflicting situation when used with the Analogue Module. I.e. The analogue module will present analogue values to Port4 whilst Port4 is trying to drive

the Digital Module outputs. It is therefore prudent to reserve the Port4 pins for analogue input whilst using the Port6 pins for digital output. This means having some idea of what MCU system resources you will require in your design and modifying both the source code and the hardware to suite.

The low level hardware drivers may therefore need to be modified when mixing modules to avoid this potential conflict.

The Digital I/O Module can also read in external input signals via an input buffer. The real world signals are referred to as DI(y) where y = 0 to 15. Signals DI(0) to DI(11) have an input protection stage and hex Schmitt trigger inverting buffer input whilst signals DI(12) to DI(15) have a different input protection arrangement. There are no buffers or inversion of these signals.
The input signals after the protection stage can be routed via jumper links to either the serial input latches or to the STR9 MCU I/O pins. Jumpers J400 and J401 provide routing for 12 inputs DI(0) to DI(11) whilst input DI(12) to DI(15) have no routing capability and are fed directly into one of the PCA9555 serial latch device. The signals which are passed into the latches are referred to as IN_P0(x) and IN_P1(x) where x = 0 to 7, whilst the signals which pass directly into the MCU pins are referred to as EDP_DI(z) where z=0 to 11.

There is no problems at all when the devices are configured as serial latch input device, although it's worth noting that the same logic level when presented to DI(0) to DI(11) will read differently when presented to DI(12) to DI(15). This is because the DI(0) to DI(11) inputs have the Schmitt inverter in series with them.

When the link options are organised for direct input digital reading it's worth noting that there may be a share conflict with other modules that may require these I/O pins as output pins.

1.7 Digital IO Module Jumper Settings

Before fitting the DIO54 module to your EDP baseboard, you must configure the jumpers and solder bridges to suit the CPU module you are intending to use. The possible settings are given in the following table.

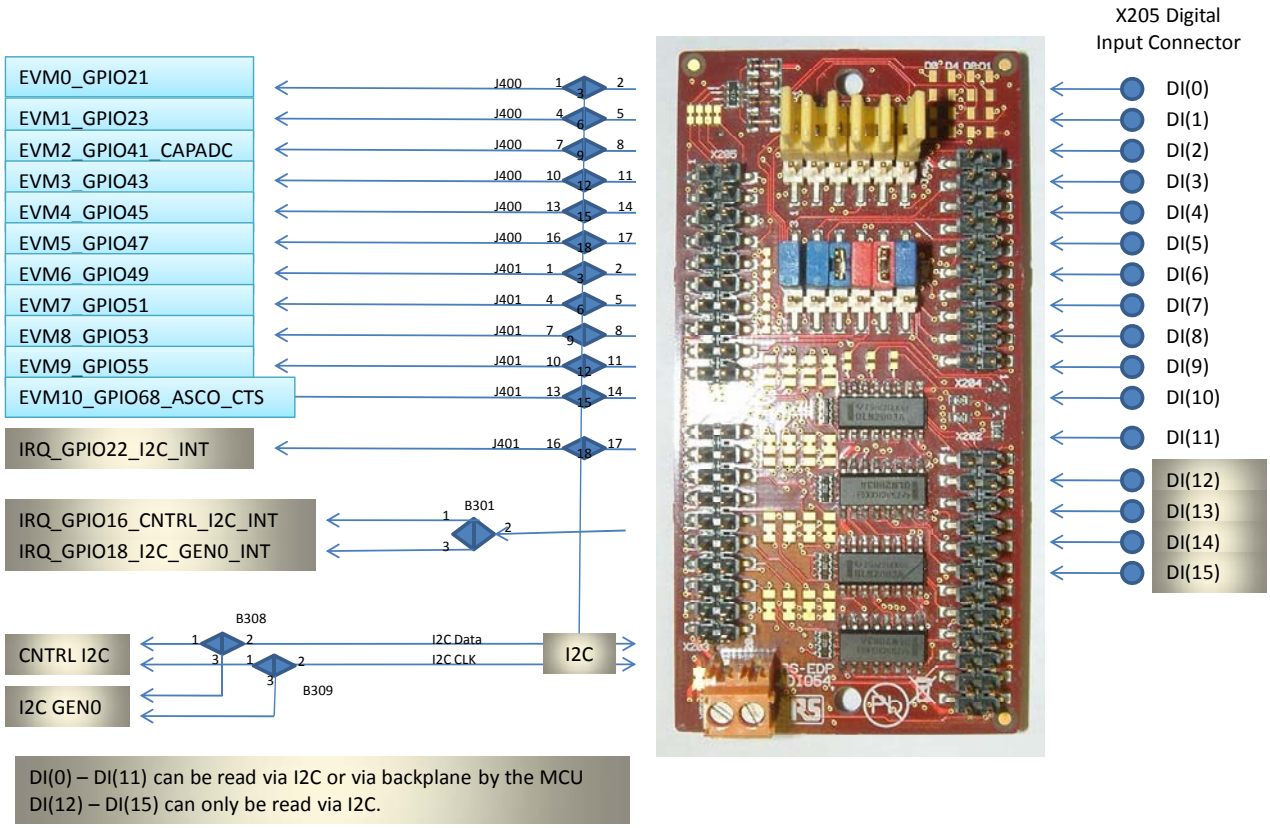
Jumper	Type	Purpose	Default State	Default
B300	Cut & Solder	Set operating voltage of I2C GPIO devices	Use CPU's Vcc	1-2
B301	Cut & Solder	Select which I2C channel interrupt to use with both I2C GPIO devices	I2C_CTRL INT	1-2
B302	Cut & Solder	Set address bit A0 for U300 (input) I2C GPIO device	A0=0	1-2
B303	Cut & Solder	Set address bit A1 for U300 (input) I2C GPIO device	A1=1	2-3
B304	Cut & Solder	Set address bit A2 for U300 (input) I2C GPIO device	A2=0	1-2
B305	Cut & Solder	Set address bit A0 for U301 (output) I2C GPIO device	A0=1	2-3
B306	Cut & Solder	Set address bit A1 for U301 (output) I2C GPIO device	A1=1	2-3
B307	Cut & Solder	Set address bit A2 for U301 (output) I2C GPIO device	A2=0	1-2
B308	Cut & Solder	Select I2C_CTRL bus or I2C GEN0 bus	I2C_CTRL	1-2
B309	Cut & Solder	Select I2C_CTRL bus or I2C GEN0 bus	I2C_CTRL	1-2
B310	Solder	Bypass PCA9306	Not Bypassed	Open
B311	Solder	Bypass PCA9306	Not Bypassed	Open
B312	Solder	Connect blue LED in RGB array to DO0	Not connected	Open
B313	Solder	Connect green LED in RGB array to DO0	Not connected	Open
B314	Solder	Connect red LED in RGB array to DO0	Not connected	Open
B400	Cut	Pull up DI0 digital input to DIO54 module	Pulled-up	Closed
B401	Cut	Pull up DI1 digital input to DIO54 module	Pulled-up	Closed
B402	Cut	Pull up DI2 digital input to DIO54 module	Pulled-up	Closed
B403	Cut	Pull up DI3 digital input to DIO54 module	Pulled-up	Closed
B404	Cut	Pull up DI4 digital input to DIO54 module	Pulled-up	Closed
B405	Cut	Pull up DI5 digital input to DIO54 module	Pulled-up	Closed
B406	Cut	Pull up DI6 digital input to DIO54 module	Pulled-up	Closed
B407	Cut	Pull up DI7 digital input to DIO54 module	Pulled-up	Closed
B408	Cut	Pull up DI8 digital input to DIO54 module	Pulled-up	Closed
B409	Cut	Pull up DI9 digital input to DIO54 module	Pulled-up	Closed
B410	Cut	Pull up DI10 digital input to DIO54 module	Pulled-up	Closed
B411	Cut	Pull up DI11 digital input to DIO54 module	Pulled-up	Closed
B412	Cut	Pull up DI12 digital input to DIO54 module	Pulled-up	Closed
B413	Cut	Pull up DI13 digital input to DIO54 module	Pulled-up	Closed
B414	Cut	Pull up DI14 digital input to DIO54 module	Pulled-up	Closed
B415	Cut	Pull up DI15 digital input to DIO54 module	Pulled-up	Closed

= CPU output option may not be available with all EDP CPU modules

Jumper	Type	Purpose	Default State	Default
B501	Cut & Solder	Connect ULN2003 input to either CPU output pin or U301 I2C GPIO device	CPU output	1-2
B502	Cut & Solder	Connect ULN2003 input to either CPU output pin or U301 I2C GPIO device	CPU output	1-2
B503	Cut & Solder	Connect ULN2003 input to either CPU output pin or U301 I2C GPIO device	CPU output	1-2
B504	Cut & Solder	Connect ULN2003 input to either CPU output pin or U301 I2C GPIO device	CPU output	1-2
B505	Cut & Solder	Connect ULN2003 input to either CPU output pin or U301 I2C GPIO device	CPU output	1-2
B506	Cut & Solder	Connect ULN2003 input to either CPU output pin or U301 I2C GPIO device	CPU output	1-2
B507	Cut & Solder	Connect ULN2003 input to either CPU output pin or U301 I2C GPIO device	CPU output	1-2
B508	Cut & Solder	Connect ULN2003 input to either CPU output pin or U301 I2C GPIO device	CPU output	1-2
B602	Cut & Solder	Connect ULN2003 input to either CPU output pin or U301 I2C GPIO device	CPU output	1-2
B603	Cut & Solder	Connect ULN2003 input to either CPU output pin or U301 I2C GPIO device	CPU output	1-2
B604	Cut & Solder	Connect ULN2003 input to either CPU output pin or U301 I2C GPIO device	CPU output	1-2
B605	Cut & Solder	Connect ULN2003 input to either CPU output pin or U301 I2C GPIO device	CPU output	1-2
B606	Cut & Solder	Connect ULN2003 input to either CPU output pin or U301 I2C GPIO device	CPU output	1-2
B607	Cut & Solder	Connect ULN2003 input to either CPU output pin or U301 I2C GPIO device	CPU output	1-2
B608	Cut & Solder	Connect ULN2003 input to either CPU output pin or U301 I2C GPIO device	CPU output	1-2
B609	Cut & Solder	Connect ULN2003 input to either CPU output pin or U301 I2C GPIO device	CPU output	1-2
J400A	Jumper	Route DI0 input to CPU digital input pin via EDP or to I2C GPIO U300	Use CPU input	1-2
J400B	Jumper	Route DI0 input to CPU digital input pin via EDP or to I2C GPIO U300	Use CPU input	1-2
J400C	Jumper	Route DI0 input to CPU digital input pin via EDP or to I2C GPIO U300	Use CPU input	1-2
J400D	Jumper	Route DI0 input to CPU digital input pin via EDP or to I2C GPIO U300	Use CPU input	1-2
J400E	Jumper	Route DI0 input to CPU digital input pin via EDP or to I2C GPIO U300	Use CPU input	1-2
J400F	Jumper	Route DI0 input to CPU digital input pin via EDP or to I2C GPIO U300	Use CPU input	1-2
J401A	Jumper	Route DI0 input to CPU digital input pin via EDP or to I2C GPIO U300	Not fitted	Open
J401B	Jumper	Route DI0 input to CPU digital input pin via EDP or to I2C GPIO U300	Not fitted	Open
J401C	Jumper	Route DI0 input to CPU digital input pin via EDP or to I2C GPIO U300	Not fitted	Open
J401D	Jumper	Route DI0 input to CPU digital input pin via EDP or to I2C GPIO U300	Not fitted	Open
J401E	Jumper	Route DI0 input to CPU digital input pin via EDP or to I2C GPIO U300	Not fitted	Open
J401F	Jumper	Route DI0 input to CPU digital input pin via EDP or to I2C GPIO U300	Not fitted	Open

= CPU output option may not be available with all EDP CPU modules

DIO54 - Digital I/O Module Inputs to RS-EDP Backplane



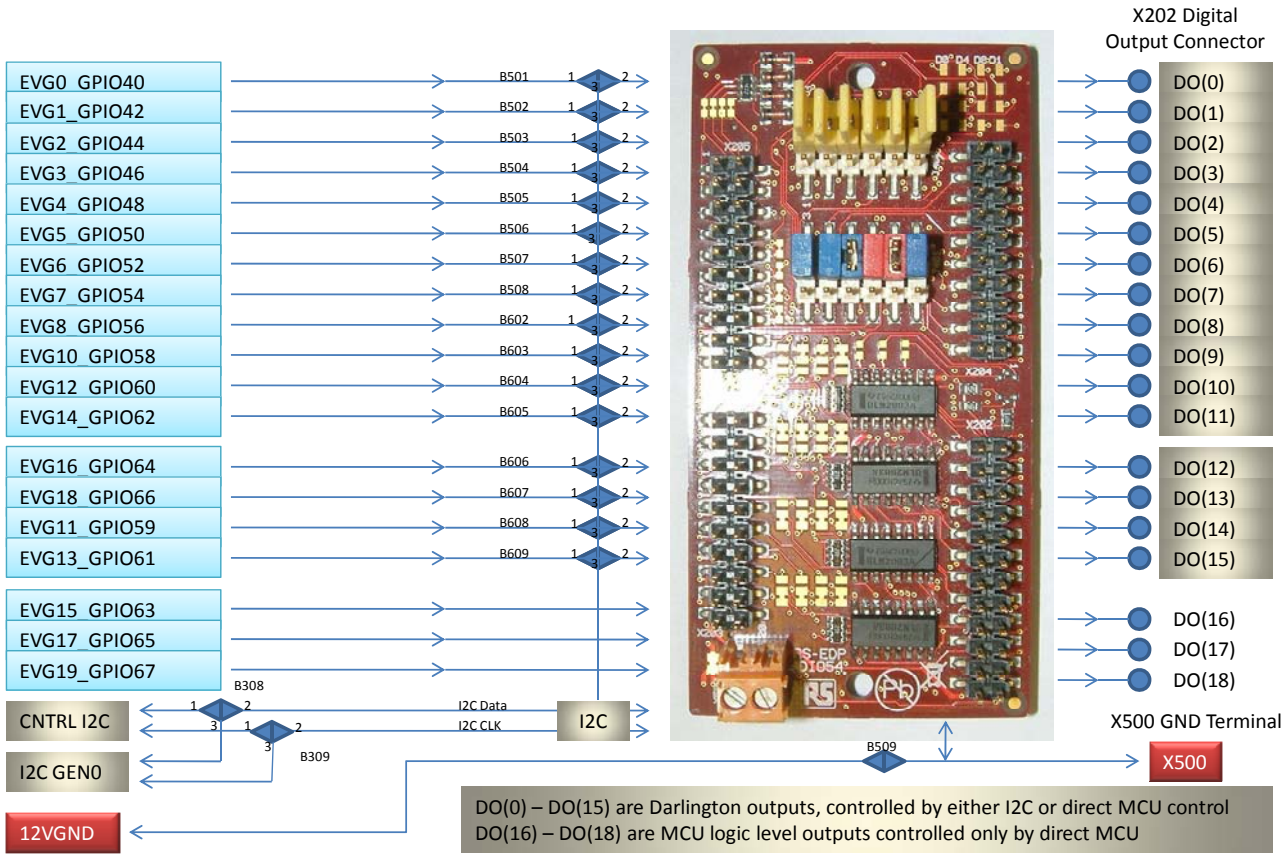
Mapping Aid summary of Digital Input jumpers and IO configuration

You can see from this diagram that inputs DI(0) to DI(15) provide the digital input pins to the system. The processed inputs are then made available on the backplane via the link options marked above as a diamond. If the inputs are required to be read via the I2C bus then the link can be set differently. DI(12) to DI(15) can only be read via the back plane and no I2C read option is available to them.

The I2C interface can be selected as either CNTRL_I2C, which is the main I2C bus within the RS-EDP system or via the I2C_GEN0 bus which is usually provided as the user own I2C independent I2C bus. Not all CMs have two I2C channels so the default is usually CNTRL_I2C. Software drivers are provided for all the CMs to talk to the Digital IO Modules over the I2C protocol.

The I2C device can generate an interrupt if required. The user can select this interrupt source via the link options shown above.

DIO54 - Digital I/O Module Outputs to RS-EDP Backplane



Mapping Aid summary of Digital Output jumpers and IO configuration

As you can see from the diagram above the Digital IO Module can be fed with output data either directly from the back plane signals EVG0 to EVG19 or via I2C packets from the I2C buses. The user can select which of these two he wishes to use via the link options shown in the diamonds above.

The diagram shows the same I2C bus interface which can be selected to be the same as the input module. i.e. CNTRL_I2C or I2C_GEN0
Note also the large X500 ground terminal which can be used to terminate large high current switching loads. As the backplane connections are only rated for up to 2A, for higher current loads the user should connect the high side load to the IO pin and use the X500 ground terminal for the return current from the load.

Software drivers are provided for each CM to talk directly to the Digital IO Outputs both by I2C and also by direct MCU port control.

EDP Digital I/O Module

RS-EDP-DIO54-A1

Rev.	Date	Name
1	06.03.2008	Ar

hitex
DEVELOPMENT TOOLS

Title: Contents

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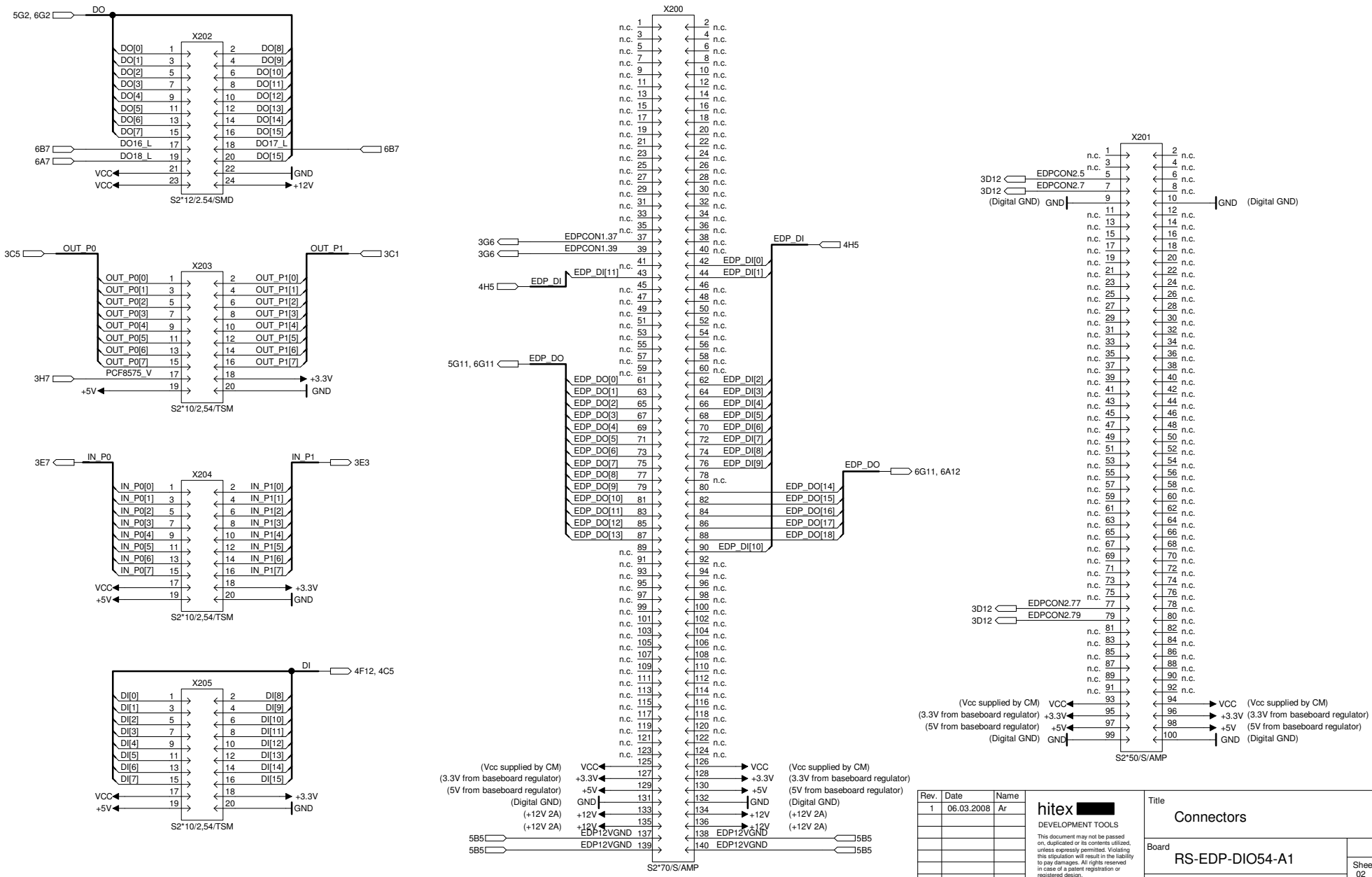

Rev.	Date	Name
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DEVELOPMENT TOOLS

Title: Connectors

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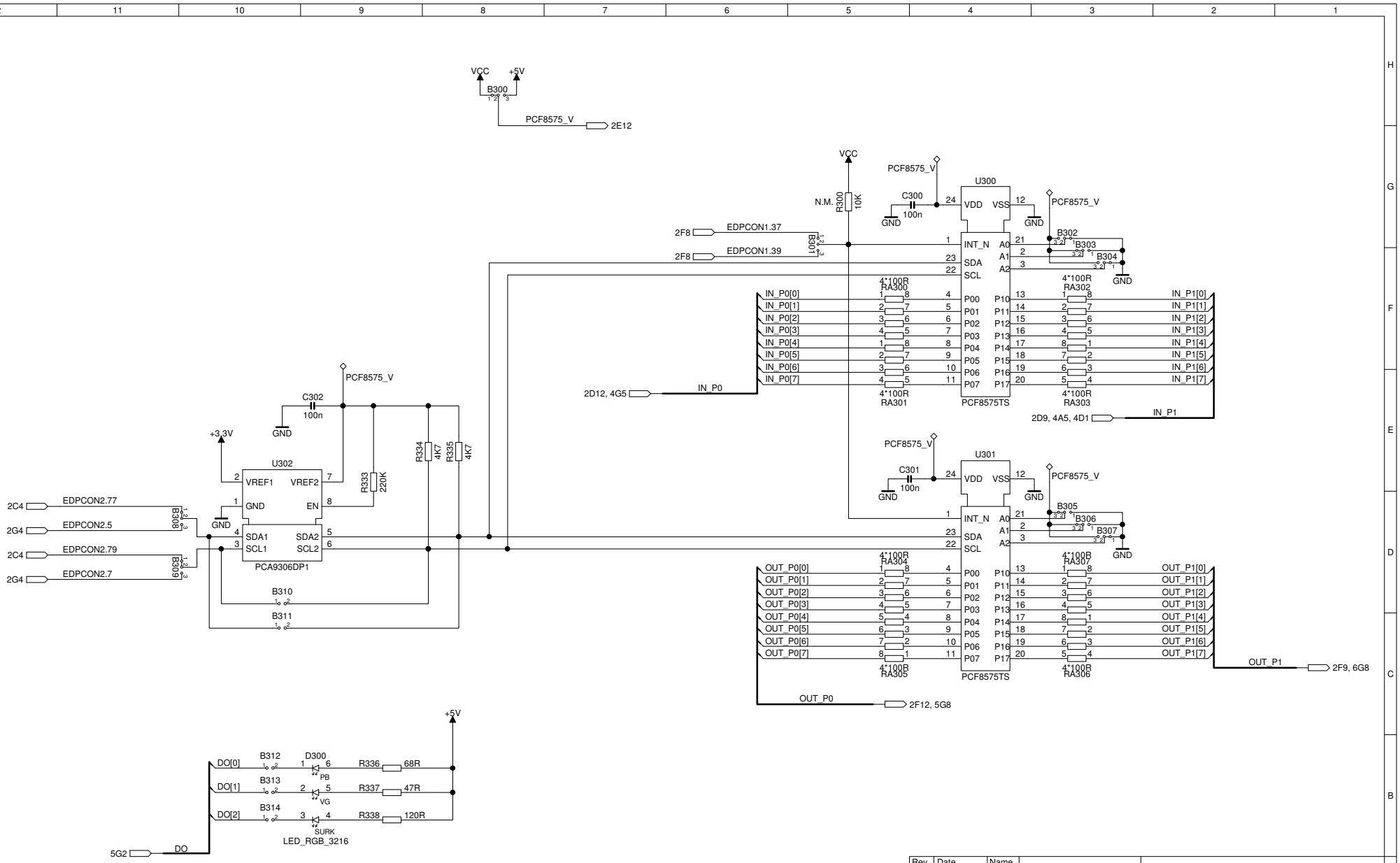

Rev.	Date	Name
1	06.03.2008	Ar

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DEVELOPMENT TOOLS

Title: I2C to 16bit Bus; LEDs

Board: RS-EDP-DIO54-A1

File modified 02.04.2008 15:40:00

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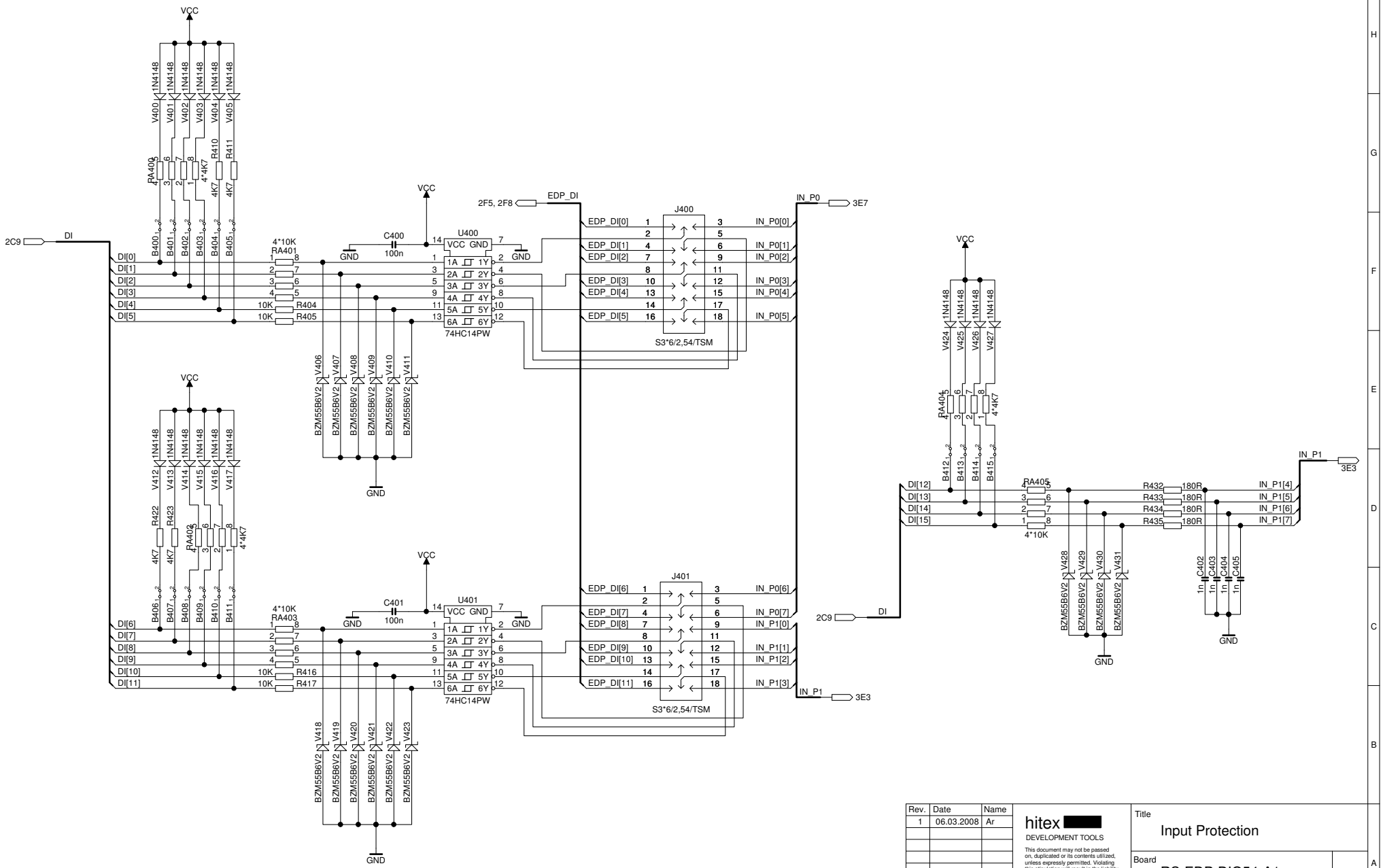


Rev.	Date	Name
1	06.03.2008	Ar

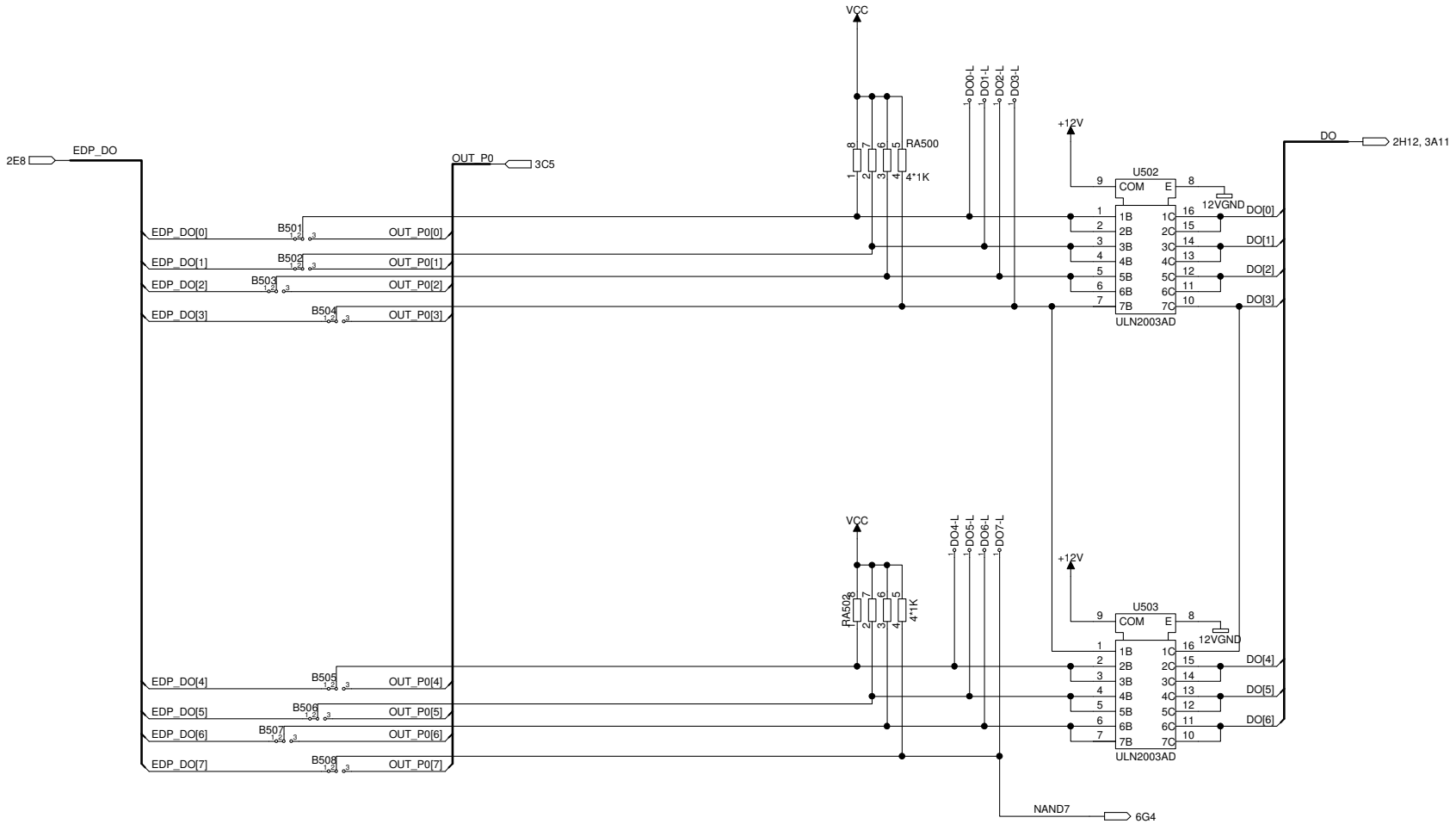
hitex
DEVELOPMENT TOOLS

Title
Input Protection

Board
RS-EDP-DIO54-A1

File modified 02.04.2008 15:40:00

Sheet 04 of 06



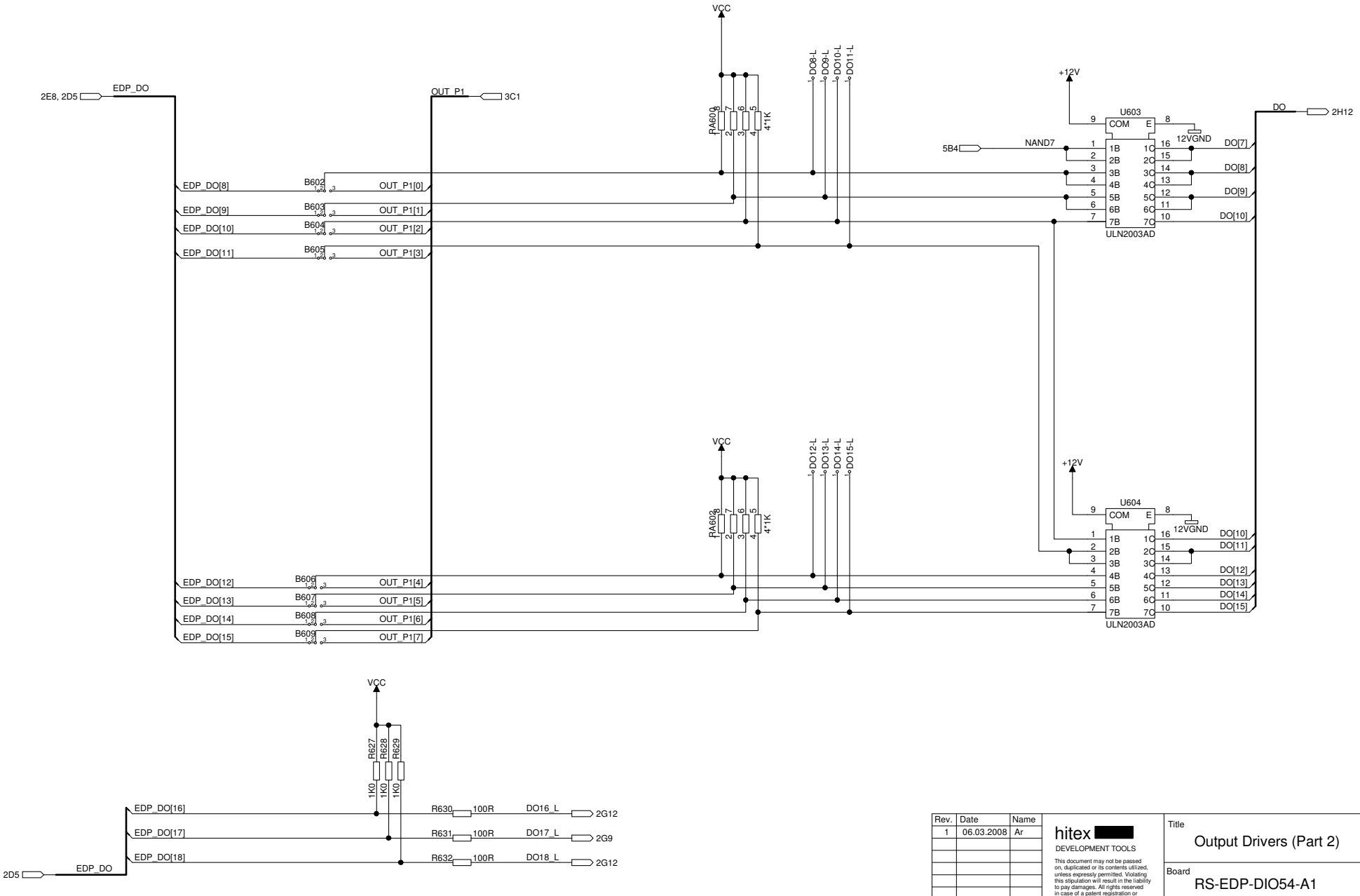
Rev.	Date	Name
1	06.03.2008	Ar

hitex
DEVELOPMENT TOOLS

Title
Output Drivers (Part 1)

Board
RS-EDP-DIO54-A1

File modified 02.04.2008 15:40:00



Rev.	Date	Name
1	06.03.2008	Ar

hitex DEVELOPMENT TOOLS

Title: Output Drivers (Part 2)

Board: RS-EDP-DIO54-A1

File modified 02.04.2008 15:40:00

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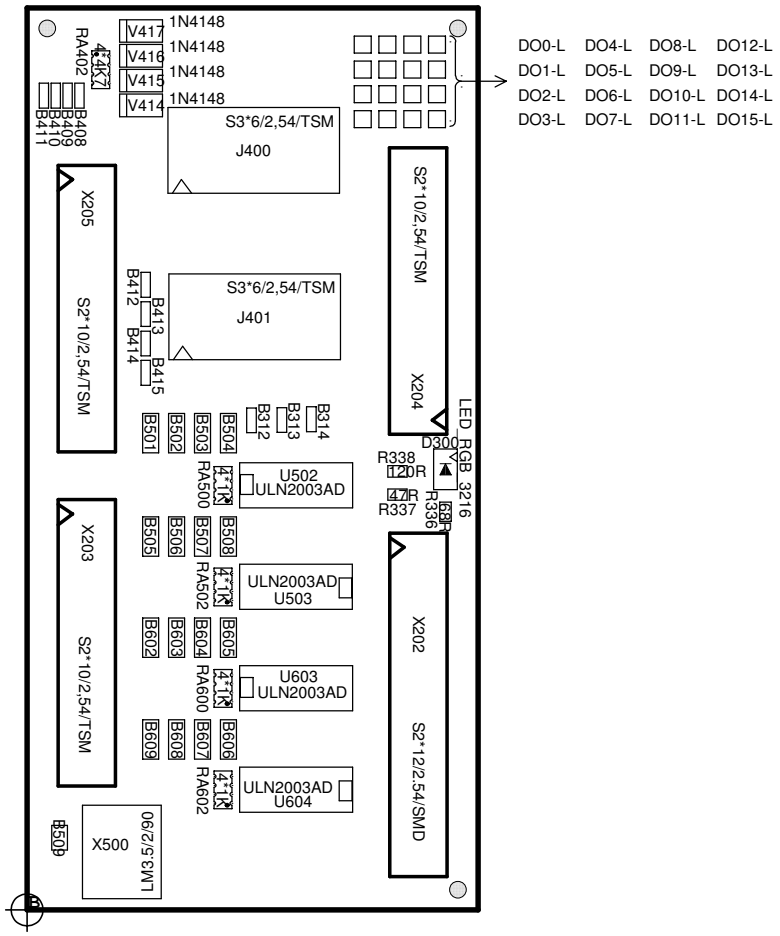
Assembly Plan Top



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Module	:	RS-EDP-DIO54-A1	Document	:	BPL
Status	:	1	Usage	:	external
Date / Name	:	02.04.2008 / Ar	Page	:	1/2

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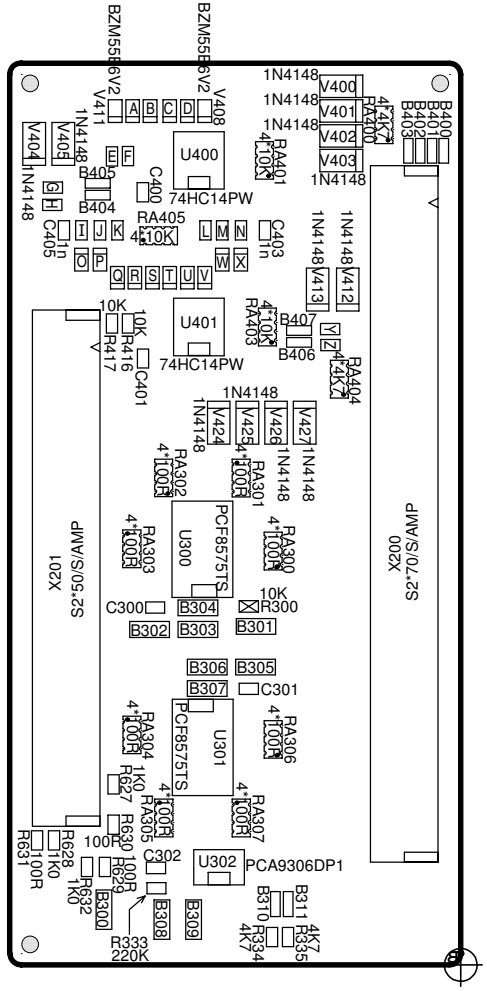
Assembly Plan Bottom



A: V410 BZM55B6V2
B: V409 BZM55B6V2
C: V406 BZM55B6V2
D: V407 BZM55B6V2
E: R405 10K
F: R404 10K
G: R411 4K7
H: R410 4K7
I: R435 180R
J: R434 180R
K: C404 1n
L: C402 1n
M: R432 180R
N: R433 180R
O: V431 BZM55B6V2
P: V430 BZM55B6V2
Q: V423 BZM55B6V2
R: V422 BZM55B6V2
S: V421 BZM55B6V2
T: V418 BZM55B6V2
U: V419 BZM55B6V2
V: V420 BZM55B6V2
W: V428 BZM55B6V2
X: V429 BZM55B6V2
Y: R423 4K7
Z: R422 4K7

All capacitors without value indication: 100n

Directory	:	EDP Modules	Variant	:	--
Module	:	RS-EDP-DIO54-A1	Document	:	BPL
Status	:	1	Usage	:	external
Date / Name	:	02.04.2008 / Ar	Page	:	2/2

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