

ZXMC3AM832

MPPS™ Miniature Package Power Solutions COMPLEMENTARY 30V ENHANCEMENT MODE MOSFET

SUMMARY

N-Channel $V_{(BR)DSS} = 30V$; $R_{DS(ON)} = 0.12\Omega$; $I_D = 3.7A$

P-Channel $V_{(BR)DSS} = -30V$; $R_{DS(ON)} = 0.21\Omega$; $I_D = -2.7A$

DESCRIPTION

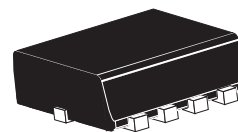
Packaged in the new innovative 3mm x 2mm MLP (Micro Leaded Package) outline this dual 30V N channel Trench MOSFET utilizes a unique structure combining the benefits of Low on-resistance with fast switching speed. This makes them ideal for high efficiency, low voltage power management applications. Users will also gain several other **key benefits**:

Performance capability equivalent to much larger packages

Improved circuit efficiency & power levels

PCB area and device placement savings

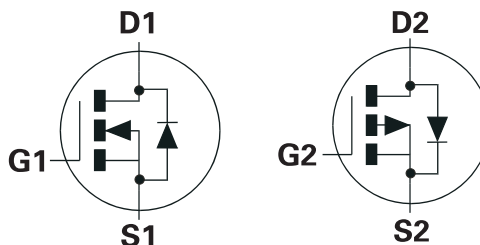
Reduced component count



3mm x 2mm Dual Die MLP

FEATURES

- Low on - resistance
- Fast switching speed
- Low threshold
- Low gate drive
- 3mm x 2mm MLP



APPLICATIONS

- MOSFET gate drive
- LCD backlight inverters
- Motor control

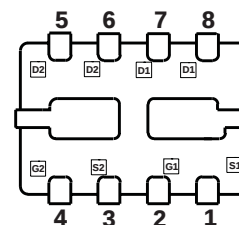
ORDERING INFORMATION

DEVICE	REEL	TAPE WIDTH	QUANTITY PER REEL
ZXMC3AM832TA	7"	8mm	3000 units
ZXMC3AM832TC	13"	8mm	10000 units

DEVICE MARKING

C01

PINOUT



3 x 2 Dual MLP
underside view

ZXMC3AM832

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	N-Channel	P-Channel	UNIT
Drain-Source Voltage	V_{DSS}	30	-30	V
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Continuous Drain Current @ $V_{GS}=10V$; $T_A=25^\circ C$ ^{(b)(f)}	I_D	3.7	-2.7	A
@ $V_{GS}=10V$; $T_A=25^\circ C$ ^{(b)(f)}		3.0	-2.2	A
@ $V_{GS}=10V$; $T_A=25^\circ C$ ^{(a)(f)}		2.9	-2.1	A
Pulsed Drain Current	I_{DM}	12.4	-9.2	A
Continuous Source Current (Body Diode) ^{(b)(f)}	I_S	2.4	-2.8	A
Pulsed Source Current (Body Diode)	I_{SM}	12.4	-9.2	A
Power Dissipation at $T_A=25^\circ C$ ^{(a)(f)}	P_D	1.5		W
Linear Derating Factor		12		mW/°C
Power Dissipation at $T_A=25^\circ C$ ^{(b)(f)}	P_D	2.45		W
Linear Derating Factor		19.6		mW/°C
Power Dissipation at $T_A=25^\circ C$ ^{(c)(f)}	P_D	1		W
Linear Derating Factor		8		mW/°C
Power Dissipation at $T_A=25^\circ C$ ^{(d)(f)}	P_D	1.13		W
Linear Derating Factor		8		mW/°C
Power Dissipation at $T_A=25^\circ C$ ^{(d)(g)}	P_D	1.7		W
Linear Derating Factor		13.6		mW/°C

THERMAL RESISTANCE

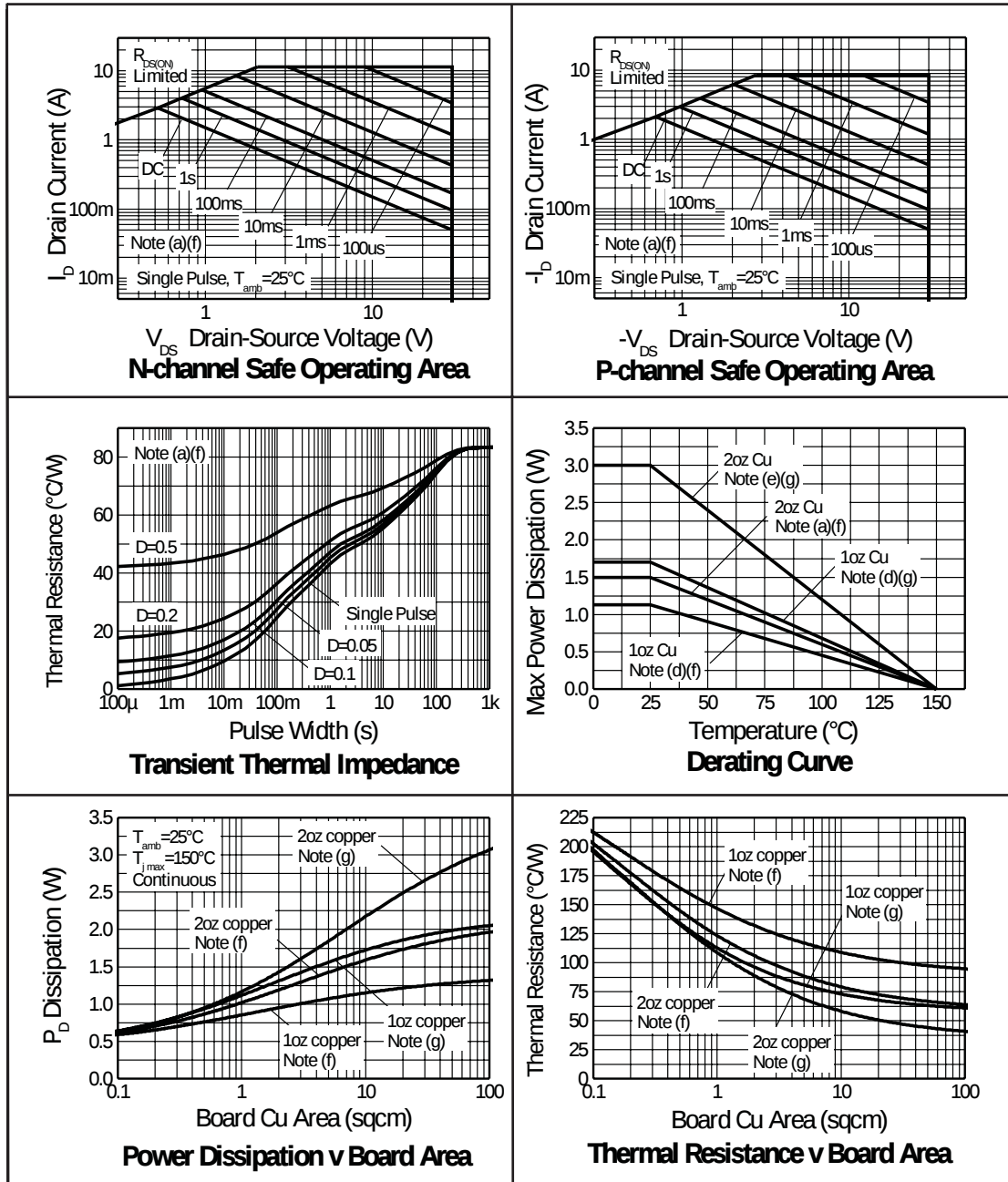
PARAMETER	SYMBOL	VALUE	UNIT
Junction to Ambient ^{(a)(f)}	$R_{\theta JA}$	83.3	°C/W
Junction to Ambient ^{(b)(f)}	$R_{\theta JA}$	51	°C/W
Junction to Ambient ^{(c)(f)}	$R_{\theta JA}$	125	°C/W
Junction to Ambient ^{(d)(f)}	$R_{\theta JA}$	111	°C/W
Junction to Ambient ^{(d)(g)}	$R_{\theta JA}$	73.5	°C/W
Junction to Ambient ^{(e)(g)}	$R_{\theta JA}$	41.7	°C/W

Notes

- (a) For a dual device surface mounted on 8 sq cm single sided 2oz copper on FR4 PCB, in still air conditions **with all exposed pads attached**. The copper are is split down the centre line into two separate areas with one half connected to each half of the dual device.
- (b) Measured at $t < 5$ secs for a dual device surface mounted on 8 sq cm single sided 2oz copper on FR4 PCB, in still air conditions **with all exposed pads attached**. The copper are is split down the centre line into two separate areas with one half connected to each half of the dual device.
- (c) For a dual device surface mounted on 8 sq cm single sided 2oz copper on FR4 PCB, in still air conditions **with minimal lead connections only**.
- (d) For a dual device surface mounted on 10 sq cm single sided 1oz copper on FR4 PCB, in still air conditions **with all exposed pads attached**. The copper are is split down the centre line into two separate areas with one half connected to each half of the dual device.
- (e) For a dual device surface mounted on 85 sq cm single sided 2oz copper on FR4 PCB, in still air conditions **with all exposed pads attached**. The copper are is split down the centre line into two separate areas with one half connected to each half of the dual device.
- (f) For a dual device with one active die.
- (g) For dual device with 2 active die running at equal power.
- (h) Repetitive rating - pulse width limited by max junction temperature. Refer to Transient Thermal Impedance graph.
- (i) The minimum copper dimensions required for mounting are no smaller than the exposed metal pads on the base if the device as shown in the package dimensions data. The thermal resistance for a dual device mounted on 1.5mm thick FR4 board using minimum copper 1 oz weight, 1mm wide tracks and one half of the device active is $R_{th} = 250^\circ C/W$ giving a power rating of $P_{tot} = 500mW$.

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TYPICAL CHARACTERISTICS



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N-CHANNEL

ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	30			V	I _D =250μA, V _{GS} =0V
Zero Gate Voltage Drain Current	I _{DSS}			0.5	μA	V _{DS} =30V, V _{GS} =0V
Gate-Body Leakage	I _{GSS}			100	nA	V _{GS} =±20V, V _{DS} =0V
Gate-Source Threshold Voltage	V _{GS(th)}	1			V	I _D =250μA, V _{DS} = V _{GS}
Static Drain-Source On-State Resistance ⁽¹⁾	R _{DS(on)}		0.106	0.12 0.18	Ω Ω	V _{GS} =10V, I _D =2.5A V _{GS} =4.5V, I _D =2.0A
Forward Transconductance ⁽¹⁾⁽³⁾	g _{fs}		3.5		S	V _{DS} =4.5V,I _D =2.5A
DYNAMIC ⁽³⁾						
Input Capacitance	C _{iss}		190		pF	V _{DS} =25 V, V _{GS} =0V, f=1MHz
Output Capacitance	C _{oss}		38		pF	
Reverse Transfer Capacitance	C _{rss}		20		pF	
SWITCHING ^{(2) (3)}						
Turn-On Delay Time	t _{d(on)}		1.7		ns	V _{DD} =15V, I _D =2.5A R _G =6.0Ω, V _{GS} =10V
Rise Time	t _r		2.3		ns	
Turn-Off Delay Time	t _{d(off)}		6.6		ns	
Fall Time	t _f		2.9		ns	
Gate Charge	Q _g		2.3		nC	V _{DS} =15V,V _{GS} =5V, I _D =2.5A
Total Gate Charge	Q _g		3.9		nC	V _{DS} =15V,V _{GS} =10V, I _D =2.5A
Gate-Source Charge	Q _{gs}		0.6		nC	
Gate-Drain Charge	Q _{gd}		0.9		nC	
SOURCE-DRAIN DIODE						
Diode Forward Voltage ⁽¹⁾	V _{SD}		0.85	0.95	V	T _J =25°C, I _S =1.7A, V _{GS} =0V
Reverse Recovery Time ⁽³⁾	t _{rr}		17.7		ns	T _J =25°C, I _F =2.5A, di/dt= 100A/μs
Reverse Recovery Charge ⁽³⁾	Q _{rr}		13.0		nC	

NOTES

(1) Measured under pulsed conditions. Width $\leq 300\mu\text{s}$. Duty cycle $\leq 2\%$.

(2) Switching characteristics are independent of operating junction temperature.

(3) For design aid only, not subject to production testing.

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P-CHANNEL

ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	-30			V	I _D =-250μA, V _{GS} =0V
Zero Gate Voltage Drain Current	I _{DSS}			1	μA	V _{DS} =-30V, V _{GS} =0V
Gate-Body Leakage	I _{GSS}			100	nA	V _{GS} =±20V, V _{DS} =0V
Gate-Source Threshold Voltage	V _{GS(th)}	-0.8			V	I _D =-250μA, V _{DS} = V _{GS}
Static Drain-Source On-State Resistance ⁽¹⁾	R _{DS(on)}			0.210 0.330	Ω Ω	V _{GS} =-10V, I _D =-1.4A V _{GS} =-4.5V, I _D =-1.1A
Forward Transconductance ⁽¹⁾⁽³⁾	g _{fs}		2.48		S	V _{DS} =-15V,I _D =-1.4A
DYNAMIC ⁽³⁾						
Input Capacitance	C _{iss}		204		pF	V _{DS} =-15 V, V _{GS} =0V, f=1MHz
Output Capacitance	C _{oss}		39.8		pF	
Reverse Transfer Capacitance	C _{rss}		25.8		pF	
SWITCHING ^{(2) (3)}						
Turn-On Delay Time	t _{d(on)}		1.5		ns	V _{DD} =-15V, I _D =-1A R _G =6.0Ω, V _{GS} =-10V
Rise Time	t _r		2.8		ns	
Turn-Off Delay Time	t _{d(off)}		11.3		ns	
Fall Time	t _f		7.5		ns	
Gate Charge	Q _g		2.58		nC	V _{DS} =-15V,V _{GS} =-5V, I _D =-1.4A
Total Gate Charge	Q _g		5.15		nC	V _{DS} =-15V,V _{GS} =-10V, I _D =-1.4A
Gate-Source Charge	Q _{gs}		0.65		nC	
Gate-Drain Charge	Q _{gd}		0.92		nC	
SOURCE-DRAIN DIODE						
Diode Forward Voltage ⁽¹⁾	V _{SD}		-0.85	-0.95	V	T _J =25°C, I _S =-1.1A, V _{GS} =0V
Reverse Recovery Time ⁽³⁾	t _{rr}		18.6		ns	T _J =25°C, I _F =-0.95A, di/dt= 100A/μs
Reverse Recovery Charge ⁽³⁾	Q _{rr}		14.8		nC	

NOTES

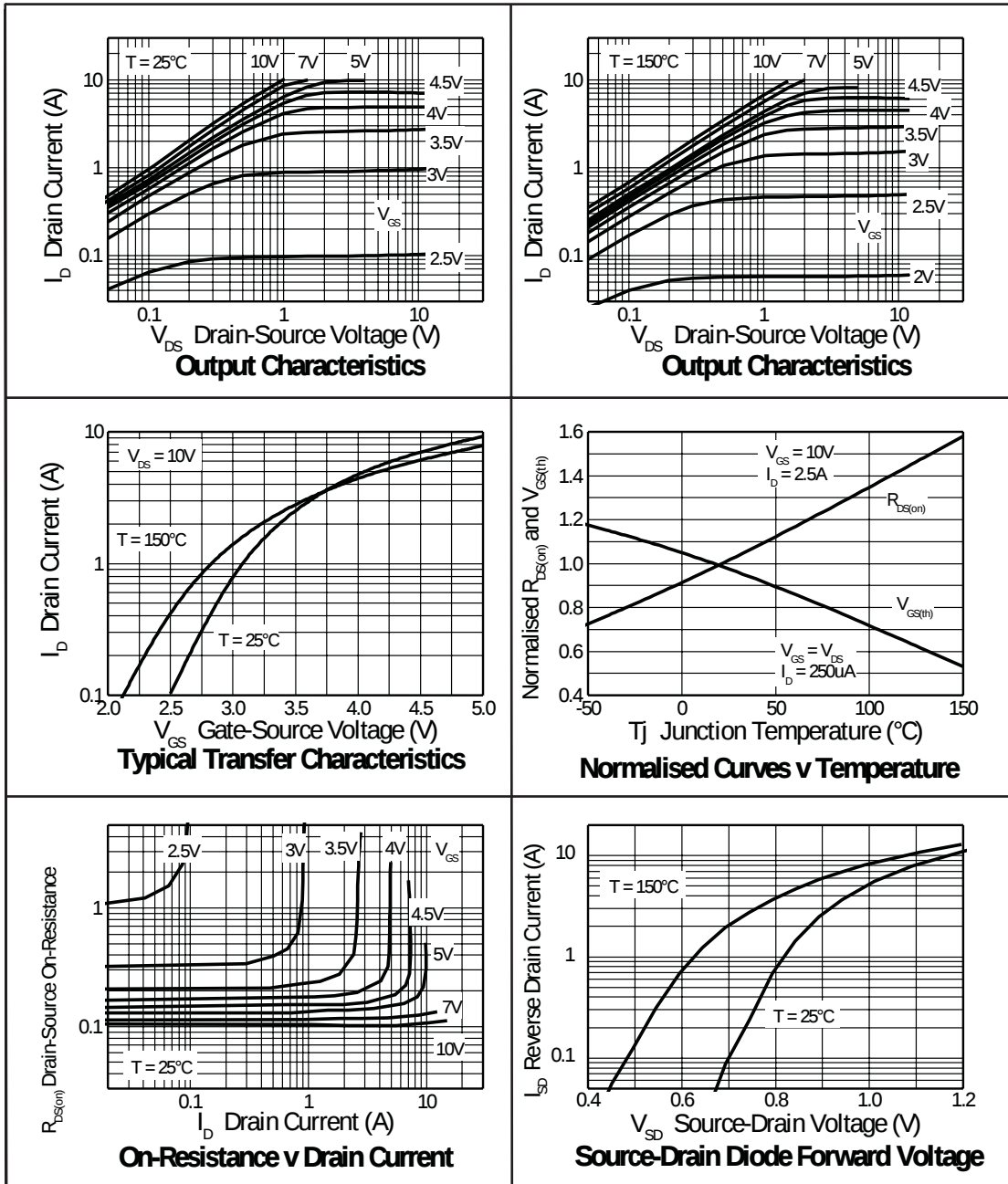
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(2) Switching characteristics are independent of operating junction temperature.

(3) For design aid only, not subject to production testing.

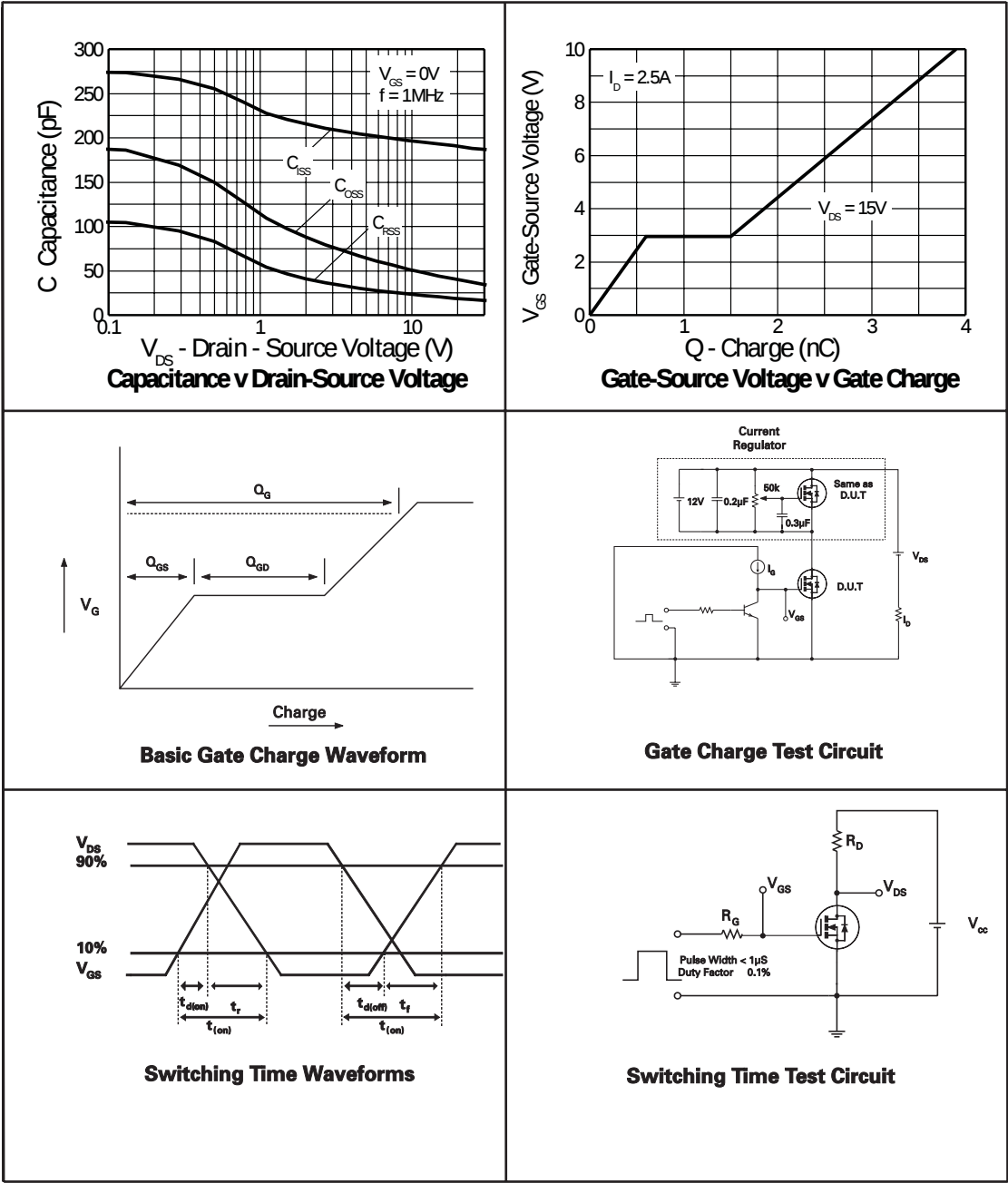
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N-CHANNEL TYPICAL CHARACTERISTICS



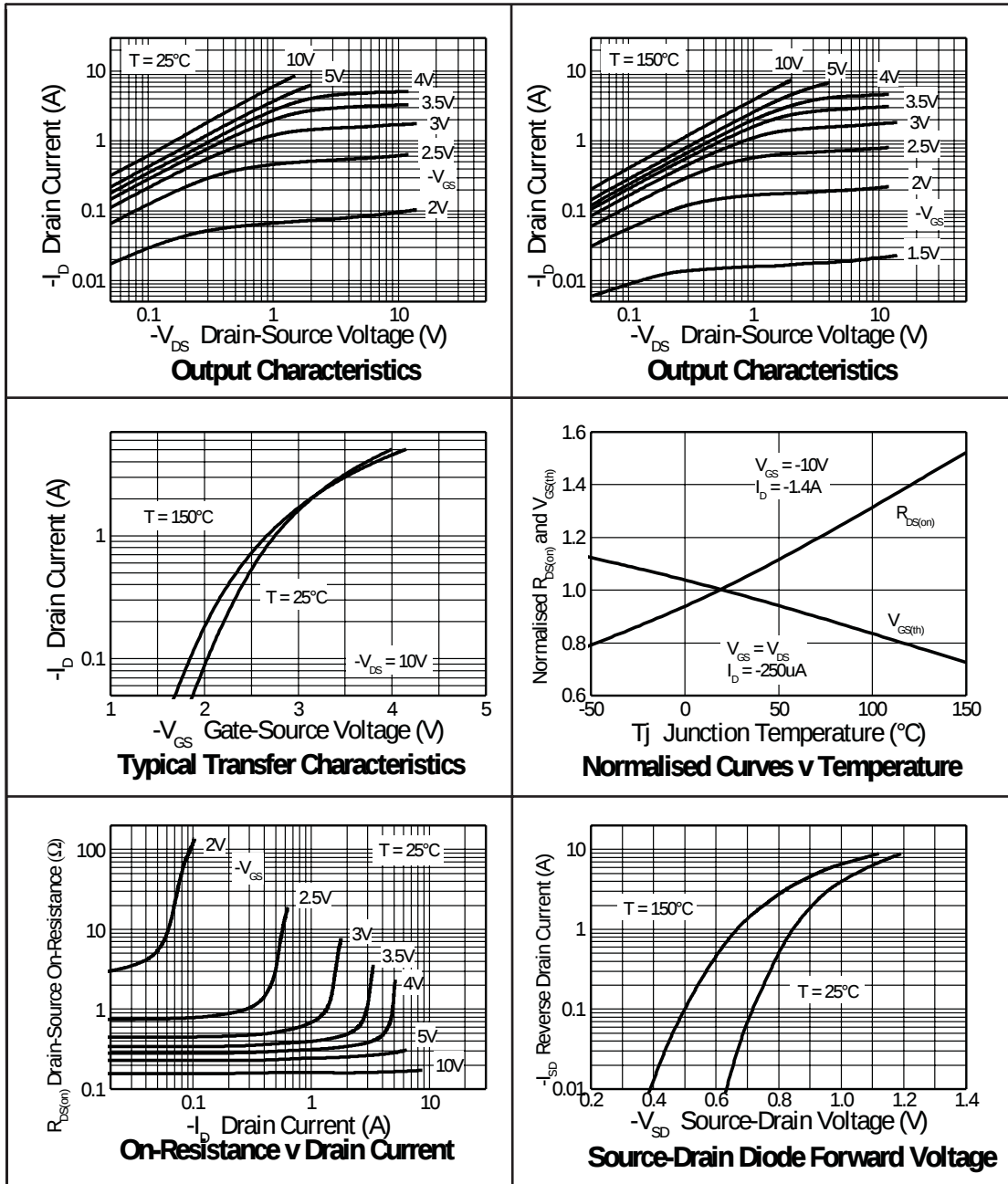
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N-CHANNEL TYPICAL CHARACTERISTICS



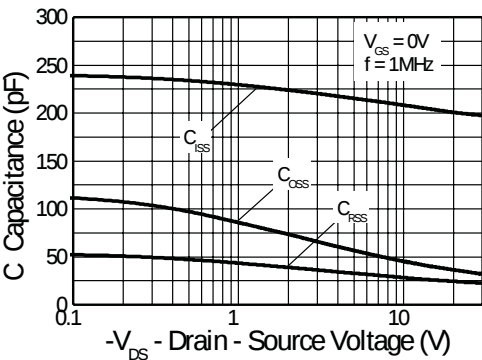
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P-CHANNEL TYPICAL CHARACTERISTICS

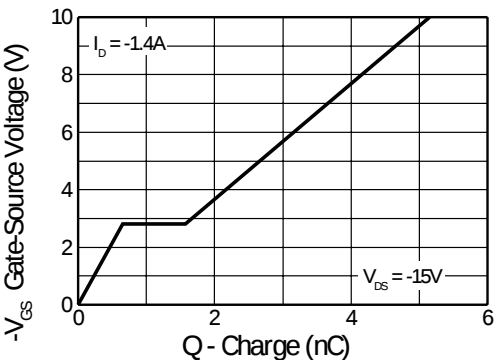


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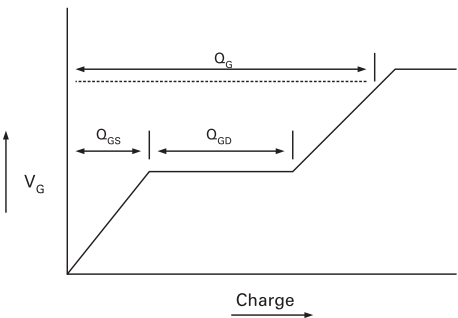
P-CHANNEL TYPICAL CHARACTERISTICS



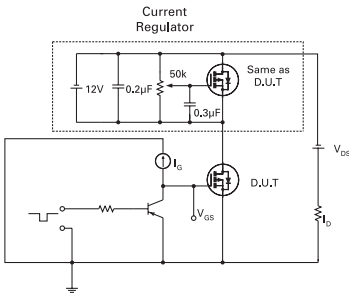
Capacitance v Drain-Source Voltage



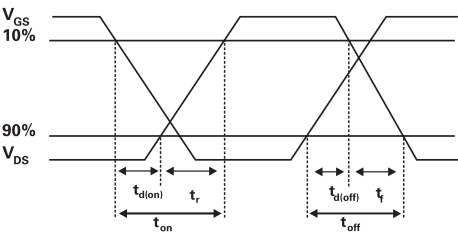
Gate-Source Voltage v Gate Charge



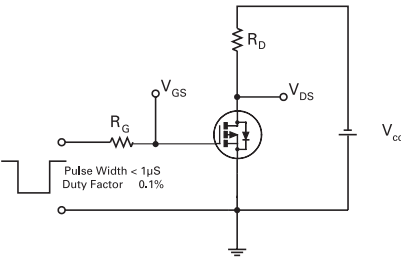
Basic Gate Charge Waveform



Gate Charge Test Circuit



Switching Time Waveforms



Switching Time Test Circuit

