TI德州仪器无线链接产品数据手册

CC2540

TEXAS INSTRUMENTS

信驰达简介

信驰达科技（RF-star）是一家集合方案设计功能和核心器件供应的专业本地电子元器件分销商，专注低功耗射频 LPRF 和低功耗 MCU 领域，公司成立于2010年，作为中国区唯一具有美国 TI 公司授予的 LPRF Product Reseller 和 Third Party 双重资质的公司，一直引领着 LPRF 技术在国内的推广和应用，是国内唯一一家可提供 LPRF 软硬件产品、技术支持、解决方案和核心元器件供应一条龙服务的专业化公司；

公司在美国新泽西州、中国深圳、上海、北京、天津、无锡、长沙、成都、重庆设有研发中心和办事处，拥有资深的技术研发团队和销售团队以及 SMT 生产工厂。

无线射频器件用于低于1GHz 和2.4GHz 频段、ANT、蓝牙(Bluetooth)、低功耗蓝牙、射频识别（RFID）、PurePath 无线音频、ZigBee、IEEE802.15.4、Zigbee RF4CE、6LoWPAN、Wi-Fi 的射频集成电路(RF IC)和专有协议。

产品市场应用：ZigBee 无线传感网络，各种数据采集及遥测监控(含数据, 语音,图像等),可应用于安防、医疗、能源、水力、电力、交通监控、防盗，无线自动抄表；仪器仪表远程数据遥测、工业无线遥控；消防安全自动报警、煤矿安全监控及人员定位；汽车防盗、胎压检测，四轮定位；无线键盘、鼠标、打印机、游戏杆、遥控玩具、机器人等广泛的领域。适用于合乎全世界免费频段315MHz、433 MHz、470MHz、868 MHz、915 MHz、2.4GHz，符合 FCC、CE、SGS、RoHs 认证规范,产品和信誉受到国内外顾客的一致好评。

RF-star 将一如既往，为客户提供更多、更好的产品，更具优势的技术服务，良好的商务服务，和更完善的物流服务。RF-star 将跨上一个新的平台，获得更大的发展空间。RF-star 将继续本着“务实、诚信、学习、创新”的专业精神，团结一致、奋勇开拓、锐意进取，为成为全球无线射频技术绝对第一之产品、服务及解决方案提供者，把科技与客户联系在一起，为供应链注入动力，并提供卓越的投资回报而不懈努力。

如果您在产品开发过程中发现技术难题以及高频困扰，竭诚欢迎来电洽询。我们将为您提供技术支持和解决方案，让您能更快把产品推向市场。

我们深信射频技术将会得到迅速的发展与普及，我们愿意分享多年来在射频行业积累的经验与教训，为无线的明天做出贡献。专业源于专注，科技铸就未来。

重要特性：

- 真正的低功耗蓝牙片上系统解决方案：CC2540 集合低功耗蓝牙协议栈，包括外设接口和广泛的传感器等。
- 封装 6mm *6mm
- RF 部分

— 蓝牙低功耗兼容技术

— 出色的链路预算（高达 97dB）,支持无外部前段的远程应用

— 精确的数据接收信号强度检测（RSSI）

— 适用于针对世界范围内的无线电频率调节系统，规则：ETSI EN 300 328 ,EN 300 440 2 类（欧洲），FCC CFR47 15 部分(美国),ARIB STD-T66(日本)

- 布局

— 很少外部元件

— 提供参考设计

— 6mm*6mm QFN-40 封装：

- 低功耗

— 接收模式低至 19.6mA

— 发送模式（-6dBm）:24mA

— 功率模式 1（3-us 唤醒）：235uA

— 功率模式 2（睡眠计时器开启）：0.9uA

— 功率模式 3:（外部中断）:0.4uA

— 供电范围：2V-3.6V

— 在所有电源模式下都有 RAM 和寄存器存储

- 微控制处理器

— 高性能，低功耗的 2051 内核

— 系统可编程闪存 56KB

— 静态随机存储器 8KB

- 外围设备

— 含 8 个通道和可配置分辨率的 12 位数模转换

— 集成高性能比较器

— 通用定时器 16 字节，2 个 8 字节）

— 21 个多功能 I/O 口（19*4mA.2*20mA）

— 32kHz 休眠定时器

— 2 个串口

— 全速 USB 接口

— 红外发生电路

— 功能强大的 5 个通道直接内存访问（DMA）

— AES 安全协处理器

— 电池监控和温度传感器

— 每个 CC2540 内涵一个唯一的 48 位 IEEE 地址。

应用：

2.4G 低功耗蓝牙系统

移动配件

运动和健身设备

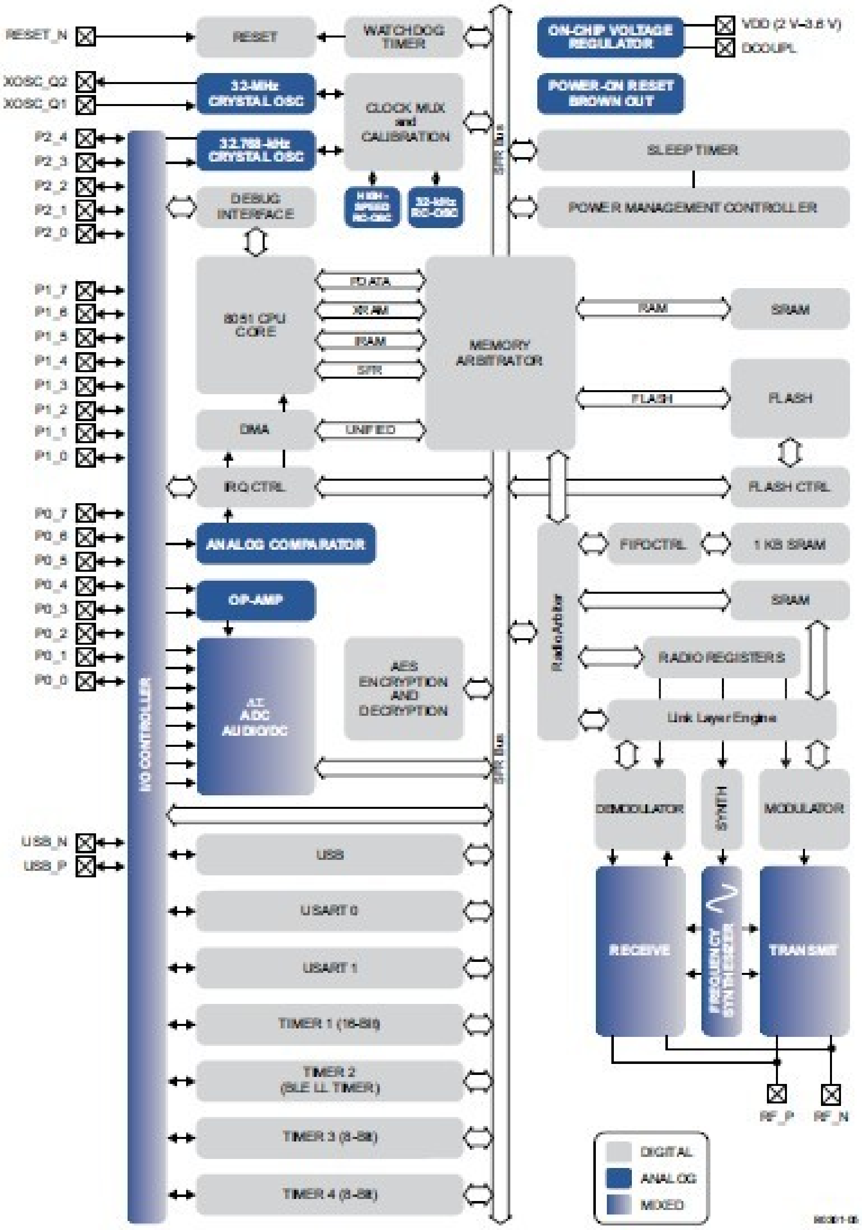
消费电子

人机接口器件

USB 软件狗

健康和医疗

CC2540 是一款高性价比，低功耗的正在片上系统（Soc）解决方案，适合蓝牙低耗能应用，它使低总体物料清单成本建立强健的网络节点成为可能。CC2540 包含一个出色的工业标准的 8051 内核的 RF 收发器，系统编程闪存记忆，8KB RAM 和其他功能强大的配套特征以及外设。CC2540 适用于低功耗系统，超低的睡眠模式，以及运行模式的超低功耗的转换进一步实现了超低功耗。CC2540 有 2 中不同的版本:CC2540F128/F256，分别拥有 128 和 256KB 闪存记忆。与 TI 的蓝牙低功耗协议栈相连接，CC2540F128/256 形成市场上最灵活，高性价比的单模式蓝牙低耗能解决方案。



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

		MIN	MAX	UNIT
Supply voltage	All supply pins must have the same voltage	–0.3	3.9	V
Voltage on any digital pin		–0.3	VDD + 0.3, ≤ 3.9	V
Input RF level			10	dBm
Storage temperature range		–40	85	°C
ESD(2)	All pads, according to human-body model, JEDEC STD 22, method A114		2	kV
	According to charged-device model, JEDEC STD 22, method C101		500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) CAUTION: ESD sensitive device. Precautions should be used when handing the device in order to prevent permanent damage.

RECOMMENDED OPERATING CONDITIONS

	MIN	MAX	UNIT
Operating ambient temperature range, T_A	–40	85	°C
Operating supply voltage	2	3.6	V

ELECTRICAL CHARACTERISTICS

Measured on Texas Instruments CC2540 EM reference design with T_A = 25°C and VDD = 3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{core}	Core current consumption	Power mode 1. Digital regulator on; 16-MHz RCOSC and 32-MHz crystal oscillator off; 32.768-kHz XOSC, POR, BOD and sleep timer active; RAM and register retention		235		µA
		Power mode 2. Digital regulator off; 16-MHz RCOSC and 32-MHz crystal oscillator off; 32.768-kHz XOSC, POR, and sleep timer active; RAM and register retention		0.9		µA
		Power mode 3. Digital regulator off; no clocks; POR active; RAM and register retention		0.4		µA
		Low MCU activity: 32-MHz XOSC running. No radio or peripherals. No flash access, no RAM access.		6.7		mA
I_{peri}	Peripheral current consumption (Adds to core current I_{core} for each peripheral unit activated)	Timer 1. Timer running, 32-MHz XOSC used		90		µA
		Timer 2. Timer running, 32-MHz XOSC used		90		µA
		Timer 3. Timer running, 32-MHz XOSC used		60		µA
		Timer 4. Timer running, 32-MHz XOSC used		70		µA
		Sleep timer, including 32.753-kHz RCOSC		0.6		µA
		ADC, when converting		1.2		mA

GENERAL CHARACTERISTICS

Measured on Texas Instruments CC2540 EM reference design with T_A = 25°C and VDD = 3 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
WAKE-UP AND TIMING					
Power mode 1 → Active	Digital regulator on, 16-MHz RCOSC and 32-MHz crystal oscillator off. Start-up of 16-MHz RCOSC		4		µs
Power mode 2 or 3 → Active	Digital regulator off, 16-MHz RCOSC and 32-MHz crystal oscillator off. Start-up of regulator and 16-MHz RCOSC		120		µs
Active → TX or RX	Crystal ESR = 16 Ω. Initially running on 16-MHz RCOSC, with 32-MHz XOSC OFF		410		µs
	With 32-MHz XOSC initially on		160		µs
RX/TX turnaround			150		µs
RADIO PART					
RF frequency range	Programmable in 2-MHz steps	2402		2480	MHz
Data rate and modulation format	1 Mbps, GFSK, 250 kHz deviation				

RF RECEIVE SECTION

Measured on Texas Instruments CC2540 EM reference design with T_A = 25°C, VDD = 3 V, f_c = 2440 MHz
1 Mbps, GFSK, 250-kHz deviation, *Bluetooth* low energy mode, and 0.1% BER(1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver sensitivity(2)	High-gain mode		–93		dBm
Receiver sensitivity(2)	Standard mode		–87		dBm
Saturation(3)			6		dBm
Co-channel rejection(3)			–5		dB
Adjacent-channel rejection(3)	±1 MHz		5		dB
Alternate-channel rejection(3)	±2 MHz		30		dB
Blocking(3)			–30		dBm
Frequency error tolerance(4)	Including both initial tolerance and drift	–250		250	kHz
Symbol rate error tolerance(5)		–80		80	ppm
Spurious emission. Only largest spurious emission stated within each band.	Conducted measurement with a 50-Ω single-ended load. Complies with EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66		–75		dBm
Current consumption	RX mode, standard mode, no peripherals active, low MCU activity, MCU at 250 kHz		19.6		mA
	RX mode, high-gain mode, no peripherals active, low MCU activity, MCU at 250 kHz		22.1		mA

(1) 0.1% BER maps to 30.8% PER
(2) The receiver sensitivity setting is programmable using a TI BLE stack vendor-specific API command. The default value is standard mode.
(3) Results based on standard gain mode
(4) Difference between center frequency of the received RF signal and local oscillator frequency
(5) Difference between incoming symbol rate and the internally generated symbol rate

RF TRANSMIT SECTION

Measured on Texas Instruments CC2540 EM reference design with T_A = 25°C, VDD = 3 V and f_c = 2440 MHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output power	Delivered to a single-ended 50-Ω load through a balun using maximum recommended output power setting		4		dBm
	Delivered to a single-ended 50-Ω load through a balun using minimum recommended output power setting		–20		
Programmable output power range	Delivered to a single-ended 50 Ω load through a balun		24		dB
Spurious emissions	Conducted measurement with a 50-Ω single-ended load. Complies with EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66 (1)		–41		dBm
Current consumption	TX mode, –23-dBm output power, no peripherals active, low MCU activity, MCU at 250 kHz		21.1		mA
	TX mode, –6-dBm output power, no peripherals active, low MCU activity, MCU at 250 kHz		23.8		
	TX mode, 0-dBm output power, no peripherals active, low MCU activity, MCU at 250 kHz		27		
	TX mode, 4-dBm output power, no peripherals active, low MCU activity, MCU at 250 kHz		31.6		
Optimum load impedance	Differential impedance as seen from the RF port (RF_P and RF_N) toward the antenna		70 + j30		Ω

(1) Designs with antenna connectors that require conducted ETSI compliance at 64 MHz should insert an LC resonator in front of the antenna connector. Use a 1.6-nH inductor in parallel with a 1.8-pF capacitor. Connect both from the signal trace to a good RF ground.

32-MHz CRYSTAL OSCILLATOR

Measured on Texas Instruments CC2540 EM reference design with T_A = 25°C and VDD = 3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Crystal frequency			32		MHz
	Crystal frequency accuracy requirement(1)		–40		40	ppm
ESR	Equivalent series resistance		6		60	Ω
C_0	Crystal shunt capacitance		1		7	pF
C_L	Crystal load capacitance		10		16	pF
	Start-up time			0.25		ms
	Power-down guard time	The crystal oscillator must be in power down for a guard time before it is used again. This requirement is valid for all modes of operation. The need for power-down guard time can vary with crystal type and load.	3			ms

(1) Including aging and temperature dependency, as specified by [1]

32.768-kHz CRYSTAL OSCILLATOR

Measured on Texas Instruments CC2540 EM reference design with T_A = 25°C and VDD = 3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Crystal frequency			32.768		kHz
	Crystal frequency accuracy requirement(1)		–40		40	ppm
ESR	Equivalent series resistance			40	130	kΩ
C_0	Crystal shunt capacitance			0.9	2	pF
C_L	Crystal load capacitance			12	16	pF
	Start-up time			0.4		s

(1) Including aging and temperature dependency, as specified by [1]

32-kHz RC OSCILLATOR

Measured on Texas Instruments CC2540 EM reference design with T_{ω} = 25°C and VDD = 3 V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Calibrated frequency(1)			32.753		kHz
Frequency accuracy after calibration			±0.2%		
Temperature coefficient(2)			0.4		%/°C
Supply-voltage coefficient(3)			3		%/V
Calibration time(4)			2		ms

(1) The calibrated 32-kHz RC oscillator frequency is the 32-MHz XTAL frequency divided by 977.
(2) Frequency drift when temperature changes after calibration
(3) Frequency drift when supply voltage changes after calibration
(4) When the 32-kHz RC oscillator is enabled, it is calibrated when a switch from the 16-MHz RC oscillator to the 32-MHz crystal oscillator is performed while SLEEPCMD.OSC32K_CALDIS is set to 0.

16-MHz RC OSCILLATOR

Measured on Texas Instruments CC2540 EM reference design with T_A = 25°C and VDD = 3 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency (1)			16		MHz
Uncalibrated frequency accuracy			±18%		
Calibrated frequency accuracy			±0.6%		
Start-up time			10		μs
Initial calibration time (2)			50		μs

(1) The calibrated 16-MHz RC oscillator frequency is the 32-MHz XTAL frequency divided by 2.
(2) When the 16-MHz RC oscillator is enabled, it is calibrated when a switch from the 16-MHz RC oscillator to the 32-MHz crystal oscillator is performed while SLEEPCMD.OSC_PD is set to 0.

RSSI CHARACTERISTICS

Measured on Texas Instruments CC2540 EM reference design with T_A = 25°C and VDD = 3 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Useful RSSI range (1)	High-gain mode		–99 to –44		dBm
	Standard mode		–90 to –35		
Absolute uncalibrated RSSI accuracy (1)	High-gain mode		±4		dB
Step size (LSB value)			1		dB

(1) Assuming CC2540 EM reference design. Other RF designs give an offset from the reported value.

FREQUENCY SYNTHESIZER CHARACTERISTICS

Measured on Texas Instruments CC2540 EM reference design with T_A = 25°C, VDD = 3 V and f_c = 2440 MHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phase noise, unmodulated carrier	At ±1-MHz offset from carrier		–109		dBc/Hz
	At ±3-MHz offset from carrier		–112		
	At ±5-MHz offset from carrier		–119		

ANALOG TEMPERATURE SENSOR

Measured on Texas Instruments CC2540 EM reference design with T_A = 25°C and VDD = 3 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output	Measured using integrated ADC, internal band-gap voltage reference, and maximum resolution		1480		12-bit
Temperature coefficient			4.5		mv/°C
Voltage coefficient			1		/ 0.1 V
Initial accuracy without calibration			±10		°C
Accuracy using 1-point calibration			±5		°C
Current consumption when enabled			0.5		mA

OP-AMP CHARACTERISTICS

T_A = 25°C, VDD = 3 V, . All measurement results are obtained using the CC2540 reference designs post-calibration.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Chopping Configuration, Register APCFG = 0x07, OPAMPMC = 0x03, OPAMPC = 0x01						
	Output maximum voltage			VDD – 0.07		V
	Output minimum voltage			0.07		V
	Open-loop gain			108		dB
	Gain-bandwidth product			2		MHz
	Slew rate			107		V/µs
	Input maximum voltage			VDD + 0.13		V
	Intput minimum voltage			–55		mV
	Input offset voltage			40		µV
CMRR	Common-mode rejection ratio			90		dB
	Supply current			0.4		mA
	Input noise voltage	f = 0.01 Hz to 1 Hz		1.1		nV/√(Hz)
		f = 0.1 Hz to 10 Hz		1.7		
Non-Chopping Configuration, Register APCFG = 0x07, OPAMPMC = 0x00, OPAMPC = 0x01						
	Output maximum voltage			VDD – 0.07		V
	Output minimum voltage			0.07		V
	Open-loop gain			108		dB
	Gain-bandwidth product			2		MHz
	Slew rate			107		V/µs
	Input maximum voltage			VDD + 0.13		V
	Intput minimum voltage			–55		mV
	Input offset voltage			0.8		mV
CMRR	Common-mode rejection ratio			90		dB
	Supply current			0.4		mA
	Input noise voltage	f = 0.01 Hz to 1 Hz		60		nV/√(Hz)
		f = 0.1 Hz to 10 Hz		65		

COMPARATOR CHARACTERISTICS

T_A = 25°C, VDD = 3 V. All measurement results are obtained using the CC2540 reference designs, post-calibration.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Common-mode maximum voltage			VDD		V
Common-mode minimum voltage			–0.3		
Input offset voltage			1		mV
Offset vs temperature			16		µV/°C
Offset vs operating voltage			4		mV/V
Supply current			230		nA
Hysteresis			0.15		mV

ADC CHARACTERISTICS

T_A = 25°C and VDD = 3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input voltage	VDD is voltage on AVDD5 pin	0		VDD	V
	External reference voltage	VDD is voltage on AVDD5 pin	0		VDD	V
	External reference voltage differential	VDD is voltage on AVDD5 pin	0		VDD	V
	Input resistance, signal	Simulated using 4-MHz clock speed		197		kΩ
	Full-scale signal (1)	Peak-to-peak, defines 0 dBFS		2.97		V
ENOB (1)	Effective number of bits	Single-ended input, 7-bit setting		5.7		bits
		Single-ended input, 9-bit setting		7.5		
		Single-ended input, 10-bit setting		9.3		
		Single-ended input, 12-bit setting		10.3		
		Differential input, 7-bit setting		6.5		
		Differential input, 9-bit setting		8.3		
		Differential input, 10-bit setting		10		
		Differential input, 12-bit setting		11.5		
		10-bit setting, clocked by RCOSC		9.7		
		12-bit setting, clocked by RCOSC		10.9		
	Useful power bandwidth	7-bit setting, both single and differential		0–20		kHz
THD	Total harmonic distortion	Single ended input, 12-bit setting, –6 dBFS (1)		–75.2		dB
		Differential input, 12-bit setting, –6 dBFS (1)		–86.6		
	Signal to nonharmonic ratio	Single-ended input, 12-bit setting (1)		70.2		dB
		Differential input, 12-bit setting (1)		79.3		
		Single-ended input, 12-bit setting, –6 dBFS (1)		78.8		
		Differential input, 12-bit setting, –6 dBFS (1)		88.9		
CMRR	Common-mode rejection ratio	Differential input, 12-bit setting, 1-kHz sine (0 dBFS), limited by ADC resolution		>84		dB
	Crosstalk	Single ended input, 12-bit setting, 1-kHz sine (0 dBFS), limited by ADC resolution		>84		dB
	Offset	Midscale		–3		mV
	Gain error			0.68%		
DNL	Differential nonlinearity	12-bit setting, mean (1)		0.05		LSB
		12-bit setting, maximum (1)		0.9		
INL	Integral nonlinearity	12-bit setting, mean (1)		4.6		LSB
		12-bit setting, maximum (1)		13.3		
		12-bit setting, mean, clocked by RCOSC		10		
		12-bit setting, max, clocked by RCOSC		29		
SINAD (–THD+N)	Signal-to-noise-and-distortion	Single ended input, 7-bit setting (1)		35.4		dB
		Single ended input, 9-bit setting (1)		46.8		
		Single ended input, 10-bit setting (1)		57.5		
		Single ended input, 12-bit setting (1)		66.6		
		Differential input, 7-bit setting (1)		40.7		
		Differential input, 9-bit setting (1)		51.6		
		Differential input, 10-bit setting (1)		61.8		
		Differential input, 12-bit setting (1)		70.8		

(1) Measured with 300-Hz sine-wave input and VDD as reference.

ADC CHARACTERISTICS (continued)

T_A = 25°C and VDD = 3 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Conversion time	7-bit setting		20		µs
	9-bit setting		36		
	10-bit setting		68		
	12-bit setting		132		
Power consumption			1.2		mA
Internal reference VDD coefficient			4		mV/V
Internal reference temperature coefficient			0.4		mV/10°C
Internal reference voltage			1.15		V

CONTROL INPUT AC CHARACTERISTICS

T_A = –40°C to 85°C, VDD = 2 V to 3.6 V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
System clock, f_{SYSCLK} t_{SYSCLK} = 1/ f_{SYSCLK}	The undivided system clock is 32 MHz when crystal oscillator is used. The undivided system clock is 16 MHz when calibrated 16-MHz RC oscillator is used.	16		32	MHz
RESET_N low duration	See item 1, Figure 1. This is the shortest pulse that is recognized as a complete reset pin request. Note that shorter pulses may be recognized but do not lead to complete reset of all modules within the chip.	1			µs
Interrupt pulse duration	See item 2, Figure 1.This is the shortest pulse that is recognized as an interrupt request.	20			ns

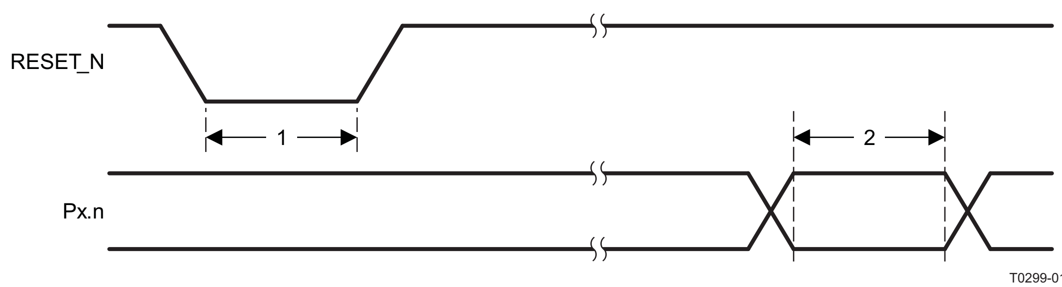


Figure 1. Control Input AC Characteristics

SPI AC CHARACTERISTICS

T_A = –40°C to 125°C, VDD = 2 V to 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	SCK period	Master, RX and TX	250			ns
		Slave, RX and TX	250			
	SCK duty cycle	Master		50%		
t_2	SSN low to SCK	Master	63			ns
		Slave	63			
t_3	SCK to SSN high	Master	63			ns
		Slave	63			
t_4	MOSI early out	Master, load = 10 pF			7	ns
t_5	MOSI late out	Master, load = 10 pF			10	ns
t_6	MISO setup	Master	90			ns
t_7	MISO hold	Master	10			ns
	SCK duty cycle	Slave		50%		ns
t_{10}	MOSI setup	Slave	35			ns
t_{11}	MOSI hold	Slave	10			ns
t_9	MISO late out	Slave, load = 10 pF			95	ns
	Operating frequency	Master, TX only			8	MHz
		Master, RX and TX			4	
		Slave, RX only			8	
		Slave, RX and TX			4	

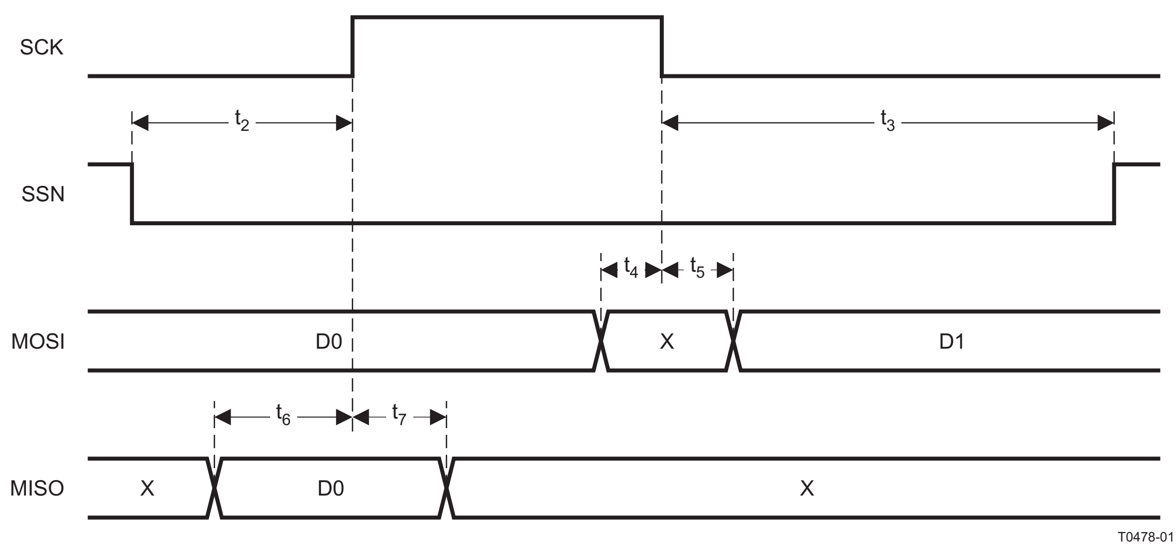


Figure 2. SPI Master AC Characteristics

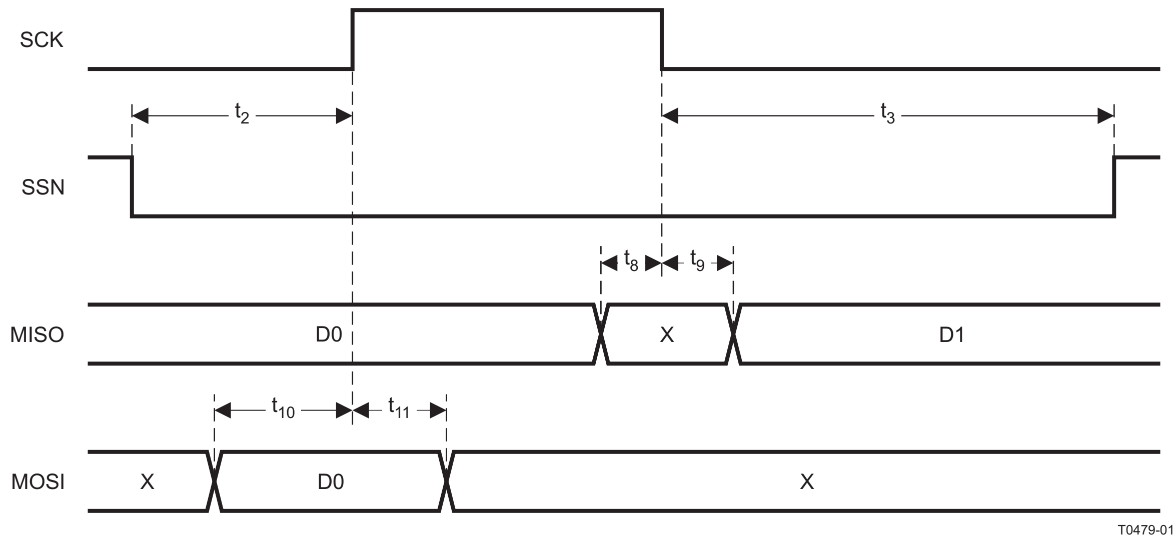


Figure 3. SPI Slave AC Characteristics

DEBUG INTERFACE AC CHARACTERISTICS

T_A = –40°C to 125°C, VDD = 2 V to 3.6 V

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clk_dbg}	Debug clock frequency (see Figure 4)				12	MHz
t_1	Allowed high pulse on clock (see Figure 4)		35			ns
t_2	Allowed low pulse on clock (see Figure 4)		35			ns
t_3	EXT_RESET_N low to first falling edge on debug clock (see Figure 6)		167			ns
t_4	Falling edge on clock to EXT_RESET_N high (see Figure 6)		83			ns
t_5	EXT_RESET_N high to first debug command (see Figure 6)		83			ns
t_6	Debug data setup (see Figure 5)		2			ns
t_7	Debug data hold (see Figure 5)		4			ns
t_8	Clock-to-data delay (see Figure 5)	Load = 10 pF			30	ns

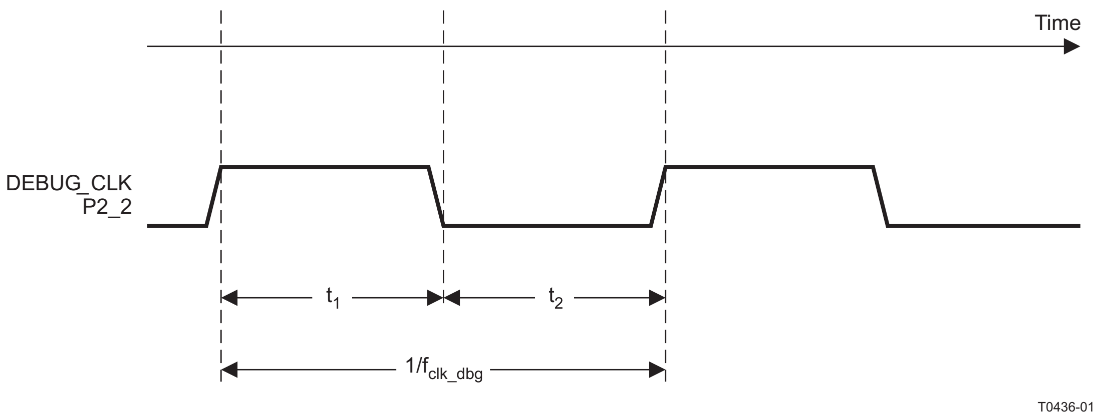


Figure 4. Debug Clock – Basic Timing

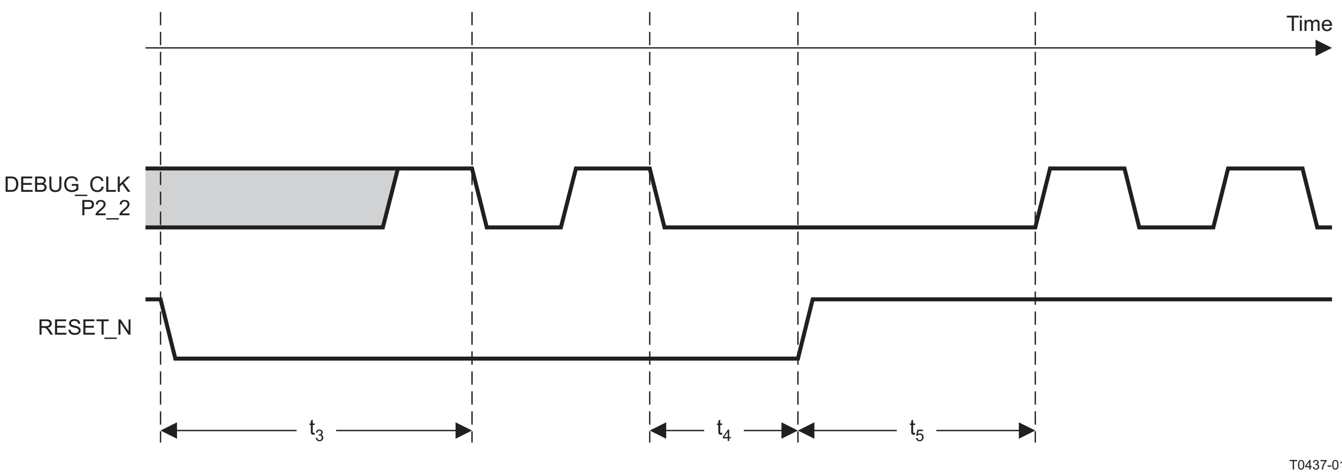


Figure 5. Debug Enable Timing

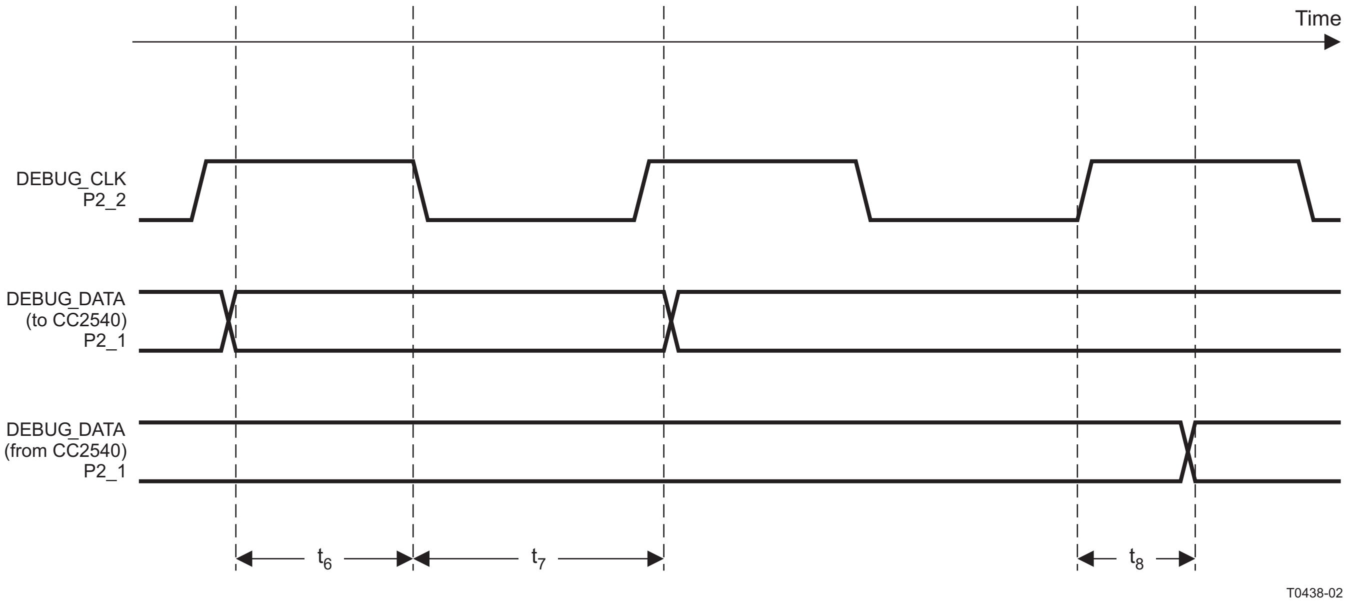


Figure 6. Data Setup and Hold Timing

TIMER INPUTS AC CHARACTERISTICS

T_A = –40°C to 85°C, VDD = 2 V to 3.6 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input capture pulse duration	Synchronizers determine the shortest input pulse that can be recognized. The synchronizers operate at the current system clock rate (16 MHz or 32 MHz).	1.5			t_{SYSCLK}

DC CHARACTERISTICS

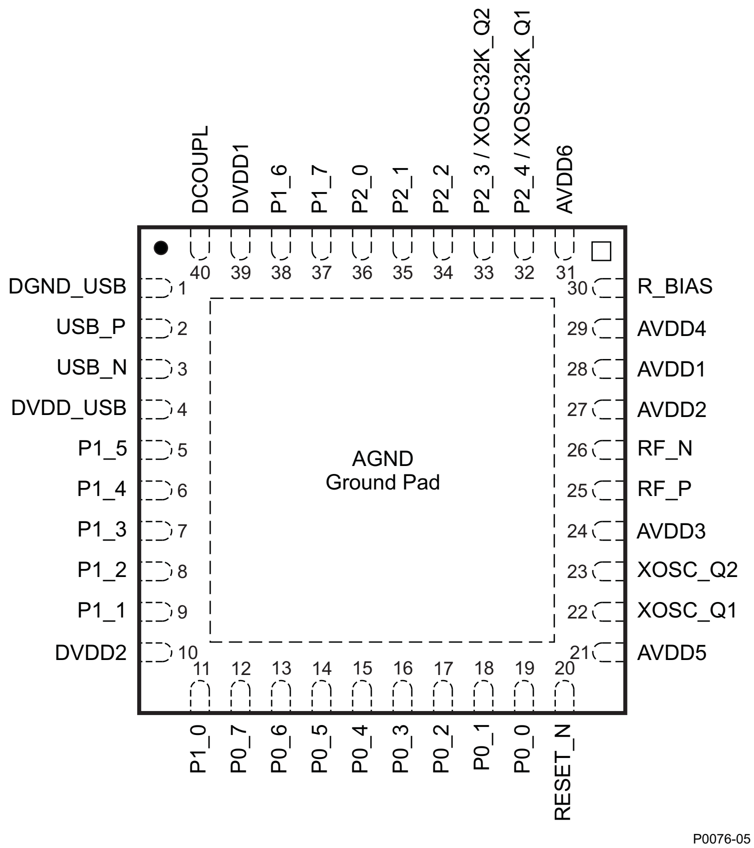
T_A = 25°C, VDD = 3 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Logic-0 input voltage				0.5	V
Logic-1 input voltage		2.5			V
Logic-0 input current	Input equals 0 V	–50		50	nA
Logic-1 input current	Input equals VDD	–50		50	nA
I/O-pin pullup and pulldown resistors			20		kΩ
Logic-0 output voltage, 4- mA pins	Output load 4 mA			0.5	V
Logic-1 output voltage, 4-mA pins	Output load 4 mA	2.4			V

DEVICE INFORMATION

PIN DESCRIPTIONS

The CC2540 pinout is shown in Figure 7 and a short description of the pins follows.



NOTE: The exposed ground pad must be connected to a solid ground plane, as this is the ground connection for the chip.

Figure 7. Pinout Top View

PIN DESCRIPTIONS

PIN NAME	PIN	PIN TYPE	DESCRIPTION
AVDD1	28	Power (analog)	2-V–3.6-V analog power-supply connection
AVDD2	27	Power (analog)	2-V–3.6-V analog power-supply connection
AVDD3	24	Power (analog)	2-V–3.6-V analog power-supply connection
AVDD4	29	Power (analog)	2-V–3.6-V analog power-supply connection
AVDD5	21	Power (analog)	2-V–3.6-V analog power-supply connection
AVDD6	31	Power (analog)	2-V–3.6-V analog power-supply connection
DCOUPL	40	Power (digital)	1.8-V digital power-supply decoupling. Do not use for supplying external circuits.
DGND_USB	1	Ground pin	Connect to GND
DVDD_USB	4	Power (digital)	2-V–3.6-V digital power-supply connection
DVDD1	39	Power (digital)	2-V–3.6-V digital power-supply connection
DVDD2	10	Power (digital)	2-V–3.6-V digital power-supply connection
GND	—	Ground	The ground pad must be connected to a solid ground plane.
P0_0	19	Digital I/O	Port 0.0
P0_1	18	Digital I/O	Port 0.1
P0_2	17	Digital I/O	Port 0.2
P0_3	16	Digital I/O	Port 0.3
P0_4	15	Digital I/O	Port 0.4
P0_5	14	Digital I/O	Port 0.5
P0_6	13	Digital I/O	Port 0.6
P0_7	12	Digital I/O	Port 0.7
P1_0	11	Digital I/O	Port 1.0 – 20-mA drive capability
P1_1	9	Digital I/O	Port 1.1 – 20-mA drive capability
P1_2	8	Digital I/O	Port 1.2
P1_3	7	Digital I/O	Port 1.3
P1_4	6	Digital I/O	Port 1.4
P1_5	5	Digital I/O	Port 1.5
P1_6	38	Digital I/O	Port 1.6
P1_7	37	Digital I/O	Port 1.7
P2_0	36	Digital I/O	Port 2.0
P2_1	35	Digital I/O	Port 2.1
P2_2	34	Digital I/O	Port 2.2
P2_3/ XOSC32K_Q2	33	Digital I/O, Analog I/O	Port 2.3/32.768 kHz XOSC
P2_4/ XOSC32K_Q1	32	Digital I/O, Analog I/O	Port 2.4/32.768 kHz XOSC
RBIAS	30	Analog I/O	External precision bias resistor for reference current
RESET_N	20	Digital input	Reset, active-low
RF_N	26	RF I/O	Negative RF input signal to LNA during RX Negative RF output signal from PA during TX
RF_P	25	RF I/O	Positive RF input signal to LNA during RX Positive RF output signal from PA during TX
USB_N	3	Digital I/O	USB N
USB_P	2	Digital I/O	USB P
XOSC_Q1	22	Analog I/O	32-MHz crystal oscillator pin 1 or external-clock input
XOSC_Q2	23	Analog I/O	32-MHz crystal oscillator pin 2

BLOCK DIAGRAM

A block diagram of the CC2540 is shown in Figure 8. The modules can be roughly divided into one of three categories: CPU-related modules; modules related to power, test, and clock distribution; and radio-related modules. In the following subsections, a short description of each module is given.

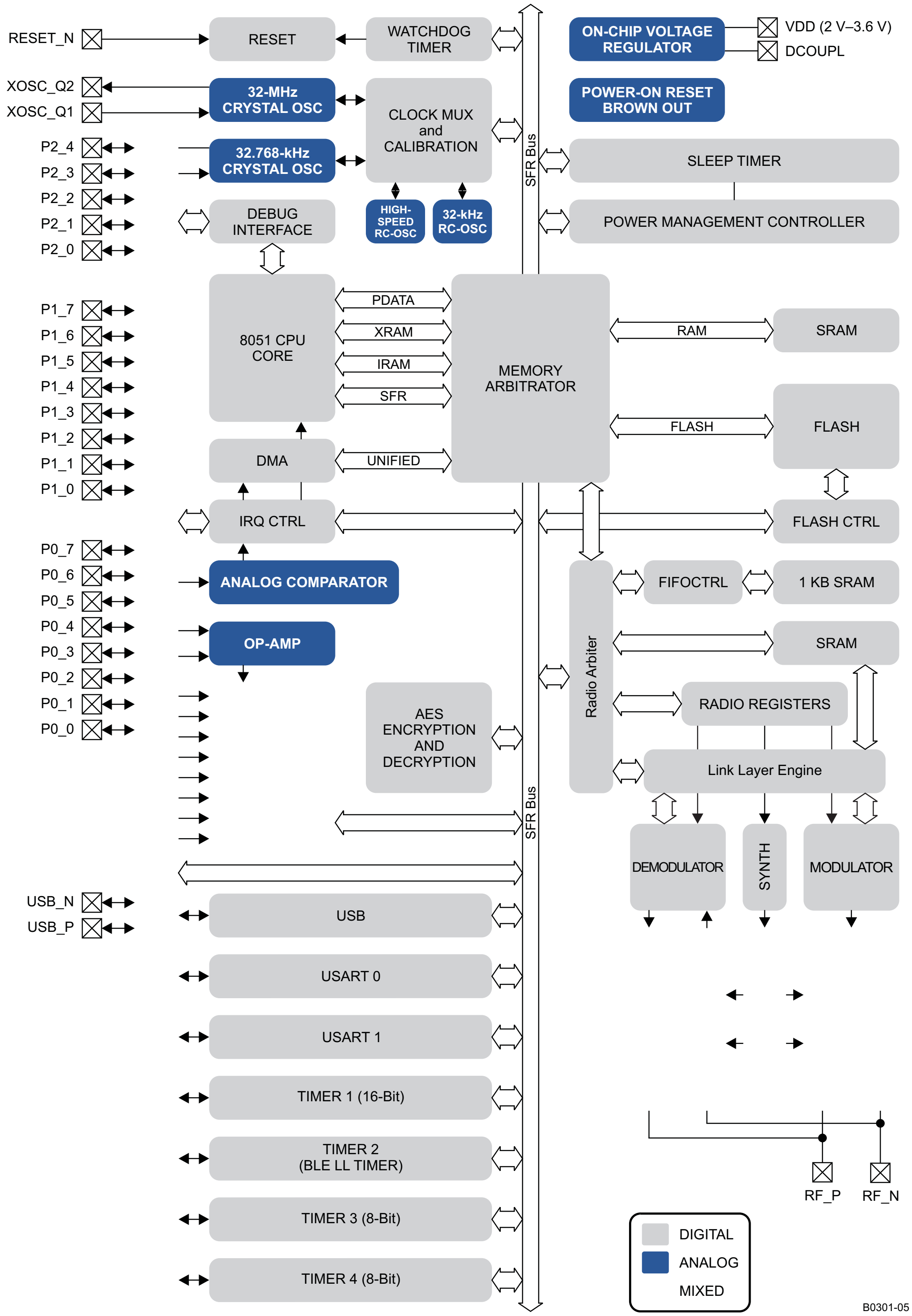


Figure 8. CC2540 Block Diagram

BLOCK DESCRIPTIONS

CPU and Memory

The **8051 CPU core** is a single-cycle 8051-compatible core. It has three different memory access busses (SFR, DATA, and CODE/XDATA), a debug interface, and an 18-input extended interrupt unit.

The **memory arbiter** is at the heart of the system, as it connects the CPU and DMA controller with the physical memories and all peripherals through the SFR bus. The memory arbiter has four memory-access points, access of which can map to one of three physical memories: an SRAM, flash memory, and XREG/SFR registers. It is responsible for performing arbitration and sequencing between simultaneous memory accesses to the same physical memory.

The **SFR bus** is drawn conceptually in Figure 8 as a common bus that connects all hardware peripherals to the memory arbiter. The SFR bus in the block diagram also provides access to the radio registers in the radio register bank, even though these are indeed mapped into XDATA memory space.

The **8-KB SRAM** maps to the DATA memory space and to parts of the XDATA memory spaces. The SRAM is an ultralow-power SRAM that retains its contents even when the digital part is powered off (power modes 2 and 3).

The **128/256 KB flash block** provides in-circuit programmable non-volatile program memory for the device, and maps into the CODE and XDATA memory spaces.

Peripherals

Writing to the flash block is performed through a **flash controller** that allows page-wise erasure and 4-bytewise programming. See User Guide for details on the flash controller.

A versatile five-channel **DMA controller** is available in the system, accesses memory using the XDATA memory space, and thus has access to all physical memories. Each channel (trigger, priority, transfer mode, addressing mode, source and destination pointers, and transfer count) is configured with DMA descriptors that can be located anywhere in memory. Many of the hardware peripherals (AES core, flash controller, USARTs, timers, ADC interface, etc.) can be used with the DMA controller for efficient operation by performing data transfers between a single SFR or XREG address and flash/SRAM.

Each CC2540 contains a unique 48-bit IEEE address that can be used as the public device address for a *Bluetooth* device. Designers are free to use this address, or provide their own, as described in the *Bluetooth* specfication.

The **interrupt controller** services a total of 18 interrupt sources, divided into six interrupt groups, each of which is associated with one of four interrupt priorities. I/O and sleep timer interrupt requests are serviced even if the device is in a sleep mode (power modes 1 and 2) by bringing the CC2540 back to the active mode.

The **debug interface** implements a proprietary two-wire serial interface that is used for in-circuit debugging. Through this debug interface, it is possible to erase or program the entire flash memory, control which oscillators are enabled, stop and start execution of the user program, execute instructions on the 8051 core, set code breakpoints, and single-step through instructions in the code. Using these techniques, it is possible to perform in-circuit debugging and external flash programming elegantly.

The **I/O controller** is responsible for all general-purpose I/O pins. The CPU can configure whether peripheral modules control certain pins or whether they are under software control, and if so, whether each pin is configured as an input or output and if a pullup or pulldown resistor in the pad is connected. Each peripheral that connects to the I/O pins can choose between two different I/O pin locations to ensure flexibility in various applications.

The **sleep timer** is an ultralow-power timer that can either use an external 32.768-kHz crystal oscillator or an internal 32.753-kHz RC oscillator. The sleep timer runs continuously in all operating modes except power mode 3. Typical applications of this timer are as a real-time counter or as a wake-up timer to get out of power modes 1 or 2.

A built-in **watchdog timer** allows the CC2540 to reset itself if the firmware hangs. When enabled by software, the watchdog timer must be cleared periodically; otherwise, it resets the device when it times out.

Timer 1 is a 16-bit timer with timer/counter/PWM functionality. It has a programmable prescaler, a 16-bit period value, and five individually programmable counter/capture channels, each with a 16-bit compare value. Each of the counter/capture channels can be used as a PWM output or to capture the timing of edges on input signals. It can also be configured in IR generation mode, where it counts timer 3 periods and the output is ANDed with the output of timer 3 to generate modulated consumer IR signals with minimal CPU interaction.

Timer 2 is a 40-bit timer used by the *Bluetooth* low energy stack. It has a 16-bit counter with a configurable timer period and a 24-bit overflow counter that can be used to keep track of the number of periods that have transpired. A 40-bit capture register is also used to record the exact time at which a start-of-frame delimiter is received/transmitted or the exact time at which transmission ends. There are two 16-bit timer-compare registers and two 24-bit overflow-compare registers that can be used to give exact timing for start of RX or TX to the radio or general interrupts.

Timer 3 and timer 4 are 8-bit timers with timer/counter/PWM functionality. They have a programmable prescaler, an 8-bit period value, and one programmable counter channel with an 8-bit compare value. Each of the counter channels can be used as PWM output.

USART 0 and USART 1 are each configurable as either an SPI master/slave or a UART. They provide double buffering on both RX and TX and hardware flow control and are thus well suited to high-throughput full-duplex applications. Each USART has its own high-precision baud-rate generator, thus leaving the ordinary timers free for other uses. When configured as SPI slaves, the USARTs sample the input signal using SCK directly instead of using some oversampling scheme, and are thus well-suited for high data rates.

The **AES encryption/decryption core** allows the user to encrypt and decrypt data using the AES algorithm with 128-bit keys. The AES core also supports ECB, CBC, CFB, OFB, CTR, and CBC-MAC, as well as hardware support for CCM.

The **ADC** supports 7 to 12 bits of resolution with a corresponding range of bandwidths from 30-kHz to 4-kHz, respectively. DC and audio conversions with up to eight input channels (I/O controller pins) are possible. The inputs can be selected as single-ended or differential. The reference voltage can be internal, AVDD, or a single-ended or differential external signal. The ADC also has a temperature-sensor input channel. The ADC can automate the process of periodic sampling or conversion over a sequence of channels.

The **operational amplifier** is intended to provide front-end buffering and gain for the ADC. Both inputs as well as the output are available on pins, so the feedback network is fully customizable. A chopper-stabilized mode is available for applications that need good accuracy with high gain.

The ultralow-power **analog comparator** enables applications to wake up from PM2 or PM3 based on an analog signal. Both inputs are brought out to pins; the reference voltage must be provided externally. The comparator output is connected to the I/O controller interrupt detector and can be treated by the MCU as a regular I/O pin interrupt.

TYPICAL CHARACTERISTICS

RX CURRENT IN WAIT FOR SYNC
vs
TEMPERATURE

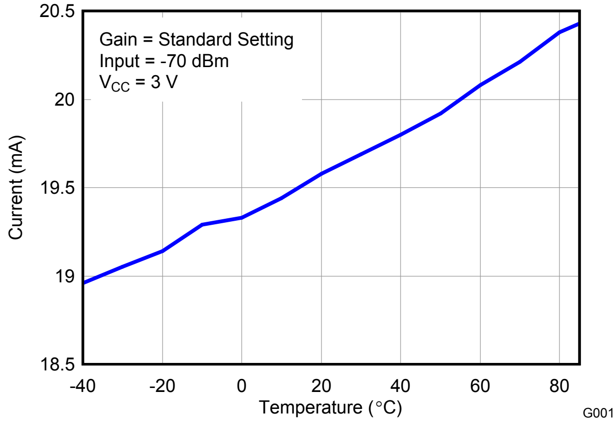


Figure 9.

TX CURRENT
vs
TEMPERATURE

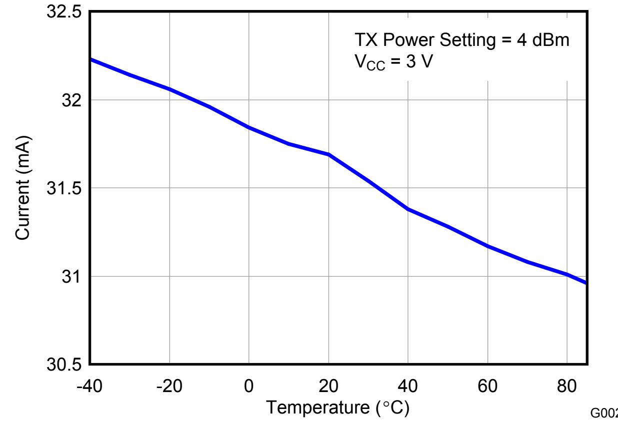


Figure 10.

RX SENSITIVITY
vs
TEMPERATURE

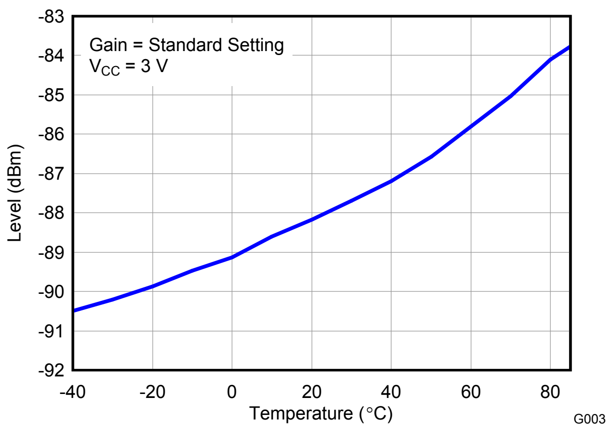


Figure 11.

TX POWER
vs
TEMPERATURE

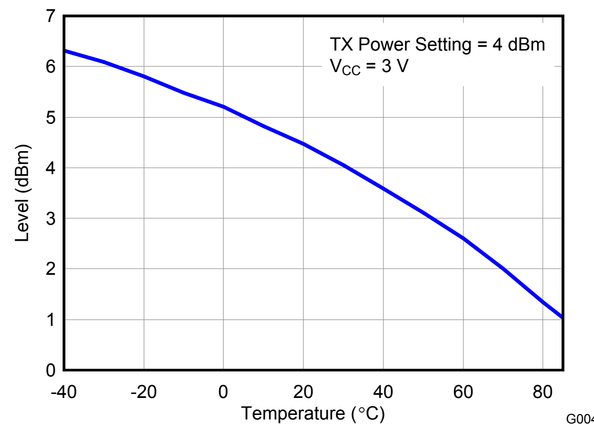


Figure 12.

RX CURRENT IN WAIT FOR SYNC
vs
SUPPLY VOLTAGE

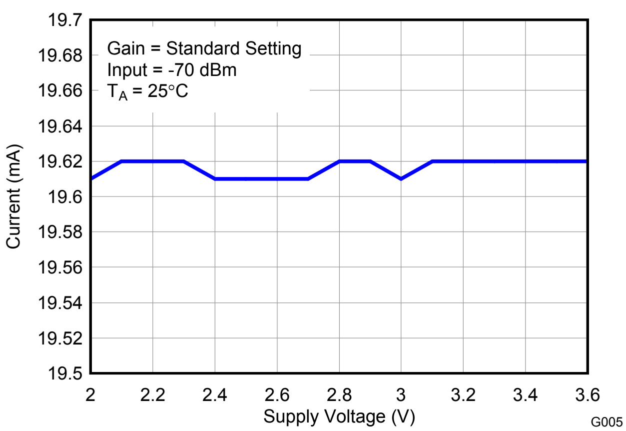


Figure 13.

TX CURRENT
vs
SUPPLY VOLTAGE

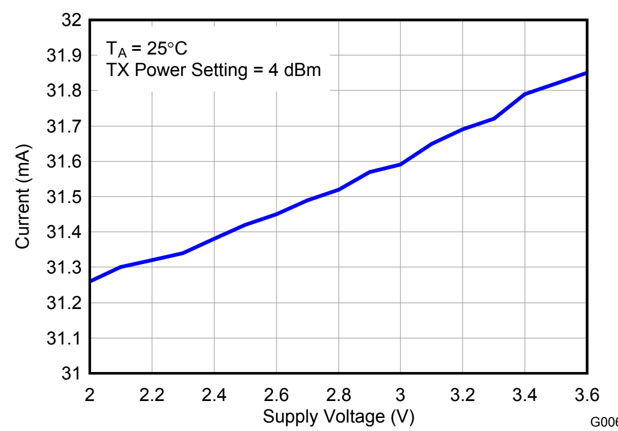


Figure 14.

TYPICAL CHARACTERISTICS (continued)

RX SENSITIVITY vs SUPPLY VOLTAGE

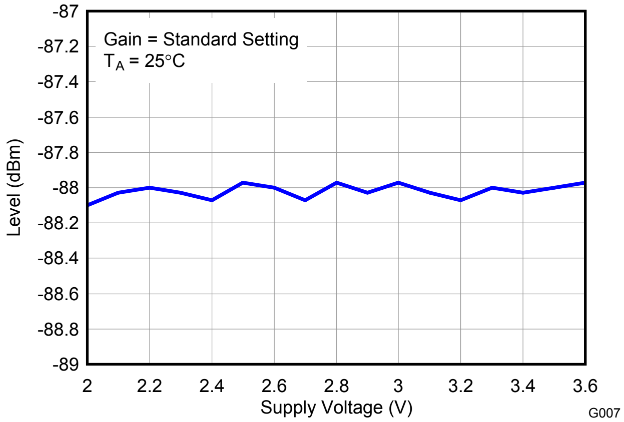


Figure 15.

TX POWER vs SUPPLY VOLTAGE

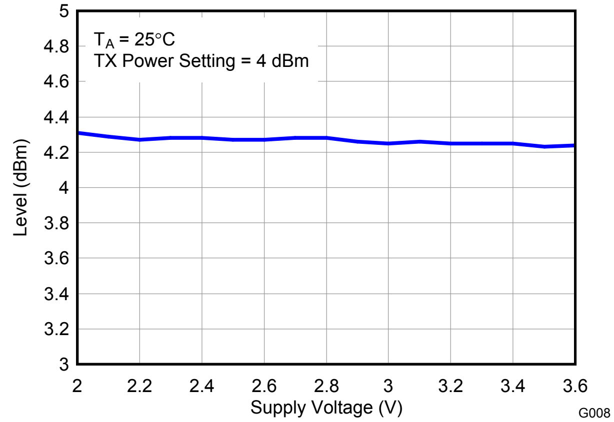


Figure 16.

RX SENSITIVITY vs FREQUENCY

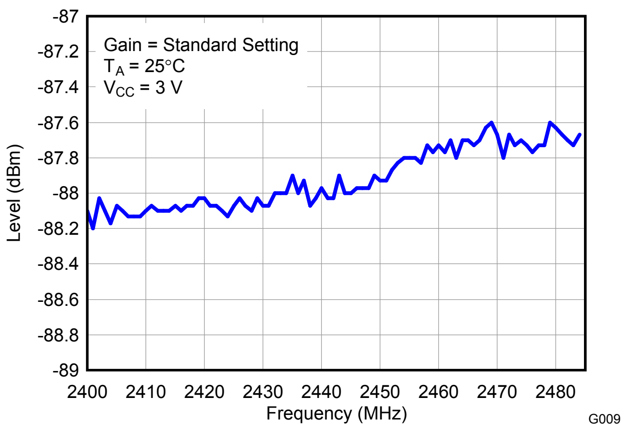


Figure 17.

RX INTERFERER REJECTION (SELECTIVITY) vs INTERFERER FREQUENCY

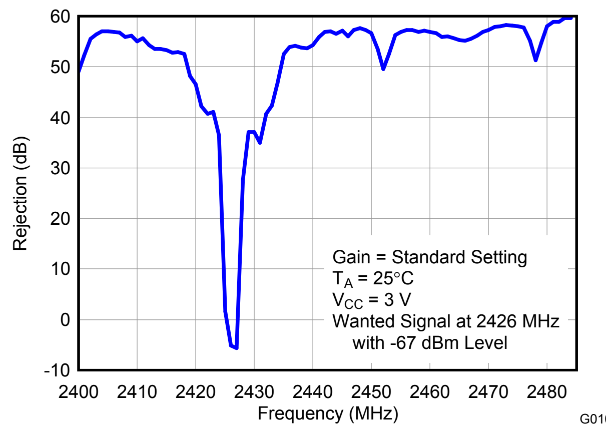


Figure 18.

TX POWER vs FREQUENCY

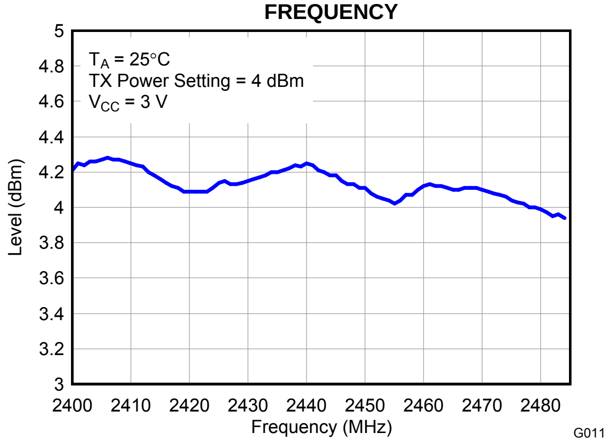


Figure 19.

TYPICAL CHARACTERISTICS (continued)

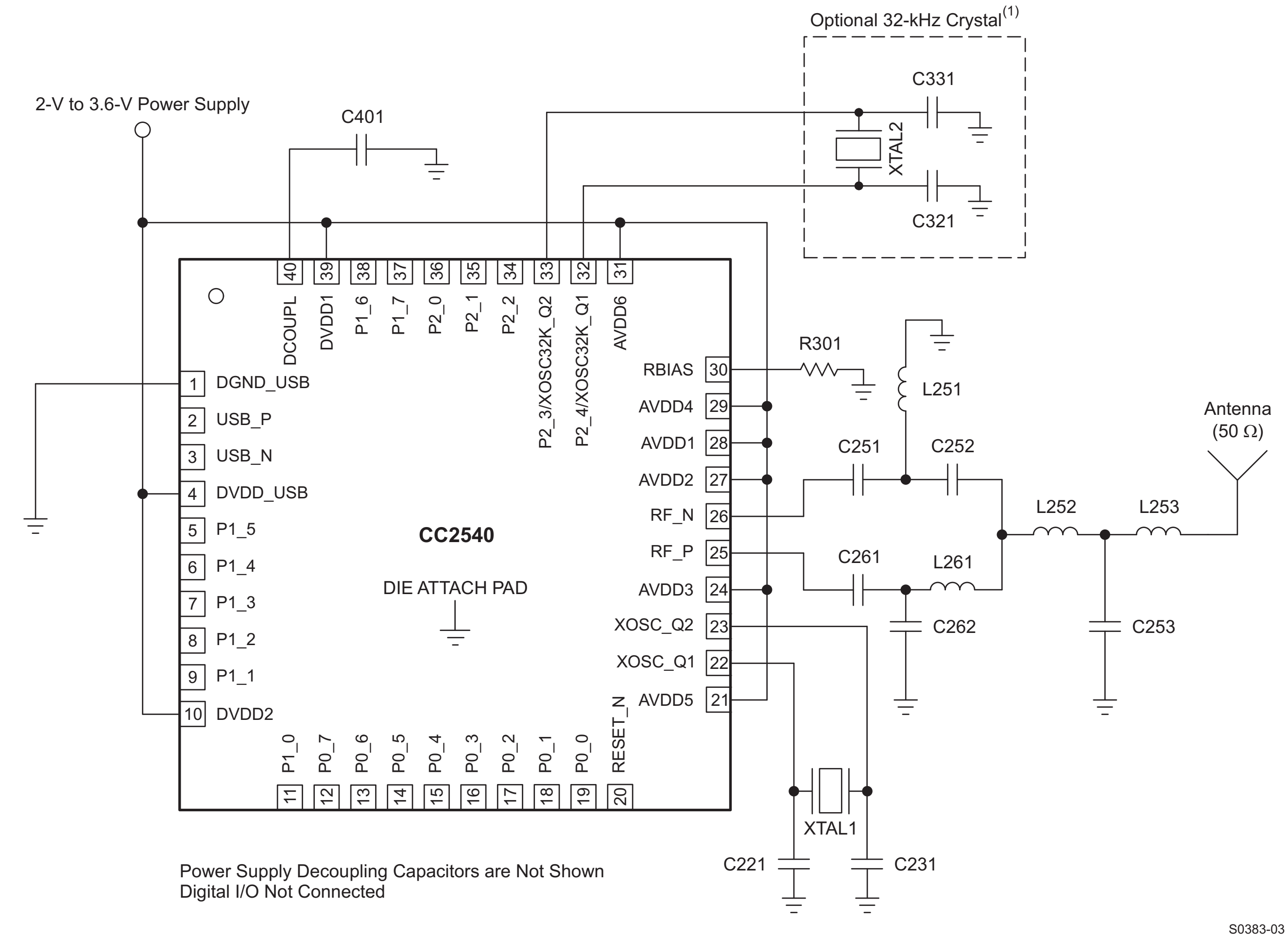
Table 1. Output Power and Current Consumption(1)(2)

Typical Output Power (dBm)	Typical Current Consumption (mA)
4	32
0	27
–6	24
–23	21

(1) Measured on Texas Instruments CC2540 EM reference design with T_A = 25°C, VDD = 3 V and f_c = 2440 MHz.
(2) The transmitter output power setting is programmable using a TI BLE stack vendor-specific API command. The default value is 0 dBm.

APPLICATION INFORMATION

Few external components are required for the operation of the CC2540. A typical application circuit is shown in Figure 20.



(1) 32-kHz crystal is mandatory when running the chip in low-power modes, except if the link layer is in the standby state (Vol. 6 Part B Section 1.1 in [1]).

NOTE: Different antenna alternatives will be provided as reference designs.

Figure 20. CC2540 Application Circuit

Table 2. Overview of External Components (Excluding Supply Decoupling Capacitors)

Component	Description	Value
C221	32-MHz xtal loading capacitor	12 pF
C231	32-MHz xtal loading capacitor	12 pF
C251	Part of the RF matching network	18 pF
C252	Part of the RF matching network	1 pF
C253	Part of the RF matching network	1 pF
C261	Part of the RF matching network	18 pF
C262	Part of the RF matching network	1 pF
C321	32-kHz xtal loading capacitor	15 pF
C331	32-kHz xtal loading capacitor	15 pF
C401	Decoupling capacitor for the internal digital regulator	1 µF

Table 2. Overview of External Components (Excluding Supply Decoupling Capacitors) (continued)

Component	Description	Value
L251	Part of the RF matching network	2 nH
L252	Part of the RF matching network	1 nH
L253	Part of the RF matching network	3 nH
L261	Part of the RF matching network	2 nH
R301	Resistor used for internal biasing	56 kΩ

Input/Output Matching

When using an unbalanced antenna such as a monopole, a balun should be used to optimize performance. The balun can be implemented using low-cost discrete inductors and capacitors. The recommended balun shown consists of C262, L261, C252, and L252.

Crystal

An external 32-MHz crystal, XTAL1, with two loading capacitors (C221 and C231) is used for the 32-MHz crystal oscillator. See 32-MHz CRYSTAL OSCILLATOR for details. The load capacitance seen by the 32-MHz crystal is given by:

$$C_L = \frac{1}{\frac{1}{C_{221}} + \frac{1}{C_{231}}} + C_{parasitic} \quad (1)$$

XTAL2 is an optional 32.768-kHz crystal, with two loading capacitors (C321 and C331) used for the 32.768-kHz crystal oscillator. The 32.768-kHz crystal oscillator is used in applications where both very low sleep-current consumption and accurate wake-up times are needed. The load capacitance seen by the 32.768-kHz crystal is given by:

$$C_L = \frac{1}{\frac{1}{C_{321}} + \frac{1}{C_{331}}} + C_{parasitic} \quad (2)$$

A series resistor may be used to comply with the ESR requirement.

On-Chip 1.8-V Voltage Regulator Decoupling

The 1.8-V on-chip voltage regulator supplies the 1.8-V digital logic. This regulator requires a decoupling capacitor (C401) for stable operation.

Power-Supply Decoupling and Filtering

Proper power-supply decoupling must be used for optimum performance. The placement and size of the decoupling capacitors and the power supply filtering are very important to achieve the best performance in an application. TI provides a compact reference design that should be followed very closely.

References

1. *Bluetooth*® Core Technical Specification document, version 4.0
   http://www.bluetooth.com/SiteCollectionDocuments/Core_V40.zip
2. CC253x System-on-Chip Solution for 2.4-GHz IEEE 802.15.4 and ZigBee® Applications/CC2540 System-on-Chip Solution for 2.4-GHz *Bluetooth* low energy Applications (SWRU191)

Additional Information

Texas Instruments offers a wide selection of cost-effective, low-power RF solutions for proprietary and standard-based wireless applications for use in industrial and consumer applications. Our selection includes RF transceivers, RF transmitters, RF front ends, and System-on-Chips as well as various software solutions for the sub-1- and 2.4-GHz frequency bands.

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- Forums, videos, and blogs
- RF design help
- E2E interaction

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- Low-power RF and ZigBee module solutions and development tools
- RF certification services and RF circuit manufacturing

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
CC2540F128RHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Purchase Samples
CC2540F128RHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Purchase Samples
CC2540F256RHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Request Free Samples
CC2540F256RHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Purchase Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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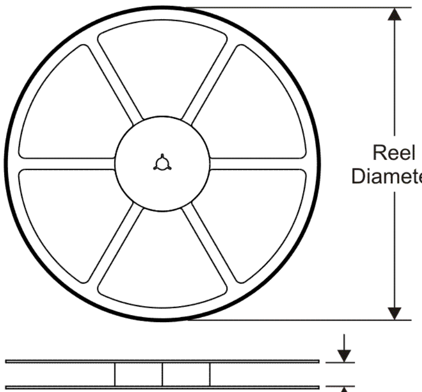
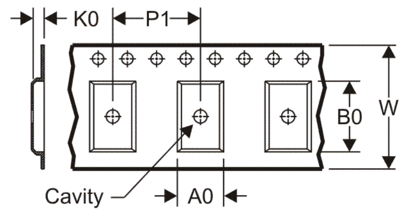
TAPE AND REEL INFORMATION

REEL DIMENSIONS

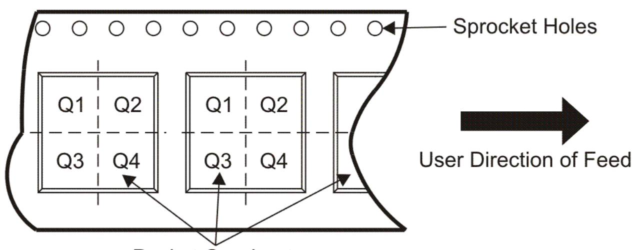


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

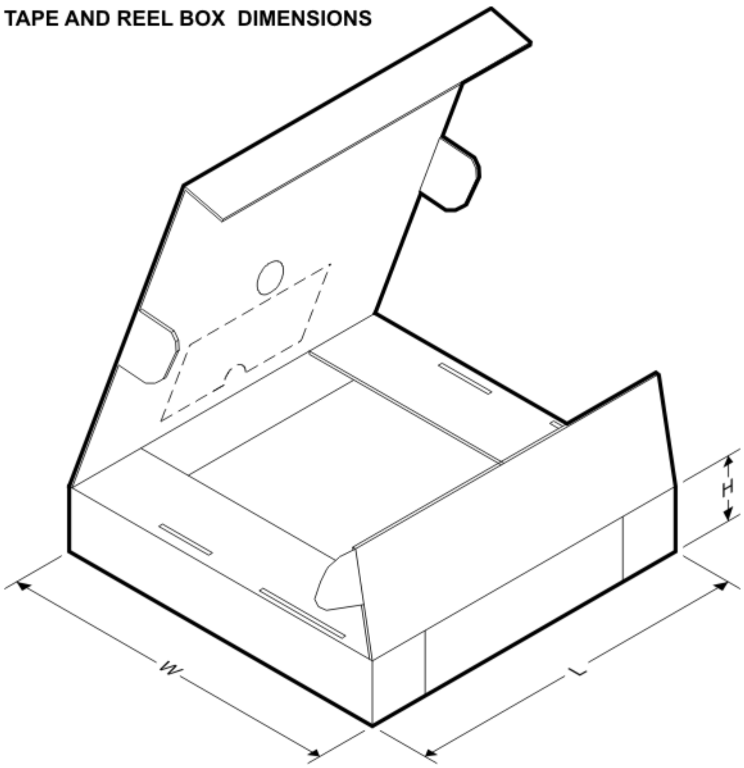
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC2540F128RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2
CC2540F128RHAT	VQFN	RHA	40	250	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2
CC2540F256RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2

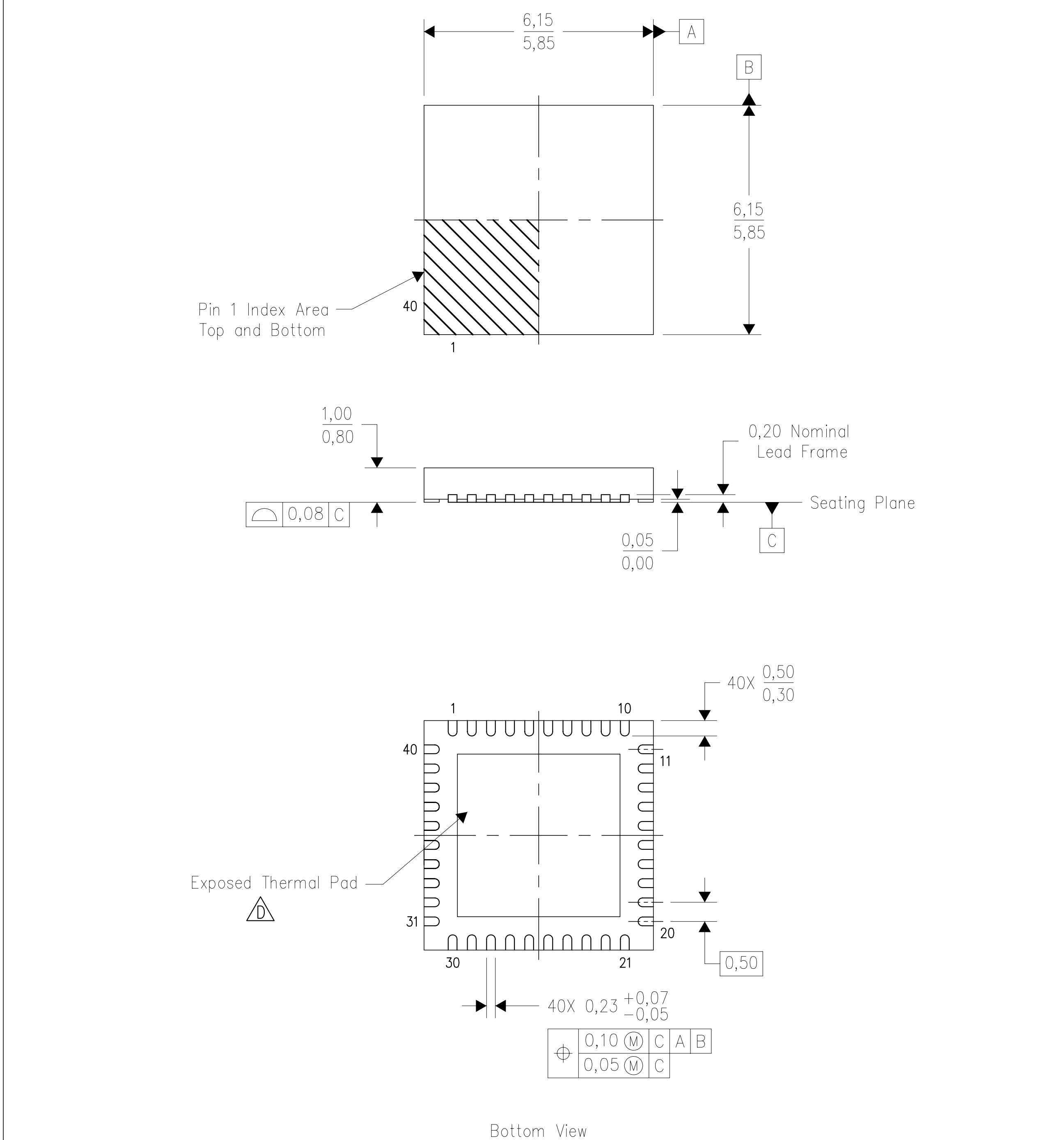
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC2540F128RHAR	VQFN	RHA	40	2500	333.2	345.9	28.6
CC2540F128RHAT	VQFN	RHA	40	250	333.2	345.9	28.6
CC2540F256RHAR	VQFN	RHA	40	2500	333.2	345.9	28.6

RHA (S-PVQFN-N40) PLASTIC QUAD FLATPACK NO-LEAD



4204276/D 08/10

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No−Lead) Package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
- E. Package complies to JEDEC MO−220 variation VJJD−2.

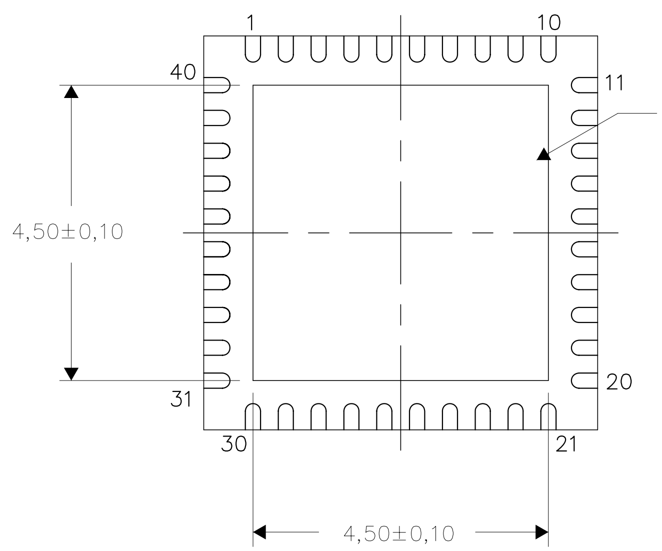
RHA (S-PVQFN-N40) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



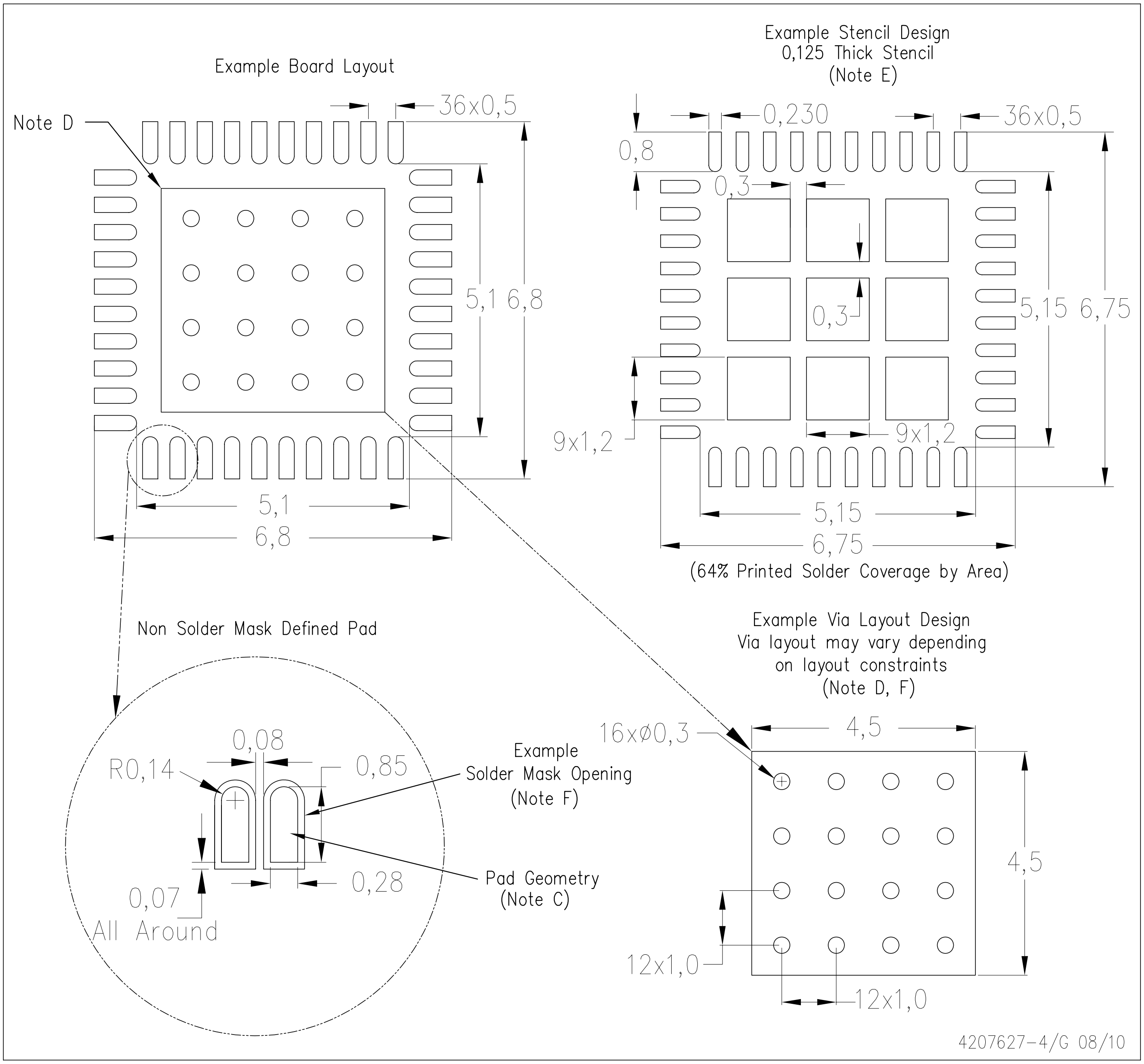
Bottom View

Exposed Thermal Pad Dimensions

4206355-4/L 08/10

NOTES: A. All linear dimensions are in millimeters

RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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