

# Linear LTM2987 Power System Manager Datasheet

<http://www.manuallib.com/linear/ltm2987-power-system-manager-datasheet.html>

The LTM<sup>®</sup>2987 is a 16-channel  $\mu$ Module<sup>®</sup> (micromodule) Power System Manager used to sequence, trim (servo), margin, supervise, manage faults, provide telemetry and create fault logs. PMBus commands support power supply sequencing, precision point-of-load voltage adjustment and margining. DACs use a proprietary soft-connect algorithm to minimize supply disturbances. Supervisory functions include overvoltage and undervoltage threshold limits for sixteen power supply output channels and two power supply input channels, as well as over and under temperature limits. Programmable fault responses can disable the power supplies with optional retry after a fault is detected.

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## FEATURES

- Sequence, Trim, Margin and Supervise 16 Power Supplies
- Manage Faults, Monitor Telemetry and Create Fault Logs
- PMBus™ Compliant Command Set
- Supported by LTpowerPlay™ GUI
- Margin or Trim Supplies to 0.25% Accuracy
- Fast OV/UV Supervisors Per Channel
- Coordinate Sequencing and Fault Management Across Multiple LTC PSM Devices
- Automatic Fault Logging to Internal EEPROM
- Operate Autonomously without Additional Software
- Internal Temperature and Input Voltage Supervisors
- Accurate Monitoring of 16 Output Voltages, Two Input Voltages and Internal Die Temperature
- I<sup>2</sup>C/SMBus Serial Interface
- Can Be Powered from 3.3V, or 4.5V to 15V
- Programmable Watchdog Timer
- Available in 144-Lead 15mm × 15mm BGA Package

## APPLICATIONS

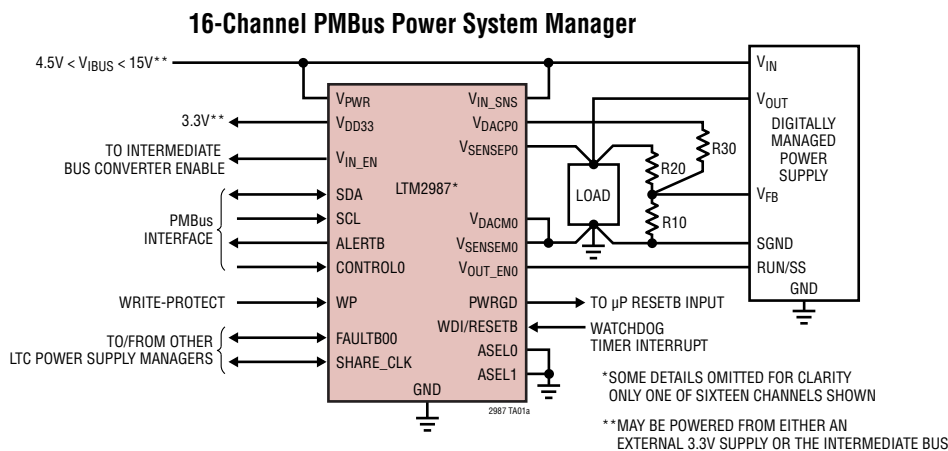
- Computers and Network Servers
- Industrial Test and Measurement
- High Reliability Systems
- Medical Imaging
- Video

## DESCRIPTION

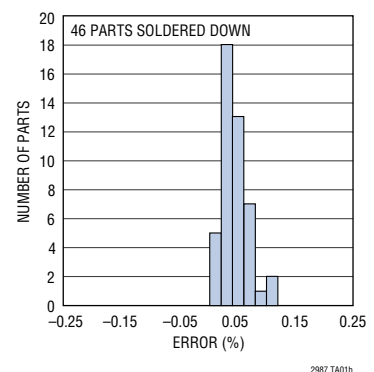
The LTM<sup>®</sup>2987 is a 16-channel  $\mu$ Module<sup>®</sup> (micromodule) Power System Manager used to sequence, trim (servo), margin, supervise, manage faults, provide telemetry and create fault logs. PMBus commands support power supply sequencing, precision point-of-load voltage adjustment and margining. DACs use a proprietary soft-connect algorithm to minimize supply disturbances. Supervisory functions include overvoltage and undervoltage threshold limits for sixteen power supply output channels and two power supply input channels, as well as over and under temperature limits. Programmable fault responses can disable the power supplies with optional retry after a fault is detected. Faults that disable a power supply can automatically trigger black box EEPROM storage of fault status and associated telemetry. An internal 16-bit ADC monitors sixteen output voltages, two input voltages, and die temperature. In addition, odd numbered channels can be configured to measure the voltage across a current sense resistor. A programmable watchdog timer monitors microprocessor activity for a stalled condition and resets the microprocessor if necessary. A single wire bus synchronizes power supplies across multiple LTC Power System Management (PSM) devices. Configuration EEPROM supports autonomous operation without additional software.

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## TYPICAL APPLICATION



**Power Supply Accuracy**



## ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2, 3)

### Supply Voltages:

$V_{PWR}$ to GND .....	-0.3V to 15V
$V_{IN\_SNS}$ to GND.....	-0.3V to 15V
$V_{DD33}$ to GND .....	-0.3V to 3.6V
$V_{DD25}$ to GND .....	-0.3V to 2.75V

### Digital Input/Output Voltages:

ALERTB, SDA, SCL, CONTROL0, CONTROL1 .....	-0.3V to 5.5V
PWRGD, SHARE_CLK, WDI/RESETB, WP .....	-0.3V to $V_{DD33} + 0.3V$
FAULTB00, FAULTB01, FAULTB10, FAULTB11 .....	-0.3V to $V_{DD33} + 0.3V$
ASELO, ASEL1 .....	-0.3V to $V_{DD33} + 0.3V$

### Analog Voltages:

REFP to GND .....	-0.3V to 1.35V
REFM to GND.....	-0.3V to 0.3V
$V_{SENSE[7:0]}$ to GND .....	-0.3V to 6V
$V_{SENSEM[7:0]}$ to GND .....	-0.3V to 6V
$V_{OUT\_EN[3:0]}$ , $V_{IN\_EN}$ to GND .....	-0.3V to 15V
$V_{OUT\_EN[7:4]}$ to GND .....	-0.3V to 6V
$V_{DACP[7:0]}$ to GND .....	-0.3V to 6V
$V_{DACM[7:0]}$ to GND .....	-0.3V to 0.3V

### Pull-Up Resistors:

$V_{PU}$ .....	-0.3V to 5.5V
$R_{PU1}$ , $R_{PU2}$ , $R_{PU3}$ , $R_{PU4}$ .....	-0.3V to 5.5V

### Operating Junction Temperature Range:

LTM2987C .....	0°C to 70°C
LTM2987I .....	-40°C to 105°C*

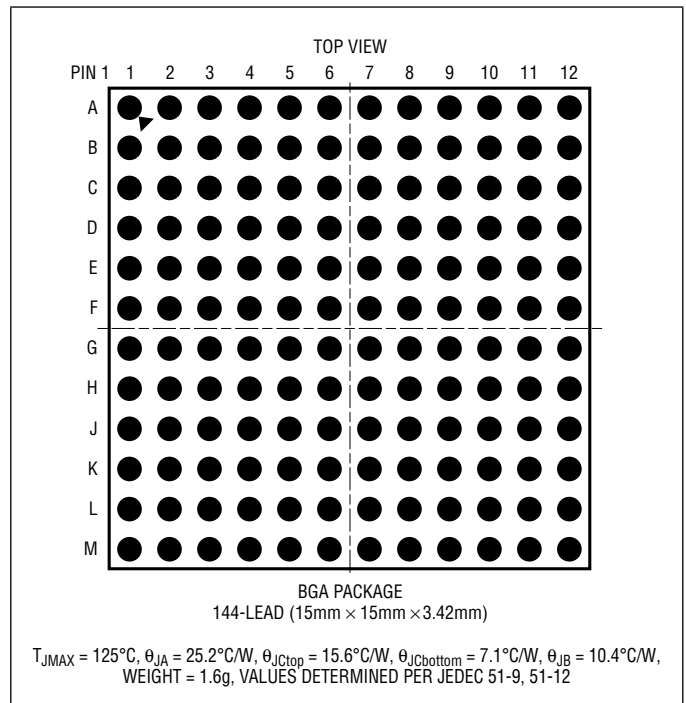
Storage Temperature Range ..... -55°C to 125°C\*

Maximum Junction Temperature ..... 125°C\*

Maximum Solder Temperature..... 245°C

\*See OPERATION section of the LTC2977 data sheet for detailed EEPROM derating information for junction temperatures in excess of 105°C.

## PIN CONFIGURATION



## ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	OPERATING JUNCTION TEMPERATURE RANGE
		DEVICE	FINISH CODE			
LTM2987CY#PBF	SAC305 (RoHS)	LTM2987Y	e1	BGA	3	0°C to 70°C
LTM2987IY#PBF	SAC305 (RoHS)	LTM2987Y	e1	BGA	3	-40°C to 105°C

Consult Marketing for parts specified with wider operating temperature ranges. \*Device temperature grade is indicated by a label on the shipping container. Pad or ball finish code is per IPC/JEDEC J-STD-609.

• Terminal Finish Part Marking:  
[www.linear.com/leadfree](http://www.linear.com/leadfree)

• Recommended LGA and BGA PCB Assembly and Manufacturing Procedures:

[www.linear.com/umodule/pcbassembly](http://www.linear.com/umodule/pcbassembly)

• LGA and BGA Package and Tray Drawings:

[www.linear.com/packaging](http://www.linear.com/packaging)

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_J = 25^\circ\text{C}$ .  $V_{PWR} = V_{IN\_SNS} = 12\text{V}$ ,  $V_{DD33}$ , REFP and REFM pins floating, unless otherwise indicated. (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>Power-Supply Characteristics</b>							
$V_{PWR}$	$V_{PWR}$ Supply Input Operating Range		● 4.5		15	V	
$I_{PWR}$	$V_{PWR}$ Supply Current	$4.5\text{V} \leq V_{PWR} \leq 15\text{V}$ , $V_{DD33}$ Floating	●	10	13	mA	
$I_{VDD33}$	$V_{DD33}$ Supply Current	$3.13\text{V} \leq V_{DD33} \leq 3.47\text{V}$ , $V_{PWR} = V_{DD33}$	●	10	13	mA	
$V_{UVLO\_VDD33}$	$V_{DD33}$ Undervoltage Lockout	$V_{DD33}$ Ramping Up, $V_{PWR} = V_{DD33}$	●	2.35	2.55	2.8	V
	$V_{DD33}$ Undervoltage Lockout Hysteresis			120		mV	
$V_{DD33}$	Supply Input Operating Range	$V_{PWR} = V_{DD33}$	●	3.13		3.47	V
	Regulator Output Voltage	$4.5\text{V} \leq V_{PWR} \leq 15\text{V}$	●	3.13	3.26	3.47	V
	Regulator Output Short-Circuit Current	$V_{PWR} = 4.5\text{V}$ , $V_{DD33} = 0\text{V}$	●	75	90	140	mA
$V_{DD25}$	Regulator Output Voltage	$3.13\text{V} \leq V_{DD33} \leq 3.47\text{V}$	●	2.35	2.5	2.6	V
	Regulator Output Short-Circuit Current	$V_{PWR} = V_{DD33} = 3.47\text{V}$ , $V_{DD25} = 0\text{V}$	●	30	55	80	mA
$t_{INIT}$	Initialization Time	Time from $V_{IN}$ Applied Until the TON_DELAY Timer Starts		30		ms	
<b>Voltage Reference Characteristics</b>							
$V_{REF}$	Output Voltage			1.232		V	
	Temperature Coefficient			3		ppm/ $^\circ\text{C}$	
	Hysteresis	(Note 4)		100		ppm	
<b>ADC Characteristics</b>							
$V_{IN\_ADC}$	Voltage Sense Input Range	Differential Voltage: $V_{IN\_ADC} = (V_{SENSEPN} - V_{SENSEMN})$	●	0	6	V	
		Single-Ended Voltage: $V_{SENSEMN}$	●	-0.1	0.1	V	
	Current Sense Input Range (Odd Numbered Channels Only)	Single-Ended Voltage: $V_{SENSEPN}$ , $V_{SENSEMN}$	●	-0.1	6	V	
		Differential Voltage: $V_{IN\_ADC}$	●	-170	170	mV	
$N\_ADC$	Voltage Sense Resolution (Uses L16 Format)	$0\text{V} \leq V_{IN\_ADC} \leq 6\text{V}$ $Mfr\_config\_adc\_hires = 0$		122		$\mu\text{V}/\text{LSB}$	
	Current Sense Resolution (Odd Numbered Channels Only)	$0\text{mV} \leq  V_{IN\_ADC}  < 16\text{mV}$ (Note 5)		15.625		$\mu\text{V}/\text{LSB}$	
		$16\text{mV} \leq  V_{IN\_ADC}  < 32\text{mV}$		31.25		$\mu\text{V}/\text{LSB}$	
$32\text{mV} \leq  V_{IN\_ADC}  < 63.9\text{mV}$			62.5		$\mu\text{V}/\text{LSB}$		
	$63.9\text{mV} \leq  V_{IN\_ADC}  < 127.9\text{mV}$		125		$\mu\text{V}/\text{LSB}$		
	$127.9\text{mV} \leq  V_{IN\_ADC} $		250		$\mu\text{V}/\text{LSB}$		
		$Mfr\_config\_adc\_hires = 1$					
$TUE\_ADC\_VOLT\_SNS$	Total Unadjusted Error	Voltage Sense Mode $V_{IN\_ADC} \geq 1\text{V}$	●		$\pm 0.25$	% of Reading	
		Voltage Sense Mode $0 \leq V_{IN\_ADC} \leq 1\text{V}$	●		$\pm 2.5$	mV	
$TUE\_ADC\_CURR\_SNS$	Total Unadjusted Error	Current Sense Mode, Odd Numbered Channels Only, $20\text{mV} \leq V_{IN\_ADC} \leq 170\text{mV}$	●		$\pm 0.7$	% of Reading	
		Current Sense Mode, Odd Numbered Channels Only, $V_{IN\_ADC} \leq 20\text{mV}$	●		140	$\mu\text{V}$	
$V_{OS\_ADC}$	Offset Error	Current Sense Mode, Odd Numbered Channels Only	●		$\pm 35$	$\mu\text{V}$	
$t_{CONV\_ADC}$	Conversion Time	Voltage Sense Mode (Note 6)		6.15		ms	
		Current Sense Mode (Note 6)		24.6		ms	
		Temperature Input (Note 6)		24.6		ms	

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## ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_{UPDATE\_ADC}$	Maximum Update Time	Odd Numbered Channels in Current Sense Mode (Note 6)		160		ms
$C_{IN\_ADC}$	Input Sampling Capacitance			1		pF
$f_{IN\_ADC}$	Input Sampling Frequency			62.5		kHz
$I_{IN\_ADC}$	Input Leakage Current	$V_{IN\_ADC} = 0\text{V}$ , $0\text{V} \leq V_{COMMONMODE} \leq 6\text{V}$ , Current Sense Mode	●		±0.5	μA
	Differential Input Current	$V_{IN\_ADC} = 0.17\text{V}$ , Current Sense Mode	●	80	250	nA
		$V_{IN\_ADC} = 6\text{V}$ , Voltage Sense Mode	●	10	15	μA

### DAC Output Characteristics

$N\_VDACP$	Resolution			10		Bits		
$V_{FS\_VDACP}$	Full-Scale Output Voltage (Programmable)	DAC Code = 0x3FF	Buffer Gain Setting_0	●	1.3	1.38	1.44	V
		DAC Polarity = 1	Buffer Gain Setting_1	●	2.5	2.65	2.77	V
$INL\_VDACP$	Integral Nonlinearity	(Note 7)	●			±2	LSB	
$DNL\_VDACP$	Differential Nonlinearity	(Note 7)	●			±2.4	LSB	
$V_{OS\_VDACP}$	Offset Voltage	(Note 7)	●			±10	mV	
$V_{DACP}$	Load Regulation ( $V_{DACPn} - V_{DACMn}$ )	$V_{DACPn} = 2.65\text{V}$ , $I_{VDACPn}$ Sourcing = 2mA			100		ppm/mA	
		$V_{DACPn} = 0.1\text{V}$ , $I_{VDACPn}$ Sinking = 2mA			100		ppm/mA	
	PSRR ( $V_{DACPn} - V_{DACMn}$ )	DC: $3.13\text{V} \leq V_{DD33} \leq 3.47\text{V}$ , $V_{PWR} = V_{DD33}$			60		dB	
		100mV Step in 20ns with 50pF Load			40		dB	
	DC CMRR ( $V_{DACPn} - V_{DACMn}$ )	$-0.1\text{V} \leq V_{DACMn} \leq 0.1\text{V}$			60		dB	
	Leakage Current	$V_{DACPn}$ Hi-Z, $0\text{V} \leq V_{DACPn} \leq 6\text{V}$	●			±100	nA	
	Short-Circuit Current Low	$V_{DACPn}$ Shorted to GND	●	-10		-4	mA	
	Short-Circuit Current High	$V_{DACPn}$ Shorted to $V_{DD33}$	●	4		10	mA	
$C_{OUT}$	Output Capacitance	$V_{DACPn}$ Hi-Z			10	pF		
$t_{S\_VDACP}$	DAC Output Update Rate	Fast Servo Mode			250	μs		

### DAC Soft-Connect Comparator Characteristics

$V_{OS\_CMP}$	Offset Voltage	$V_{DACPn} = 0.2\text{V}$	●	±1	±18	mV
		$V_{DACPn} = 1.3\text{V}$	●	±2	±26	mV
		$V_{DACPn} = 2.65\text{V}$	●	±3	±52	mV

### Voltage Supervisor Characteristics

$V_{IN\_VS}$	Input Voltage Range (Programmable)	$V_{IN\_VS} = (V_{SENSEn} - V_{SENSEMn})$	Low Resolution Mode	●	0	6	V
			High Resolution Mode	●	0	3.8	V
		Single-Ended Voltage: $V_{SENSEMn}$	●	-0.1	0.1	V	
$N\_VS$	Voltage Sensing Resolution	0V to 3.8V Range: High Resolution Mode			4		mV/LSB
		0V to 6V Range: Low Resolution Mode			8		mV/LSB
$TUE\_VS$	Total Unadjusted Error	$2\text{V} \leq V_{IN\_VS} \leq 6\text{V}$ , Low Resolution Mode	●			±1.25	% of Reading
		$1.5\text{V} < V_{IN\_VS} \leq 3.8\text{V}$ , High Resolution Mode	●			±1.0	% of Reading
		$0.8\text{V} \leq V_{IN\_VS} \leq 1.5\text{V}$ , High Resolution Mode	●			±1.5	% of Reading
$t_{S\_VS}$	Update Rate				12.21		μs

## ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
<b><math>V_{IN\_SNS}</math> Input Characteristics</b>							
$V_{IN\_SNS}$	$V_{IN\_SNS}$ Input Voltage Range		●	0		15	V
$R_{VIN\_SNS}$	$V_{IN\_SNS}$ Input Resistance		●	70	90	110	k $\Omega$
$TUE_{VIN\_SNS}$	VIN_ON, VIN_OFF Threshold Total Unadjusted Error	$3\text{V} \leq V_{VIN\_SNS} \leq 8\text{V}$	●			$\pm 2.0$	% of Reading
		$V_{VIN\_SNS} > 8\text{V}$	●			$\pm 1.0$	% of Reading
	READ_VIN Total Unadjusted Error	$3\text{V} \leq V_{VIN\_SNS} \leq 8\text{V}$	●			$\pm 1.5$	% of Reading
		$V_{VIN\_SNS} > 8\text{V}$	●			$\pm 1.0$	% of Reading
<b>Temperature Sensor Characteristics</b>							
$TUE_{TS}$	Total Unadjusted Error				$\pm 1$		$^\circ\text{C}$
<b><math>V_{OUT\_ENn}</math> Output (<math>V_{OUT\_EN}</math> [3:0]) Characteristics</b>							
$V_{VOUT\_ENn}$	Output High Voltage (Note 8)	$I_{VOUT\_ENn} = -5\mu\text{A}$ , $V_{DD33} = 3.3\text{V}$	●	10	12.5	14.7	V
$I_{VOUT\_ENn}$	Output Sourcing Current	$V_{VOUT\_ENn}$ Pull-Up Enabled, $V_{VOUT\_ENn} = 1\text{V}$	●	-5	-6	-8	$\mu\text{A}$
	Output Sinking Current	Strong Pull-Down Enabled, $V_{VOUT\_ENn} = 0.4\text{V}$	●	3	5	8	mA
		Weak Pull-Down Enabled, $V_{VOUT\_ENn} = 0.4\text{V}$	●	33	50	60	$\mu\text{A}$
	Output Leakage Current	Internal Pull-Up Disabled, $0\text{V} \leq V_{VOUT\_ENn} \leq 15\text{V}$	●			$\pm 1$	$\mu\text{A}$
<b><math>V_{OUT\_ENn}</math> Output (<math>V_{OUT\_EN}</math> [7:4]) Characteristics</b>							
$I_{VOUT\_ENn}$	Output Sinking Current	Strong Pull-Down Enabled, $V_{OUT\_ENn} = 0.1\text{V}$	●	3	6	9	mA
	Output Leakage Current	$0\text{V} \leq V_{VOUT\_ENn} \leq 6\text{V}$	●			$\pm 1$	$\mu\text{A}$
<b><math>V_{IN\_EN}</math> Enable Output (<math>V_{IN\_EN}</math>) Characteristics</b>							
$V_{VIN\_EN}$	Output High Voltage	$I_{VIN\_EN} = -5\mu\text{A}$ , $V_{DD33} = 3.3\text{V}$	●	10	12.5	14.7	V
$I_{VIN\_EN}$	Output Sourcing Current	$V_{IN\_EN}$ Pull-Up Enabled, $V_{VIN\_EN} = 1\text{V}$	●	-5	-6	-8	$\mu\text{A}$
	Output Sinking Current	$V_{VIN\_EN} = 0.4\text{V}$	●	3	5	8	mA
	Leakage Current	Internal Pull-Up Disabled, $0\text{V} \leq V_{VIN\_EN} \leq 15\text{V}$	●			$\pm 1$	$\mu\text{A}$
<b>EEPROM Characteristics</b>							
Endurance	(Notes 9, 10)	$0^\circ\text{C} < T_J < 85^\circ\text{C}$ During EEPROM Write Operations	●	10,000			Cycles
Retention	(Notes 9, 10)	$T_J < 105^\circ\text{C}$	●	20			Years
Mass_Write	Mass Write Operation Time (Note 11)	STORE_USER_ALL, $0^\circ\text{C} < T_J < 85^\circ\text{C}$ During EEPROM Write Operations	●		440	4100	ms
<b>General Purpose Pull-Up Resistors</b>							
$R_{PU}$	Pull-Up Resistance				10		k $\Omega$
<b>Digital Inputs SCL, SDA, CONTROL0, CONTROL1, WDI/RESETB, FAULTB00, FAULTB01, FAULTB10, FAULTB11, WP</b>							
$V_{IH}$	High Level Input Voltage		●	2.1			V
$V_{IL}$	Low Level Input Voltage		●			1.5	V
$V_{HYST}$	Input Hysteresis				20		mV

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
$I_{LEAK}$	Input Leakage Current	$0\text{V} \leq V_{PIN} \leq 5.5\text{V}$ , SDA, SCL, CONTROL $n$ Pins Only	●		±2	μA	
		$0\text{V} \leq V_{PIN} \leq V_{DD33} + 0.3\text{V}$ , FAULTB $zn$ , WDI/RESETB, WP Pins Only	●		±2	μA	
$t_{SP}$	Pulse Width of Spike Suppressed	FAULTB $zn$ , CONTROL $n$ Pins Only		10		μs	
		SDA, SCL Pins Only		98		ns	
$t_{FAULT\_MIN}$	Minimum Low Pulse Width for Externally Generated Faults		110			ms	
$t_{RESETB}$	Pulse Width to Assert Reset	$V_{WDI/RESETB} \leq 1.5\text{V}$	●	300		μs	
$t_{WDI}$	Pulse Width to Reset Watchdog Timer	$V_{WDI/RESETB} \leq 1.5\text{V}$	●	0.3	200	μs	
$f_{WDI}$	Watchdog Interrupt Input Frequency		●		1	MHz	
$C_{IN}$	Digital Input Capacitance			10		pF	
<b>Digital Input SHARE_CLK</b>							
$V_{IH}$	High Level Input Voltage		●	1.6		V	
$V_{IL}$	Low Level Input Voltage		●		0.8	V	
$f_{SHARE\_CLK\_IN}$	Input Frequency Operating Range		●	90	110	kHz	
$t_{LOW}$	Assertion Low Time	$V_{SHARE\_CLK} < 0.8\text{V}$	●	0.825	1.1	μs	
$t_{RISE}$	Rise Time	$V_{SHARE\_CLK} < 0.8\text{V}$ to $V_{SHARE\_CLK} > 1.6\text{V}$	●		450	ns	
$I_{LEAK}$	Input Leakage Current	$0\text{V} \leq V_{SHARE\_CLK} \leq V_{DD33} + 0.3\text{V}$	●		±1	μA	
$C_{IN}$	Input Capacitance			10		pF	
<b>Digital Outputs SDA, ALERTB, PWRGD, SHARE_CLK, FAULTB00, FAULTB01, FAULTB10, FAULTB11</b>							
$V_{OL}$	Digital Output Low Voltage	$I_{SINK} = 3\text{mA}$	●		0.4	V	
$f_{SHARE\_CLK\_OUT}$	Output Frequency Operating Range	5.49kΩ Pull-Up to $V_{DD33}$	●	90	100	110	kHz
<b>Digital Inputs ASELO,ASEL1</b>							
$V_{IH}$	Input High Threshold Voltage		●	$V_{DD33} - 0.5$		V	
$V_{IL}$	Input Low Threshold Voltage		●		0.5	V	
$I_{IH}, I_{IL}$	High, Low Input Current	$ASEL[1:0] = 0, V_{DD33}$	●		±95	μA	
$I_{HIZ}$	Hi-Z Input Current		●		±24	μA	
$C_{IN}$	Input Capacitance			10		pF	
<b>Serial Bus Timing Characteristics</b>							
$f_{SCL}$	Serial Clock Frequency (Note 12)		●	10	400	kHz	
$t_{LOW}$	Serial Clock Low Period (Note 12)		●	1.3		μs	
$t_{HIGH}$	Serial Clock High Period (Note 12)		●	0.6		μs	
$t_{BUF}$	Bus Free Time Between Stop and Start (Note 12)		●	1.3		μs	
$t_{HD\_STA}$	Start Condition Hold Time (Note 12)		●	600		ns	
$t_{SU\_STA}$	Start Condition Setup Time (Note 12)		●	600		ns	
$t_{SU\_STO}$	Stop Condition Setup Time (Note 12)		●	600		ns	
$t_{HD\_DAT}$	Data Hold Time (LTM2987 Receiving Data) (Note 12)		●	0		ns	
	Data Hold Time (LTM2987 Transmitting Data) (Note 12)		●	300	900	ns	



## ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_{\text{SU,DAT}}$	Data Setup Time (Note 12)		●	100		ns
$t_{\text{SP}}$	Pulse Width of Spike Suppressed (Note 12)			98		ns
$t_{\text{TIMEOUT\_BUS}}$	Time Allowed to Complete any PMBus Command After Which Time SDA Will Be Released and Command Terminated	Longer Timeout = 0	●	25	35	ms
		Longer Timeout = 1	●	200	280	ms

### Additional Digital Timing Characteristics

$t_{\text{OFF\_MIN}}$	Minimum Off Time for Any Channel			100		ms
-----------------------	----------------------------------	--	--	-----	--	----

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating for extended periods may affect device reliability and lifetime.

**Note 2:** All currents into device pins are positive. All currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified. If power is supplied to the chip via the  $V_{DD33}$  pin only, connect  $V_{PWR}$  and  $V_{DD33}$  pins together.

**Note 3:** The LTM2987 electrical characteristics apply to each half of the device, unless otherwise noted. The specifications and functions are the same for both Device A pins and Device B pins.

**Note 4:** Hysteresis in the output voltage is created by package stress that differs depending on whether the module was previously at a higher or lower temperature. Output voltage is always measured at  $25^\circ\text{C}$ , but the module is cycled to  $105^\circ\text{C}$  or  $-40^\circ\text{C}$  before successive measurements. Hysteresis is roughly proportional to the square of the temperature change.

**Note 5:** The current sense resolution is determined by the L11 format and the mV units of the returned value. For example a full scale value of 170mV returns a L11 value of  $0xF2A8 = 680 \cdot 2^{-2} = 170$ . This is the lowest range that can represent this value without overflowing the L11 mantissa and the resolution for 1LSB in this range is  $2^{-2} \text{mV} = 250\mu\text{V}$ . Each successively lower range improves resolution by cutting the LSB size in half.

**Note 6:** The time between successive ADC conversions (latency of the ADC) for any given channel is given as:  $36.9\text{ms} + (6.15\text{ms} \cdot \text{number of ADC channels configured in Low Resolution mode}) + (24.6\text{ms} \cdot \text{number of ADC channels configured in High Resolution mode})$ .

**Note 7:** Nonlinearity is defined from the first code that is greater than or equal to the maximum offset specification to full-scale code, 1023.

**Note 8:** Output enable pins are charge pumped from  $V_{DD33}$ .

**Note 9:** EEPROM endurance and retention are guaranteed by design, characterization and correlation with statistical process controls. The minimum retention specification applies for devices whose EEPROM has been cycled less than the minimum endurance specification.

**Note 10:** EEPROM endurance and retention will be degraded when  $T_J > 105^\circ\text{C}$ .

**Note 11:** The LTM2987 will not acknowledge any PMBus commands while a mass write operation is being executed. This includes the STORE\_USER\_ALL and MFR\_FAULT\_LOG\_STORE commands or a fault log store initiated by a channel faulting off.

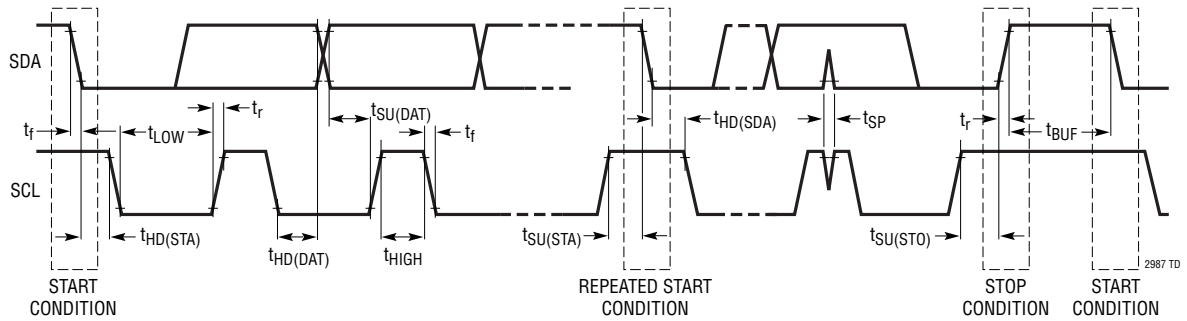
**Note 12:** Maximum capacitive load,  $C_B$ , for SCL and SDA is 400pF. Data and clock rise time ( $t_r$ ) and fall time ( $t_f$ ) are:

$$(20 + 0.1 \cdot C_B) \text{ (ns)} < t_r < 300\text{ns} \text{ and } (20 + 0.1 \cdot C_B) \text{ (ns)} < t_f < 300\text{ns}.$$

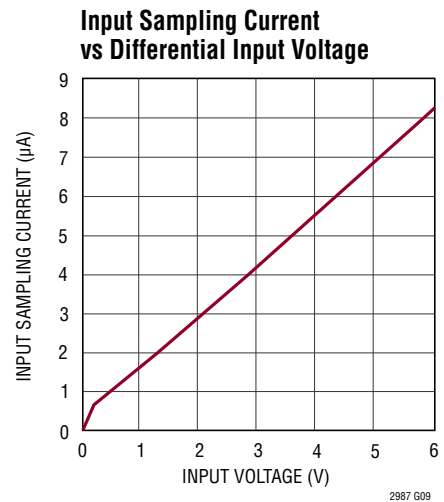
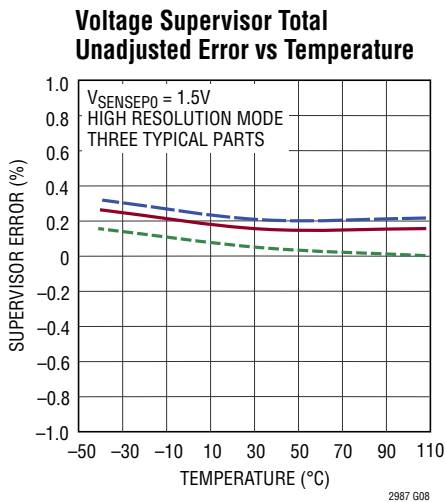
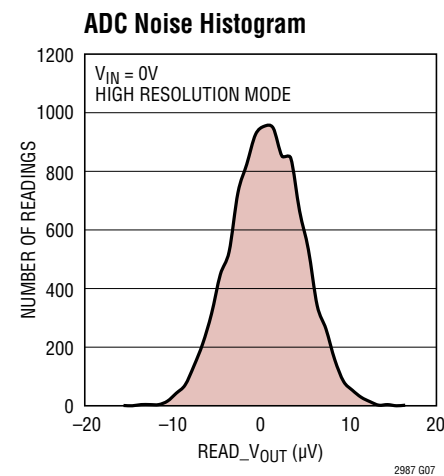
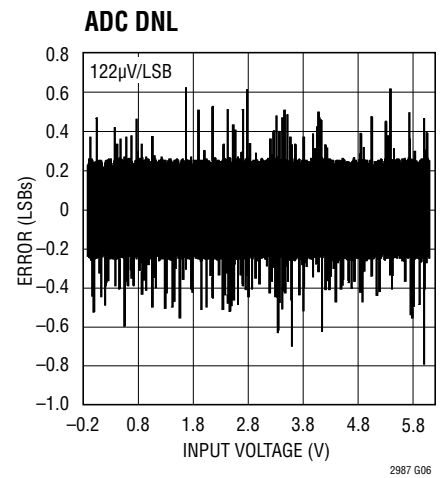
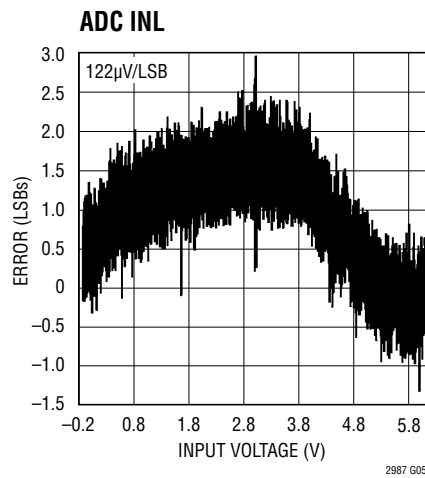
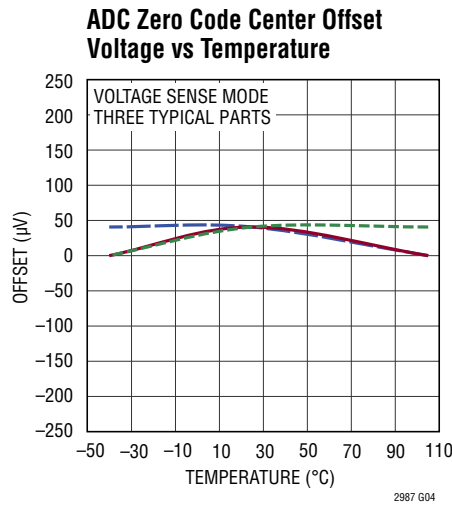
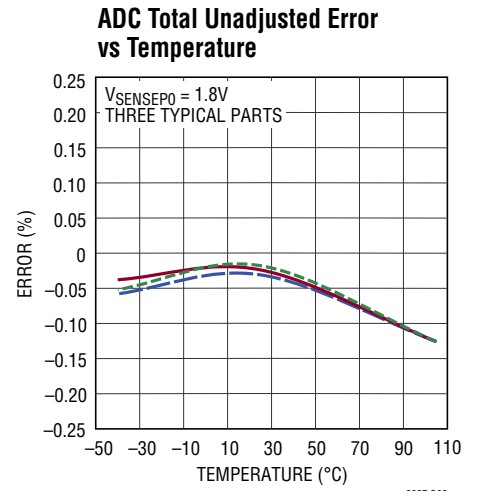
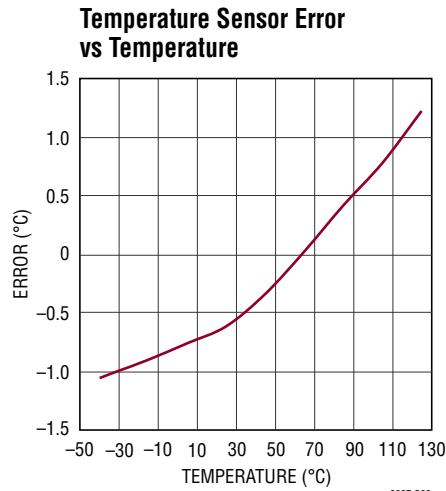
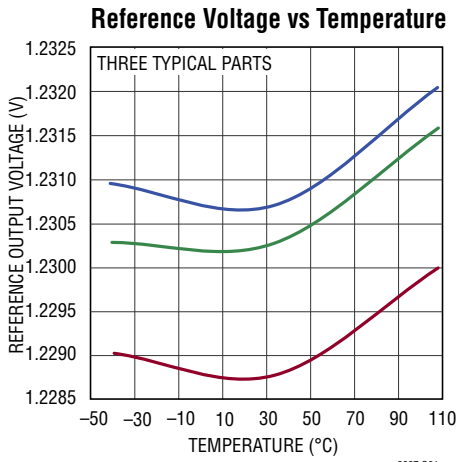
$C_B$  = capacitance of one bus line in pF. SCL and SDA external pull-up voltage,  $V_{I0}$ , is  $3.13\text{V} < V_{I0} < 5.5\text{V}$ .



**PMBUS TIMING DIAGRAM**

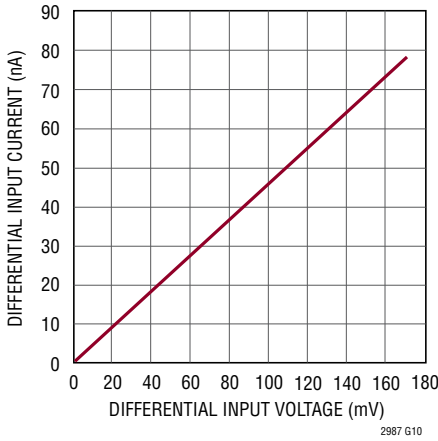


# TYPICAL PERFORMANCE CHARACTERISTICS

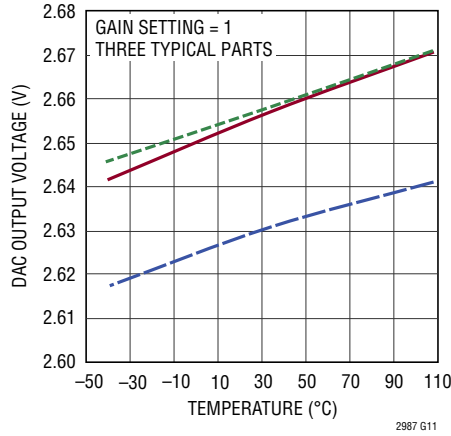


**TYPICAL PERFORMANCE CHARACTERISTICS**

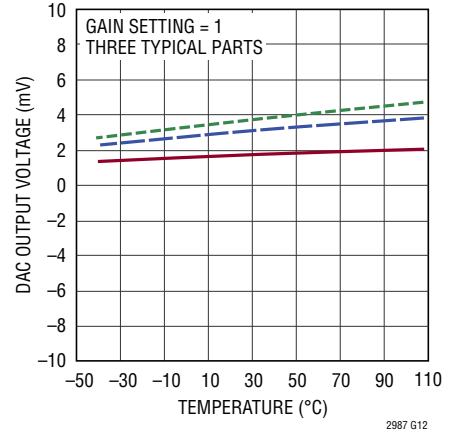
**ADC High Resolution Mode  
Differential Input Current**



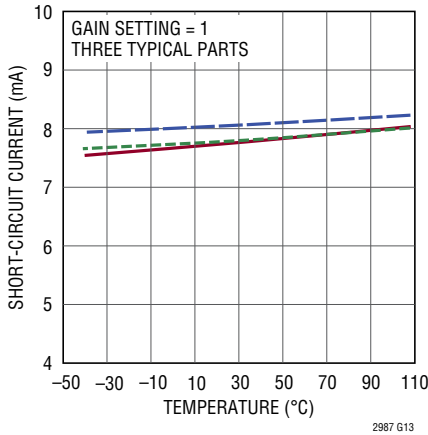
**DAC Full-Scale Output Voltage vs  
Temperature**



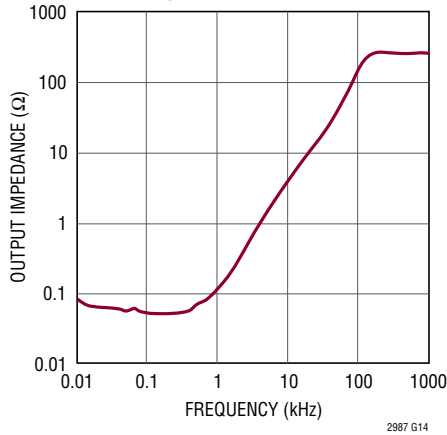
**DAC Offset Voltage vs  
Temperature**



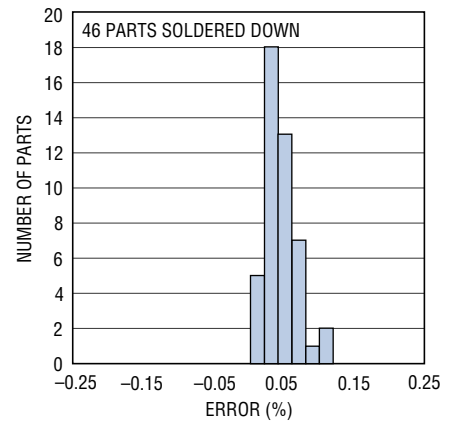
**DAC Short-Circuit Current vs  
Temperature**



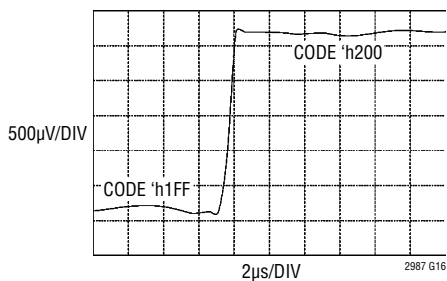
**DAC Output Impedance vs  
Frequency**



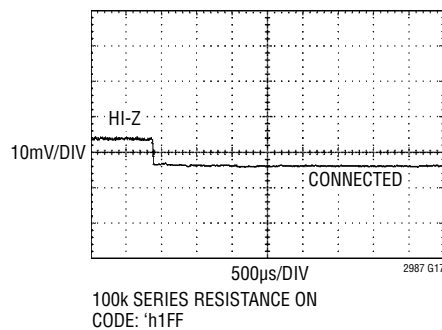
**Closed-Loop Servo Accuracy**



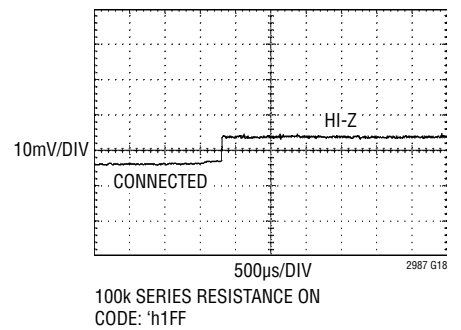
**DAC Transient Response to 1LSB  
DAC Code Change**



**DAC Soft-Connect Transient  
Response When Transitioning  
from Hi-Z State to ON State**

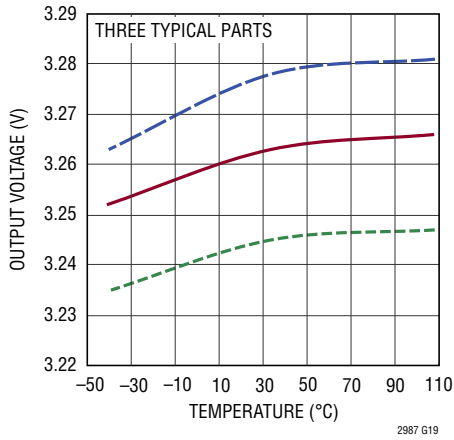


**DAC Soft-Connect Transient  
Response When Transitioning  
from ON State to Hi-Z State**

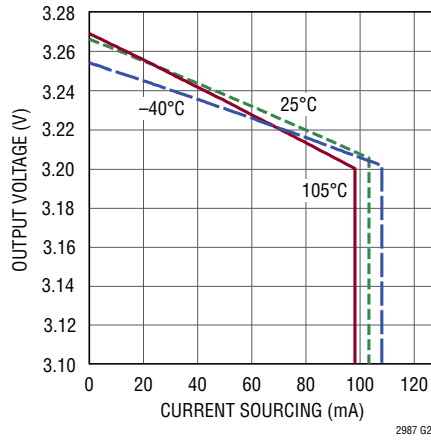


# TYPICAL PERFORMANCE CHARACTERISTICS

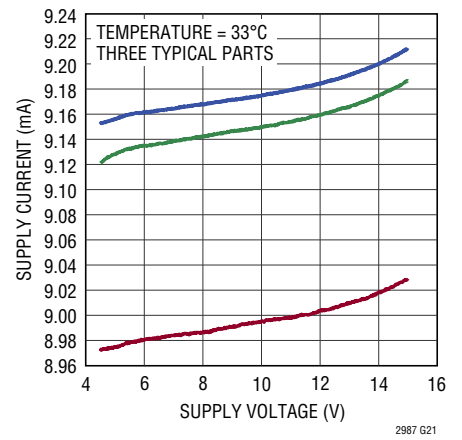
**V<sub>DD33</sub> Regulator Output Voltage vs Temperature**



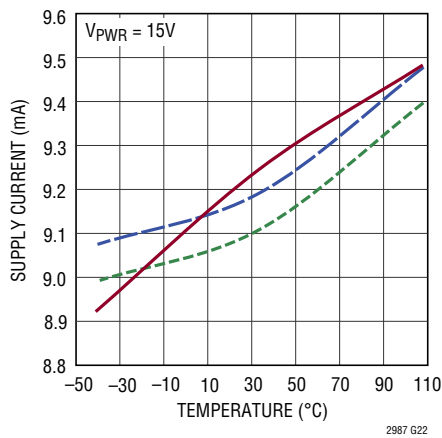
**V<sub>DD33</sub> Regulator Load Regulation**



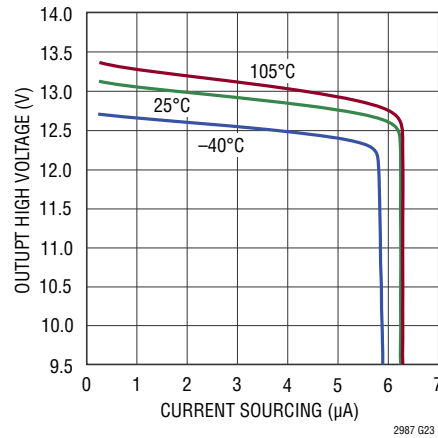
**Supply Current vs Supply Voltage (1/2 LTM2987)**



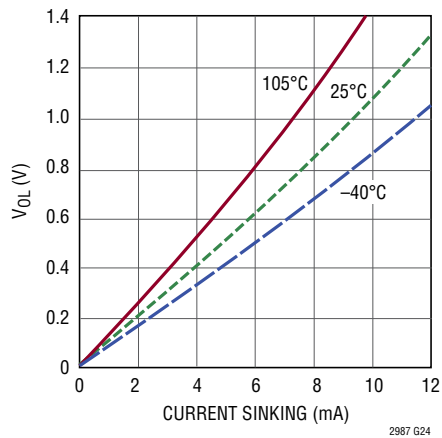
**Supply Current vs Temperature (1/2 LTM2987)**



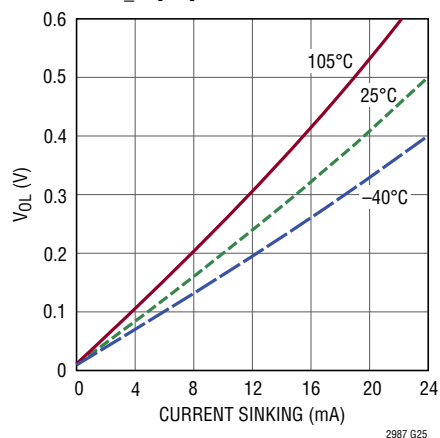
**V<sub>OUT\_EN[3:0]</sub> and V<sub>IN\_EN</sub> Output High Voltage vs Current**



**V<sub>OUT\_EN[3:0]</sub> and V<sub>IN\_EN</sub> Output V<sub>OL</sub> vs Current**



**V<sub>OUT\_EN[7:4]</sub> V<sub>OL</sub> vs Current**



## PIN FUNCTIONS

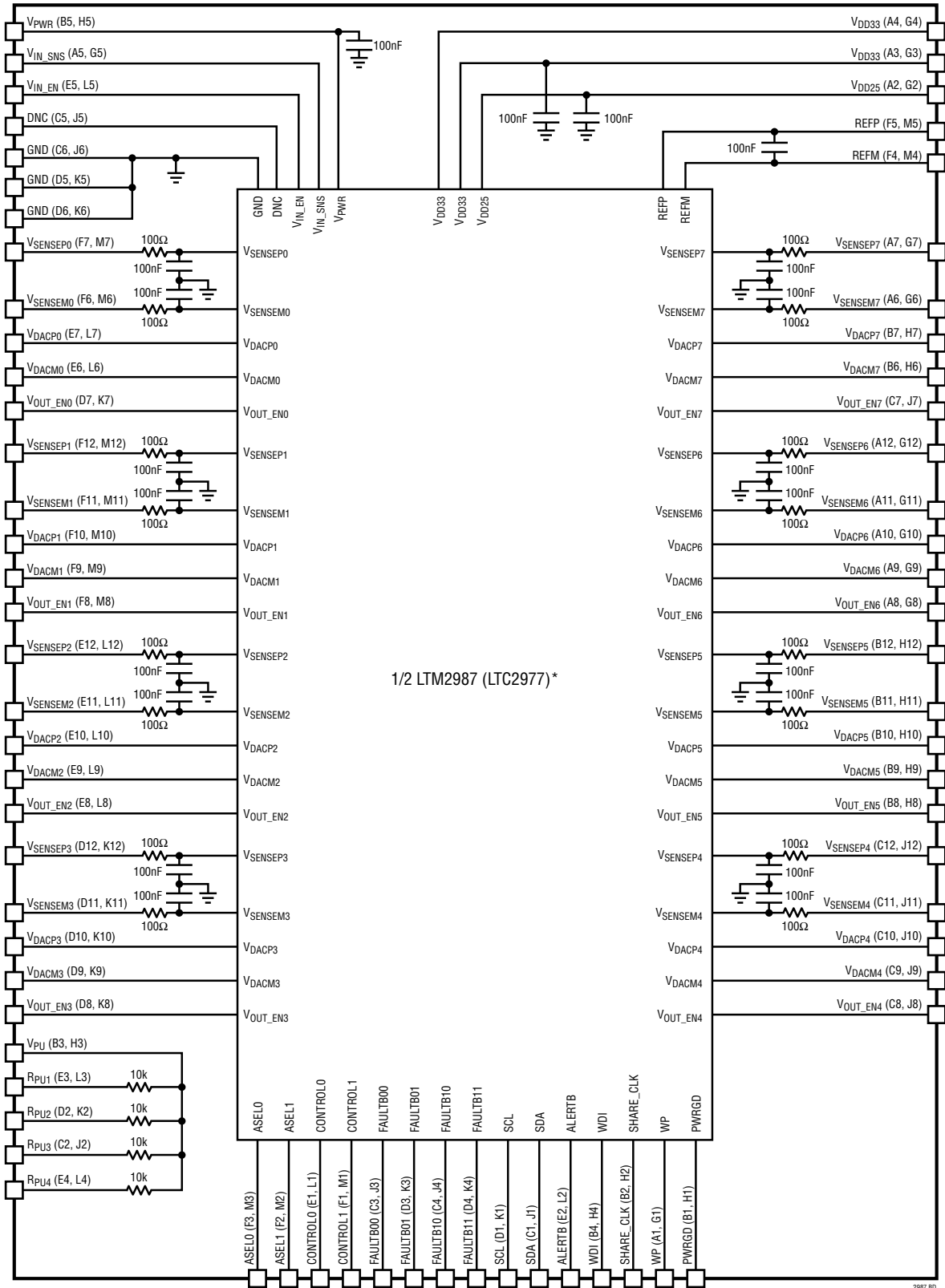
PIN NAME	PIN		PIN TYPE	DESCRIPTION
	Device A	Device B		
V <sub>SENSE</sub> P0	F7*	M7*	In	DC/DC Converter Differential (+) Output Voltage-0 Sensing Pin
V <sub>SENSE</sub> M0	F6*	M6*	In	DC/DC Converter Differential (-) Output Voltage-0 Sensing Pin
V <sub>SENSE</sub> P1	F12*	M12*	In	DC/DC Converter Differential (+) Output Voltage or Current-1 Sensing Pins.
V <sub>SENSE</sub> M1	F11*	M11*	In	DC/DC Converter Differential (-) Output Voltage or Current-1 Sensing Pins.
V <sub>SENSE</sub> P2	E12*	L12*	In	DC/DC Converter Differential (+) Output Voltage-2 Sensing Pin
V <sub>SENSE</sub> M2	E11*	L11*	In	DC/DC Converter Differential (-) Output Voltage-2 Sensing Pin
V <sub>SENSE</sub> P3	D12*	K12*	In	DC/DC Converter Differential (+) Output Voltage or Current-3 Sensing Pins.
V <sub>SENSE</sub> M3	D11*	K11*	In	DC/DC Converter Differential (-) Output Voltage or Current-3 Sensing Pins.
V <sub>SENSE</sub> P4	C12*	J12*	In	DC/DC Converter Differential (+) Output Voltage-4 Sensing Pin
V <sub>SENSE</sub> M4	C11*	J11*	In	DC/DC Converter Differential (-) Output Voltage-4 Sensing Pin
V <sub>SENSE</sub> P5	B12*	H12*	In	DC/DC Converter Differential (+) Output Voltage or Current-5 Sensing Pins.
V <sub>SENSE</sub> M5	B11*	H11*	In	DC/DC Converter Differential (-) Output Voltage or Current-5 Sensing Pins.
V <sub>SENSE</sub> P6	A12*	G12*	In	DC/DC Converter Differential (+) Output Voltage-6 Sensing Pin
V <sub>SENSE</sub> M6	A11*	G11*	In	DC/DC Converter Differential (-) Output Voltage-6 Sensing Pin
V <sub>SENSE</sub> P7	A7*	G7*	In	DC/DC Converter Differential (+) Output Voltage or Current-7 Sensing Pin
V <sub>SENSE</sub> M7	A6*	G6*	In	DC/DC Converter Differential (-) Output Voltage or Current-7 Sensing Pin
V <sub>OUT_EN</sub> 0	D7	K7	Out	DC/DC Converter Enable-0 Pin. Output High Voltage Optionally Pulled Up to 12V by 5μA
V <sub>OUT_EN</sub> 1	F8	M8	Out	DC/DC Converter Enable-1 Pin. Output High Voltage Optionally Pulled Up to 12V by 5μA
V <sub>OUT_EN</sub> 2	E8	L8	Out	DC/DC Converter Enable-2 Pin. Output High Voltage Optionally Pulled Up to 12V by 5μA
V <sub>OUT_EN</sub> 3	D8	K8	Out	DC/DC Converter Enable-3 Pin. Output High Voltage Optionally Pulled Up to 12V by 5μA
V <sub>OUT_EN</sub> 4	C8	J8	Out	DC/DC Converter Enable-4 Pin. Open-Drain Pull-Down Output.
V <sub>OUT_EN</sub> 5	B8	H8	Out	DC/DC Converter Enable-5 Pin. Open-Drain Pull-Down Output.
V <sub>OUT_EN</sub> 6	A8	G8	Out	DC/DC Converter Enable-6 Pin. Open-Drain Pull-Down Output.
V <sub>OUT_EN</sub> 7	C7	J7	Out	DC/DC Converter Enable-7 Pin. Open-Drain Pull-Down Output.
V <sub>IN_EN</sub>	E5	L5	Out	DC/DC Converter V <sub>IN</sub> ENABLE Pin. Output High Voltage Optionally Pulled Up to 12V by 5μA
V <sub>IN_SNS</sub>	A5	G5	In	V <sub>IN</sub> SENSE Input. This Voltage is Compared Against the V <sub>IN</sub> On and Off Voltage Thresholds in Order to Determine When to Enable and Disable, Respectively, the Downstream DC/DC Converters
V <sub>PWR</sub>	B5	H5	In	V <sub>PWR</sub> Serves as the Unregulated Power Supply Input to the Chip (4.5V to 15V). If a 4.5V to 15V Supply Voltage is Unavailable, Short V <sub>PWR</sub> to V <sub>DD33</sub> and Power the Chip Directly from a 3.3V Supply
V <sub>DD33</sub>	A4	G4	In/Out	If Shorted to V <sub>PWR</sub> , it Serves as 3.13V to 3.47V Supply Input Pin. Otherwise it is a 3.3V Internally Regulated Voltage Output.
V <sub>DD33</sub>	A3	G3	In	Input for Internal 2.5V Sub-Regulator. Short Pin A3 to Pin A4 and Pin G3 to Pin G4
V <sub>DD25</sub>	A2	G2	In/Out	2.5V Internally Regulated Voltage Output
WP	A1	G1	In	Digital Input. Write-Protect Input Pin, Active High
PWRGD	B1	H1	Out	Power Good Open-Drain Output. Indicates When Outputs are Power Good. Can be Used as System Power-On Reset. The Latency of This Signal May Be as Long as the ADC Latency. See Note 6
SHARE_CLK	B2	H2	In/Out	Bidirectional Clock Sharing Pin. Connect a 5.49k Pull-Up Resistor to V <sub>DD33</sub>
WDI/RESETB	B4	H4	In	Watchdog Timer Interrupt and Chip Reset Input. Connect a 10k Pull-Up Resistor to V <sub>DD33</sub> . Rising Edge Resets Watchdog Counter. Holding This Pin Low for More Than t <sub>RESETB</sub> Resets the Chip
FAULTB00	C3	J3	In/Out	Open-Drain Output and Digital Input. Active Low Bidirectional Fault Indicator-00. Connect a 10k Pull-Up Resistor to V <sub>DD33</sub>
FAULTB01	D3	K3	In/Out	Open-Drain Output and Digital Input. Active Low Bidirectional Fault Indicator-01. Connect a 10k Pull-Up Resistor to V <sub>DD33</sub>
FAULTB10	C4	J4	In/Out	Open-Drain Output and Digital Input. Active Low Bidirectional Fault Indicator-10. Connect a 10k Pull-Up Resistor to V <sub>DD33</sub>
FAULTB11	D4	K4	In/Out	Open-Drain Output and Digital Input. Active Low Bidirectional Fault Indicator-11. Connect a 10k Pull-Up Resistor to V <sub>DD33</sub>

## PIN FUNCTIONS

PIN NAME	PIN		PIN TYPE	DESCRIPTION
	Device A	Device B		
SDA	C1	J1	In/Out	PMBus Bidirectional Serial Data Pin
SCL	D1	K1	In	PMBus Serial Clock Input Pin (400kHz Maximum)
ALERTB	E2	L2	Out	Open-Drain Output. Generates an Interrupt Request in a Fault/Warning Situation
CONTROL0	E1	L1	In	Control Pin 0 Input
CONTROL1	F1	M1	In	Control Pin 1 Input
ASEL0	F3	M3	In	Ternary Address Select Pin 0 Input. Connect to $V_{DD33}$ , GND or Float to Encode 1 of 3 Logic States
ASEL1	F2	M2	In	Ternary Address Select Pin 1 Input. Connect to $V_{DD33}$ , GND or Float to Encode 1 of 3 Logic States
REFP	F5	M5	Out	Reference Voltage Output
REFM	F4	M4	Out	Reference Return Pin
$V_{DACP0}$	E7	L7	Out	DAC0 Output
$V_{DACM0}$	E6*	L6*	Out	DAC0 Return. Connect to Channel 0 DC/DC Converter's GND Sense or Return to GND
$V_{DACP1}$	F10	M10	Out	DAC1 Output
$V_{DACM1}$	F9*	M9*	Out	DAC1 Return. Connect to Channel 1 DC/DC Converter's GND Sense or Return to GND
$V_{DACP2}$	E10	L10	Out	DAC2 Output
$V_{DACM2}$	E9*	L9*	Out	DAC2 Return. Connect to Channel 2 DC/DC Converter's GND Sense or Return to GND
$V_{DACP3}$	D10	K10	Out	DAC3 Output
$V_{DACM3}$	D9*	K9*	Out	DAC3 Return. Connect to Channel 3 DC/DC Converter's GND Sense or Return to GND
$V_{DACP4}$	C10	J10	Out	DAC4 Output
$V_{DACM4}$	C9*	J9*	Out	DAC4 Return. Connect to Channel 4 DC/DC Converter's GND Sense or Return to GND
$V_{DACP5}$	B10	H10	Out	DAC5 Output
$V_{DACM5}$	B9*	H9*	Out	DAC5 Return. Connect to Channel 5 DC/DC Converter's GND Sense or Return to GND
$V_{DACP6}$	A10	G10	Out	DAC6 Output
$V_{DACM6}$	A9*	G9*	Out	DAC6 Return. Connect to Channel 6 DC/DC Converter's GND Sense or Return to GND
$V_{DACP7}$	B7	H7	Out	DAC7 Output
$V_{DACM7}$	B6*	H6*	Out	DAC7 Return. Connect to Channel 7 DC/DC Converter's GND Sense or Return to GND
$V_{PU}$	B3	H3	In	Common Connection for Internal Pull-Up Resistors
$R_{PU1}$	E3	L3	Out	General Purpose 10k Pull-Up Resistor 1
$R_{PU2}$	D2	K2	Out	General Purpose 10k Pull-Up Resistor 2
$R_{PU3}$	C2	J2	Out	General Purpose 10k Pull-Up Resistor 3
$R_{PU4}$	E4	L4	Out	General Purpose 10k Pull-Up Resistor 4
GND	C6, D5, D6	J6, K5, K6	Ground	Device A Ground Pins are Isolated from the Device B Ground Pins
DNC	C5	J5	Do Not Connect	Do Not Connect to This Pin

\*Any unused  $V_{SENSEPN}$  or  $V_{SENSEMn}$  or  $V_{DACMn}$  pins must be tied to GND.

**BLOCK DIAGRAM**



\*NOTES: 1. ONLY 1/2 OF THE LTM2987 MODULE SHOWN  
 2. THE TWO 8-CHANNEL LTC2977 HALVES ARE IDENTICAL AND COMPLETELY ISOLATED  
 3. PIN NAMES REFER TO (DEVICE A, DEVICE B)

2987 B0



## OPERATION

### Overview

The LTM2987 contains two independent LTC2977 devices and most of the passive components required to make a complete 16-channel power system manager. The LTM2987 simplifies power system design by integrating the required passive components, reducing the bill-of-materials and improving PC board routing efficiency.

Each half of the LTM2987 behaves the same as a standalone LTC2977 including independent power supply and ground pins. This feature can be used to increase redundancy in a system while keeping the overall solution size small.

Refer to the LTC2977 data sheet for a detailed description of the device operation, the PMBus command set, and applications information.

### Device Address

Since the LTM2987 consists of two independent LTC2977 devices, each half of the LTM2987 must be configured

for a unique address. The I<sup>2</sup>C/SMBus addresses of the LTM2987 are configured in the same manner as for individual LTC2977 devices. The LTM2987 also responds to the LTC2977 global address and the SMBus Alert Response address, regardless of the state of the ASEL pins and the MFR\_I2C\_BASE\_ADDRESS register. Please refer to the Device Address section in the LTC2977 data sheet for more details.

### MFR\_SPECIAL\_ID

The LTM2987 contains unique MFR\_SPECIAL\_ID values to differentiate it from the LTC2977. Table 1 lists the MFR\_SPECIAL\_ID values for the LTM2987.

**Table 1. LTM2987 MFR\_SPECIAL\_ID Values**

LTM2987 DEVICE	MFR_SPECIAL_ID
Device A	0x8010
Device B	0x8020

## APPLICATIONS INFORMATION

### OVERVIEW

The LTM2987 is a Power System Manager that is capable of sequencing, margining, trimming, supervising output voltage for OV/UV conditions, providing fault management, and voltage readback for sixteen DC/DC converters. Input voltage and LTM2987 junction temperature readback are also available. Odd numbered channels can be configured to read back current sense resistor voltages. Multiple LTM2987s can be synchronized to operate in unison using the SHARE\_CLK, FAULTB and CONTROL pins. The LTM2987 utilizes a PMBus compliant interface and command set.

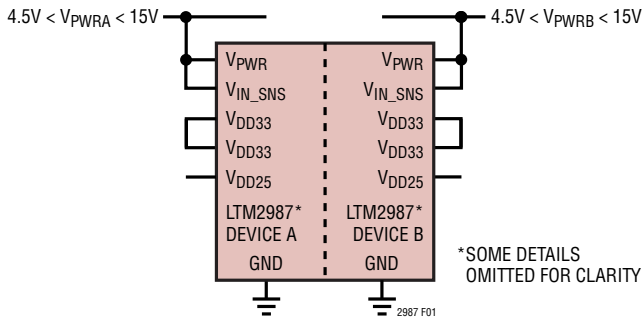


Figure 1. Powering LTM2987 Directly from an Intermediate Bus

### POWERING THE LTM2987

The LTM2987 can be powered two ways. The first method requires that a voltage between 4.5V and 15V be applied to the  $V_{PWR}$  pin. See Figure 1. Internal linear regulators convert  $V_{PWR}$  down to 3.3V which drives all of the internal circuitry in each device. Do not tie the  $V_{DD33(A)}$  and  $V_{DD33(B)}$  pins together since each half of the LTM2987 has independent voltage regulators.

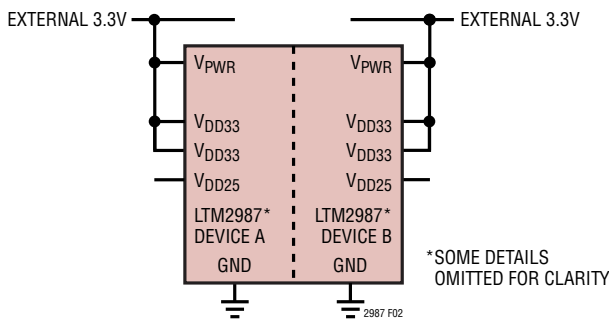


Figure 2. Powering LTM2987 from External 3.3V Supply

Alternatively, power from an external 3.3V supply may be applied directly to the  $V_{DD33}$  pins using a voltage between 3.13V and 3.47V. Tie  $V_{PWR}$  to the  $V_{DD33}$  pins. See Figure 2. In this case,  $V_{DD33(A)}$  and  $V_{DD33(B)}$  may be tied together. All functionality is available when using this alternate power method. The higher voltages needed for the  $V_{OUT\_EN[0:3]}$  pins and bias for the  $V_{SENSE}$  pins are charge pumped from  $V_{DD33}$ .

The method used to power each device in the LTM2987 is independent of the other device. Either method may be used in any combination.

### APPLICATION CIRCUITS

#### Undedicated Pull-Up Resistors

Each half of the LTM2987 module has four undedicated 10k pull-up resistors as shown in Figure 3. The common pull-up voltage is applied to the  $V_{PU}$  pin, and the individual pull-up resistors are on  $R_{PU1}$ ,  $R_{PU2}$ ,  $R_{PU3}$  and  $R_{PU4}$ . These pull-up resistors can be used for the open-drain pins such as SDA, SCL, ALERTB or  $FAULTB_{zn}$  in which case the common pull-up voltage  $V_{PU}$  should be connected to a 3.3V supply. To simplify the layout, the pin  $V_{PU}$  is adjacent to the  $V_{DD33}$  pin.

#### Anti-Aliasing Filter Considerations

Since most of the passive components required for operation are integrated into the LTM2987, no external filter components are required.

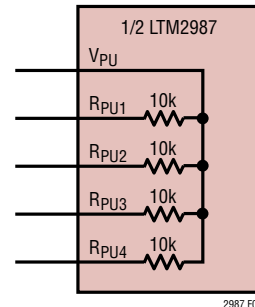


Figure 3. Undedicated Pull-Up Resistors

## APPLICATIONS INFORMATION

### $V_{IN}$ Sense

Voltages other than  $V_{IN}$  can be monitored and supervised using the  $V_{IN\_SNS}$  pins. Each  $V_{IN\_SNS}$  pin has a calibrated internal divider allowing it to directly sense voltages up to 15V.

### Unused ADC Sense Inputs

Connect all unused ADC sense inputs ( $V_{SENSEPN}$  or  $V_{SENSEMn}$ ) to GND. In a system where the inputs are connected to removable cards and may be left floating in certain situations, connect the inputs to GND using 100k resistors, as shown in Figure 4.

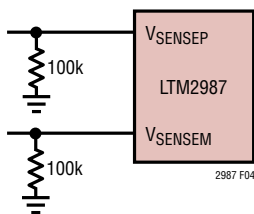


Figure 4. Connecting Unused Inputs to GND

## PCB ASSEMBLY AND LAYOUT SUGGESTIONS

### Bypass Capacitor Placement

All required bypass capacitors are integrated into the LTM2987. No additional bypass capacitance is required. The PCB layout should adhere to good layout guidelines. A multilayer PCB that dedicates a layer to power and ground is recommended. Low resistance and low inductance power and ground connections are important to minimize power supply noise and ensure proper device operation.

## DESIGN CHECKLIST

### I<sup>2</sup>C

- Each half of the LTM2987 must be configured for a unique address. Unique hardware  $ASELn$  values are recommended for simplest in system programming.
- The address select pins ( $ASELn$ ) are tri-level; Check Table 1 of the LTC2977 data sheet.
- Check addresses for collision with other devices on the bus and any global addresses.

### Output Enables

- Use appropriate pull-up resistors on all  $V_{OUT\_ENn}$  pins.
- Verify that the absolute maximum ratings of the  $V_{OUT\_ENn}$  pins are not exceeded.

### $V_{IN}$ Sense

- No external resistive divider is required to sense  $V_{IN}$ ;  $V_{IN\_SNS}$  already has an internal calibrated divider.

### Logic Signals

- Verify the absolute maximum ratings of the digital pins (SCL, SDA, ALERTB, FAULTBzn, CONTROLn, SHARE\_CLK, WDI, ASELn, PWRGD) are not exceeded.
- Connect all SHARE\_CLK pins in the system together and pull up to 3.3V with a 5.49k resistor.
- Do not leave CONTROLn pins floating. Pull up to 3.3V with a 10k resistor.
- Tie WDI/RESETB to VDD33 with a 10k resistor. Do not connect a capacitor to the WDI/RESETB pin.
- Tie WP to either VDD33 or GND. Do not leave floating.

### Unused Inputs

- Connect all unused  $V_{SENSEPN}$ ,  $V_{SENSEMn}$  and DACMn pins to GND. Do not float unused inputs.

### DAC Outputs

- Select appropriate resistor for desired margin range. Refer to the resistor selection tool in LTpowerPlay for assistance.

### Power Supplies

- If powered from VPWR, do not connect the VDD33(A) and VDD33(B) pins together. Each VDD33 pin has an independent, internal regulator.

For a more complete list of design considerations and a schematic checklist, see the LTpowerPlay help menu.

## PACKAGE DESCRIPTION

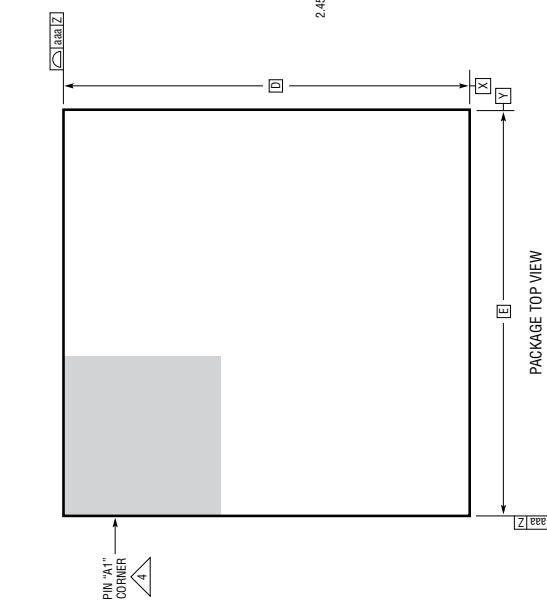
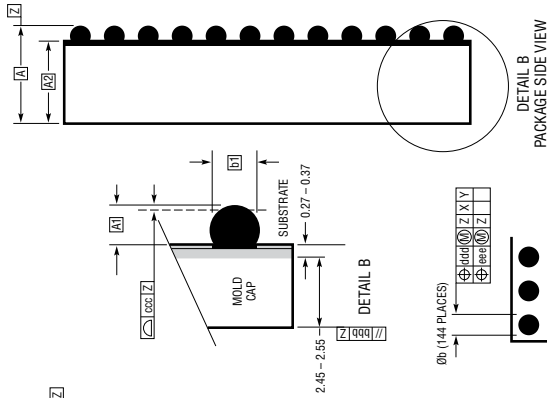
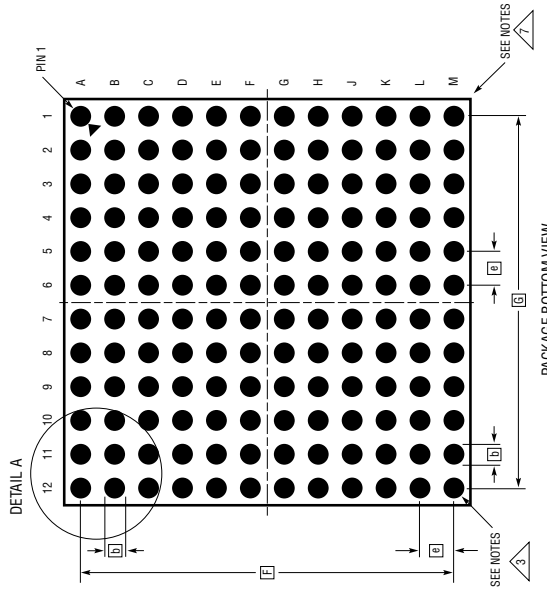
LTM2987 Component BGA Pinout (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	
<b>Device A</b>	<b>A</b>	WP	V <sub>DD25</sub>	V <sub>DD33</sub>	V <sub>DD33</sub>	V <sub>IN_SNS</sub>	V <sub>SENSEM7</sub>	V <sub>SENSEP7</sub>	V <sub>OUT_EN6</sub>	V <sub>DACM6</sub>	V <sub>DACP6</sub>	V <sub>SENSEM6</sub>	V <sub>SENSEP6</sub>
	<b>B</b>	PWRGD	SHARE_CLK	V <sub>PU</sub>	WDI	V <sub>PWR</sub>	V <sub>DACM7</sub>	V <sub>DACP7</sub>	V <sub>OUT_EN5</sub>	V <sub>DACM5</sub>	V <sub>DACP5</sub>	V <sub>SENSEM5</sub>	V <sub>SENSEP5</sub>
	<b>C</b>	SDA	R <sub>PU3</sub>	FAULTB00	FAULTB10	DNC	GND	V <sub>OUT_EN7</sub>	V <sub>OUT_EN4</sub>	V <sub>DACM4</sub>	V <sub>DACP4</sub>	V <sub>SENSEM4</sub>	V <sub>SENSEP4</sub>
	<b>D</b>	SCL	R <sub>PU2</sub>	FAULTB01	FAULTB11	GND	GND	V <sub>OUT_EN0</sub>	V <sub>OUT_EN3</sub>	V <sub>DACM3</sub>	V <sub>DACP3</sub>	V <sub>SENSEM3</sub>	V <sub>SENSEP3</sub>
	<b>E</b>	CONTROL0	ALERTB	R <sub>PU1</sub>	R <sub>PU4</sub>	V <sub>IN_EN</sub>	V <sub>DACM0</sub>	V <sub>DACP0</sub>	V <sub>OUT_EN2</sub>	V <sub>DACM2</sub>	V <sub>DACP2</sub>	V <sub>SENSEM2</sub>	V <sub>SENSEP2</sub>
	<b>F</b>	CONTROL1	ASEL1	ASEL0	REFM	REFP	V <sub>SENSEM0</sub>	V <sub>SENSEP0</sub>	V <sub>OUT_EN1</sub>	V <sub>DACM1</sub>	V <sub>DACP1</sub>	V <sub>SENSEM1</sub>	V <sub>SENSEP1</sub>
<b>Device B</b>	<b>G</b>	WP	V <sub>DD25</sub>	V <sub>DD33</sub>	V <sub>DD33</sub>	V <sub>IN_SNS</sub>	V <sub>SENSEM7</sub>	V <sub>SENSEP7</sub>	V <sub>OUT_EN6</sub>	V <sub>DACM6</sub>	V <sub>DACP6</sub>	V <sub>SENSEM6</sub>	V <sub>SENSEP6</sub>
	<b>H</b>	PWRGD	SHARE_CLK	V <sub>PU</sub>	WDI	V <sub>PWR</sub>	V <sub>DACM7</sub>	V <sub>DACP7</sub>	V <sub>OUT_EN5</sub>	V <sub>DACM5</sub>	V <sub>DACP5</sub>	V <sub>SENSEM5</sub>	V <sub>SENSEP5</sub>
	<b>J</b>	SDA	R <sub>PU3</sub>	FAULTB00	FAULTB10	DNC	GND	V <sub>OUT_EN7</sub>	V <sub>OUT_EN4</sub>	V <sub>DACM4</sub>	V <sub>DACP4</sub>	V <sub>SENSEM4</sub>	V <sub>SENSEP4</sub>
	<b>K</b>	SCL	R <sub>PU2</sub>	FAULTB01	FAULTB11	GND	GND	V <sub>OUT_EN0</sub>	V <sub>OUT_EN3</sub>	V <sub>DACM3</sub>	V <sub>DACP3</sub>	V <sub>SENSEM3</sub>	V <sub>SENSEP3</sub>
	<b>L</b>	CONTROL0	ALERTB	R <sub>PU1</sub>	R <sub>PU4</sub>	V <sub>IN_EN</sub>	V <sub>DACM0</sub>	V <sub>DACP0</sub>	V <sub>OUT_EN2</sub>	V <sub>DACM2</sub>	V <sub>DACP2</sub>	V <sub>SENSEM2</sub>	V <sub>SENSEP2</sub>
	<b>M</b>	CONTROL1	ASEL1	ASEL0	REFM	REFP	V <sub>SENSEM0</sub>	V <sub>SENSEP0</sub>	V <sub>OUT_EN1</sub>	V <sub>DACM1</sub>	V <sub>DACP1</sub>	V <sub>SENSEM1</sub>	V <sub>SENSEP1</sub>

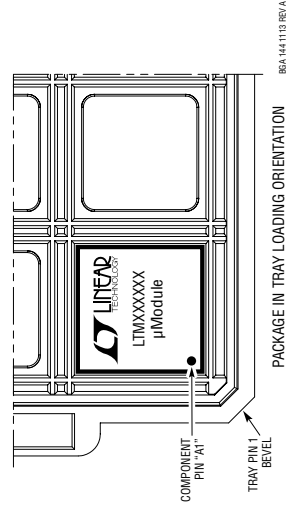
# PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

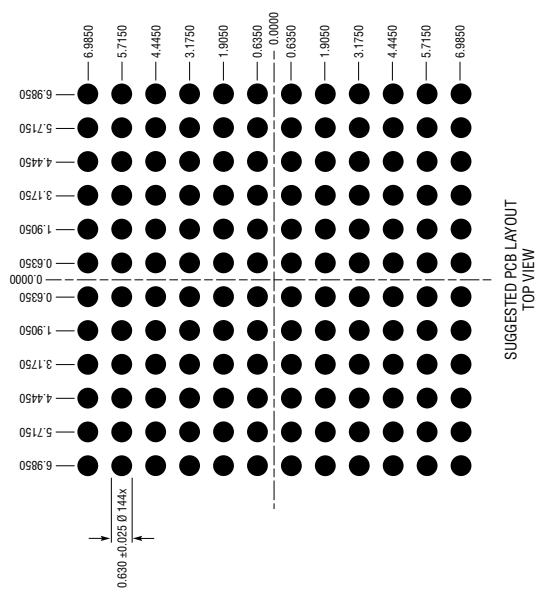
**BGA Package**  
**144-Lead (15mm × 15mm × 3.42mm)**  
 (Reference LTC DWG # 05-08-1946 Rev A)



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  2. ALL DIMENSIONS ARE IN MILLIMETERS
  3. BALL DESIGNATION PER JEDEC MS-028 AND JEP95
  4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
  5. PRIMARY DATUM - Z - IS SEATING PLANE
  6. SOLDER BALL COMPOSITION IS 96.5% Sn/3.0% Ag/0.5% Cu
  7. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG  $\mu$ Module PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY



SYMBOL	DIMENSIONS		NOTES
	MIN	MAX	
A	3.22	3.42	3.62
A1	0.50	0.60	0.70
A2	2.72	2.82	2.92
b	0.60	0.75	0.90
b1	0.60	0.63	0.66
D	15.0		
E	15.0		
e	1.27		
F	13.97		
G	13.97		
aaa			0.15
bbb			0.10
ccc			0.20
ddd			0.30
eee			0.15
TOTAL NUMBER OF BALLS:			144



TYPICAL APPLICATION

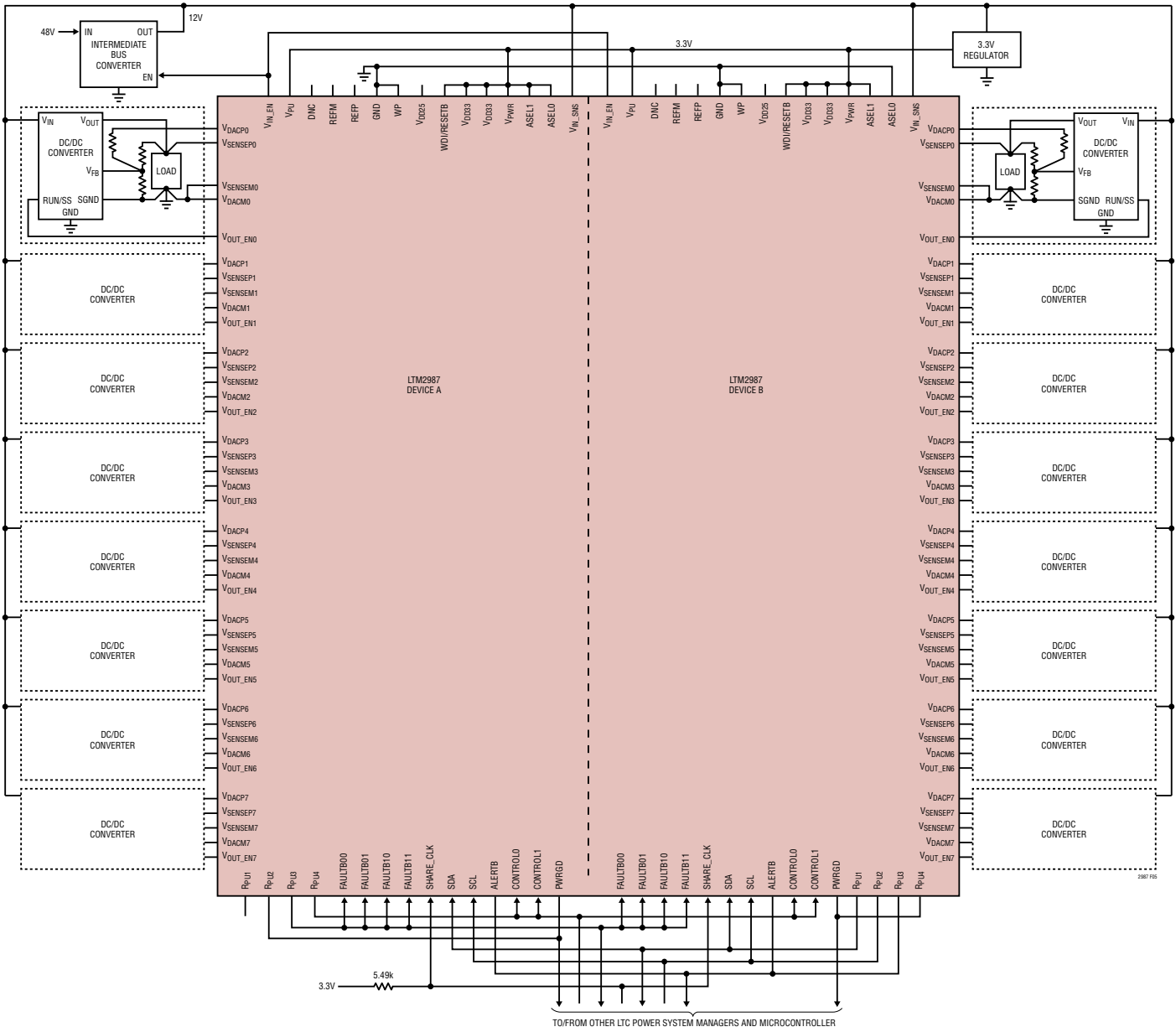


Figure 5. LTM2987 16-Channel Application Circuit with External 3.3V Chip Power

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2970	Dual I <sup>2</sup> C Power Supply Monitor and Margining Controller	5V to 15V, 0.5% TUE 14-Bit ADC, 8-Bit DAC, Temperature Sensor
LTC2974	4-Channel PMBus Power System Manager	0.25% TUE 16-Bit ADC, Voltage/Current/Temperature Monitoring and Supervision
LTC2977	8-Channel PMBus Power System Manager	0.25% TUE 16-Bit ADC, Voltage/Temperature Monitoring and Supervision
LTC3880	Dual Output PolyPhase Step-Down DC/DC Controller	0.5% TUE 16-Bit ADC, Voltage/Current/Temperature Monitoring and Supervision
LTC3883	Single Output PolyPhase Step-Down DC/DC Controller	0.5% TUE 16-Bit ADC, Voltage/Current/Temperature Monitoring and Supervision