

# **NXP PMXB65UPE MOSFET datasheet**

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P-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN1010D-3 (SOT1215) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

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# PMXB65UPE

12 V, P-channel Trench MOSFET

18 February 2014

Preliminary data sheet

## 1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN1010D-3 (SOT1215) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

## 2. Features and benefits

- Trench MOSFET technology
- Leadless ultra small and ultra thin SMD plastic package: 1.1 × 1.0 × 0.37 mm
- Exposed drain pad for excellent thermal conduction
- ElectroStatic Discharge (ESD) protection 1.5 kV HBM
- Drain-source on-state resistance  $R_{DSon} = 59 \text{ m}\Omega$
- Very low gate-source threshold voltage for portable applications  $V_{GS(th)} = -0.68 \text{ V}$

## 3. Applications

- High-side load switch and charging switch for portable devices
- Power management in battery driven portables
- LED driver
- DC-to-DC converter

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25 \text{ }^\circ\text{C}$	-	-	-12	V
$V_{GS}$	gate-source voltage		-8	-	8	V
$I_D$	drain current	$V_{GS} = -4.5 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$	[1]	-	-3.2	A
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -4.5 \text{ V}; I_D = -3.2 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	59	72	m $\Omega$

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.

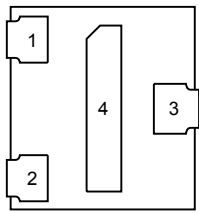
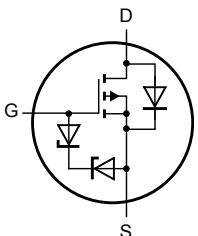


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### 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>Transparent top view <b>DFN1010D-3 (SOT1215)</b></p>	 <p>017aaa259</p>
2	S	source		
3	D	drain		
4	D	drain		

### 6. Ordering information

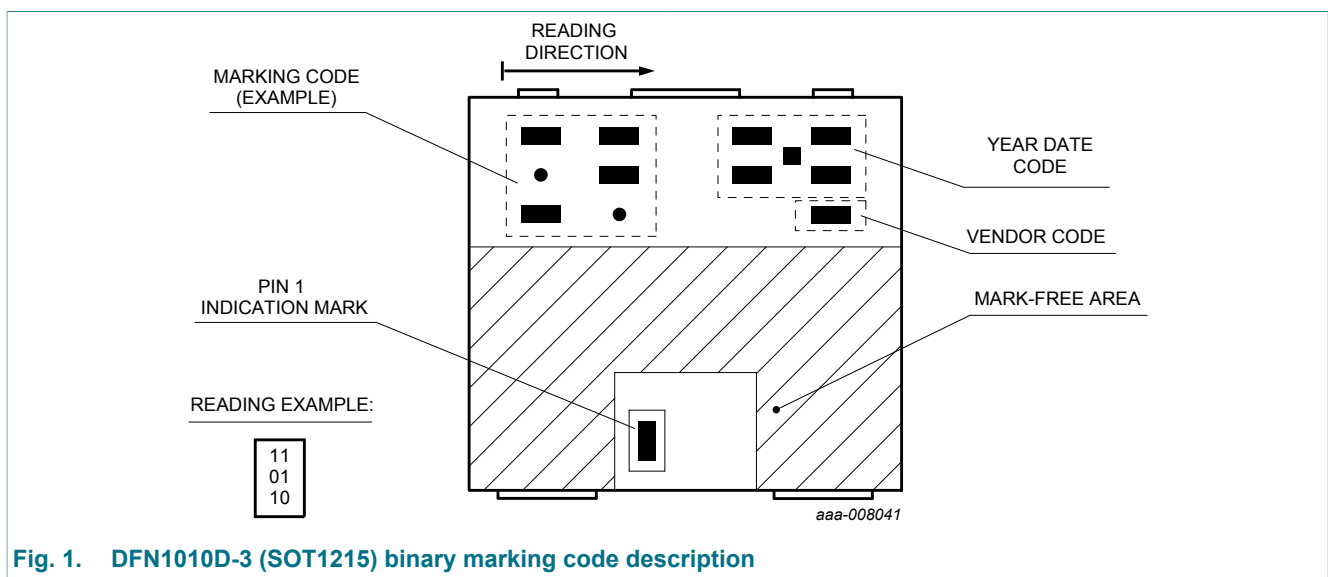
Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMXB65UPE	DFN1010D-3	DFN1010D-3: plastic thermal enhanced ultra thin small outline package; no leads; 3 terminals; body 1.1 x 1.0 x 0.37 mm	SOT1215

### 7. Marking

Table 4. Marking codes

Type number	Marking code
PMXB65UPE	01 10 00



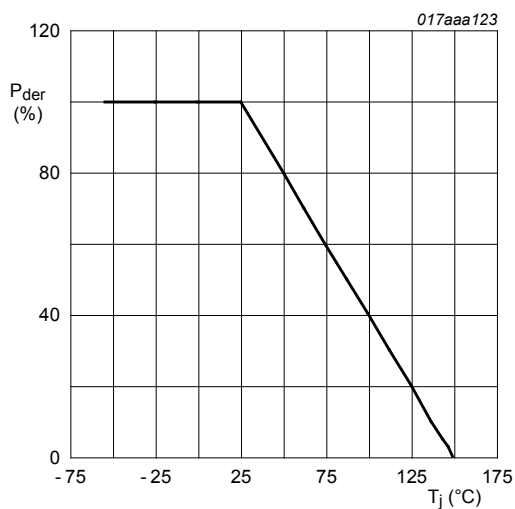
## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

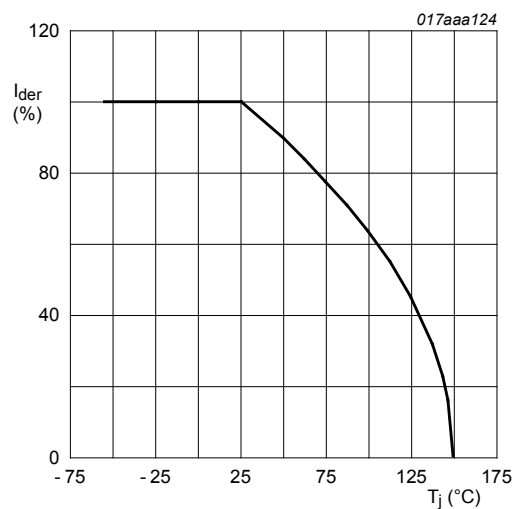
Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> = 25 °C		-	-12	V
V <sub>GS</sub>	gate-source voltage			-8	8	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = -4.5 V; T <sub>amb</sub> = 25 °C	[1]	-	-3.2	A
		V <sub>GS</sub> = -4.5 V; T <sub>amb</sub> = 100 °C	[1]	-	-2.1	A
I <sub>DM</sub>	peak drain current	T <sub>amb</sub> = 25 °C; single pulse; t <sub>p</sub> ≤ 10 μs		-	-13	A
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C	[2]	-	317	mW
			[1]	-	1070	mW
		T <sub>sp</sub> = 25 °C		-	8330	mW
T <sub>j</sub>	junction temperature			-55	150	°C
T <sub>amb</sub>	ambient temperature			-55	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>amb</sub> = 25 °C	[1]	-	-1	A

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



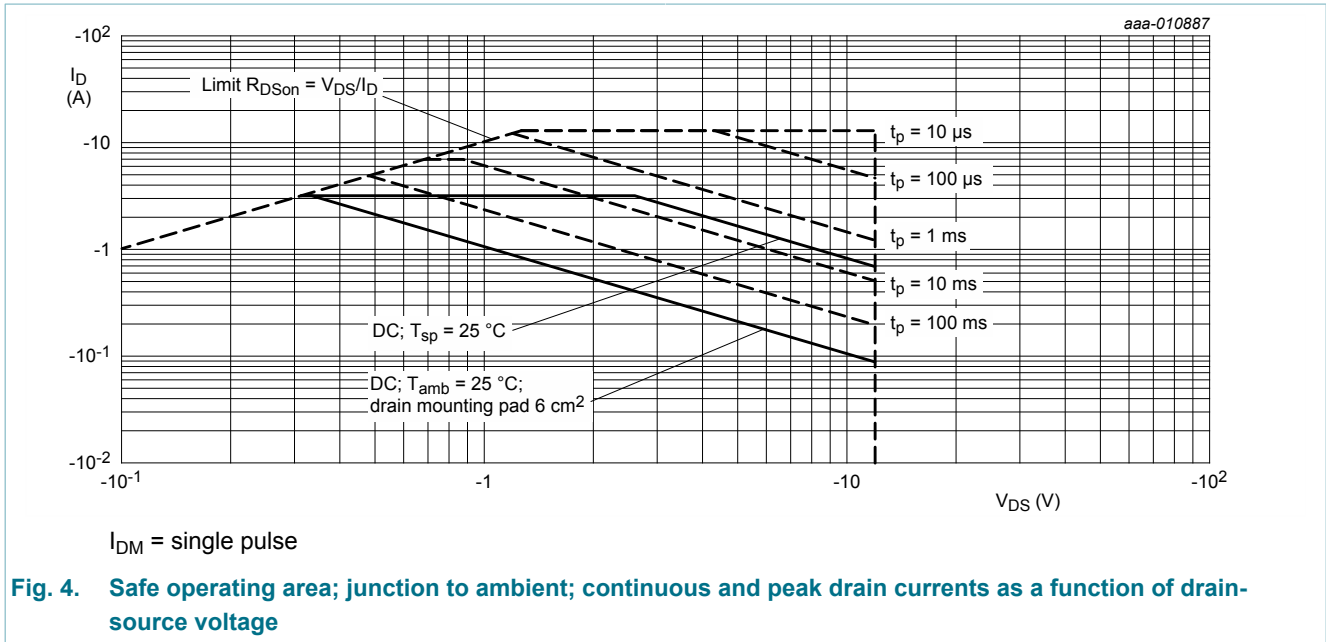
**Fig. 2. Normalized total power dissipation as a function of junction temperature**

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$



**Fig. 3. Normalized continuous drain current as a function of junction temperature**

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100 \%$$



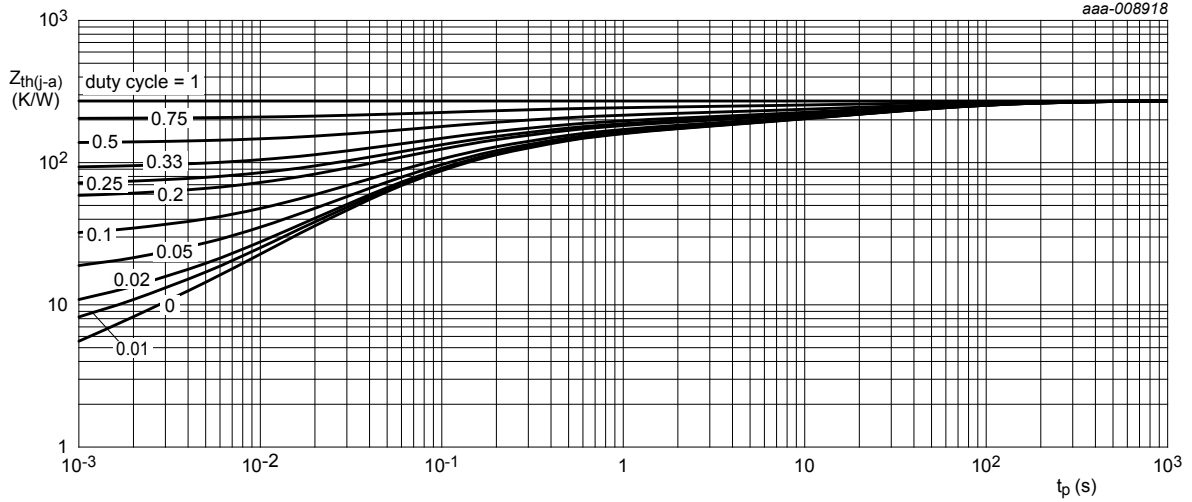
## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	271	312	K/W
			[2]	-	102	117	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	10	15	K/W

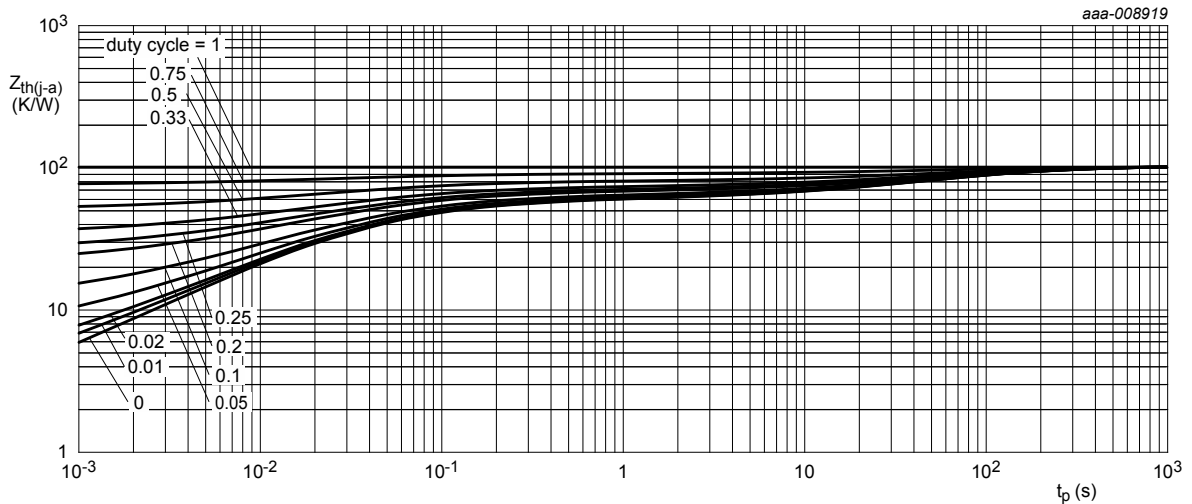
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain  $6 \text{ cm}^2$ .



FR4 PCB, standard footprint

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



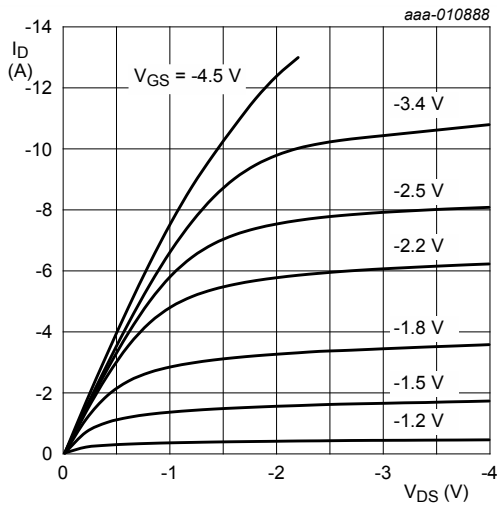
FR4 PCB, mounting pad for drain  $6\text{ cm}^2$

Fig. 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

## 10. Characteristics

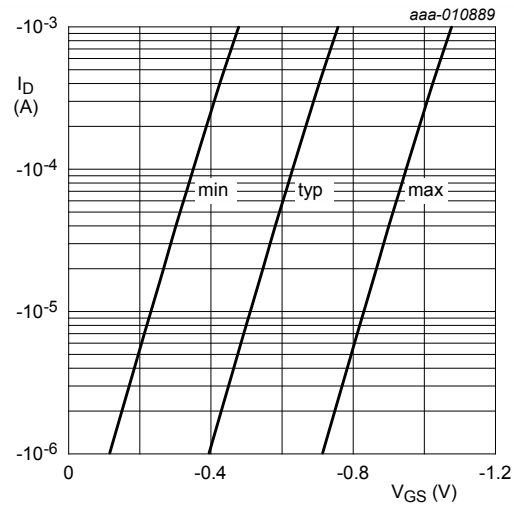
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-12	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = -250 \mu A; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	-0.4	-0.68	-1	V
$I_{DSS}$	drain leakage current	$V_{DS} = -12 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-1	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = -8 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-10	$\mu A$
		$V_{GS} = 8 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	10	$\mu A$
		$V_{GS} = -4.5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-1	$\mu A$
		$V_{GS} = 4.5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	1	$\mu A$
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -4.5 V; I_D = -3.2 A; T_j = 25 \text{ }^\circ C$	-	59	72	m $\Omega$
		$V_{GS} = -4.5 V; I_D = -3.2 A; T_j = 150 \text{ }^\circ C$	-	80	98	m $\Omega$
		$V_{GS} = -2.5 V; I_D = -2.7 A; T_j = 25 \text{ }^\circ C$	-	78	98	m $\Omega$
		$V_{GS} = -1.8 V; I_D = -1 A; T_j = 25 \text{ }^\circ C$	-	120	[tbd]	m $\Omega$
		$V_{GS} = -1.5 V; I_D = -0.1 A; T_j = 25 \text{ }^\circ C$	-	198	[tbd]	m $\Omega$
		$V_{GS} = -1.2 V; I_D = -50 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	880	-	m $\Omega$
$g_{fs}$	forward transconductance	$V_{DS} = -10 V; I_D = -2 A; T_j = 25 \text{ }^\circ C$	-	9.4	-	S
$R_G$	gate resistance	$f = 1 \text{ MHz}$	-	8.7	-	$\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -6 V; I_D = -3.2 A; V_{GS} = -4.5 V; T_j = 25 \text{ }^\circ C$	-	6.7	12	nC
$Q_{GS}$	gate-source charge		-	1	-	nC
$Q_{GD}$	gate-drain charge		-	1.9	-	nC
$C_{iss}$	input capacitance	$V_{DS} = -6 V; f = 1 \text{ MHz}; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	634	-	pF
$C_{oss}$	output capacitance		-	167	-	pF
$C_{rss}$	reverse transfer capacitance		-	146	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -6 V; I_D = -3.2 A; V_{GS} = -4.5 V; R_{G(ext)} = 6 \Omega; T_j = 25 \text{ }^\circ C$	-	6.2	-	ns
$t_r$	rise time		-	22	-	ns
$t_{d(off)}$	turn-off delay time		-	27	-	ns
$t_f$	fall time		-	17	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = -1 A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-0.7	-1.2	V



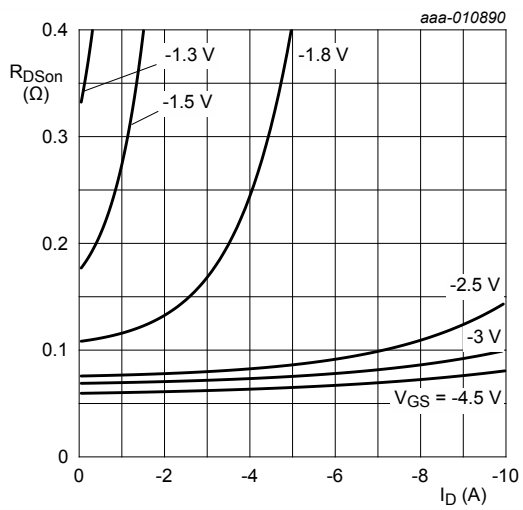
$T_j = 25\text{ }^\circ\text{C}$

Fig. 7. Output characteristics: drain current as a function of drain-source voltage; typical values



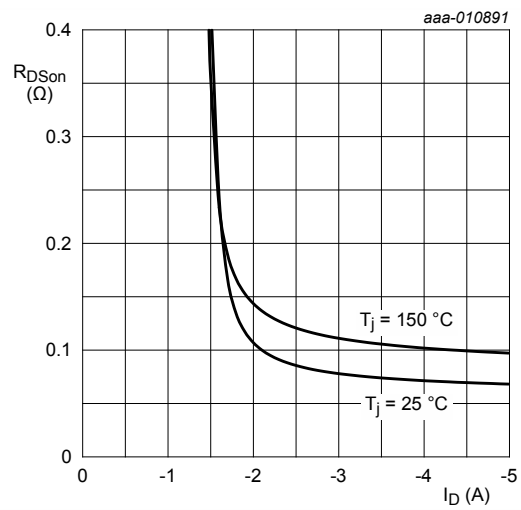
$T_j = 25\text{ }^\circ\text{C}; V_{DS} = -5\text{ V}$

Fig. 8. Sub-threshold drain current as a function of gate-source voltage



$T_j = 25\text{ }^\circ\text{C}$

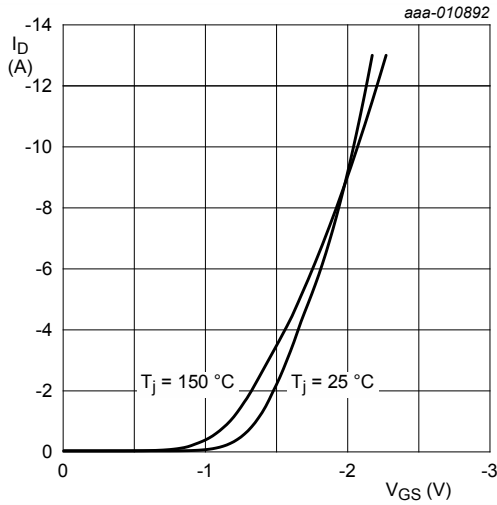
Fig. 9. Drain-source on-state resistance as a function of drain current; typical values



$I_D = -3.2\text{ A}$

Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values





$$V_{DS} > I_D \times R_{DSon}$$

Fig. 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values

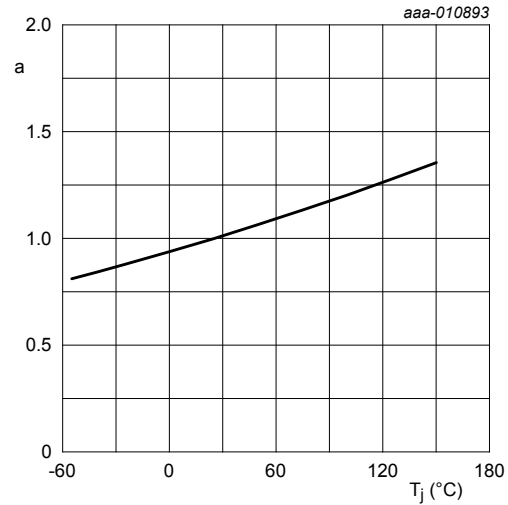
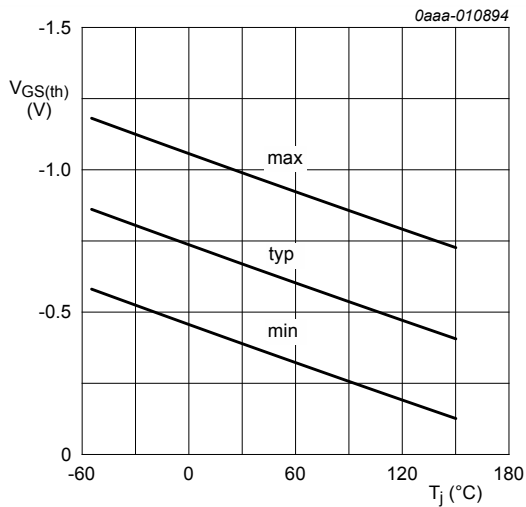


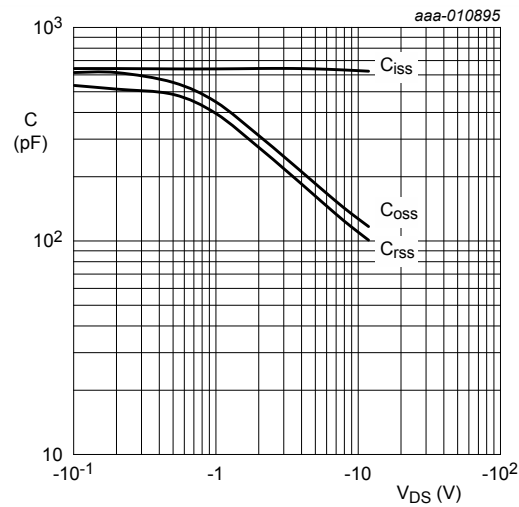
Fig. 12. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$



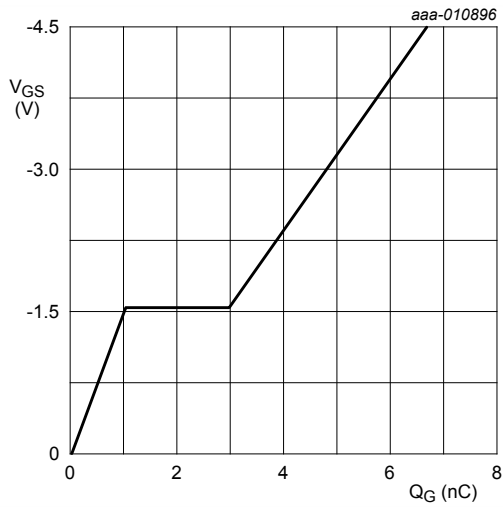
$$I_D = -0.25 \text{ mA}; V_{DS} = V_{GS}$$

Fig. 13. Gate-source threshold voltage as a function of junction temperature



$$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$$

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$I_D = -3.2 \text{ A}; V_{DS} = -6 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$

Fig. 15. Gate-source voltage as a function of gate charge; typical values

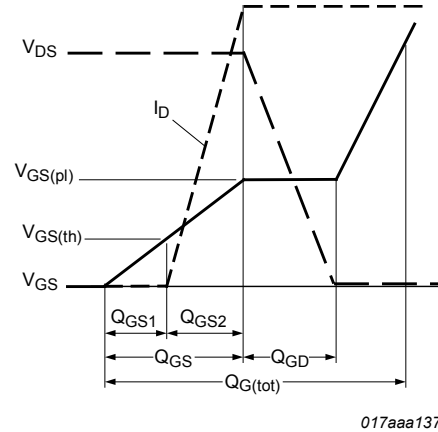
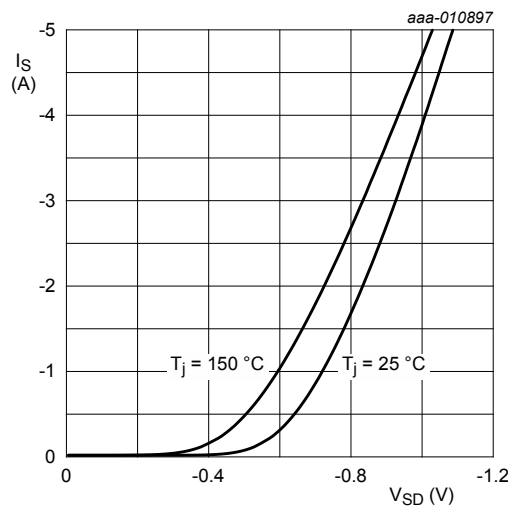


Fig. 16. MOSFET transistor: Gate charge waveform definitions



$V_{GS} = 0 \text{ V}$

Fig. 17. Source current as a function of source-drain voltage; typical values

## 11. Test information

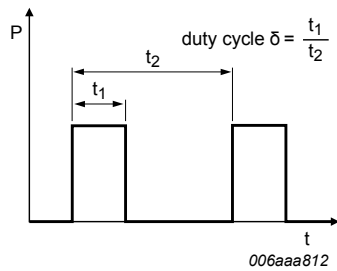


Fig. 18. Duty cycle definition

## 12. Package outline

DFN1010D-3: plastic thermal enhanced ultra thin small outline package; no leads; 3 terminals; body: 1.1 x 1.0 x 0.37 mm

SOT1215

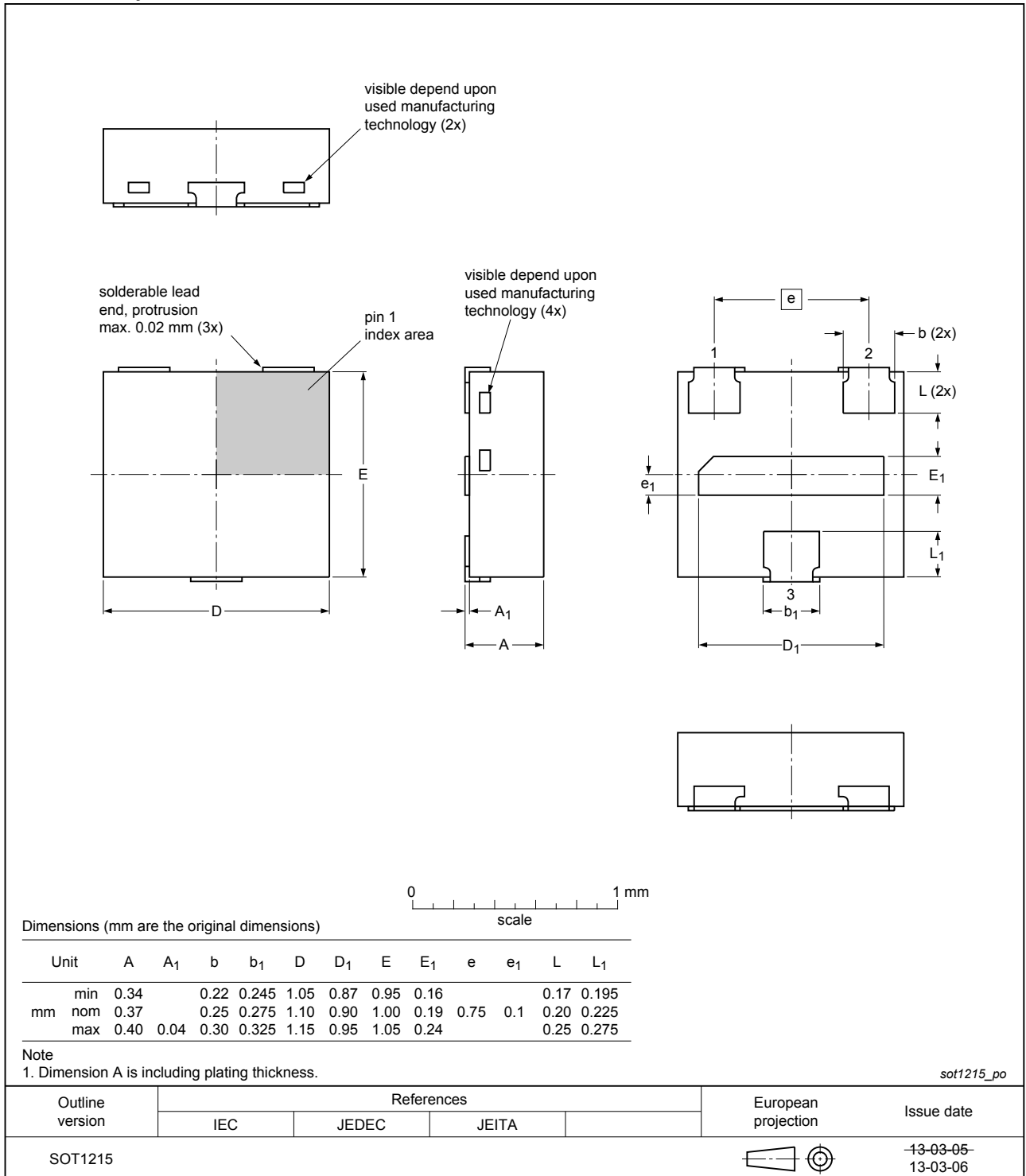


Fig. 19. Package outline DFN1010D-3 (SOT1215)

### 13. Soldering

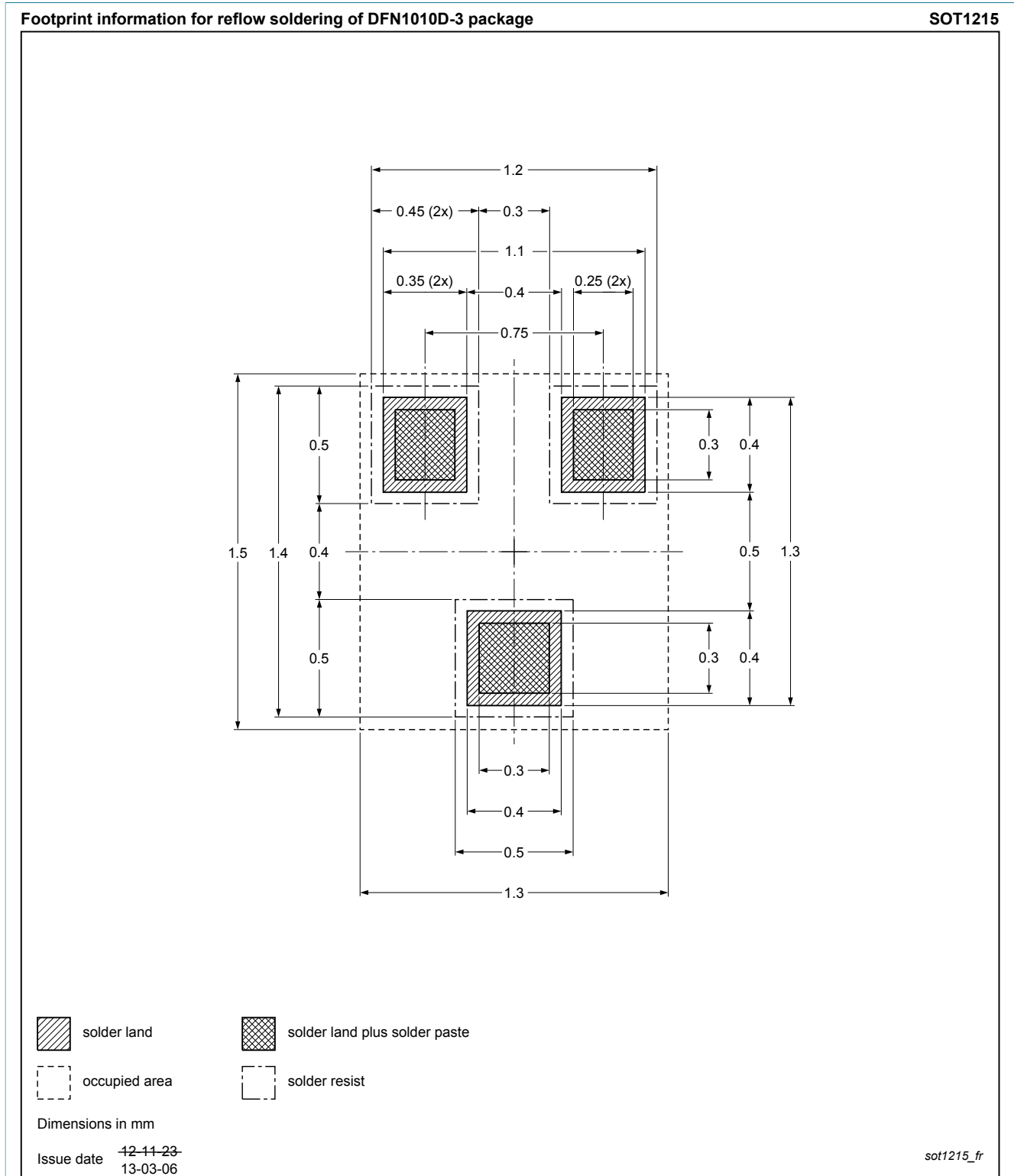


Fig. 20. Reflow soldering footprint for DFN1010D-3 (SOT1215)

## 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMXB65UPE v.2	20140218	Preliminary data sheet	-	PMXB65UPE v.1
Modifications:	<ul style="list-style-type: none"><li>Table 7: Maximum values of <math>R_{DS(on)}</math> parameter are to be determined.</li></ul>			
PMXB65UPE v.1	20140204	Preliminary data sheet	-	-

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### 15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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