CD4013B Types

CMOS Dual 'D'-Type Flip-Flop

High-Voltage Types (20-Volt Rating)

■ CD4013B consists of two identical, independent data-type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs and Q and $\overline{Q}$ outputs. These devices can be used for shift register applications, and, by connecting $\overline{Q}$ output to the data input, for counter and toggle applications. The logic level present at the D input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line, respectively.
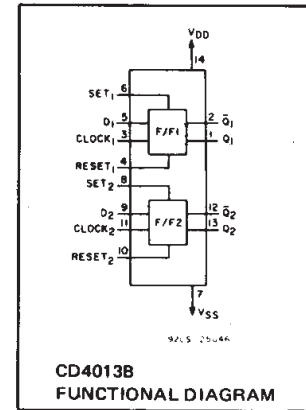
The CD4013B types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

■ Set-Reset capability
■ Static flip-flop operation – retains state indefinitely with clock level either "high" or "low"
■ Medium-speed operation – 16 MHz (typ.) clock toggle rate at 10V
■ Standardized symmetrical output characteristics
■ 100% tested for quiescent current at 20 V

■ Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
■ Noise margin (over full package temperature range):   1 V at V_{DD}=5 V
                                                        2 V at V_{DD}=10 V
                                                        2.5 V at V_{DD}=15 V
■ 5-V, 10-V, and 15-V parametric ratings

■ Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

■ Registers, counters, control circuits

CD4013B FUNCTIONAL DIAGRAM

Fig. 1 – Typical output low (sink) current characteristics.

Fig. 2 – Minimum output low (sink) current characteristics.

RECOMMENDED OPERATING CONDITIONS

At T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	–	3	18	V
Data Setup Time t_S	5	40	–	ns
	10	20	–	
	15	15	–	
Clock Pulse Width t_W	5	140	–	ns
	10	60	–	
	15	40	–	
Clock Input Frequency f_{CL}	5	dc	3.5	MHz
	10		8	
	15		12	
Clock Rise or Fall Time $t_r CL$, $t_f CL$	5	–	15	μs
	10	–	10	
	15	–	5	
Set or Reset Pulse Width t_W	5	180	–	ns
	10	80	–	
	15	50	–	

*If more than one unit is cascaded in a parallel clocked operation, $t_r CL$ should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.
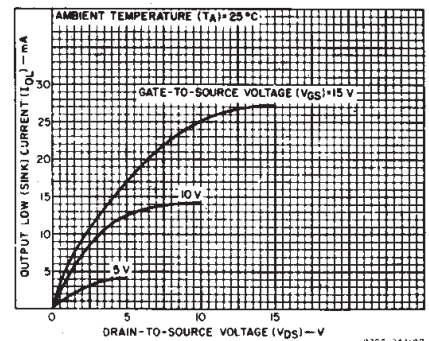

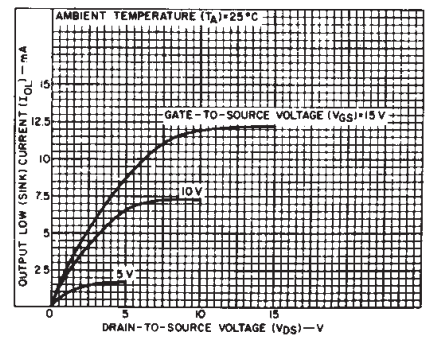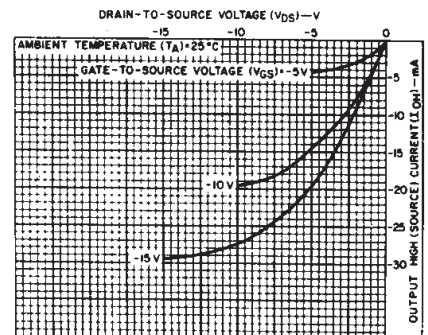Fig. 3 – Typical output high (source) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

| CHARAC-TERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) −55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current I_{DD} Max.	−	0,5	5	1	1	30	30	−	0.02	1	μA
	−	0,10	10	2	2	60	60	−	0.02	2	
	−	0,15	15	4	4	120	120	−	0.02	4	
	−	0,20	20	20	20	600	600	−	0.04	20	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	−	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	−	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	−	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	−	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	−	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	−	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	−	
Output Voltage: Low-Level, V_{OL} Max.	−	0,5	5	0.05				−	0	0.05	V
	−	0,10	10	0.05				−	0	0.05	
	−	0,15	15	0.05				−	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	−	0,5	5	4.95				4.95	5	−	
	−	0,10	10	9.95				9.95	10	−	
	−	0,15	15	14.95				14.95	15	−	
Input Low Voltage, V_{IL} Max.	0.5,4.5	−	5	1.5				−	−	1.5	V
	1,9	−	10	3				−	−	3	
	1.5,13.5	−	15	4				−	−	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	−	5	3.5				3.5	−	−	
	1,9	−	10	7				7	−	−	
	1.5,13.5	−	15	11				11	−	−	
Input Current, I_{IN} Max.	−	0,18	18	±0.1	±0.1	±1	±1	−	±10^{-5}	±0.1	μA
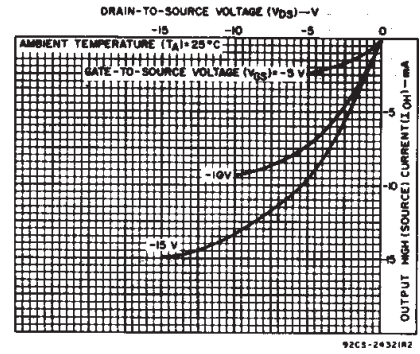
Fig. 4 — Minimum output high (source) current characteristics.
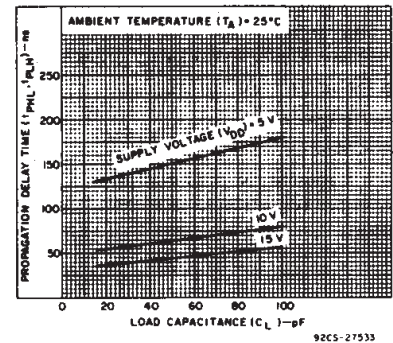

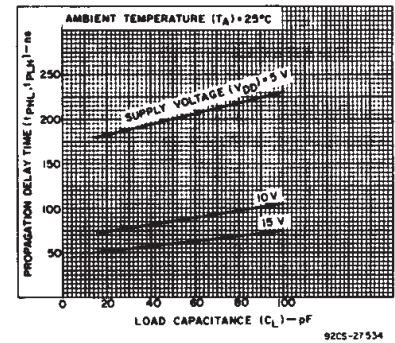Fig. 5 — Typical propagation delay time vs. load capacitance (CLOCK or SET to Q, CLOCK or RESET to $\overline{Q}$).

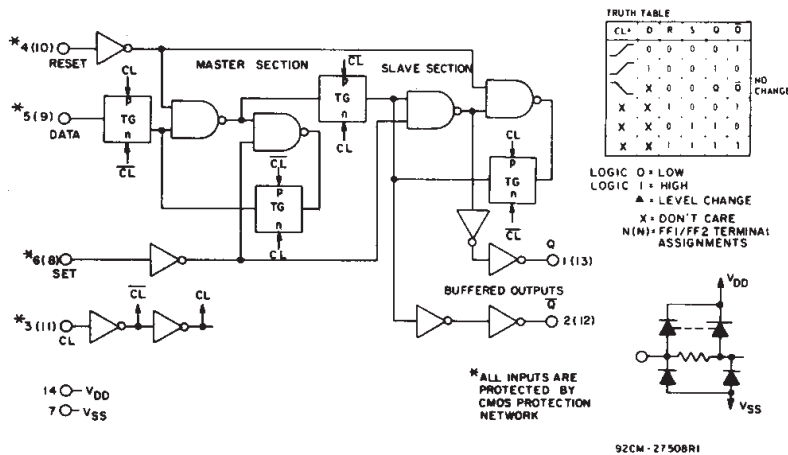Fig. 6 — Typical propagation delay time vs. load capacitance (SET to $\overline{Q}$ or RESET to Q.

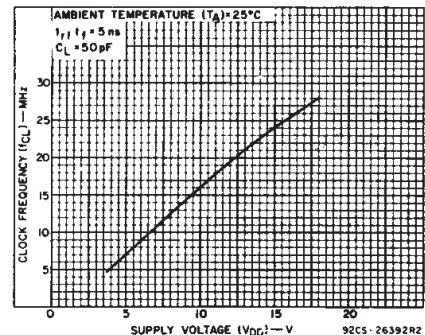Fig. 7 — Logic diagram and truth table for CD4013B (one of two identical flip-flops).

Fig. 8 — Typical maximum clock frequency vs. supply voltage.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

  Voltages referenced to V_{SS} Terminal) .... −0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS .... −0.5V to V_{DD} +0.5V

DC INPUT CURRENT, ANY ONE INPUT .... ±10mA

POWER DISSIPATION PER PACKAGE (P_D):

  For T_A = −55°C to +100°C 500mW

  For T_A = +100°C to +125°C .... Derate Linearity at 12mW/°C to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

  FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW

OPERATING-TEMPERATURE RANGE (T_A) .... −55°C to +125°C

STORAGE TEMPERATURE RANGE (T_{stg}) .... −65°C to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

  At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max .... +265°C
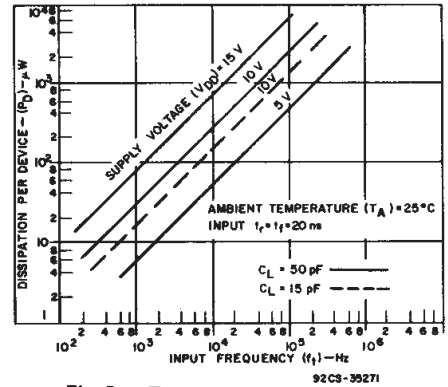

Fig. 9 — *Typical power dissipation
vs. frequency.*

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 20 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Propagation Delay Time: Clock to Q or $\overline{Q}$ Outputs t_{PHL}, t_{PLH}	5	—	150	300	
	10	—	65	130	ns
	15	—	45	90	
Set to Q or Reset to $\overline{Q}$ t_{PLH}	5	—	150	300	
	10	—	65	130	ns
	15	—	45	90	
Set to $\overline{Q}$ or Reset to Q t_{PHL}	5	—	200	400	
	10	—	85	170	ns
	15	—	60	120	
Transition Time t_{THL}, t_{TLH}	5	—	100	200	
	10	—	50	100	ns
	15	—	40	80	
Maximum Clock Input Frequency# f_{CL}	5	3.5	7	—	
	10	8	16	—	MHz
	15	12	24	—	
Minimum Clock Pulse Width t_W	5	—	70	140	
	10	—	30	60	ns
	15	—	20	40	
Minimum Set or Reset Pulse Width t_W	5	—	90	180	
	10	—	40	80	ns
	15	—	25	50	
Minimum Data Setup Time t_S	5	—	20	40	
	10	—	10	20	ns
	15	—	7	15	
Minimum Data Hold Time t_H	5	—	2	5	
	10	—	2	5	ns
	15	—	2	5	
Clock Input Rise or Fall Time t_rCL, t_fCL	5	—	—	15	
	10	—	—	10	μs
	15	—	—	5	
Input Capacitance C_{IN}	Any Input	—	5	7.5	pF

#Input t_r, t_f = 5 ns.

TEST CIRCUITS
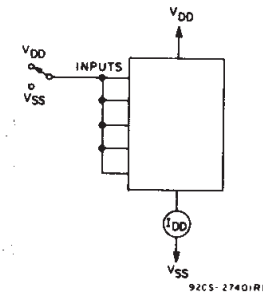

Fig. 10 — *Quiescent device current.*
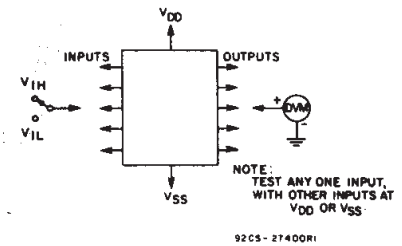
Fig. 11 — *Input voltage.*
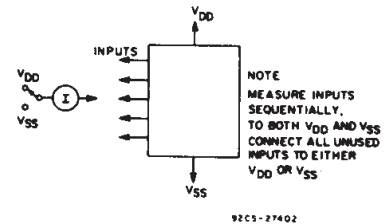
Fig. 12 — *Input current.*

TERMINAL ASSIGNMENT
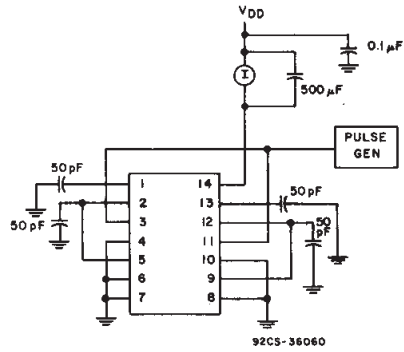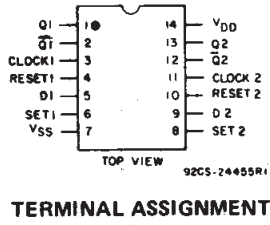
Fig. 13—Dynamic power dissipation test circuit.

DIMENSIONS AND PAD LAYOUT FOR CD4013BH

64 - 72
(1.626 - 1.829)

64 - 72
(1.626 - 1.829)
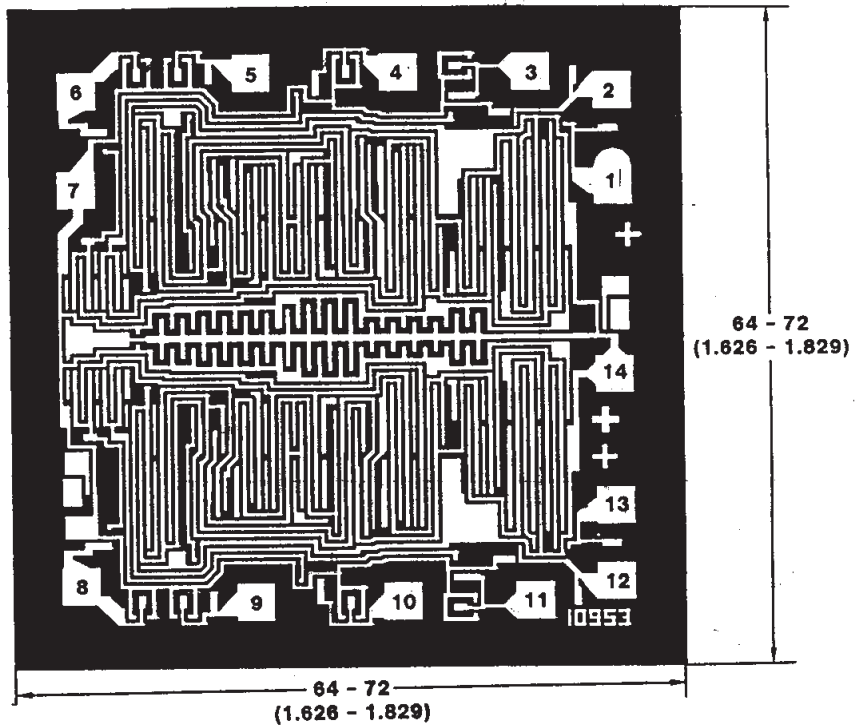
Dimensions in parentheses are in millimeters and are
derived from the basic inch dimensions as indicated.
Grid graduations are in mils (10^{-3} inch).

IMPORTANT NOTICE

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
89267AKB3T	OBSOLETE	CFP	WR	14		TBD	Call TI	Call TI
CD4013BE	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4013BEE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4013BF	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
CD4013BF3A	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
CD4013BK3	OBSOLETE	CFP	WR	14		TBD	Call TI	Call TI
CD4013BM	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4013BM96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4013BM96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4013BM96G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4013BME4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4013BMG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4013BMT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4013BMTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4013BMTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4013BNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4013BNSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4013BNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4013BPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4013BPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4013BPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4013BPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4013BPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4013BPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
JM38510/05151BCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4013BM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4013BNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4013BPWR	TSSOP	PW	14	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4013BM96	SOIC	D	14	2500	346.0	346.0	33.0
CD4013BNSR	SO	NS	14	2000	346.0	346.0	33.0
CD4013BPWR	TSSOP	PW	14	2000	346.0	346.0	29.0

MECHANICAL DATA

1,27

0,51
0,35

⊕ 0,25 Ⓜ

14

8

5,60
5,00

8,20
7,40

1

7

A

0,15 NOM

Gage Plane

0,25

0°–10°

1,05
0,55

0,15
0,05

2,00 MAX

Seating Plane

△ 0,10

DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R—GDIP—T**)   CERAMIC DUAL IN—LINE PACKAGE
14 LEADS SHOWN

DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

1   7

0.065 (1,65)
0.045 (1,14)

C

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°—15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package is hermetically sealed with a ceramic lid using glass frit.
         D.   Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E.   Falls within MIL STD 1835 GDIP1—T14, GDIP1—T16, GDIP1—T18 and GDIP1—T20.

PW (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

PINS ** DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

D (R−PDSO−G14) PLASTIC SMALL−OUTLINE PACKAGE

0.344 (8,75)
0.337 (8,55)

/C\

14 8

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) /D\

Pin 1
Index Area

1 7

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

Gauge Plane

0.004 (0,10)

Seating Plane

0.010 (0,25) 0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−3/H 11/2006

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
/C\ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
/D\ Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS−012 variation AB.

N (R−PDIP−T**)
16 PINS SHOWN

PLASTIC DUAL−IN−LINE PACKAGE

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

A

16   9

0.260 (6,60)
0.240 (6,10)

1   8

0.070 (1,78)
0.045 (1,14) /D\

0.045 (1,14)
0.030 (0,76) /D\

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option /D\

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

/C\

4040049/E   12/2002

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
        /C\ Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
        /D\ The 20 pin end lead shoulder width is a vendor option, either half or full width.