FAST CMOS 16-BIT BUFFER/LINE DRIVER

Integrated Device Technology, Inc.

IDT54/74FCT16244T/AT/CT/ET
IDT54/74FCT162244T/AT/CT/ET
IDT54/74FCT166244T/AT/CT
IDT54/74FCT162H244T/AT/CT/ET

FEATURES:

- **Common features:**
  - 0.5 MICRON CMOS Technology
  - **High-speed, low-power CMOS replacement for ABT functions**
  - **Typical $t_{SK}(o)$ (Output Skew) < 250ps**
  - **Low input and output leakage $\leq 1\mu A$ (max.)**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - Packages include 25 mil pitch SSOP, 19.6 mil pitch TSSOP, 15.7 mil pitch TVSOP and 25 mil pitch Cerpack
  - Extended commercial range of -40°C to +85°C
- **Features for FCT16244T/AT/CT/ET:**
  - High drive outputs (-32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162244T/AT/CT/ET:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT166244T/AT/CT:**
  - Light Drive Balanced Output: ±8mA (commercial), ±6mA (military)
  - Minimal system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.25V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162H244T/AT/CT/ET:**
  - Bus-Hold retains last active bus state during 3-state
  - Eliminates the need for external pull up resistors

DESCRIPTION:

The 16-Bit Buffer/Line Driver is for bus interface or signal buffering applications requiring high speed and low power dissipation. These devices have a flow through pin organization, and shrink packaging to simplify board layout. All inputs are designed with hysteresis for improved noise margin. The three-state controls allow independent 4-bit, 8-bit or combined 16-bit operation. These parts are plug in replacements for 54/74ABT16244 where higher speed, lower noise or lower power dissipation levels are desired.

The FCT16244T/AT/CT/ET are ideally suited for driving high capacitance loads (>200pF) and low impedance backplanes. These "high drive" buffers are designed with power off disable capability to allow "live insertion" of boards when used in a backplane interface.

The FCT162244T/AT/CT/ET have balanced output current levels and current limiting resistors. These offer low ground bounce, minimal undershoot, and controlled output fall times, reducing the need for external series terminating resistors while still providing very high speed operation for loads of less than 200pF.

The FCT166244T/AT/CT are suited for very low noise, point-to-point driving where there is a single receiver, or a very light lumped load (<100pF). The buffers are designed to limit the output current to levels which will avoid noise and ringing on the signal lines without using external series terminating resistors.

The FCT162H244T/AT/CT/ET have "Bus-Hold" which retains the input's last state whenever the input goes to high impedance. This prevents "floating" inputs and eliminates the need for pull-up/down resistors.
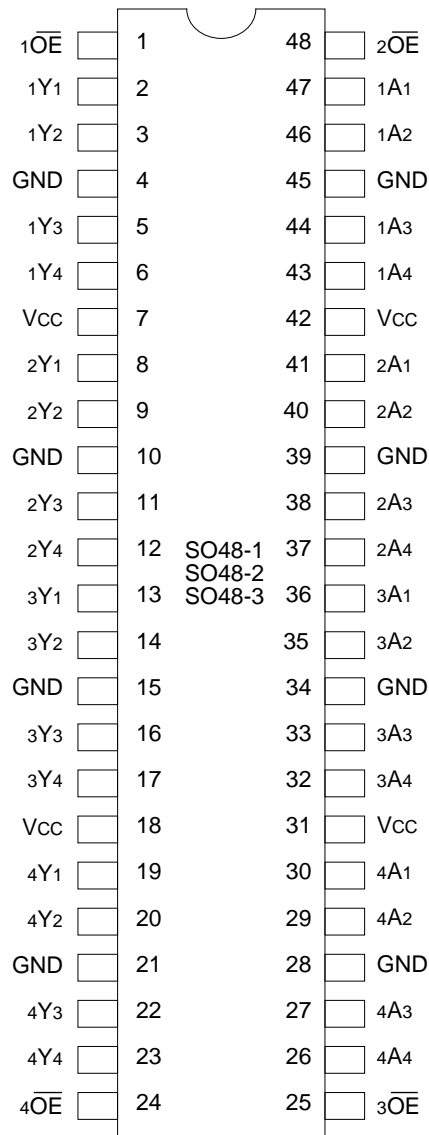
FUNCTIONAL BLOCK DIAGRAM

2544 drw 01
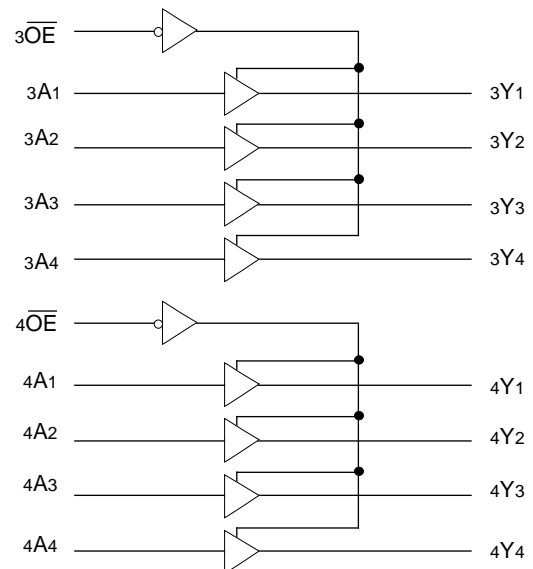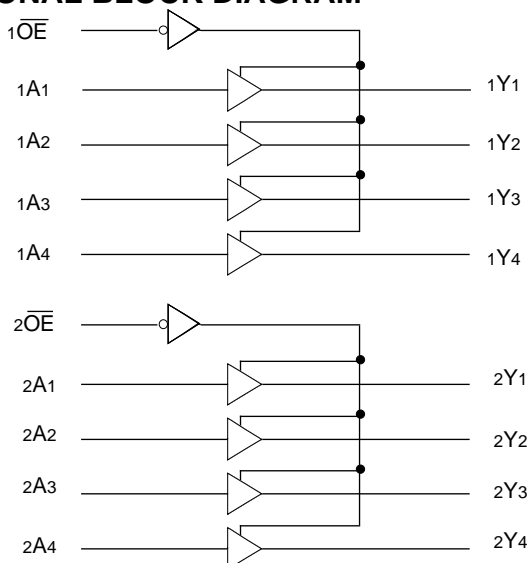
2544 drw 02

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

OCTOBER 1996

5.2
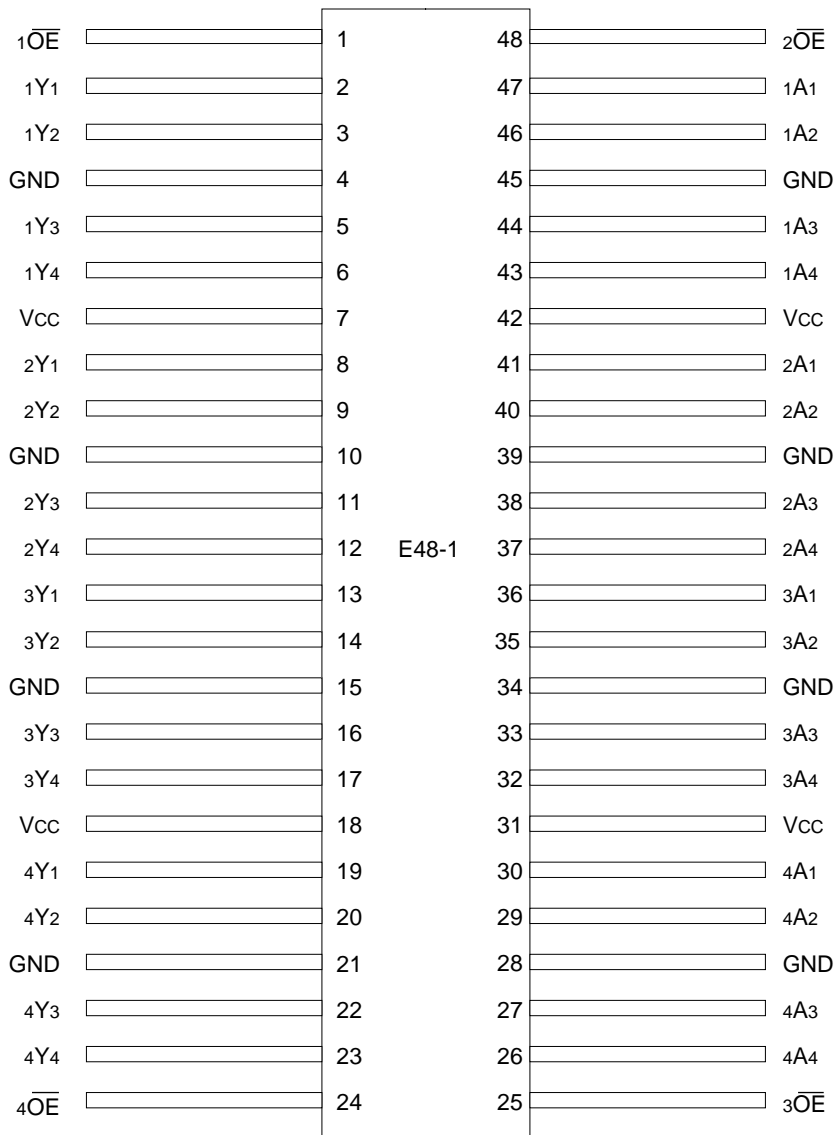
PIN CONFIGURATIONS

	SSOP/TSSOP/TVSOP TOP VIEW			CERPACK TOP VIEW	
1$\overline{\text{OE}}$	1	48	2$\overline{\text{OE}}$		
1Y1	2	47	1A1		
1Y2	3	46	1A2		
GND	4	45	GND		

SSOP/TSSOP/TVSOP

1$\overline{\text{OE}}$	1	48	2$\overline{\text{OE}}$
1Y1	2	47	1A1
1Y2	3	46	1A2
GND	4	45	GND
1Y3	5	44	1A3
1Y4	6	43	1A4
Vcc	7	42	Vcc
2Y1	8	41	2A1
2Y2	9	40	2A2
GND	10	39	GND
2Y3	11	38	2A3
2Y4	12	37	2A4
3Y1	13	36	3A1
3Y2	14	35	3A2
GND	15	34	GND
3Y3	16	33	3A3
3Y4	17	32	3A4
Vcc	18	31	Vcc
4Y1	19	30	4A1
4Y2	20	29	4A2
GND	21	28	GND
4Y3	22	27	4A3
4Y4	23	26	4A4
4$\overline{\text{OE}}$	24	25	3$\overline{\text{OE}}$

SO48-1
SO48-2
SO48-3

**SSOP/
TSSOP/TVSOP
TOP VIEW**

2544 drw 03

CERPACK (E48-1)

1$\overline{\text{OE}}$	1	48	2$\overline{\text{OE}}$
1Y1	2	47	1A1
1Y2	3	46	1A2
GND	4	45	GND
1Y3	5	44	1A3
1Y4	6	43	1A4
Vcc	7	42	Vcc
2Y1	8	41	2A1
2Y2	9	40	2A2
GND	10	39	GND
2Y3	11	38	2A3
2Y4	12	37	2A4
3Y1	13	36	3A1
3Y2	14	35	3A2
GND	15	34	GND
3Y3	16	33	3A3
3Y4	17	32	3A4
Vcc	18	31	Vcc
4Y1	19	30	4A1
4Y2	20	29	4A2
GND	21	28	GND
4Y3	22	27	4A3
4Y4	23	26	4A4
4$\overline{\text{OE}}$	24	25	3$\overline{\text{OE}}$

E48-1

**CERPACK
TOP VIEW**

2544 drw 04

PIN DESCRIPTION

Pin Names	Description
x$\overline{\text{OE}}$	3–State Output Enable Inputs (Active LOW)
xAx	Data Inputs[1]
xYx	3-State Outputs

NOTE: 2544 tbl 01
1. On FCT16xH these pins have "Bus-hold". All other pins are standard inputs, outputs or I/Os.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Description	Max.	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	−0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	−0.5 to V_{CC} +0.5	V
T_{STG}	Storage Temperature	−65 to +150	°C
I_{OUT}	DC Output Current	−60 to +120	mA

2544 tbl 03

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT and FCT166XXXT output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT and FCT166XXXT.

FUNCTION TABLE[1]

Inputs		Outputs
x$\overline{OE}$	xAx	xYx
L	L	L
L	H	H
H	X	Z

2544 tbl 02

NOTE:

1. H = HIGH Voltage Level
   X = Don't Care
   L = LOW Voltage Level
   Z = High Impedance

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	3.5	8.0	pF

2544 tbl 04

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (STANDARD PARTS)

Following Conditions Apply Unless Otherwise Specified:

Commercial: T_A = −40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[5]	V_{CC} = Max.	$V_I = V_{CC}$	—	—	±1	µA
	Input HIGH Current (I/O pins)[5]			—	—	±1	
I_{IL}	Input LOW Current (Input pins)[5]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[5]			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	$V_O = 2.7V$	—	—	±1	µA
I_{OZL}	(3-State Output pins)[5]		$V_O = 0.5V$	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = −18mA		—	−0.7	−1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		−80	−140	−225	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

2544 tbl 05

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = −55°C.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (BUS-HOLD)

Following Conditions Apply Unless Otherwise Specified:
Commercial: $T_A = -40°C$ to $+85°C$, $V_{CC} = 5.0V \pm 10\%$; Military: $T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter		Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level		Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level		Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	Standard Input[5]	V_{CC} = Max.	$V_I = V_{CC}$	—	—	±1	µA
		Standard I/O[5]			—	—	±1	
		Bus-hold Input			—	—	±100	
		Bus-hold I/O			—	—	±100	
I_{IL}	Input LOW Current[4]	Standard Input[5]		V_I = GND	—	—	±1	
		Standard I/O[5]			—	—	±1	
		Bus-hold Input			—	—	±100	
		Bus-hold I/O			—	—	±100	
I_{BHH}	Bus Hold Sustain Current[4]	Bus-hold Input	V_{CC} = Min.	V_I = 2.0V	−50	—	—	µA
I_{BHL}				V_I = 0.8V	+50	—	—	
I_{OZH}	High Impedance Output Current (3-State Output pins)[5,6]		V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}				V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage		V_{CC} = Min., I_{IN} = −18mA		—	−0.7	−1.2	V
I_{OS}	Short Circuit Current		V_{CC} = Max., V_O = GND[3]		−80	−140	−225	mA
V_H	Input Hysteresis		—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current		V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

NOTES: 2544 lnk 06

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time.   Duration of the test should not exceed one second.
4. Pins with Bus-hold are identified in the pin description.
5. The test limit for this parameter is ± 5µA at T_A = −55°C.
6. Does not include Bus-hold I/O pins.

OUTPUT DRIVE CHARACTERISTICS FOR FCT16244T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
IO	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		−50	—	−180	mA
VOH	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	IOH = −3mA	2.5	3.5	—	V
			IOH = −12mA MIL. IOH = −15mA COM'L.	2.4	3.5	—	V
			IOH = −24mA MIL. IOH = −32mA COM'L.[4]	2.0	3.0	—	V
VOL	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	IOL = 48mA MIL. IOL = 64mA COM'L.	—	0.2	0.55	V
IOFF	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	μA

2544 lnk 07

OUTPUT DRIVE CHARACTERISTICS FOR FCT162244T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
IODL	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	200	mA
IODH	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		−60	−115	−200	mA
VOH	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	IOH = −16mA MIL. IOH = −24mA COM'L.	2.4	3.3	—	V
VOL	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	IOL = 16mA MIL. IOL = 24mA COM'L.	—	0.3	0.55	V

2544 lnk 08

OUPUT DRIVE CHARACTERISTICS FOR FCT166244T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
IODL	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		16	48	96	mA
IODH	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		−16	−48	−96	mA
VOH	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	IOH = −6mA MIL. IOH = −8mA COM'L.	2.4	3.3	—	V
VOL	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	IOL = 6mA MIL. IOL = 8mA COM'L.	—	0.3	0.55	V

2544 lnk 09

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5μA at T_A = −55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC} ΔICC	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
ICCD	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open xOE = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz
IC	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz	V_{IN} = V_{CC} V_{IN} = GND	—	0.6	1.5	mA
		50% Duty Cycle xOE = GND One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	0.9	2.3	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz	V_{IN} = V_{CC} V_{IN} = GND	—	2.4	4.5[5]	
		50% Duty Cycle xOE = GND Sixteen Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	6.4	16.5[5]	

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NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$

   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})

   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

   D_H = Duty Cycle for TTL Inputs High

   N_T = Number of TTL Inputs at D_H

   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

   N_{CP} = Number of Clock Inputs at f_{CP}

   f_i = Input Frequency

   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT16244T/FCT162244T

Symbol	Parameter	Condition[1]	FCT16244T/162244T/166244T				FCT16244AT/162244AT/166244AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay xAx to xYx	$C_L = 50pF$ $R_L = 500\Omega$	1.5	6.5	1.5	7.0	1.5	4.8	1.5	5.1	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	8.0	1.5	8.5	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	7.0	1.5	7.5	1.5	5.6	1.5	5.9	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	ns

2544 tbl 11

| Symbol | Parameter | Condition[1] | FCT16244CT/162244CT/166244CT | | | | FCT16244ET/162244ET | | | | Unit |
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay xAx to xYx	$C_L = 50pF$ $R_L = 500\Omega$	1.5	4.1	1.5	4.6	1.5	3.2	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	5.8	1.5	6.5	1.5	4.4	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	5.2	1.5	5.7	1.5	3.6	—	—	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	—	ns

2544 tbl 12

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

TEST CIRCUITS AND WAVEFORMS

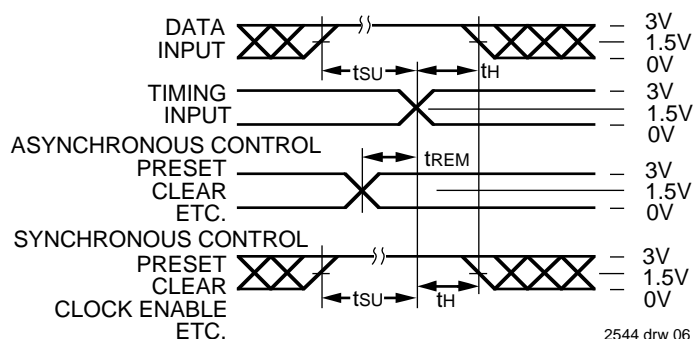## TEST CIRCUITS FOR ALL OUTPUTS
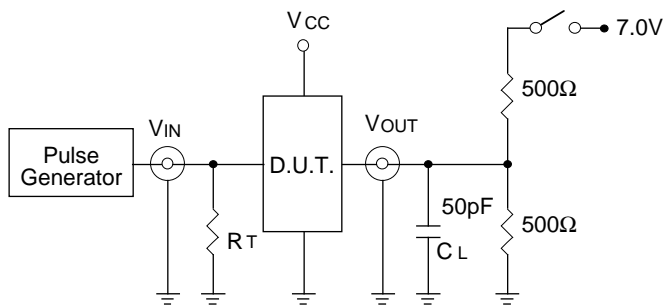
2544 drw 05

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

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DEFINITIONS:

C_L= Load capacitance: includes jig and probe capacitance.

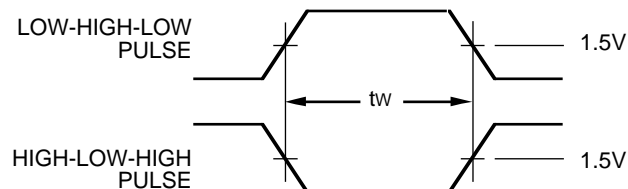R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.
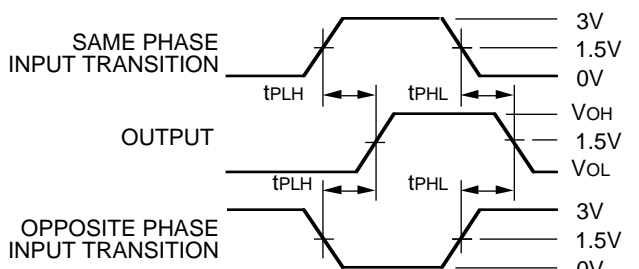
SET-UP, HOLD AND RELEASE TIMES
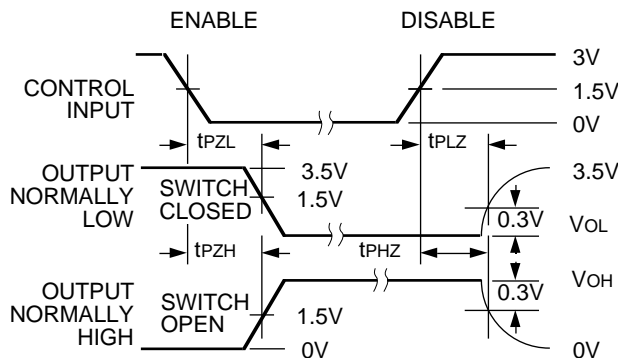

2544 drw 06

PULSE WIDTH

2544 drw 07

PROPAGATION DELAY

2544 drw 08

ENABLE AND DISABLE TIMES

2544 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH

2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION

```
IDT     XX      FCT      X        X       XXXX         X           X
     Temp. Range        Drive  Bus Hold  Device Type  Package   Process
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Blank	Commercial
B	MIL-STD-883, Class B
PV	Shrink Small Outline Package (SO48-1)
PA	Thin Shrink Small Outline Package (SO48-2)
PF	Thin Very Small Outline Package (SO48-3)
E	CERPACK (E48-1)
244T	Non-Inverting 16-Bit Buffer/Line Driver
244AT	
244CT	
244ET	
Blank	Standard
H	Bus-hold
16	16-Bit High Drive
162	16-Bit Balanced Drive
166	16-Bit Light Drive
54	−55°C to +125°C
74	−40°C to +85°C

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