ULN2001A, ULN2002A, ULN2003A, ULN2004A, ULQ2003A, ULQ2004A
HIGH-VOLTAGE HIGH-CURRENT
DARLINGTON TRANSISTOR ARRAY

SLRS027G – DECEMBER 1976 – REVISED JUNE 2004

The ULN2001A is obsolete and is no longer supplied.

- **500-mA-Rated Collector Current (Single Output)**
- **High-Voltage Outputs . . . 50 V**
- **Output Clamp Diodes**
- **Inputs Compatible With Various Types of Logic**
- **Relay-Driver Applications**

description/ordering information

The ULN2001A, ULN2002A, ULN2003A, ULN2004A, ULQ2003A, and ULQ2004A are high-voltage, high-current Darlington transistor arrays. Each consists of seven npn Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single Darlington pair is 500 mA. The Darlington pairs can be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. For 100-V (otherwise interchangeable) versions of the ULN2003A and ULN2004A, see the SN75468 and SN75469, respectively.

ULN2001A . . . D OR N PACKAGE
ULN2002A . . . N PACKAGE
ULN2003A . . . D, N, NS, OR PW PACKAGE
ULN2004A . . . D, N, OR NS PACKAGE
ULQ2003A, ULQ2004A . . . D OR N PACKAGE
(TOP VIEW)

1B	1	16	1C
2B	2	15	2C
3B	3	14	3C
4B	4	13	4C
5B	5	12	5C
6B	6	11	6C
7B	7	10	7C
E	8	9	COM
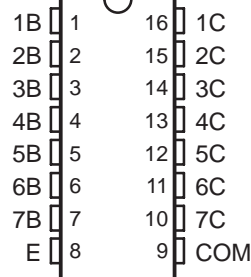
ORDERING INFORMATION

T$_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−20°C to 70°C	PDIP (N)	Tube of 25	ULN2002AN	ULN2002AN
			ULN2003AN	ULN2003AN
			ULN2004AN	ULN2004AN
	SOIC (D)	Tube of 40	ULN2003AD	ULN2003A
		Reel of 2500	ULN2003ADR	
		Tube of 40	ULN2004AD	ULN2004A
		Reel of 2500	ULN2004ADR	
	SOP (NS)	Reel of 2000	ULN2003ANSR	ULN2003A
			ULN2004ANSR	ULN2004A
	TSSOP (PW)	Tube of 90	ULN2003APW	UN2003A
		Reel of 2000	ULN2003APWR	
−40°C to 85°C	PDIP (N)	Tube of 25	ULQ2003AN	ULQ2003A
			ULQ2004AN	ULQ2004AN
	SOIC (D)	Tube of 40	ULQ2003AD	ULQ2003A
		Reel of 2500	ULQ2003ADR	ULQ2003A
		Tube of 40	ULQ2004AD	ULQ2004A
		Reel of 2500	ULQ2004ADR	ULQ2004A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

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ULN2001A, ULN2002A, ULN2003A, ULN2004A, ULQ2003A, ULQ2004A
HIGH-VOLTAGE HIGH-CURRENT
DARLINGTON TRANSISTOR ARRAY
SLRS027G – DECEMBER 1976 – REVISED JUNE 2004

**The ULN2001A is obsolete
and is no longer supplied.**

description/ordering information (continued)

The ULN2001A is a general-purpose array and can be used with TTL and CMOS technologies. The ULN2002A is designed specifically for use with 14-V to 25-V PMOS devices. Each input of this device has a Zener diode and resistor in series to control the input current to a safe limit. The ULN2003A and ULQ2003A have a 2.7-kΩ series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices. The ULN2004A and ULQ2004A have a 10.5-kΩ series base resistor to allow operation directly from CMOS devices that use supply voltages of 6 V to 15 V. The required input current of the ULN/ULQ2004A is below that of the ULN/ULQ2003A, and the required voltage is less than that required by the ULN2002A.

logic diagram

**The ULN2001A is obsolete
and is no longer supplied.**

schematics (each Darlington pair)

ULN2001A

ULN2002A

ULN/ULQ2003A: R_B = 2.7 kΩ
ULN/ULQ2004A: R_B = 10.5 kΩ

ULN2003A, ULN2004A, ULQ2003A, ULQ2004A
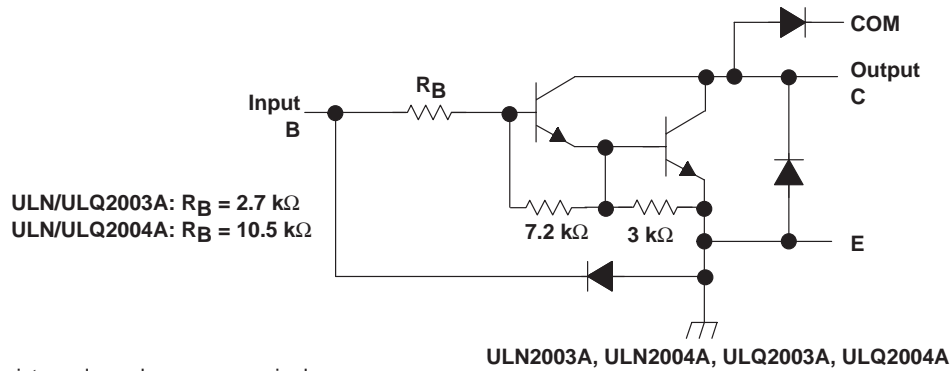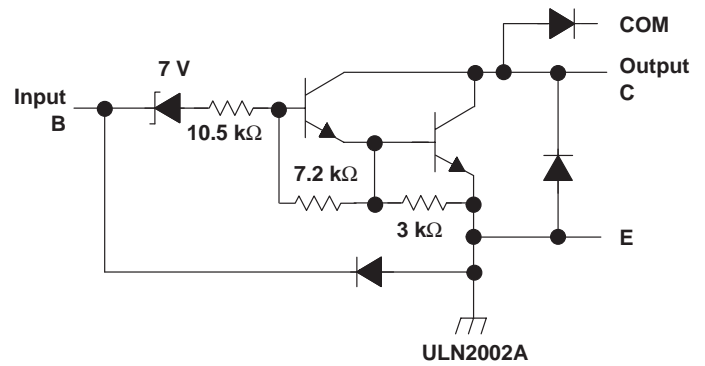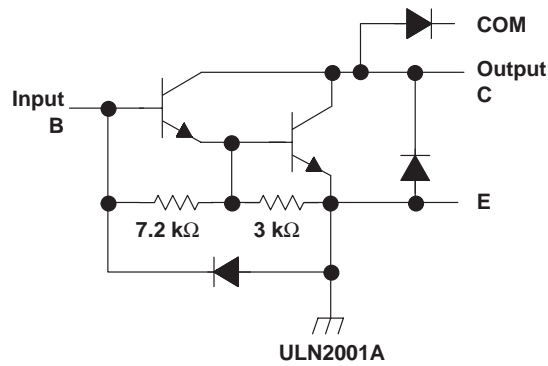
All resistor values shown are nominal.

ULN2001A, ULN2002A, ULN2003A, ULN2004A, ULQ2003A, ULQ2004A
HIGH-VOLTAGE HIGH-CURRENT
DARLINGTON TRANSISTOR ARRAY

The ULN2001A is obsolete
and is no longer supplied.

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absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)†

Collector-emitter voltage . . . . 50 V

Clamp diode reverse voltage (see Note 1) . . . . 50 V

Input voltage, V_I (see Note 1) . . . . 30 V

Peak collector current (see Figures 14 and 15) . . . . 500 mA

Output clamp current, I_{OK} . . . . 500 mA

Total emitter-terminal current . . . . –2.5 A

Operating free-air temperature range, T_A, ULN200xA . . . . −20°C to 70°C

ULQ200xA . . . . −40°C to 85°C

ULQ200xAT . . . . −40°C to 105°C

Package thermal impedance, θ_{JA} (see Notes 2 and 3): D package . . . . 73°C/W

N package . . . . 67°C/W

NS package . . . . 64°C/W

PW package . . . . 108°C/W

Package thermal impedance, θ_{JC} (see Notes 4 and 5): D package . . . . 36°C/W

N package . . . . 54°C/W

Operating virtual junction temperature, T_J . . . . 150°C

Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

Storage temperature range, T_{stg} . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.
2. Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable
ambient temperature is $P_D = (T_J(\text{max}) − T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. Maximum power dissipation is a function of T_J(max), θ_{JC}, and T_C. The maximum allowable power dissipation at any allowable case
temperature is $P_D = (T_J(\text{max}) − T_C)/\theta_{JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
5. The package thermal impedance is calculated in accordance with MIL-STD-883.

electrical characteristics, T_A = 25°C (unless otherwise noted)

	PARAMETER	TEST FIGURE	TEST CONDITIONS		ULN2001A MIN	ULN2001A TYP	ULN2001A MAX	ULN2002A MIN	ULN2002A TYP	ULN2002A MAX	UNIT
$V_{I(on)}$	On-state input voltage	6	V_{CE} = 2 V,	I_C = 300 mA						13	V
$V_{CE(sat)}$	Collector-emitter saturation voltage	5	I_I = 250 µA,	I_C = 100 mA		0.9	1.1		0.9	1.1	V
			I_I = 350 µA,	I_C = 200 mA		1	1.3		1	1.3	
			I_I = 500 µA,	I_C = 350 mA		1.2	1.6		1.2	1.6	
V_F	Clamp forward voltage	8	I_F = 350 mA			1.7	2		1.7	2	V
I_{CEX}	Collector cutoff current	1	V_{CE} = 50 V,	I_I = 0			50			50	µA
		2	V_{CE} = 50 V, T_A = 70°C	I_I = 0			100			100	
				V_I = 6 V						500	
$I_{I(off)}$	Off-state input current	3	V_{CE} = 50 V, T_A = 70°C	I_C = 500 µA,	50	65		50	65		µA
I_I	Input current	4	V_I = 17 V						0.82	1.25	mA
I_R	Clamp reverse current	7	V_R = 50 V,	T_A = 70°C			100			100	µA
			V_R = 50 V				50			50	
h_{FE}	Static forward-current transfer ratio	5	V_{CE} = 2 V,	I_C = 350 mA	1000						
C_i	Input capacitance		V_I = 0,	f = 1 MHz		15	25		15	25	pF

**The ULN2001A is obsolete
and is no longer supplied.**

electrical characteristics, T_A = 25°C (unless otherwise noted) (continued)

PARAMETER		TEST FIGURE	TEST CONDITIONS		ULN2003A			ULN2004A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
$V_{I(on)}$	On-state input voltage	6	V_{CE} = 2 V	I_C = 125 mA						5	V
				I_C = 200 mA			2.4			6	
				I_C = 250 mA			2.7				
				I_C = 275 mA						7	
				I_C = 300 mA			3				
				I_C = 350 mA						8	
$V_{CE(sat)}$	Collector-emitter saturation voltage	5	I_I = 250 µA,	I_C = 100 mA		0.9	1.1		0.9	1.1	V
			I_I = 350 µA,	I_C = 200 mA		1	1.3		1	1.3	
			I_I = 500 µA,	I_C = 350 mA		1.2	1.6		1.2	1.6	
I_{CEX}	Collector cutoff current	1	V_{CE} = 50 V,	I_I = 0			50			50	µA
		2	V_{CE} = 50 V, T_A = 70°C	I_I = 0			100			100	
				V_I = 1 V						500	
V_F	Clamp forward voltage	8	I_F = 350 mA			1.7	2		1.7	2	V
$I_{I(off)}$	Off-state input current	3	V_{CE} = 50 V, T_A = 70°C	I_C = 500 µA,	50	65		50	65		µA
I_I	Input current	4	V_I = 3.85 V			0.93	1.35				mA
			V_I = 5 V						0.35	0.5	
			V_I = 12 V						1	1.45	
I_R	Clamp reverse current	7	V_R = 50 V				50			50	µA
			V_R = 50 V,	T_A = 70°C			100			100	
C_i	Input capacitance		V_I = 0,	f = 1 MHz		15	25		15	25	pF

TEXAS INSTRUMENTS

ULN2001A, ULN2002A, ULN2003A, ULN2004A, ULQ2003A, ULQ2004A
HIGH-VOLTAGE HIGH-CURRENT
DARLINGTON TRANSISTOR ARRAY

The ULN2001A is obsolete and is no longer supplied.

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electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		ULQ2003A			ULQ2004A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
$V_{I(on)}$	On-state input voltage	6	$V_{CE} = 2$ V	$I_C = 125$ mA						5	V
				$I_C = 200$ mA			2.7			6	
				$I_C = 250$ mA			2.9				
				$I_C = 275$ mA						7	
				$I_C = 300$ mA			3				
				$I_C = 350$ mA						8	
$V_{CE(sat)}$	Collector-emitter saturation voltage	5	$I_I = 250$ μA, $I_C = 100$ mA		0.9	1.2		0.9	1.1		V
			$I_I = 350$ μA, $I_C = 200$ mA		1	1.4		1	1.3		
			$I_I = 500$ μA, $I_C = 350$ mA		1.2	1.7		1.2	1.6		
I_{CEX}	Collector cutoff current	1	$V_{CE} = 50$ V, $I_I = 0$				100			50	μA
		2	$V_{CE} = 50$ V	$I_I = 0$			100			100	
				$V_I = 1$ V						500	
V_F	Clamp forward voltage	8	$I_F = 350$ mA			1.7	2.3		1.7	2	V
$I_{I(off)}$	Off-state input current	3	$V_{CE} = 50$ V, $I_C = 500$ μA			65		50	65		μA
I_I	Input current	4	$V_I = 3.85$ V			0.93	1.35				mA
			$V_I = 5$ V						0.35	0.5	
			$V_I = 12$ V						1	1.45	
I_R	Clamp reverse current	7	$V_R = 50$ V, $T_A = 25°C$				100			50	μA
			$V_R = 50$ V				100			100	
C_i	Input capacitance		$V_I = 0$, $f = 1$ MHz			15	25		15	25	pF

switching characteristics, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	ULN2001A, ULN2002A, ULN2003A, ULN2004A			UNIT
			MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 9		0.25	1	μs
t_{PHL}	Propagation delay time, high- to low-level output	See Figure 9		0.25	1	μs
V_{OH}	High-level output voltage after switching	$V_S = 50$ V, $I_O \approx 300$ mA, See Figure 10	V_S-20			mV

switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	ULQ2003A, ULQ2004A			UNIT
			MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 9		1	10	μs
t_{PHL}	Propagation delay time, high- to low-level output	See Figure 9		1	10	μs
V_{OH}	High-level output voltage after switching	$V_S = 50$ V, $I_O \approx 300$ mA, See Figure 10	V_S-500			mV

TEXAS INSTRUMENTS

**The ULN2001A is obsolete
and is no longer supplied.**

PARAMETER MEASUREMENT INFORMATION
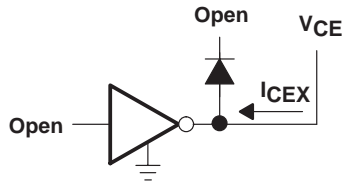
Figure 1. I_{CEX} Test Circuit
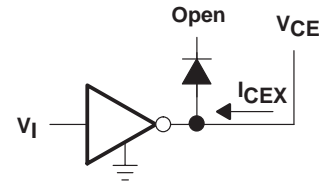
Figure 2. I_{CEX} Test Circuit
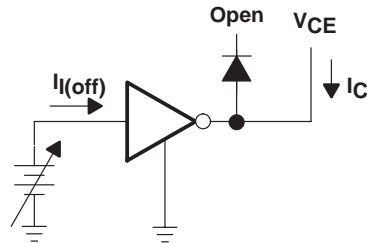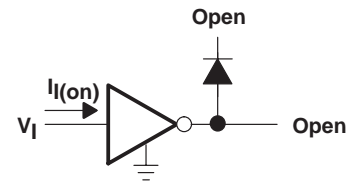
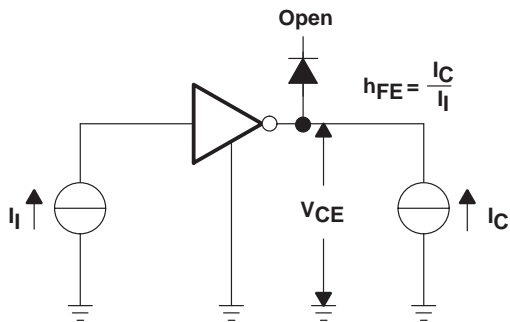

Figure 3. $I_{I(off)}$ Test Circuit

Figure 4. I_I Test Circuit

$$h_{FE} = \frac{I_C}{I_I}$$

NOTE: I_I is fixed for measuring $V_{CE(sat)}$, variable for
measuring h_{FE}.
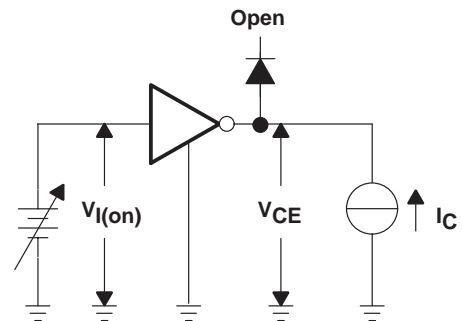
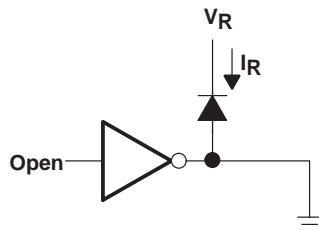**Figure 5. h_{FE}, $V_{CE(sat)}$ Test Circuit**
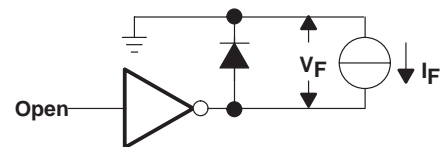

Figure 6. $V_{I(on)}$ Test Circuit

Figure 7. I_R Test Circuit

Figure 8. V_F Test Circuit

**TEXAS
INSTRUMENTS**

ULN2001A, ULN2002A, ULN2003A, ULN2004A, ULQ2003A, ULQ2004A
HIGH-VOLTAGE HIGH-CURRENT
DARLINGTON TRANSISTOR ARRAY
SLRS027G – DECEMBER 1976 – REVISED JUNE 2004

The ULN2001A is obsolete
and is no longer supplied.

PARAMETER MEASUREMENT INFORMATION

VOLTAGE WAVEFORMS
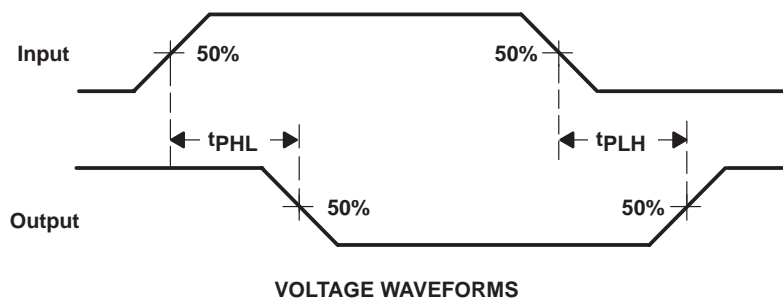
Figure 9. Propagation Delay-Time Waveforms

TEST CIRCUIT

VOLTAGE WAVEFORMS
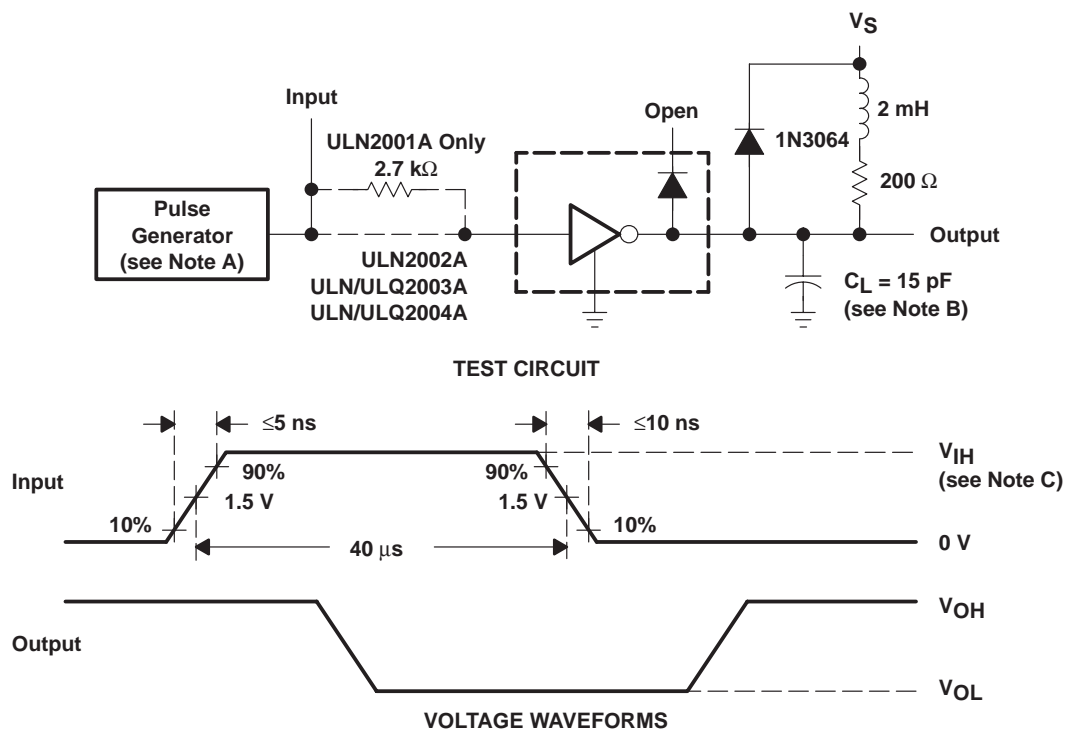
NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.
        B. C_L includes probe and jig capacitance.
        C. For testing the ULN2001A, the ULN2003A, and the ULQ2003A, V_{IH} = 3 V; for the ULN2002A, V_{IH} = 13 V;
            for the ULN2004A and the ULQ2004A, V_{IH} = 8 V.

Figure 10. Latch-Up Test Circuit and Voltage Waveforms

TEXAS
INSTRUMENTS
POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

**The ULN2001A is obsolete
and is no longer supplied.**

TYPICAL CHARACTERISTICS

COLLECTOR-EMITTER
SATURATION VOLTAGE
vs
COLLECTOR CURRENT
(ONE DARLINGTON)
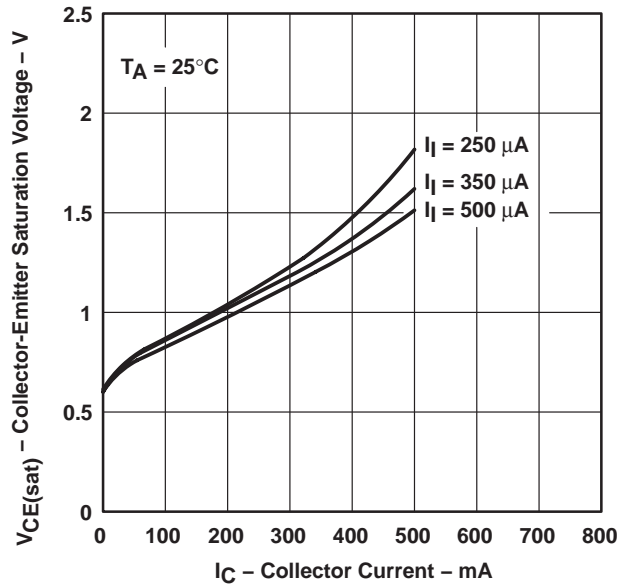
COLLECTOR-EMITTER
SATURATION VOLTAGE
vs
TOTAL COLLECTOR CURRENT
(TWO DARLINGTONS IN PARALLEL)
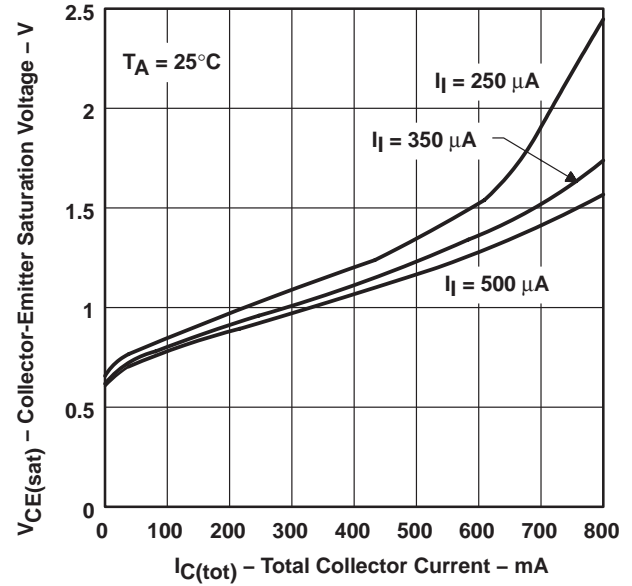
Figure 11

Figure 12

COLLECTOR CURRENT
vs
INPUT CURRENT
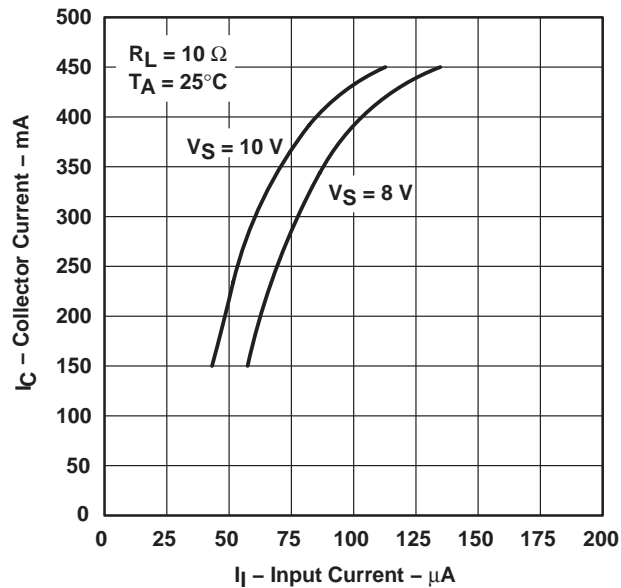
Figure 13

ULN2001A, ULN2002A, ULN2003A, ULN2004A, ULQ2003A, ULQ2004A
HIGH-VOLTAGE HIGH-CURRENT
DARLINGTON TRANSISTOR ARRAY
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The ULN2001A is obsolete
and is no longer supplied.

THERMAL INFORMATION

D PACKAGE
MAXIMUM COLLECTOR CURRENT
vs
DUTY CYCLE
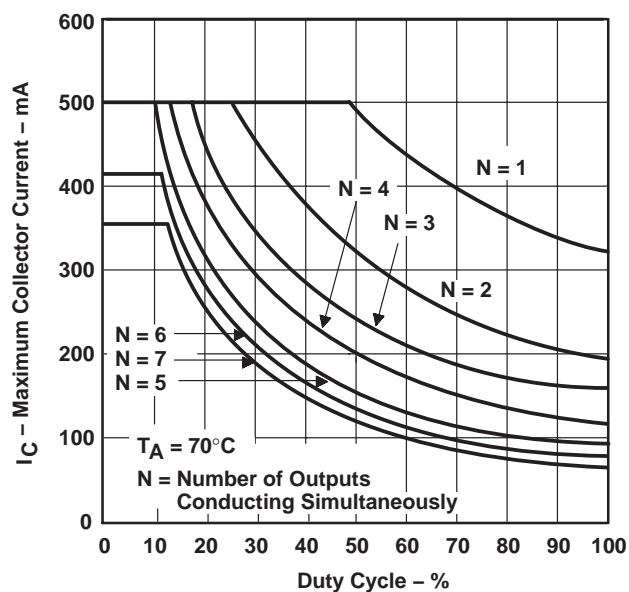
Figure 14

N PACKAGE
MAXIMUM COLLECTOR CURRENT
vs
DUTY CYCLE
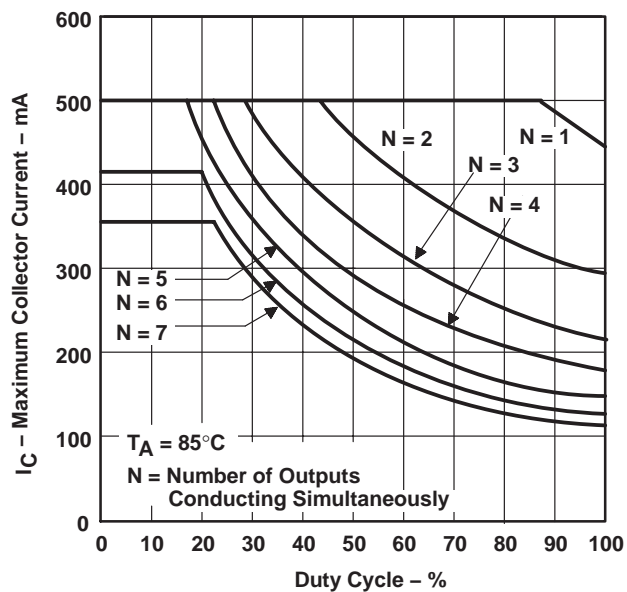
Figure 15

TEXAS
INSTRUMENTS

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**The ULN2001A is obsolete
and is no longer supplied.**

APPLICATION INFORMATION
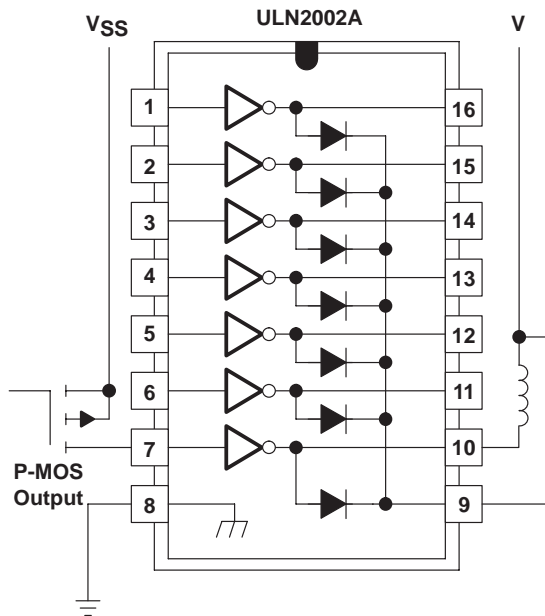
Figure 16. P-MOS to Load
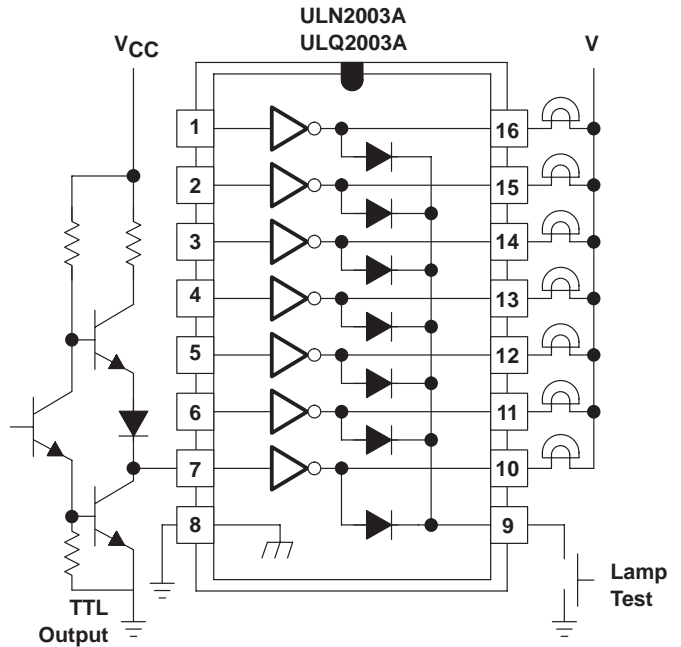
Figure 17. TTL to Load
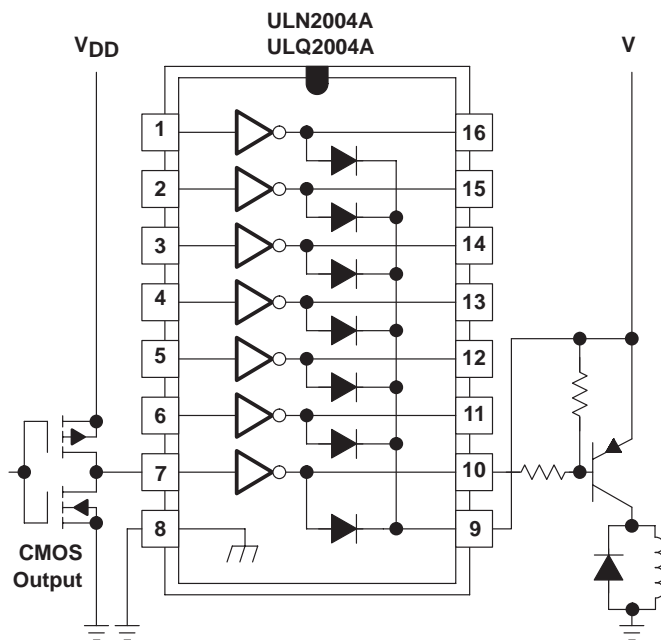
Figure 18. Buffer for Higher Current Loads
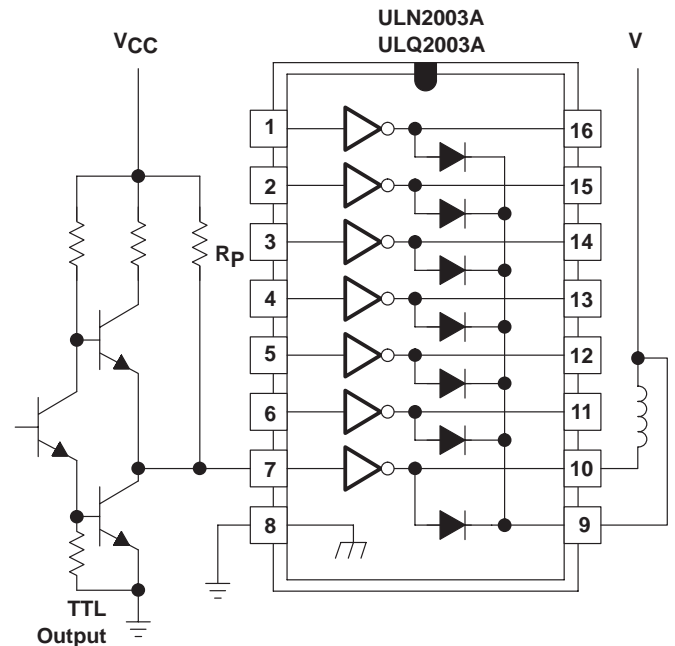
**Figure 19. Use of Pullup Resistors
to Increase Drive Current**

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
ULN2001AD	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
ULN2001ADR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
ULN2001AN	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
ULN2002AD	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
ULN2002AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
ULN2002ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
ULN2003AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULN2003ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULN2003ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULN2003ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULN2003ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULN2003ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULN2003AJ	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
ULN2003AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
ULN2003ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
ULN2003ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULN2003ANSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULN2003ANSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULN2003APW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULN2003APWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULN2003APWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULN2003APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULN2003APWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULN2003APWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULN2004AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULN2004ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULN2004ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
ULN2004ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULN2004ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULN2004ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULN2004AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
ULN2004ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
ULN2004ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULN2004ANSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULQ2003AD	NRND	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
ULQ2003ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULQ2003ADR	NRND	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
ULQ2003ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULQ2003AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
ULQ2004AD	NRND	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
ULQ2004ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULQ2004ADR	NRND	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
ULQ2004ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULQ2004AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
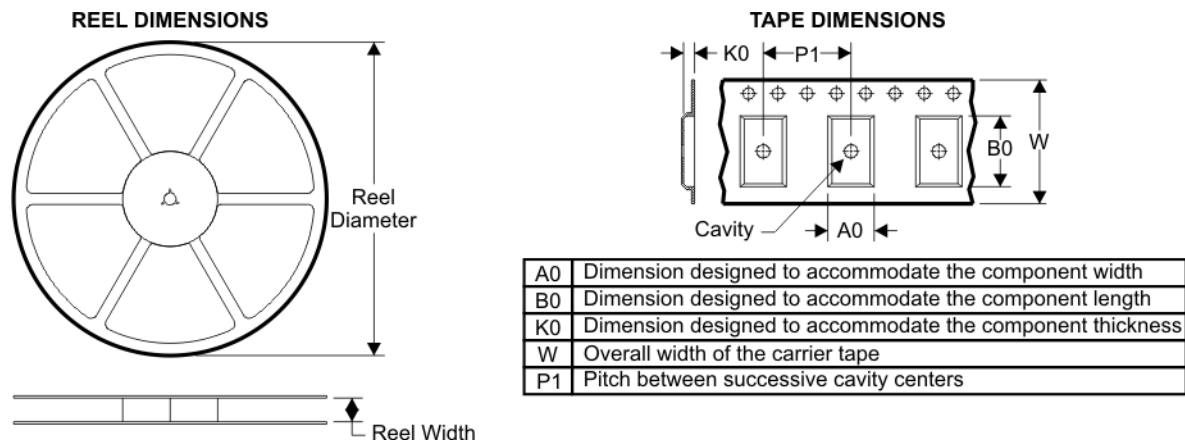**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
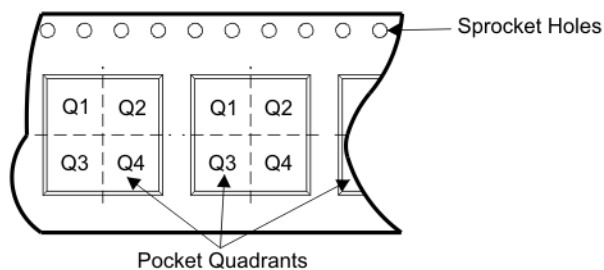
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TAPE AND REEL BOX INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ULN2003ADR	D	16	SITE 27	330	16	6.5	10.3	2.1	8	16	Q1
ULN2003ADR	D	16	SITE 41	330	16	6.5	10.3	2.1	8	16	Q1
ULN2003ANSR	NS	16	SITE 41	330	16	8.2	10.5	2.5	12	16	Q1
ULN2003APWR	PW	16	SITE 41	330	12	7.0	5.6	1.6	8	12	Q1
ULN2004ADR	D	16	SITE 27	330	16	6.5	10.3	2.1	8	16	Q1
ULN2004ADR	D	16	SITE 41	330	16	6.5	10.3	2.1	8	16	Q1
ULN2004ANSR	NS	16	SITE 41	330	16	8.2	10.5	2.5	12	16	Q1

TAPE AND REEL BOX DIMENSIONS

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
ULN2003ADR	D	16	SITE 27	342.9	336.6	0.0
ULN2003ADR	D	16	SITE 41	346.0	346.0	0.0
ULN2003ANSR	NS	16	SITE 41	346.0	346.0	0.0
ULN2003APWR	PW	16	SITE 41	346.0	346.0	0.0
ULN2004ADR	D	16	SITE 27	342.9	336.6	0.0
ULN2004ADR	D	16	SITE 41	346.0	346.0	0.0
ULN2004ANSR	NS	16	SITE 41	346.0	346.0	0.0

DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

0.065 (1,65)
0.045 (1,14)

1   7

C

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°−15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. This package is hermetically sealed with a ceramic lid using glass frit.
         D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E. Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

N (R-PDIP-T**)
16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE

PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14)

0.045 (1,14) / 0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

0.010 (0,25) M

14/18 Pin Only
20 Pin vendor option

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

TEXAS INSTRUMENTS
www.ti.com

D (R−PDSO−G16) PLASTIC SMALL−OUTLINE PACKAGE

0.394 (10,00)
0.386 (9,80)
⟨C⟩

16

9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) ⟨D⟩

1

8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−4/H 11/2006

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
      ⟨C⟩   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
             not exceed .006 (0,15) per end.
      ⟨D⟩   Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
         E.   Reference JEDEC MS−012 variation AC.

TEXAS
INSTRUMENTS
www.ti.com

NS (R-PDSO-G)**   PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

PINS ** DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G)**   **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

PINS ** DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
        D. Falls within JEDEC MO-153