TMS320F28335, TMS320F28334, TMS320F28332
Digital Signal Controllers (DSCs)

Data Manual

Literature Number: SPRS439
June 2007

TEXAS INSTRUMENTS

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  - **1.9-V Core, 3.3-V I/O Design**
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- **Temperature Options:**
  - **A: -40°C to 85°C**
  - **S: -40°C to 125°C**

(1) IEEE Standard 1149.1-1990 Standard Test Access Port and Boundary Scan Architecture

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1.2 Getting Started

This section gives a brief overview of the steps to take when first developing for a C28x device. For more detail on each of these steps, see the following:

- *Getting Started With TMS320C28x™ Digital Signal Controllers* (literature number SPRAAM0).
- C2000 Getting Started Website (http://www.ti.com/c2000getstarted)

2 Introduction

The TMS320F28335, TMS320F28334, and TMS320F28332, devices, members of the TMS320C28x™ DSC generation, are highly integrated, high-performance solutions for demanding control applications.

Throughout this document, TMS320F28335, TMS320F28334, and TMS320F28332, are abbreviated as F28335, F28334, and F28332, respectively. Table 2-1 provides a summary of features for each device.

Table 2-1. Hardware Features

FEATURE		F28335 (150 MHz)	F28334 (150 MHz)	F28332 (100 MHz)
Instruction cycle		6.67 ns	6.67 ns	10 ns
Floating-point Unit		Yes	Yes	Yes
3.3-V on-chip flash (16-bit word)		256K	128K	64K
Single-access RAM (SARAM) (16-bit word)		34K	34K	26K
Code security for on-chip flash/SARAM/OTP blocks		Yes	Yes	Yes
Boot ROM (8K X16)		Yes	Yes	Yes
One-time programmable (OTP) ROM (16-bit word)		1K	1K	1K
6-channel Direct Memory Access (DMA)		Yes	Yes	Yes
PWM outputs		ePWM1/2/3/4/5/6	ePWM1/2/3/4/5/6	ePWM1/2/3/4/5/6
HRPWM channels		ePWM1A/2A/3A/4A/5A/6A	ePWM1A/2A/3A/4A/5A/6A	ePWM1A/2A/3A/4A
32-bit Capture inputs or auxiliary PWM outputs		6	6	4
32-bit QEP channels (four inputs/channel)		2	2	2
Watchdog timer		Yes	Yes	Yes
12-Bit ADC	No. of channels	16	16	16
	MSPS	12.5	12.5	12.5
	Conversion time	80 ns	80 ns	80 ns
32-Bit CPU timers		3	3	3
Multichannel Buffered Serial Port (McBSP)/SPI		2	2	1
Serial Peripheral Interface (SPI)		1	1	1
Serial Communications Interface (SCI)		3	3	2
Enhanced Controller Area Network (eCAN)		2	2	2
Inter-Integrated Circuit (I2C)		1	1	1
Digital I/O pins (shared)		88	88	88
External interrupts		8	8	8
Packaging	100-Pin PGF	Yes	Yes	Yes
	100-Ball ZHH	Yes	Yes	Yes
Temperature options	A: -40°C to 85°C	(PGF, ZHH)	(PGF, ZHH)	(PGF, ZHH)
Product status		TMX	TMX	TMX

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2.1 Pin Assignments

The 176-pin PZ low-profile quad flatpack (LQFP) pin assignments are shown in Figure 2-1. The 179-ball ZHH ball grid array (BGA) terminal assignments are shown in Figure 2-2 through Figure 2-5. Table 2-2 describes the function(s) of each pin.

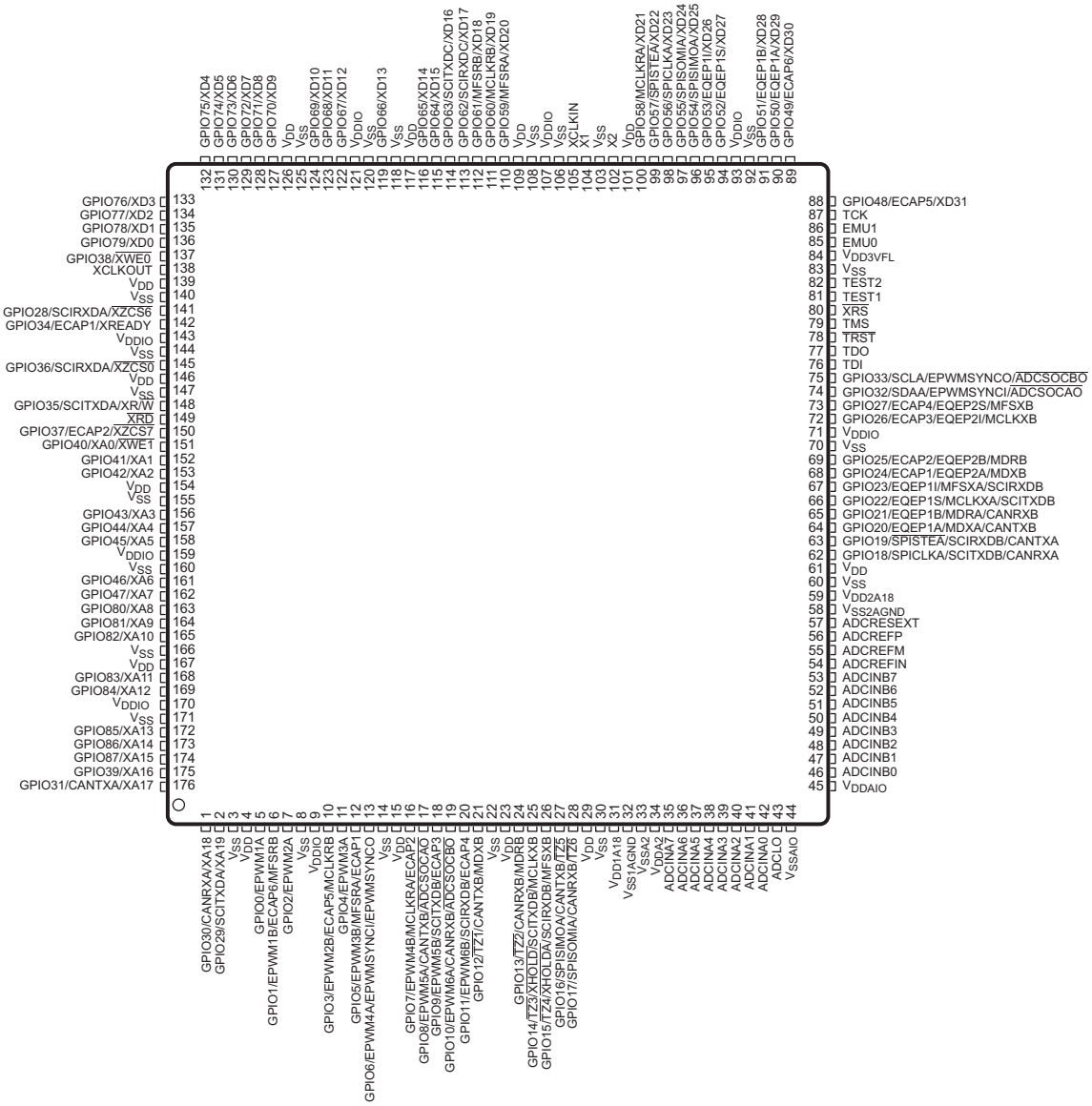

Figure 2-1. F28335, F28334, F28332 176-Pin PGF LQFP (Top View)

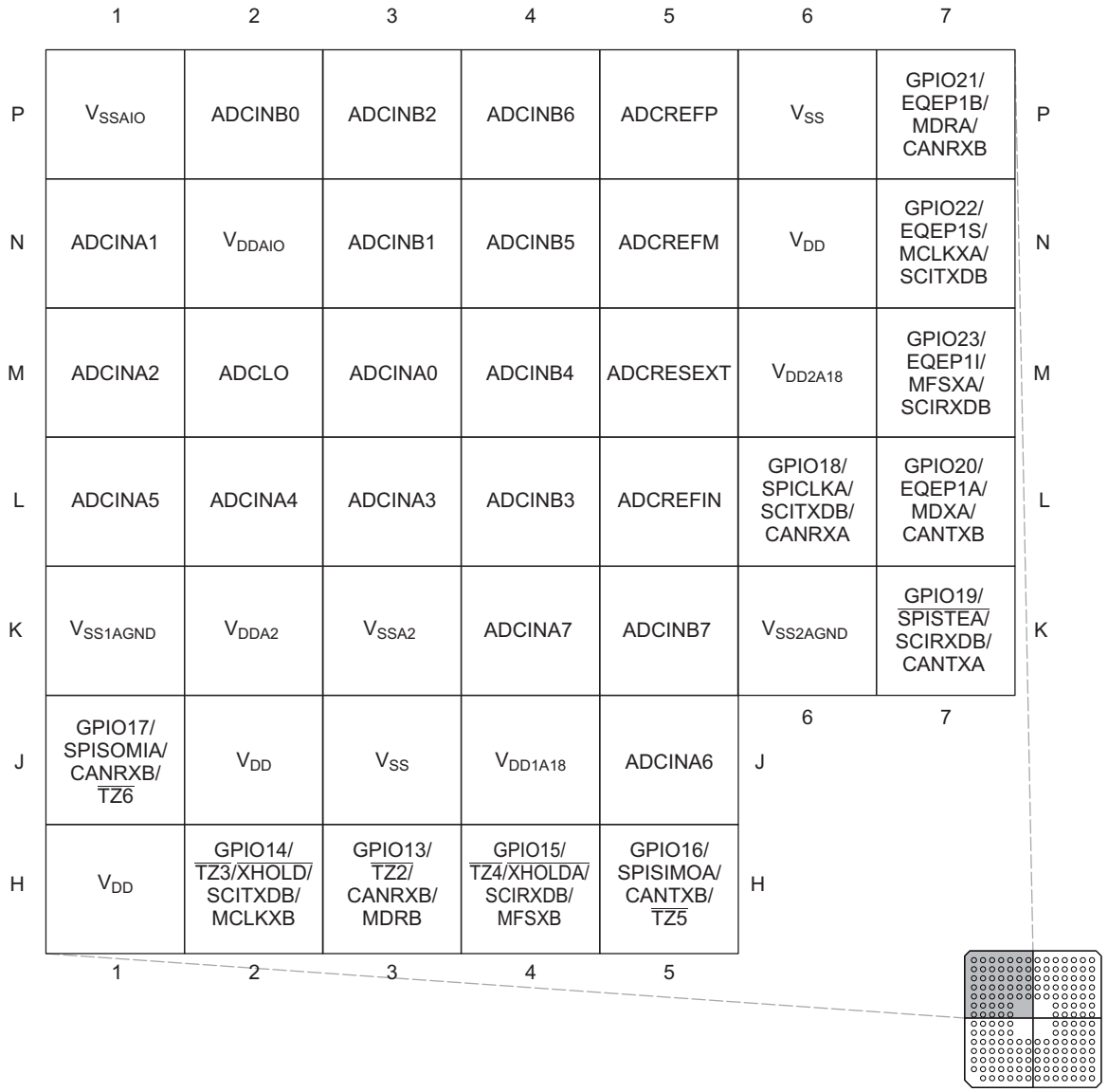

Figure 2-2. F28335, F28334, F28332 179-Ball ZHH MicroStar BGA™ (Upper Left Quadrant) (Bottom View)

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	8	9	10	11	12	13	14	
P	V_{SS}	GPIO33/ SCLA/ EPWMSYNCO/ $\overline{\text{ADCSOCBO}}$	TMS	TEST2	EMU1	GPIO48/ ECAP5/ XD31	GPIO50/ EQEP1A/ XD29	P
N	GPIO25/ ECAP2/ EQEP2B/ MDRB	GPIO32/ SDAA/ EPWMSYNCI/ $\overline{\text{ADCSOCAO}}$	V_{SS}	V_{SS}	TCK	GPIO49/ ECAP6/ XD30	V_{DDIO}	N
M	GPIO24/ ECAP1/ EQEP2A/ MDXB	TDI	$\overline{\text{TRST}}$	V_{DD3VFL}	V_{SS}	GPIO51/ EQEP1B/ XD28	GPIO52/ EQEP1S/ XD27	M
L	V_{DDIO}	GPIO27/ ECAP4/ EQEP2S/ MFSXB	$\overline{\text{XRS}}$	EMU0	GPIO53/ EQEP1I/ XD26	GPIO54/ SPISIMOA/ XD25	GPIO55/ SPISOMIA/ XD24	L
K	GPIO26/ ECAP3/ EQEP2I/ MCLKXB	TDO	TEST1	GPIO56/ SPICLKA/ XD23	GPIO58/ MCLKRA/ XD21	GPIO57/ $\overline{\text{SPISTEA}}$/ XD22	V_{DD}	K
	8	9						
J			V_{SS}	X2	V_{SS}	X1	XCLKIN	J
H			V_{SS}	V_{DDIO}	V_{DD}	V_{SS}	GPIO59/ MFSRA/ XD20	H
			10	11	12	13	14	

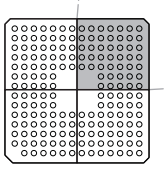


Figure 2-3. F28335, F28334, F28332 179-Ball ZHH MicroStar BGA™ (Upper Right Quadrant) (Bottom View)

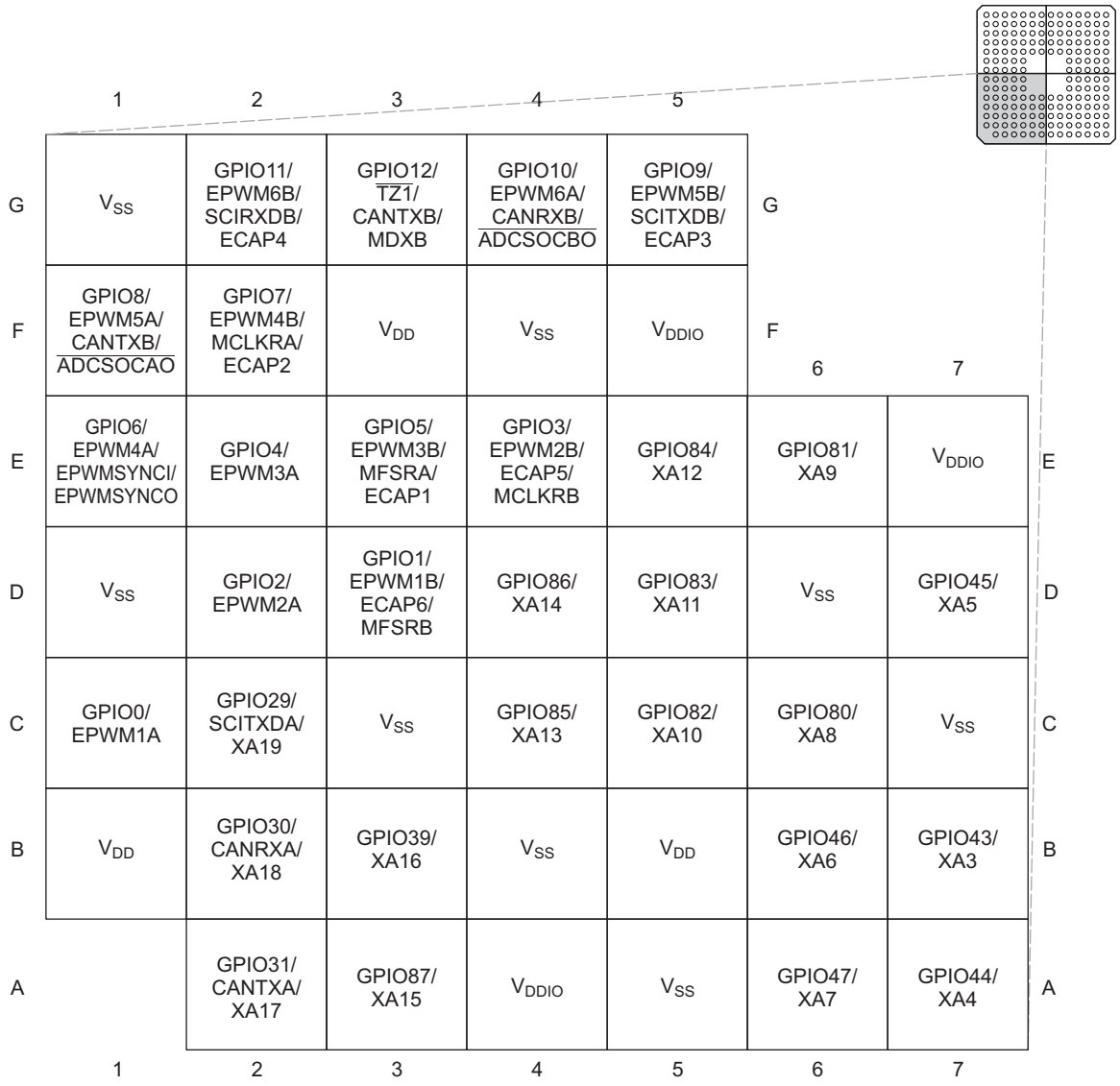
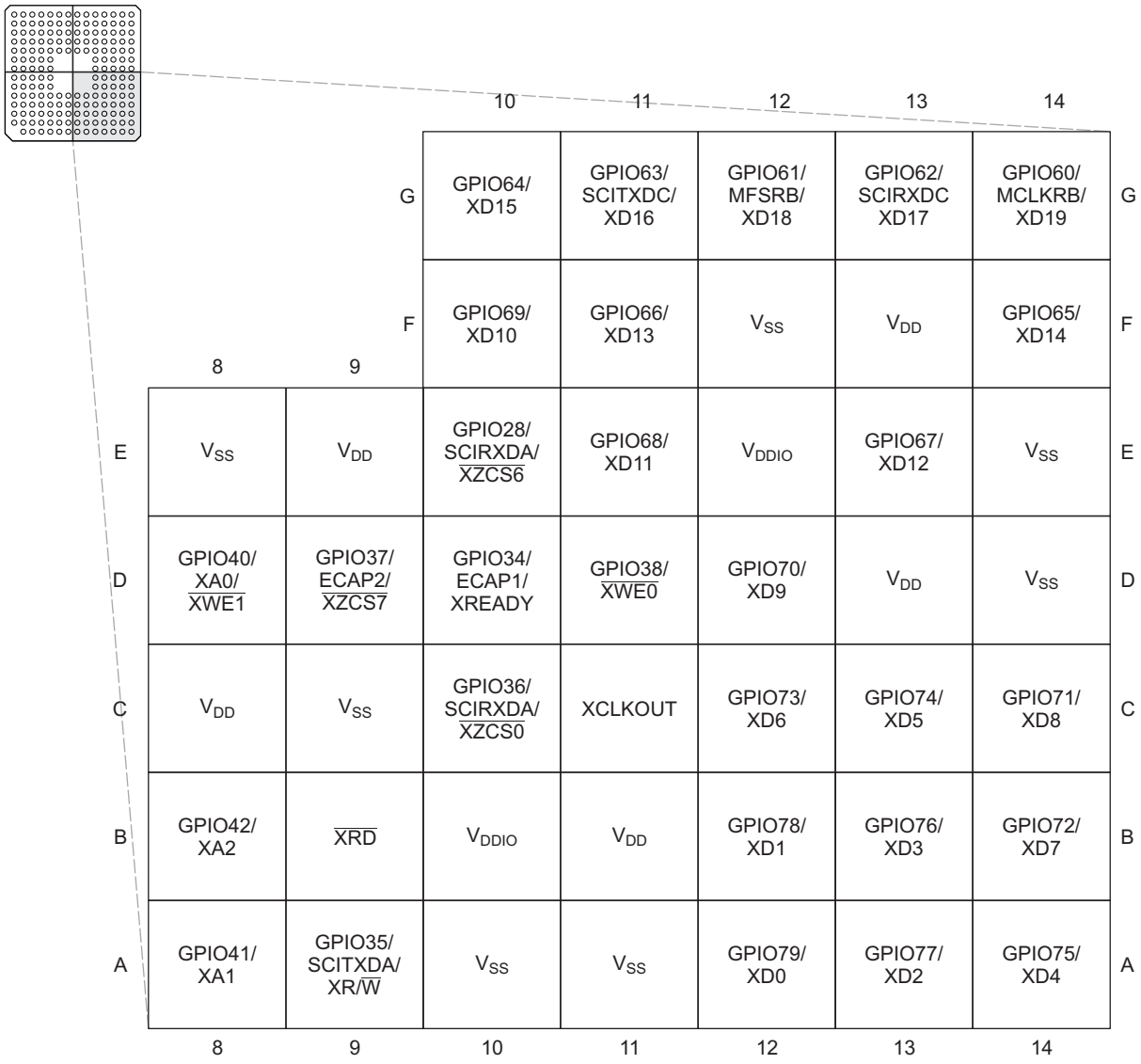


Figure 2-4. F28335, F28334, F28332 179-Ball ZHH MicroStar BGA™ (Lower Left Quadrant) (Bottom View)

PRODUCT PREVIEW



	8	9	10	11	12	13	14	
G			GPIO64/ XD15	GPIO63/ SCITXDC/ XD16	GPIO61/ MFSRB/ XD18	GPIO62/ SCIRXDC XD17	GPIO60/ MCLKRB/ XD19	G
F			GPIO69/ XD10	GPIO66/ XD13	V_{SS}	V_{DD}	GPIO65/ XD14	F
E	V_{SS}	V_{DD}	GPIO28/ SCIRXDA/ $\overline{XZCS6}$	GPIO68/ XD11	V_{DDIO}	GPIO67/ XD12	V_{SS}	E
D	GPIO40/ XA0/ $\overline{XWE1}$	GPIO37/ ECAP2/ $\overline{XZCS7}$	GPIO34/ ECAP1/ XREADY	GPIO38/ $\overline{XWE0}$	GPIO70/ XD9	V_{DD}	V_{SS}	D
C	V_{DD}	V_{SS}	GPIO36/ SCIRXDA/ $\overline{XZCS0}$	XCLKOUT	GPIO73/ XD6	GPIO74/ XD5	GPIO71/ XD8	C
B	GPIO42/ XA2	$\overline{XRD}$	V_{DDIO}	V_{DD}	GPIO78/ XD1	GPIO76/ XD3	GPIO72/ XD7	B
A	GPIO41/ XA1	GPIO35/ SCITXDA/ XR/$\overline{W}$	V_{SS}	V_{SS}	GPIO79/ XD0	GPIO77/ XD2	GPIO75/ XD4	A
	8	9	10	11	12	13	14	

Figure 2-5. F28335, F28334, F28332 179-Ball ZHH MicroStar BGA™ (Lower Right Quadrant) (Bottom View)

2.2 Signal Descriptions

Table 2-2 describes the signals on the 2833x devices. All digital inputs are TTL-compatible. All outputs are 3.3 V with CMOS levels. Inputs are not 5-V tolerant.

Table 2-2. Signal Descriptions

NAME	PIN NO.		DESCRIPTION (1)
	PGF PIN #	ZHH BALL #	
JTAG			
$\overline{\text{TRST}}$	78	M10	JTAG test reset with internal pulldown. $\overline{\text{TRST}}$, when driven high, gives the scan system control of the operations of the device. If this signal is not connected or driven low, the device operates in its functional mode, and the test reset signals are ignored. NOTE: Do not use pullup resistors on $\overline{\text{TRST}}$; it has an internal pull-down device. $\overline{\text{TRST}}$ is an active high test pin and must be maintained low at all times during normal device operation. In a low-noise environment, $\overline{\text{TRST}}$ may be left floating. In other instances, an external pulldown resistor is **highly recommended**. The value of this resistor should be based on drive strength of the debugger pods applicable to the design. A 2.2-kΩ resistor generally offers adequate protection. Since this is application-specific, it is recommended that each target board be validated for proper operation of the debugger and the application. (I, ↓)
TCK	87	N12	JTAG test clock with internal pullup (I, ↑)
TMS	79	P10	JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK. (I, ↑)
TDI	76	M9	JTAG test data input (TDI) with internal pullup. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK. (I, ↑)
TDO	77	K9	JTAG scan out, test data output (TDO). The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. (O/Z 8 mA drive)
EMU0	85	L11	Emulator pin 0. When $\overline{\text{TRST}}$ is driven high, this pin is used as an interrupt to or from the emulator system and is defined as input/output through the JTAG scan. This pin is also used to put the device into boundary-scan mode. With the EMU0 pin at a logic-high state and the EMU1 pin at a logic-low state, a rising edge on the $\overline{\text{TRST}}$ pin would latch the device into boundary-scan mode. (I/O/Z, 8 mA drive ↑) **NOTE:** An external pullup resistor is recommended on this pin. The value of this resistor should be based on the drive strength of the debugger pods applicable to the design. A 2.2-kΩ to 4.7-kΩ resistor is generally adequate. Since this is application-specific, it is recommended that each target board be validated for proper operation of the debugger and the application.
EMU1	86	P12	Emulator pin 1. When $\overline{\text{TRST}}$ is driven high, this pin is used as an interrupt to or from the emulator system and is defined as input/output through the JTAG scan. This pin is also used to put the device into boundary-scan mode. With the EMU0 pin at a logic-high state and the EMU1 pin at a logic-low state, a rising edge on the $\overline{\text{TRST}}$ pin would latch the device into boundary-scan mode. (I/O/Z, 8 mA drive ↑) **NOTE:** An external pullup resistor is recommended on this pin. The value of this resistor should be based on the drive strength of the debugger pods applicable to the design. A 2.2-kΩ to 4.7-kΩ resistor is generally adequate. Since this is application-specific, it is recommended that each target board be validated for proper operation of the debugger and the application.
FLASH			
V_{DD3VFL}	84	M11	3.3-V Flash Core Power Pin. This pin should be connected to 3.3 V at all times.
TEST1	81	K10	Test Pin. Reserved for TI. Must be left unconnected. (I/O)
TEST2	82	P11	Test Pin. Reserved for TI. Must be left unconnected. (I/O)
CLOCK			
XCLKOUT	138	C11	Output clock derived from SYSCLKOUT. XCLKOUT is either the same frequency, one-half the frequency, or one-fourth the frequency of SYSCLKOUT. This is controlled by the bits 1, 0 (XCLKOUTDIV) in the XCLK register. At reset, XCLKOUT = SYSCLKOUT/4. The XCLKOUT signal can be turned off by setting XCLKOUTDIV to 3. Unlike other GPIO pins, the XCLKOUT pin is not placed in high-impedance state during a reset. (O/Z, 8 mA drive).
XCLKIN	105	J14	External Oscillator Input. This pin is to feed a clock from an external 3.3-V oscillator. In this case, the X1 pin must be tied to GND. If a crystal/resonator is used (or if an external 1.8-V oscillator is used to feed clock to X1 pin), this pin must be tied to GND. (I)

(1) I = Input, O = Output, Z = High impedance, OD = Open drain, ↑ = Pullup, ↓ = Pulldown

Table 2-2. Signal Descriptions (continued)

NAME	PIN NO.		DESCRIPTION (1)
	PGF PIN #	ZHH BALL #	
X1	104	J13	Internal/External Oscillator Input. To use the internal oscillator, a quartz crystal or a ceramic resonator may be connected across X1 and X2. The X1 pin is referenced to the 1.8-V core digital power supply. A 1.8-V external oscillator may be connected to the X1 pin. In this case, the XCLKIN pin must be connected to ground. If a 3.3-V external oscillator is used with the XCLKIN pin, X1 must be tied to GND. (I)
X2	102	J11	Internal Oscillator Output. A quartz crystal or a ceramic resonator may be connected across X1 and X2. If X2 is not used it must be left unconnected. (O)
RESET			
$\overline{XRS}$	80	L10	Device Reset (in) and Watchdog Reset (out). Device reset. $\overline{XRS}$ causes the device to terminate execution. The PC will point to the address contained at the location 0x3FFFC0. When $\overline{XRS}$ is brought to a high level, execution begins at the location pointed to by the PC. This pin is driven low by the DSC when a watchdog reset occurs. During watchdog reset, the $\overline{XRS}$ pin is driven low for the watchdog reset duration of 512 OSCCLK cycles. (I/OD, ↑) The output buffer of this pin is an open-drain with an internal pullup. It is recommended that this pin be driven by an open-drain device.
ADC SIGNALS			
ADCINA7	35	K4	ADC Group A, Channel 7 input (I)
ADCINA6	36	J5	ADC Group A, Channel 6 input (I)
ADCINA5	37	L1	ADC Group A, Channel 5 input (I)
ADCINA4	38	L2	ADC Group A, Channel 4 input (I)
ADCINA3	39	L3	ADC Group A, Channel 3 input (I)
ADCINA2	40	M1	ADC Group A, Channel 2 input (I)
ADCINA1	41	N1	ADC Group A, Channel 1 input (I)
ADCINA0	42	M3	ADC Group A, Channel 0 input (I)
ADCINB7	53	K5	ADC Group B, Channel 7 input (I)
ADCINB6	52	P4	ADC Group B, Channel 6 input (I)
ADCINB5	51	N4	ADC Group B, Channel 5 input (I)
ADCINB4	50	M4	ADC Group B, Channel 4 input (I)
ADCINB3	49	L4	ADC Group B, Channel 3 input (I)
ADCINB2	48	P3	ADC Group B, Channel 2 input (I)
ADCINB1	47	N3	ADC Group B, Channel 1 input (I)
ADCINB0	46	P2	ADC Group B, Channel 0 input (I)
ADCLO	43	M2	Low Reference (connect to analog ground) (I)
ADCRESEXT	57	M5	ADC External Current Bias Resistor. Connect a 22-kΩ resistor to analog ground.
ADCREFIN	54	L5	External reference input (I)
ADCREFP	56	P5	Internal Reference Positive Output. Requires a low ESR (50 mΩ - 1.5 Ω) ceramic bypass capacitor of 2.2 µF to analog ground. (O)
ADCREFM	55	N5	Internal Reference Medium Output. Requires a low ESR (50 mΩ - 1.5 Ω) ceramic bypass capacitor of 2.2 µF to analog ground. (O)
CPU AND I/O POWER PINS			
V_{DDA2}	34	K2	ADC Analog Power Pin
V_{SSA2}	33	K3	ADC Analog Ground Pin
V_{DDAIO}	45	N2	ADC Analog I/O Power Pin
V_{SSAIO}	44	P1	ADC Analog I/O Ground Pin
V_{DD1A18}	31	J4	ADC Analog Power Pin
$V_{SS1AGND}$	32	K1	ADC Analog Ground Pin
V_{DD2A18}	59	M6	ADC Analog Power Pin
$V_{SS2AGND}$	58	K6	ADC Analog Ground Pin

Table 2-2. Signal Descriptions (continued)

NAME	PIN NO.		DESCRIPTION (1)
	PGF PIN #	ZHH BALL #	
V_{DD}	4	B1	CPU and Logic Digital Power Pins
V_{DD}	15	B5	
V_{DD}	23	B11	
V_{DD}	29	C8	
V_{DD}	61	D13	
V_{DD}	101	E9	
V_{DD}	109	F3	
V_{DD}	117	F13	
V_{DD}	126	H1	
V_{DD}	139	H12	
V_{DD}	146	J2	
V_{DD}	154	K14	
V_{DD}	167	N6	
V_{DDIO}	9	A4	Digital I/O Power Pin
V_{DDIO}	71	B10	
V_{DDIO}	93	E7	
V_{DDIO}	107	E12	
V_{DDIO}	121	F5	
V_{DDIO}	143	L8	
V_{DDIO}	159	H11	
V_{DDIO}	170	N14	
V_{SS}	3	A5	Digital Ground Pins
V_{SS}	8	A10	
V_{SS}	14	A11	
V_{SS}	22	B4	
V_{SS}	30	C3	
V_{SS}	60	C7	
V_{SS}	70	C9	
V_{SS}	83	D1	
V_{SS}	92	D6	
V_{SS}	103	D14	
V_{SS}	106	E8	
V_{SS}	108	E14	
V_{SS}	118	F4	
V_{SS}	120	F12	
V_{SS}	125	G1	
V_{SS}	140	H10	
V_{SS}	144	H13	
V_{SS}	147	J3	
V_{SS}	155	J10	
V_{SS}	160	J12	
V_{SS}	166	M12	
V_{SS}	171	N10	
V_{SS}		N11	
V_{SS}		P6	

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Table 2-2. Signal Descriptions (continued)

NAME	PIN NO.		DESCRIPTION (1)
	PGF PIN #	ZHH BALL #	
V_{SS}		P8	Digital Ground Pins
GPIOA AND PERIPHERAL SIGNALS(2)(3)			
GPIO0 EPWM1A - -	5	C1	General purpose input/output 0 (I/O/Z) (4) Enhanced PWM1 Output A and HRPWM channel (O) - -
GPIO1 EPWM1B ECAP6 MFSRB	6	D3	General purpose input/output 1 (I/O/Z)(4) Enhanced PWM1 Output B (O) Enhanced Capture 6 input/output (I/O) McBSP-B receive frame synch (I/O)
GPIO2 EPWM2A - -	7	D2	General purpose input/output 2 (I/O/Z)(4) Enhanced PWM2 Output A and HRPWM channel (O) - -
GPIO3 EPWM2B ECAP5 MCLKRB	10	E4	General purpose input/output 3 (I/O/Z)(4) Enhanced PWM2 Output B (O) Enhanced Capture 5 input/output (I/O) McBSP-B clock receive (I/O)
GPIO4 EPWM3A - -	11	E2	General purpose input/output 4 (I/O/Z)(4) Enhanced PWM3 output A and HRPWM channel (O) - -
GPIO5 EPWM3B MFSRA ECAP1	12	E3	General purpose input/output 5 (I/O/Z)(4) Enhanced PWM3 output B (O) McBSP-A receive frame synch (I/O) Enhanced Capture input/output 1 (I/O)
GPIO6 EPWM4A EPWMSYNCI EPWMSYNCO	13	E1	General purpose input/output 6 (I/O/Z)(4) Enhanced PWM4 output A and HRPWM channel (O) External ePWM sync pulse input (I) External ePWM sync pulse output (O)
GPIO7 EPWM4B MCLKRA ECAP2	16	F2	General purpose input/output 7 (I/O/Z)(4) Enhanced PWM4 output B (O) McBSP-A Clock Receive (I/O) Enhanced capture input/output 2 (I/O)
GPIO8 EPWM5A CANTXB $\overline{\text{ADCSOCAO}}$	17	F1	General Purpose Input/Output 8 (I/O/Z)(4) Enhanced PWM5 output A (O) Enhanced CAN-B transmit (O) ADC start-of-conversion A (O)
GPIO9 EPWM5B SCITXDB ECAP3	18	G5	General purpose input/output 9 (I/O/Z)(4) Enhanced PWM5 output B (O) SCI-B transmit data(O) Enhanced capture input/output 3 (I/O)
GPIO10 EPWM6A CANRXB $\overline{\text{ADCSOCBO}}$	19	G4	General purpose input/output 10 (I/O/Z)(4) Enhanced PWM6 output A (O) Enhanced CAN-B receive (I) ADC start-of-conversion B (O)
GPIO11 EPWM6B SCIRXDB ECAP4	20	G2	General purpose input/output 11 (I/O/Z)(4) Enhanced PWM6 output B (O) SCI-B receive data (I) Enhanced CAP Input/Output 4 (I/O)

(2) Some peripheral functions may not be available in all devices. See Table 2-1 for details.
(3) All GPIO pins are I/O/Z, 4-mA drive typical (unless otherwise indicated), and have an internal pullup, which can be selectively enabled/disabled on a per-pin basis. This feature only applies to the GPIO pins. The GPIO function (shown in Italics) is the default at reset. The peripheral signals that are listed under them are alternate functions.
(4) The pullups on GPIO0-GPIO11 pins are not enabled at reset.

Table 2-2. Signal Descriptions (continued)

NAME	PIN NO.		DESCRIPTION (1)
	PGF PIN #	ZHH BALL #	
GPIO12 TZ1 CANTXB MDXB	21	G3	General purpose input/output 12 (I/O/Z)(5) Trip Zone input 1 (I) Enhanced CAN-B transmit (O) McBSP-B transmit serial data (O)
GPIO13 TZ2 CANRXB MDRB	24	H3	General purpose input/output 13 (I/O/Z)(5) Trip Zone input 2 (I) Enhanced CAN-B receive (I) McBSP-B receive serial data (I)
GPIO14 TZ3/XHOLD SCITXDB MCLKXB	25	H2	General purpose input/output 14 (I/O/Z)(5) Trip Zone input 3/External Hold Request. XHOLD, when active (low), requests the external memory interface (XINTF) to release the external bus and place all buses and strobes into a high-impedance state. The XINTF will release the bus when any current access is complete and there are no pending accesses on the XINTF. (I) SCI-B Transmit (I) McBSP-B clock transmit (I/O)
GPIO15 TZ4/XHOLDA SCIRXDB MFSXB	26	H4	General purpose input/output 15 (I/O/Z)(5) Trip Zone input 4/External Hold Acknowledge. XHOLDA is driven active (low) when the XINTF has granted an XHOLD request. All XINTF buses and strobe signals will be in a high-impedance state. XHOLDA is released when the XHOLD signal is released. External devices should only drive the external bus when XHOLDA is active (low). (I) SCI-B receive (I) McBSP-B transmit frame synch (I/O)
GPIO16 SPISIMOA CANTXB TZ5	27	H5	General purpose input/output 16 (I/O/Z)(5) SPI slave in, master out (I/O) Enhanced CAN-B transmit (O) Trip Zone input 5 (I)
GPIO17 SPISOMIA CANRXB TZ6	28	J1	General purpose input/output 17 (I/O/Z)(5) SPI-A slave out, master in (I/O) Enhanced CAN-B receive (I) Trip zone input 6 (I)
GPIO18 SPICLKA SCITXDB CANRXA	62	L6	General purpose input/output 18 (I/O/Z)(5) SPI-A clock input/output (I/O) SCI-B transmit (O) Enhanced CAN-A receive (I)
GPIO19 SPISTEA SCIRXDB CANTXA	63	K7	General purpose input/output 19 (I/O/Z)(5) SPI-A slave transmit enable input/output (I/O) SCI-B receive (I) Enhanced CAN-A transmit (O)
GPIO20 EQEP1A MDXA CANTXB	64	L7	General purpose input/output 20 (I/O/Z)(5) Enhanced QEP1 input A (I) McBSP-A transmit serial data (O) Enhanced CAN-B transmit (O)
GPIO21 EQEP1B MDRA CANRXB	65	P7	General purpose input/output 21 (I/O/Z)(5) Enhanced QEP1 input B (I) McBSP-A receive serial data (I) Enhanced CAN-B receive (I)
GPIO22 EQEP1S MCLKXA SCITXDB	66	N7	General purpose input/output 22 (I/O/Z)(5) Enhanced QEP1 strobe (I/O) McBSP-A clock transmit (I/O) SCI-B transmit (O)
GPIO23 EQEP1I MFSXA SCIRXDB	67	M7	General purpose input/output 23 (I/O/Z)(5) Enhanced QEP1 index (I/O) McBSP-A transmit frame synch (I/O) SCI-B receive (I)

(5) The pullups on GPIO12-GPIO34 are enabled upon reset.

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Table 2-2. Signal Descriptions (continued)

NAME	PIN NO.		DESCRIPTION (1)
	PGF PIN #	ZHH BALL #	
GPIO24 ECAP1 EQEP2A MDXB	68	M8	General purpose input/output 24 (I/O/Z)(5) Enhanced capture 1 (I/O) Enhanced QEP2 input A (I) McBSP-B transmit serial data (O)
GPIO25 ECAP2 EQEP2B MDRB	69	N8	General purpose input/output 25 (I/O/Z)(5) Enhanced capture 2 (I/O) Enhanced QEP2 input B (I) McBSP-B receive serial data (I)
GPIO26 ECAP3 EQEP2I MCLKXB	72	K8	General purpose input/output 26 (I/O/Z)(5) Enhanced capture 3 (I/O) Enhanced QEP2 index (I/O) McBSP-B clock transmit (O)
GPIO27 ECAP4 EQEP2S MFSXB	73	L9	General purpose input/output 27 (I/O/Z)(5) Enhanced capture 4 (I/O) Enhanced QEP2 strobe (I/O) McBSP-B transmit frame synch (I/O)
GPIO28 SCIRXDA XZCS6	141	E10	General purpose input/output 28 (I/O/Z)(5) SCI receive data (I) External memory interface zone 6 chip select (O)
GPIO29 SCITXDA XA19	2	C2	General purpose input/output 29. (I/O/Z)(5) SCI transmit data (O) External Memory Interface Address Line 19 (O)
GPIO30 CANRXA XA18	1	B2	General purpose input/output 30 (I/O/Z)(5) Enhanced CAN-A receive (I) External Memory Interface Address Line 18 (O)
GPIO31 CANTXA XA17	176	A2	General purpose input/output 31 (I/O/Z)(5) Enhanced CAN-A transmit (O) External Memory Interface Address Line 17 (O)
GPIO32 SDAA EPWMSYNCI ADCSOCAO	74	N9	General purpose input/output 32 (I/O/Z)(5) I2C data open-drain bidirectional port (I/OD) Enhanced PWM external sync pulse input (I) ADC start-of-conversion A (O)
GPIO33 SCLA EPWMSYNCO ADCSOCBO	75	P9	General-Purpose Input/Output 33 (I/O/Z)(5) I2C clock open-drain bidirectional port (I/OD) Enhanced PWM external synch pulse output (O) ADC start-of-conversion B (O)
GPIO34 ECAP1 XREADY	142	D10	General-Purpose Input/Output 34 (I/O/Z)(5) Enhanced Capture input/output 1 (I/O) External memory interface Ready signal
GPIO35 SCITXDA XR/W	148	A9	General-Purpose Input/Output 35 (I/O/Z) SCI-A transmit data (O) External memory interface read, not write strobe
GPIO36 SCIRXDA XZCS0	145	C10	General-Purpose Input/Output 36 (I/O/Z) SCI receive data (I) External memory interface zone 0 chip select (O)
GPIO37 ECAP2 XZCS7	150	D9	General-Purpose Input/Output 37 (I/O/Z) Enhanced Capture input/output 2 (I/O) External memory interface zone 7 chip select (O)
GPIO38 - XWE0	137	D11	General-Purpose Input/Output 38 (I/O/Z) - External memory interface Write Enable 0 (O)
GPIO39 - XA016	175	B3	General-Purpose Input/Output 39 (I/O/Z) - External Memory Interface Address Line 16 (O)
GPIO40 - XA0/XWE1	151	D8	General-Purpose Input/Output 40 (I/O/Z) - External Memory Interface Address Line 0/External memory interface Write Enable 1 (O)

Table 2-2. Signal Descriptions (continued)

NAME	PIN NO.		DESCRIPTION (1)
	PGF PIN #	ZHH BALL #	
GPIO41 - XA1	152	A8	General-Purpose Input/Output 41 (I/O/Z) - External Memory Interface Address Line 1 (O)
GPIO42 - XA2	153	B8	General-Purpose Input/Output 42 (I/O/Z) - External Memory Interface Address Line 2 (O)
GPIO43 - XA3	156	B7	General-Purpose Input/Output 43 (I/O/Z) - External Memory Interface Address Line 3 (O)
GPIO44 - XA4	157	A7	General-Purpose Input/Output 44 (I/O/Z) - External Memory Interface Address Line 4 (O)
GPIO45 - XA5	158	D7	General-Purpose Input/Output 45 (I/O/Z) - External Memory Interface Address Line 5 (O)
GPIO46 - XA6	161	B6	General-Purpose Input/Output 46 (I/O/Z) - External Memory Interface Address Line 6 (O)
GPIO47 - XA7	162	A6	General-Purpose Input/Output 47 (I/O/Z) - External Memory Interface Address Line 7 (O)
GPIO48 ECAP5 XD31	88	P13	General-Purpose Input/Output 48 (I/O/Z) Enhanced Capture input/output 5 (I/O) External Memory Interface Data Line 31 (O)
GPIO49 ECAP6 XD30	89	N13	General-Purpose Input/Output 49 (I/O/Z) Enhanced Capture input/output 6 (I/O) External Memory Interface Data Line 30 (O)
GPIO50 EQEP1A XD29	90	P14	General-Purpose Input/Output 50 (I/O/Z) Enhanced QEP 1input A (I) External Memory Interface Data Line 29 (O)
GPIO51 EQEP1B XD28	91	M13	General-Purpose Input/Output 51 (I/O/Z) Enhanced QEP 1input B (I) External Memory Interface Data Line 28 (O)
GPIO52 EQEP1S XD27	94	M14	General-Purpose Input/Output 52 (I/O/Z) Enhanced QEP 1Strobe (I/O) External Memory Interface Data Line 27 (O)
GPIO53 EQEP1I XD26	95	L12	General-Purpose Input/Output 53 (I/O/Z) Enhanced CAP1 Index (I/O) External Memory Interface Data Line 26 (O)
GPIO54 SPISIMOA XD25	96	L13	General-Purpose Input/Output 54 (I/O/Z) SPI-A slave in, master out (I/O) External Memory Interface Data Line 25 (O)
GPIO55 SPISOMIA XD24	97	L14	General-Purpose Input/Output 55 (I/O/Z) SPI-A slave out, master in (I/O) External Memory Interface Data Line 24 (O)
GPIO56 SPICLKA XD23	98	K11	General-Purpose Input/Output 56 (I/O/Z) SPI-A clock (I/O) External Memory Interface Data Line 23 (O)
GPIO57 SPISTEA XD22	99	K13	General-Purpose Input/Output 57 (I/O/Z) SPI-A slave transmit enable (I/O) External Memory Interface Data Line 22 (O)
GPIO58 MCLKRA XD21	100	K12	General-Purpose Input/Output 58 (I/O/Z) McBSP-A receive clock (I/O) External Memory Interface Data Line 21 (O)
GPIO59 MFSRA XD20	110	H14	General-Purpose Input/Output 59 (I/O/Z) McBSP-A receive frame synch (I/O) External Memory Interface Data Line 20 (O)

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Table 2-2. Signal Descriptions (continued)

NAME	PIN NO.		DESCRIPTION (1)
	PGF PIN #	ZHH BALL #	
GPIO60 MCLKRB XD19	111	G14	General-Purpose Input/Output 60 (I/O/Z) McBSP-B receive clock (I/O) External Memory Interface Data Line 19 (O)
GPIO61 MFSRB XD18	112	G12	General-Purpose Input/Output 61 (I/O/Z) McBSP-B receive frame synch (I/O) External Memory Interface Data Line 18 (O)
GPIO62 SCIRXDC XD17	113	G13	General-Purpose Input/Output 62 (I/O/Z) SCI-C receive data (I) External Memory Interface Data Line 17 (O)
GPIO63 SCITXDC XD16	114	G11	General-Purpose Input/Output 63 (I/O/Z) SCI-C transmit data (O) External Memory Interface Data Line 16 (O)
GPIO64 - XD15	115	G10	General-Purpose Input/Output 64 (I/O/Z) - External Memory Interface Data Line 15 (O)
GPIO65 - XD14	116	F14	General-Purpose Input/Output 65 (I/O/Z) - External Memory Interface Data Line 14 (O)
GPIO66 - XD13	119	F11	General-Purpose Input/Output 66 (I/O/Z) - External Memory Interface Data Line 13 (O)
GPIO67 - XD12	122	E13	General-Purpose Input/Output 67 (I/O/Z) - External Memory Interface Data Line 12 (O)
GPIO68 - XD11	123	E11	General-Purpose Input/Output 68 (I/O/Z) - External Memory Interface Data Line 11 (O)
GPIO69 - XD10	124	F10	General-Purpose Input/Output 69 (I/O/Z) - External Memory Interface Data Line 10 (O)
GPIO70 - XD9	127	D12	General-Purpose Input/Output 70 (I/O/Z) - External Memory Interface Data Line 9 (O)
GPIO71 - XD8	128	C14	General-Purpose Input/Output 71 (I/O/Z) - External Memory Interface Data Line 8 (O)
GPIO72 - XD7	129	B14	General-Purpose Input/Output 72 (I/O/Z) - External Memory Interface Data Line 7 (O)
GPIO73 - XD6	130	C12	General-Purpose Input/Output 73 (I/O/Z) - External Memory Interface Data Line 6 (O)
GPIO74 - XD5	131	C13	General-Purpose Input/Output 74 (I/O/Z) - External Memory Interface Data Line 5 (O)
GPIO75 - XD4	132	A14	General-Purpose Input/Output 75 (I/O/Z) - External Memory Interface Data Line 4 (O)
GPIO76 - XD3	133	B13	General-Purpose Input/Output 76 (I/O/Z) - External Memory Interface Data Line 3 (O)
GPIO77 - XD2	134	A13	General-Purpose Input/Output 77 (I/O/Z) - External Memory Interface Data Line 2 (O)
GPIO78 - XD1	135	B12	General-Purpose Input/Output 78 (I/O/Z) - External Memory Interface Data Line 1 (O)

Table 2-2. Signal Descriptions (continued)

NAME	PIN NO.		DESCRIPTION (1)
	PGF PIN #	ZHH BALL #	
GPIO79 - XD0	136	A12	General-Purpose Input/Output 79 (I/O/Z) - External Memory Interface Data Line 0 (O)
GPIO80 - XA8	163	C6	General-Purpose Input/Output 80 (I/O/Z) - External Memory Interface Address Line 8 (O)
GPIO81 - XA9	164	E6	General-Purpose Input/Output 81 (I/O/Z) - External Memory Interface Address Line 9 (O)
GPIO82 - XA10	165	C5	General-Purpose Input/Output 82 (I/O/Z) - External Memory Interface Address Line 10 (O)
GPIO83 - XA11	168	D5	General-Purpose Input/Output 83 (I/O/Z) - External Memory Interface Address Line 11 (O)
GPIO84 - XA12	169	E5	General-Purpose Input/Output 84 (I/O/Z) External Memory Interface Address Line 12 (O)
GPIO85 - XA13	172	C4	General-Purpose Input/Output 85 (I/O/Z) - External Memory Interface Address Line 13 (O)
GPIO86 - XA14	173	D4	General-Purpose Input/Output 86 (I/O/Z) - External Memory Interface Address Line 14 (O)
GPIO87 - XA15	174	A3	General-Purpose Input/Output 87 (I/O/Z) - External Memory Interface Address Line 15 (O)
$\overline{\text{XRD}}$	149	B9	External memory interface Read Enable

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3 Functional Overview

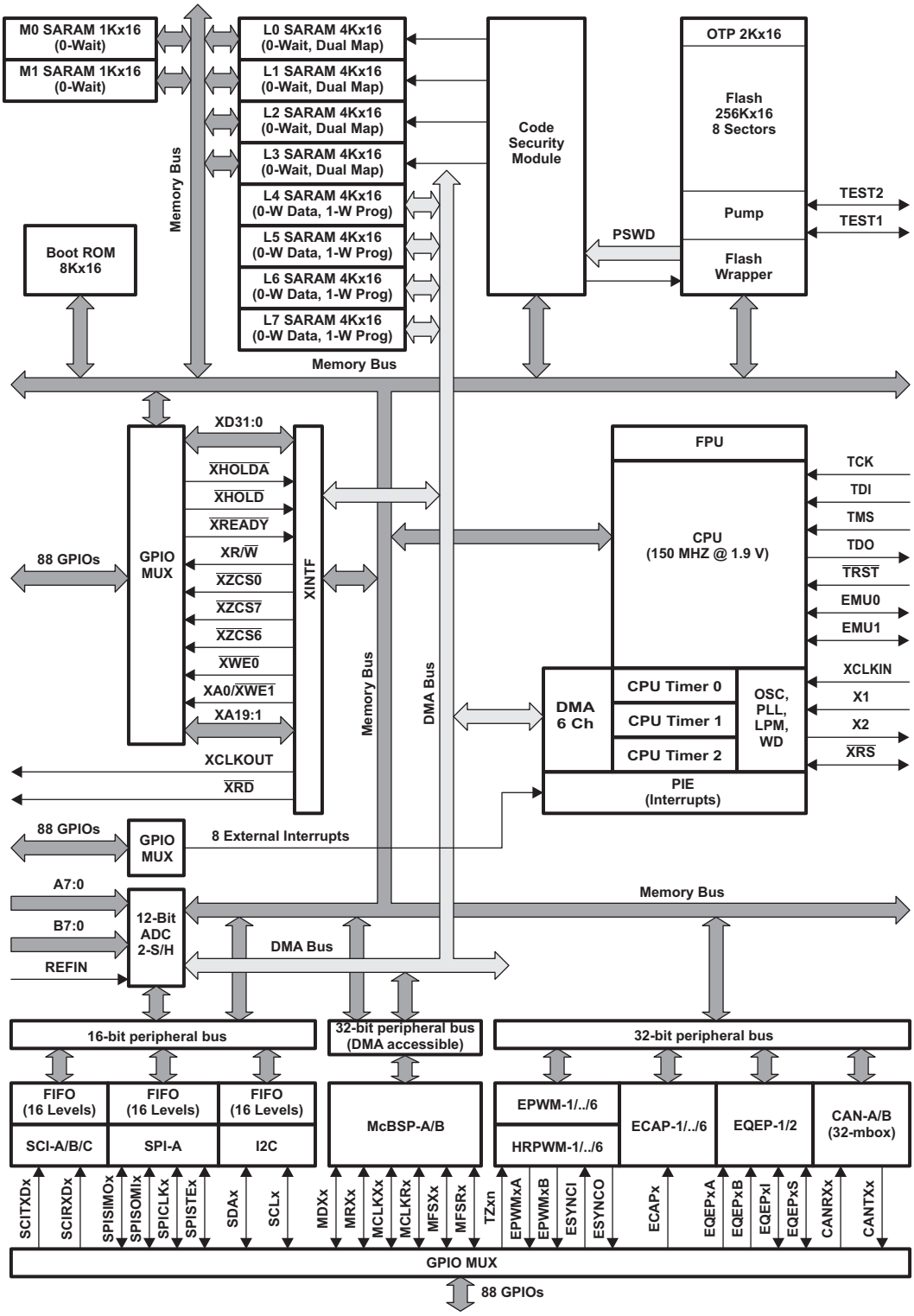

Figure 3-1. Functional Block Diagram

3.1 Memory Maps

In Figure 3-2 through Figure 3-4, the following apply:

- Memory blocks are not to scale.
- Peripheral Frame 0, Peripheral Frame 1, Peripheral Frame 2, and Peripheral Frame 3 memory maps are restricted to data memory only. A user program cannot access these memory maps in program space.
- *Protected* means the order of Write followed by Read operations is preserved rather than the pipeline order.
- Certain memory ranges are EALLOW protected against spurious writes after configuration.

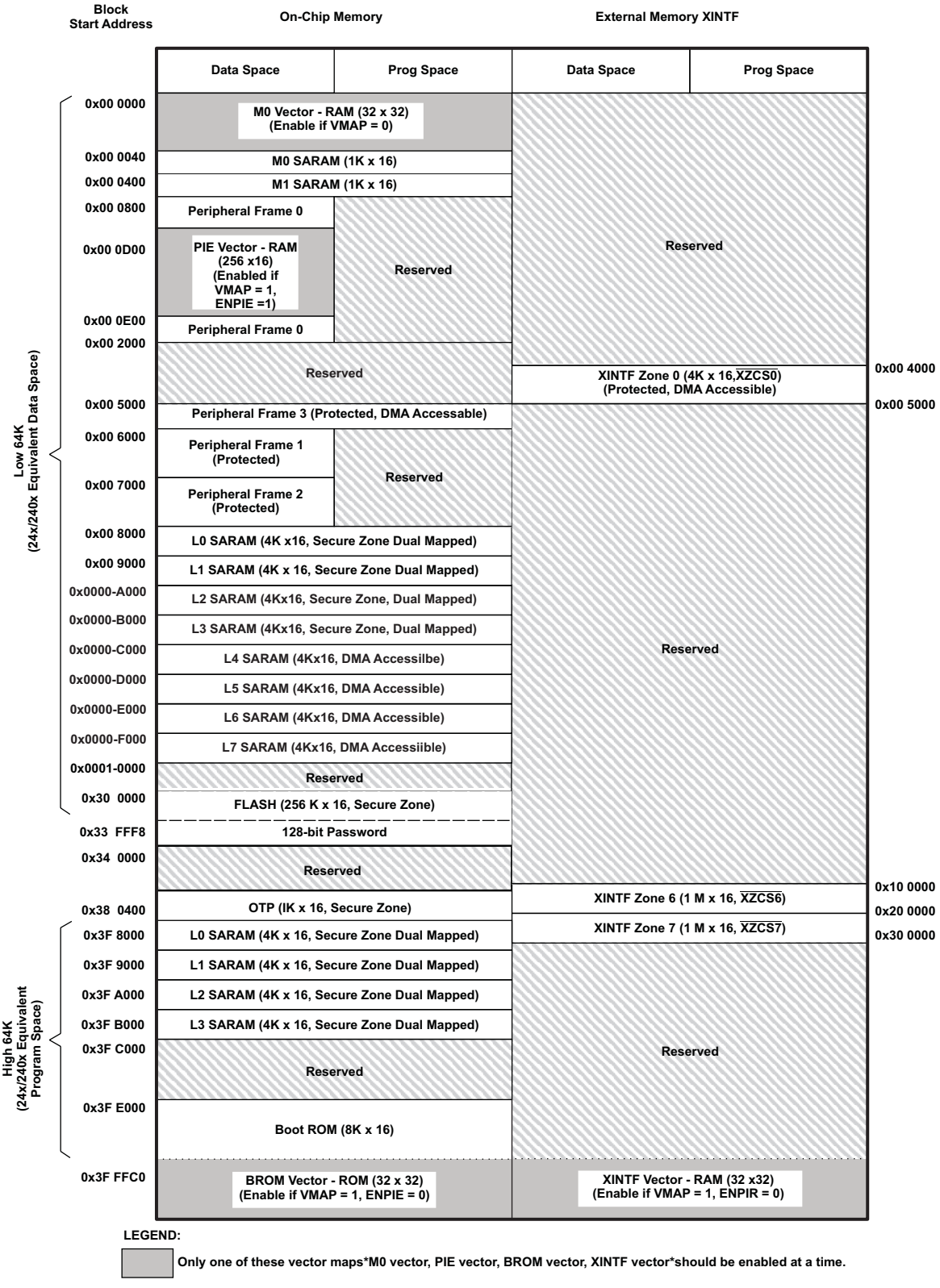

Figure 3-2. F28335 Memory Map

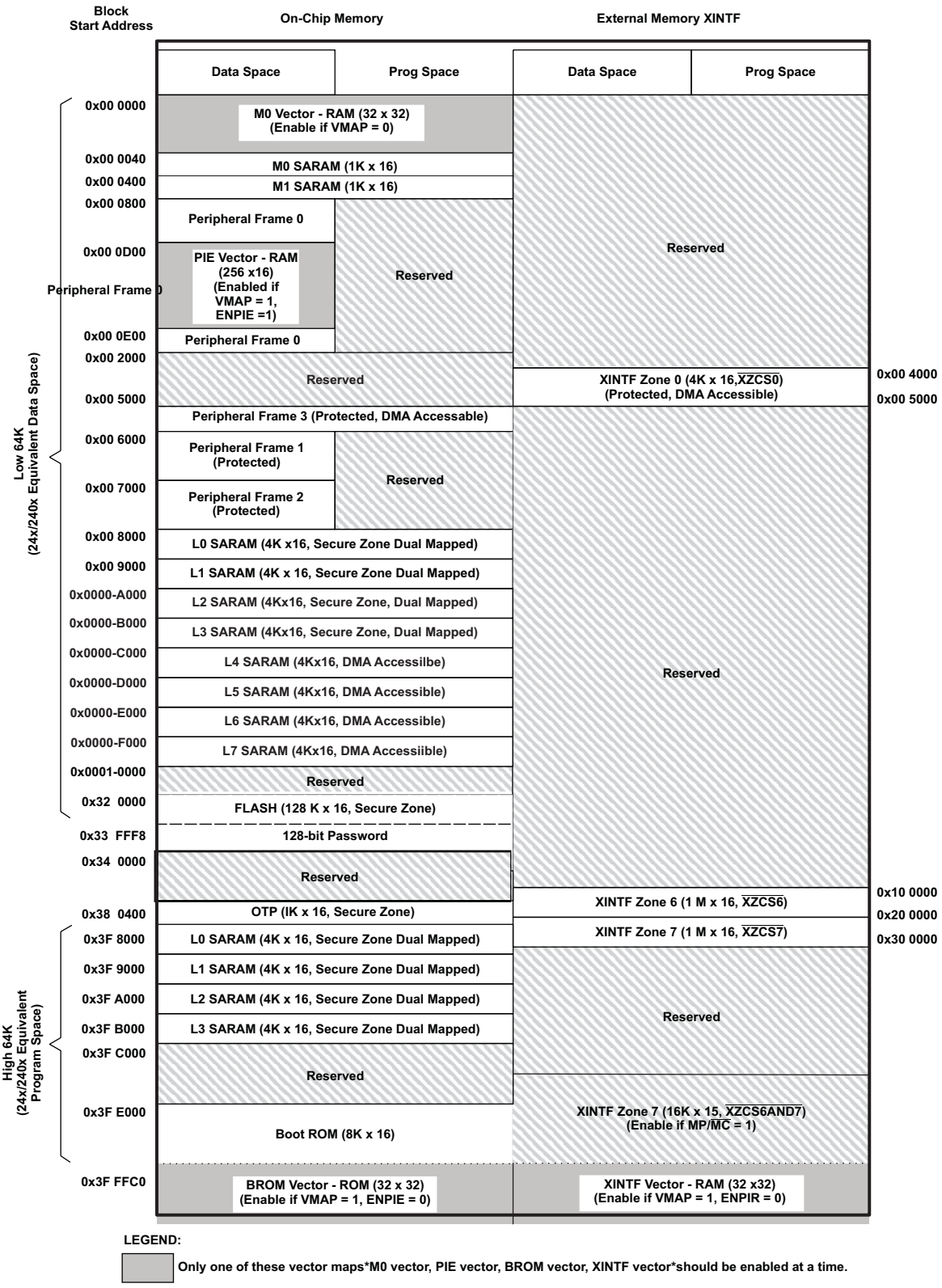

Figure 3-3. F28334 Memory Map

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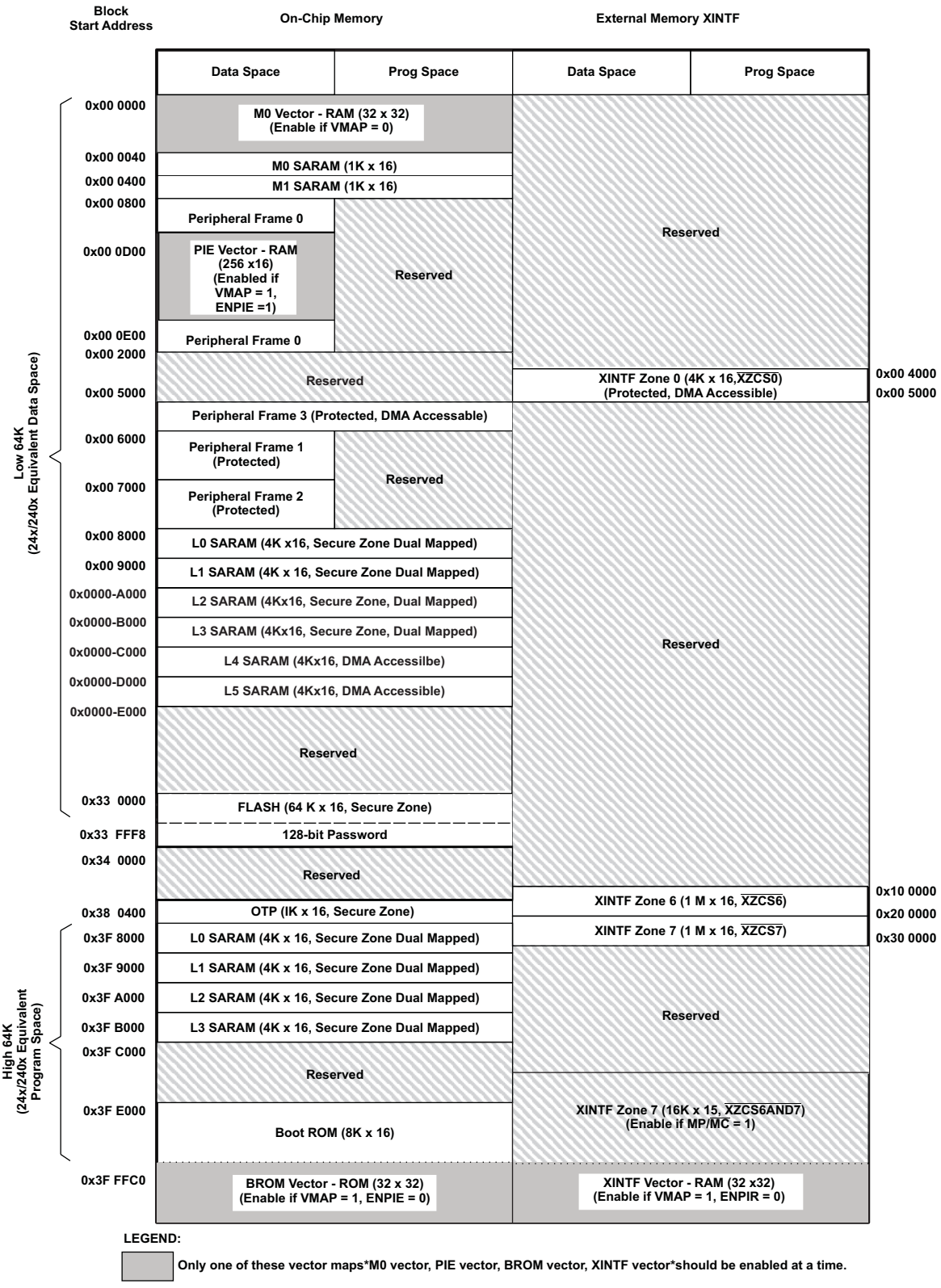

Figure 3-4. F28332 Memory Map

Table 3-1. Addresses of Flash Sectors in F28335

ADDRESS RANGE	PROGRAM AND DATA SPACE
0x30 0000 - 0x30 7FFF	Sector H (32K x 16)
0x30 8000 - 0x30 FFFF	Sector G (32K x 16)
0x31 0000 - 0x31 7FFF	Sector F (32K x 16)
0x31 8000 - 0x31 FFFF	Sector E (32K x 16)
0x32 0000 - 0x32 7FFF	Sector D (32K x 16)
0x32 8000 - 0x32 FFFF	Sector C (32K x 16)
0x33 0000 - 0x33 7FFF	Sector B (32K x 16)
0x33 8000 - 0x33 FFFF	Sector A (32K x 16)
0x33 FF80 - 0x33 FFF5	Program to 0x0000 when using the Code Security Module
0x33 FFF6 - 0x33 FFF7	Boot-to-Flash Entry Point (program branch instruction here)
0x33 FFF8 - 0x33 FFFF	Security Password (128-Bit) (Do Not Program to all zeros)

Table 3-2. Addresses of Flash Sectors in F28334

ADDRESS RANGE	PROGRAM AND DATA SPACE
0x32 0000 - 0x32 3FFF	Sector H (16K x 16)
0x32 4000 - 0x32 7FFF	Sector G (16K x 16)
0x32 8000 - 0x32 BFFF	Sector F (16K x 16)
0x32 C000 - 0x32 FFFF	Sector E (16K x 16)
0x33 0000 - 0x33 3FFF	Sector D (16K x 16)
0x33 4000 - 0x33 7FFFF	Sector C (16K x 16)
0x33 8000 - 0x33 BFFF	Sector B (16K x 16)
0x33 C000 - 0x33 FFFF	Sector A (16K x 16)
0x33 FF80 - 0x33 FFF5	Program to 0x0000 when using the Code Security Module
0x33 FFF6 - 0x33 FFF7	Boot-to-Flash Entry Point (program branch instruction here)
0x33 FFF8 - 0x33 FFFF	Security Password (128-Bit) (Do Not Program to all zeros)

Table 3-3. Addresses of Flash Sectors in F28332

ADDRESS RANGE	PROGRAM AND DATA SPACE
0x33 0000 - 0x33 3FFF	Sector D (16K x 16)
0x33 4000 - 0x33 7FFFF	Sector C (16K x 16)
0x33 8000 - 0x33 BFFF	Sector B (16K x 16)
0x33 C000 - 0x33 FFFF	Sector A (16K x 16)
0x33 FF80 - 0x33 FFF5	Program to 0x0000 when using the Code Security Module
0x33 FFF6 - 0x33 FFF7	Boot-to-Flash Entry Point (program branch instruction here)
0x33 FFF8 - 0x33 FFFF	Security Password (128-Bit) (Do Not Program to all zeros)

NOTE

- When the code-security passwords are programmed, all addresses between 0x33FF80 and 0x33FFF5 cannot be used as program code or data. These locations must be programmed to 0x0000.
- If the code security feature is not used, addresses 0x33FF80 through 0x33FFEF may be used for code or data. Addresses 0x33FFF0 – 0x33FFF5 are reserved for data and should not contain program code. .

Table 3-4 shows how to handle these memory locations.

Table 3-4. Handling Security Code Locations

ADDRESS	FLASH	
	Code security enabled	Code security disabled
0x33FF80 - 0x33FFEF	Fill with 0x0000	Application code and data
0x33FFF0 - 0x33FFF5		Reserved for data only

Peripheral Frame 1, Peripheral Frame 2, and Peripheral Frame 3 are grouped together to enable these blocks to be write/read peripheral block protected. The protected mode ensures that all accesses to these blocks happen as written. Because of the C28x pipeline, a write immediately followed by a read, to different memory locations, will appear in reverse order on the memory bus of the CPU. This can cause problems in certain peripheral applications where the user expected the write to occur first (as written). The C28x CPU supports a block protection mode where a region of memory can be protected so as to make sure that operations occur as written (the penalty is extra cycles are added to align the operations). This mode is programmable and by default, it will protect the selected zones.

The wait-states for the various spaces in the memory map area are listed in Table 3-5.

Table 3-5. Wait-states

Area	Wait-States CPU	Comments
M0 and M1 SARAMs	0-wait	Fixed
Peripheral Frame 0	1-wait (reads) 0-wait (writes)	This applies to all PF0 peripherals except the floating-point unit (FPU) (0-wait reads)
Peripheral Frame 3	0-wait (writes) 2-wait (reads)	Assumes no conflicts between CPU and DMA.
Peripheral Frame 1	0-wait (writes) 2-wait (reads)	Cycles can be extended by peripheral generated ready. Consecutive writes to the CAN will experience a 1-cycle pipeline hit.
Peripheral Frame 2	0-wait (writes) 2-wait (reads)	Fixed. Cycles cannot be extended by the peripheral.
L0 SARAM	0-wait data and prog	Assumes no CPU conflicts
L1 SARAM		
L2 SARAM		
L3 SARAM		
L4 SARAM	0-wait data (read) 0-wait data (write) 1-wait prog (read) 1-wait prog (write)	Assumes no conflicts between CPU and DMA.
L5 SARAM		
L6 SARAM		
L7 SARAM		
XINTF	Programmable	Programmed via the XTIMING registers or extendable via external XREADY signal.
	1-wait minimum	1-wait is minimum wait states allowed on external waveforms for both reads and writes on XINTF.
	0-wait minimum writes with write buffer enabled	0-wait minimum for writes assumes write buffer enabled and not full. Assumes no conflicts between CPU and DMA. When DMA and CPU attempt simultaneous conflict, 1-cycle delay is added for arbitration.
OTP	Programmable	Programmed via the Flash registers.
	1-wait minimum	1-wait is minimum number of wait states allowed. 1-wait-state operation is possible at a reduced CPU frequency.
FLASH	Programmable	Programmed via the Flash registers.
	1-wait Paged min 1-wait Random min Random > Paged	0-wait minimum for paged access is not allowed
FLASH Password	Programmable, 16-wait fixed	Wait states of password locations are fixed.
Boot-ROM	1-wait	0-wait speed is not possible.

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3.2 Brief Descriptions

3.2.1 C28x CPU

The C28x™ DSC generation is the newest member of the TMS320C2000™ DSC platform. The C28x is a very efficient C/C++ engine, hence enabling users to develop not only their system control software in a high-level language, but also enables math algorithms to be developed using C/C++. The C28x is as efficient in DSC math tasks as it is in system control tasks that typically are handled by microcontroller devices. This efficiency removes the need for a second processor in many systems. The 32 x 32-bit MAC capabilities of the C28x and its 64-bit processing capabilities, enable the C28x to efficiently handle higher numerical resolution problems. Add to this the fast interrupt response with automatic context save of critical registers, resulting in a device that is capable of servicing many asynchronous events with minimal latency. The C28x has an 8-level-deep protected pipeline with pipelined memory accesses. This pipelining enables the C28x to execute at high speeds without resorting to expensive high-speed memories. Special branch-look-ahead hardware minimizes the latency for conditional discontinuities. Special store conditional operations further improve performance.

3.2.2 Memory Bus (Harvard Bus Architecture)

As with many DSC type devices, multiple busses are used to move data between the memories and peripherals and the CPU. The C28x memory bus architecture contains a program read bus, data read bus and data write bus. The program read bus consists of 22 address lines and 32 data lines. The data read and write busses consist of 32 address lines and 32 data lines each. The 32-bit-wide data busses enable single cycle 32-bit operations. The multiple bus architecture, commonly termed Harvard Bus, enables the C28x to fetch an instruction, read a data value and write a data value in a single cycle. All peripherals and memories attached to the memory bus will prioritize memory accesses. Generally, the priority of memory bus accesses can be summarized as follows:

Highest:	Data Writes	(Simultaneous data and program writes cannot occur on the memory bus.)
	Program Writes	(Simultaneous data and program writes cannot occur on the memory bus.)
	Data Reads	
	Program Reads	(Simultaneous program reads and fetches cannot occur on the memory bus.)
Lowest:	Fetches	(Simultaneous program reads and fetches cannot occur on the memory bus.)

3.2.3 Peripheral Bus

To enable migration of peripherals between various Texas Instruments (TI) DSC family of devices, the 2833x devices adopt a peripheral bus standard for peripheral interconnect. The peripheral bus bridge multiplexes the various busses that make up the processor Memory Bus into a single bus consisting of 16 address lines and 16 or 32 data lines and associated control signals. Three versions of the peripheral bus are supported on the 2833x. One version supports only 16-bit accesses (called peripheral frame 2). Another version supports both 16- and 32-bit accesses (called peripheral frame 1). The third version supports DMA access and both 16- and 32-bit accesses (called peripheral frame 3).

3.2.4 Real-Time JTAG and Analysis

The 2833x implements the standard IEEE 1149.1 JTAG interface. Additionally, the 2833x supports real-time mode of operation whereby the contents of memory, peripheral and register locations can be modified while the processor is running and executing code and servicing interrupts. The user can also single step through non-time critical code while enabling time-critical interrupts to be serviced without interference. The 2833x implements the real-time mode in hardware within the CPU. This is a unique feature to the 2833x, no software monitor is required. Additionally, special analysis hardware is provided which allows the user to set hardware breakpoint or data/address watch-points and generate various user-selectable break events when a match occurs.

3.2.5 External Interface (XINTF)

This asynchronous interface consists of 19 address lines, 32 data lines, and three chip-select lines. The chip-select lines are mapped to three external zones, Zones 0, 6, and 7. Each of the three zones can be programmed with a different number of wait states, strobe signal setup and hold timing and each zone can be programmed for extending wait states externally or not. The programmable wait-state, chip-select and programmable strobe timing enables glueless interface to external memories and peripherals.

3.2.6 Flash

The F28335 contains 256K × 16 of embedded flash memory, segregated into eight 32K × 16 sectors. The F28334 contains 128K × 16 of embedded flash memory, segregated into eight 16K × 16 sectors. The F28332 device contains 64K ×16 of embedded flash, segregated into four 16K × 16 sectors. All the devices also contain a single 1K × 16 of OTP memory at address range 0x380400 – 0x3807FF. The user can individually erase, program, and validate a flash sector while leaving other sectors untouched. However, it is not possible to use one sector of the flash or the OTP to execute flash algorithms that erase/program other sectors. Special memory pipelining is provided to enable the flash module to achieve higher performance. The flash/OTP is mapped to both program and data space; therefore, it can be used to execute code or store data information. Note that addresses 0x33FFF0 – 0x33FFF5 are reserved for data variables and should not contain program code.

NOTE

The F28335/F28334/F28332 Flash and OTP wait-states can be configured by the application. This allows applications running at slower frequencies to configure the flash to use fewer wait-states.

Flash effective performance can be improved by enabling the flash pipeline mode in the Flash options register. With this mode enabled, effective performance of linear code execution will be much faster than the raw performance indicated by the wait-state configuration alone. The exact performance gain when using the Flash pipeline mode is application-dependent.

For more information on the Flash options, Flash wait-state, and OTP wait-state registers, see the *TMS320x280x, 2801x, 2804x System Control and Interrupts Reference Guide* (literature number SPRU712).

3.2.7 M0, M1 SARAMs

All 2833x devices contain these two blocks of single access memory, each 1K × 16 in size. The stack pointer points to the beginning of block M1 on reset. The M0 and M1 blocks, like all other memory blocks on C28x devices, are mapped to both program and data space. Hence, the user can use M0 and M1 to execute code or for data variables. The partitioning is performed within the linker. The C28x device presents a unified memory map to the programmer. This makes for easier programming in high-level languages.

3.2.8 L0, L1, L2, L3, L4, L5, L6, L7 SARAMs

The F28335 and F28334 each contain an additional 32K × 16 of single-access RAM, divided into 8 blocks (L0-L7 with 4K each). The F28332 contains an additional 24K × 16 of single-access RAM, divided into 6 blocks (L0-L5 with 4K each). Each block can be independently accessed to minimize CPU pipeline stalls. Each block is mapped to both program and data space. L4, L5, L6, and L7 are DMA accessible

3.2.9 Boot ROM

The Boot ROM is factory-programmed with boot-loading software. Boot-mode signals are provided to tell the bootloader software what boot mode to use on power up. The user can select to boot normally or to download new software from an external connection or to select boot software that is programmed in the internal Flash/ROM. The Boot ROM also contains standard tables, such as SIN/COS waveforms, for use in math related algorithms.

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Table 3-6. Boot Mode Selection

GPIO87/XA15	GPIO86/XA14	GPIO85/XA13	GPIO84/XA12	MODE(1)
1	1	1	1	Jump to Flash
1	1	1	0	SCI-A boot
1	1	0	1	SPI-A boot
1	1	0	0	I2C-A boot
1	0	1	1	eCAN-A boot
1	0	1	0	McBSP-A boot
1	0	0	1	Jump to XINTF x16
1	0	0	0	Jump to XINTF x32
0	1	1	1	Jump to OTP
0	1	1	0	Parallel GPIO I/O boot
0	1	0	1	Parallel XINTF boot
0	1	0	0	Jump to SARAM
0	0	1	1	Branch to check boot mode
0	0	1	0	Branch to Flash, skip ADC CAL
0	0	0	1	Branch to SARAM, skip ADC CAL
0	0	0	0	Branch to SCI, skip ADC CAL

(1) All four GPIO pins have an internal pullup.

3.2.10 Security

The 2833x devices support high levels of security to protect the user firmware from being reverse engineered. The security features a 128-bit password (hardcoded for 16 wait-states), which the user programs into the flash. One code security module (CSM) is used to protect the flash/OTP and the L0/L1/L2/L3 SARAM blocks. The security feature prevents unauthorized users from examining the memory contents via the JTAG port, executing code from external memory or trying to boot-load some undesirable software that would export the secure memory contents. To enable access to the secure blocks, the user must write the correct 128-bit KEY value, which matches the value stored in the password locations within the Flash.

NOTE

- When the code-security passwords are programmed, all addresses between 0x33FF80 and 0x33FFF5 cannot be used as program code or data. These locations must be programmed to 0x0000.
- If the code security feature is not used, addresses 0x33FF80 through 0x33FFEF may be used for code or data. Addresses 0x33FFF0 – 0x33FFF5 are reserved for data and should not contain program code. .

The 128-bit password (at 0x33 FFF8 – 0x33 FFFF) must not be programmed to zeros. Doing so would permanently lock the device.

NOTE

Code Security Module Disclaimer

THE CODE SECURITY MODULE (CSM) INCLUDED ON THIS DEVICE WAS DESIGNED TO PASSWORD PROTECT THE DATA STORED IN THE ASSOCIATED MEMORY (EITHER ROM OR FLASH) AND IS WARRANTED BY TEXAS INSTRUMENTS (TI), IN ACCORDANCE WITH ITS STANDARD TERMS AND CONDITIONS, TO CONFORM TO TI'S PUBLISHED SPECIFICATIONS FOR THE WARRANTY PERIOD APPLICABLE FOR THIS DEVICE.

TI DOES NOT, HOWEVER, WARRANT OR REPRESENT THAT THE CSM CANNOT BE COMPROMISED OR BREACHED OR THAT THE DATA STORED IN THE ASSOCIATED MEMORY CANNOT BE ACCESSED THROUGH OTHER MEANS. MOREOVER, EXCEPT AS SET FORTH ABOVE, TI MAKES NO WARRANTIES OR REPRESENTATIONS CONCERNING THE CSM OR OPERATION OF THIS DEVICE, INCLUDING ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

IN NO EVENT SHALL TI BE LIABLE FOR ANY CONSEQUENTIAL, SPECIAL, INDIRECT, INCIDENTAL, OR PUNITIVE DAMAGES, HOWEVER CAUSED, ARISING IN ANY WAY OUT OF YOUR USE OF THE CSM OR THIS DEVICE, WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO LOSS OF DATA, LOSS OF GOODWILL, LOSS OF USE OR INTERRUPTION OF BUSINESS OR OTHER ECONOMIC LOSS.

3.2.11 Peripheral Interrupt Expansion (PIE) Block

The PIE block serves to multiplex numerous interrupt sources into a smaller set of interrupt inputs. The PIE block can support up to 96 peripheral interrupts. On the 2833x, 58 of the possible 96 interrupts are used by peripherals. The 96 interrupts are grouped into blocks of 8 and each group is fed into 1 of 12

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CPU interrupt lines (INT1 to INT12). Each of the 96 interrupts is supported by its own vector stored in a dedicated RAM block that can be overwritten by the user. The vector is automatically fetched by the CPU on servicing the interrupt. It takes 8 CPU clock cycles to fetch the vector and save critical CPU registers. Hence the CPU can quickly respond to interrupt events. Prioritization of interrupts is controlled in hardware and software. Each individual interrupt can be enabled/disabled within the PIE block.

3.2.12 External Interrupts (XINT1-XINT7, XNMI)

The 2833x supports eight masked external interrupts (XINT1-XINT7, XNMI). XNMI can be connected to the INT13 or NMI interrupt of the CPU. Each of the interrupts can be selected for negative, positive, or both negative and positive edge triggering and can also be enabled/disabled (including the XNMI). The masked interrupts also contain a 16-bit free running up counter, which is reset to zero when a valid interrupt edge is detected. This counter can be used to accurately time stamp the interrupt. Unlike the 281x devices, there are no dedicated pins for the external interrupts. Rather, any Port A GPIO pin can be configured to trigger any external interrupt.

3.2.13 Oscillator and PLL

The 2833x can be clocked by an external oscillator or by a crystal attached to the on-chip oscillator circuit. A PLL is provided supporting up to 10 input-clock-scaling ratios. The PLL ratios can be changed on-the-fly in software, enabling the user to scale back on operating frequency if lower power operation is desired. Refer to the Electrical Specification section for timing details. The PLL block can be set in bypass mode.

3.2.14 Watchdog

The 2833x devices contain a watchdog timer. The user software must regularly reset the watchdog counter within a certain time frame; otherwise, the watchdog will generate a reset to the processor. The watchdog can be disabled if necessary.

3.2.15 Peripheral Clocking

The clocks to each individual peripheral can be enabled/disabled so as to reduce power consumption when a peripheral is not in use. Additionally, the system clock to the serial ports (except I2C and eCAN) and the ADC blocks can be scaled relative to the CPU clock. This enables the timing of peripherals to be decoupled from increasing CPU clock speeds.

3.2.16 Low-Power Modes

The 2833x devices are full static CMOS devices. Three low-power modes are provided:

IDLE:	Place CPU into low-power mode. Peripheral clocks may be turned off selectively and only those peripherals that need to function during IDLE are left operating. An enabled interrupt from an active peripheral or the watchdog timer will wake the processor from IDLE mode.
STANDBY:	Turns off clock to CPU and peripherals. This mode leaves the oscillator and PLL functional. An external interrupt event will wake the processor and the peripherals. Execution begins on the next valid cycle after detection of the interrupt event
HALT:	Turns off the internal oscillator. This mode basically shuts down the device and places it in the lowest possible power consumption mode. A reset or external signal can wake the device from this mode.

3.2.17 Peripheral Frames 0, 1, 2, 3 (PFn)

The 2833x device segregates peripherals into three sections. The mapping of peripherals is as follows:

PF0:	PIE:	PIE Interrupt Enable and Control Registers Plus PIE Vector Table
	Flash:	Flash Control, Programming, Erase, Verify Registers
	XINTF:	External Interface Registers
	DMA	DMA Registers
	FPU:	Floating-Point Unit Registers
	Timers:	CPU-Timers 0, 1, 2 Registers
	CSM:	Code Security Module KEY Registers
	ADC:	ADC Result Registers (dual-mapped)
PF1:	eCAN:	eCAN Mailbox and Control Registers
	GPIO:	GPIO MUX Configuration and Control Registers
	ePWM:	Enhanced Pulse Width Modulator Module and Registers
	eCAP:	Enhanced Capture Module and Registers
	eQEP:	Enhanced Quadrature Encoder Pulse Module and Registers
PF2:	SYS:	System Control Registers
	SCI:	Serial Communications Interface (SCI) Control and RX/TX Registers
	SPI:	Serial Port Interface (SPI) Control and RX/TX Registers
	ADC:	ADC Status, Control, and Result Register
	I2C:	Inter-Integrated Circuit Module and Registers
	XINTF	External Interface Registers
PF3:	McBSP	Multichannel Buffered Serial Port Registers

3.2.18 General-Purpose Input/Output (GPIO) Multiplexer

Most of the peripheral signals are multiplexed with general-purpose input/output (GPIO) signals. This enables the user to use a pin as GPIO if the peripheral signal or function is not used. On reset, GPIO pins are configured as inputs. The user can individually program each pin for GPIO mode or peripheral signal mode. For specific inputs, the user can also select the number of input qualification cycles. This is to filter unwanted noise glitches. The GPIO signals can also be used to bring the device out of specific low-power modes.

3.2.19 32-Bit CPU-Timers (0, 1, 2)

CPU-Timers 0, 1, and 2 are identical 32-bit timers with presettable periods and with 16-bit clock prescaling. The timers have a 32-bit count down register, which generates an interrupt when the counter reaches zero. The counter is decremented at the CPU clock speed divided by the prescale value setting. When the counter reaches zero, it is automatically reloaded with a 32-bit period value. CPU-Timer 2 is reserved for Real-Time OS (RTOS)/BIOS applications. CPU-Timer 1 is also reserved for TI system functions. CPU-Timer 2 is connected to INT14 of the CPU. CPU-Timer 1 can be connected to INT13 of the CPU. CPU-Timer 0 is for general use and is connected to the PIE block.

3.2.20 Control Peripherals

The 2833x devices support the following peripherals which are used for embedded control and communication:

- ePWM: The enhanced PWM peripheral supports independent/complementary PWM generation, adjustable dead-band generation for leading/trailing edges, latched/cycle-by-cycle trip mechanism. Some of the PWM pins support HRPWM features.
- eCAP: The enhanced capture peripheral uses a 32-bit time base and registers up to four programmable events in continuous/one-shot capture modes.
  This peripheral can also be configured to generate an auxiliary PWM signal.
- eQEP: The enhanced QEP peripheral uses a 32-bit position counter, supports low-speed measurement using capture unit and high-speed measurement using a 32-bit unit timer. This peripheral has a watchdog timer to detect motor stall and input error detection logic to identify simultaneous edge transition in QEP signals.
- ADC: The ADC block is a 12-bit converter, single ended, 16-channels. It contains two sample-and-hold units for simultaneous sampling.

3.2.21 Serial Port Peripherals

The 2833x devices support the following serial communication peripherals:

- eCAN: This is the enhanced version of the CAN peripheral. It supports 32 mailboxes, time stamping of messages, and is CAN 2.0B-compliant.
- McBSP: The multichannel buffered serial port (McBSP) connects to E1/T1 lines, phone-quality codecs for modem applications or high-quality stereo audio DAC devices. The McBSP receive and transmit registers are supported by the DMA to significantly reduce the overhead for servicing this peripheral.
- SPI: The SPI is a high-speed, synchronous serial I/O port that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmable bit-transfer rate. Normally, the SPI is used for communications between the DSC and external peripherals or another processor. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and ADCs. Multi-device communications are supported by the master/slave operation of the SPI. On the 2833x, the SPI contains a 16-level receive and transmit FIFO for reducing interrupt servicing overhead.
- SCI: The serial communications interface is a two-wire asynchronous serial port, commonly known as UART. On the 2833x, the SCI contains a 16-level receive and transmit FIFO for reducing interrupt servicing overhead.
- I2C: The inter-integrated circuit (I2C) module provides an interface between a DSC and other devices compliant with Philips Semiconductors Inter-IC bus (I2C-bus) specification version 2.1 and connected by way of an I2C-bus. External components attached to this 2-wire serial bus can transmit/receive up to 8-bit data to/from the DSC through the I2C module. On the 2833x, the I2C contains a 16-level receive and transmit FIFO for reducing interrupt servicing overhead.

3.3 Register Map

The 2833x devices contain four peripheral register spaces. The spaces are categorized as follows:

- **Peripheral Frame 0:** These are peripherals that are mapped directly to the CPU memory bus. See Table 3-7
- **Peripheral Frame 1** These are peripherals that are mapped to the 32-bit peripheral bus. See Table 3-8
- **Peripheral Frame 2:** These are peripherals that are mapped to the 16-bit peripheral bus. See Table 3-9
- **Peripheral Frame 3:** These are peripherals that are mapped to the 32-bit DMA-accessible peripheral bus. See Table 3-10

Table 3-7. Peripheral Frame 0 Registers(1)

NAME	ADDRESS RANGE	SIZE (×16)	ACCESS TYPE(2)
Device Emulation Registers	0x00 0880 - 0x00 09FF	384	EALLOW protected
FLASH Registers(3)	0x00 0A80 - 0x00 0ADF	96	EALLOW protected
Code Security Module Registers	0x00 0AE0 - 0x00 0AEF	16	EALLOW protected
ADC registers (dual-mapped) (0 wait, read only)	0x00 0B00 - 0x00 0B1F	32	Not EALLOW protected
XINTF Registers	0x00 0B20 - 0x00 0B3F	32	Not EALLOW protected
CPU–TIMER0/1/2 Registers	0x00 0C00 - 0x00 0C3F	64	Not EALLOW protected
PIE Registers	0x00 0CE0 - 0x00 0CFF	32	Not EALLOW protected
PIE Vector Table	0x00 0D00 - 0x00 0DFF	256	EALLOW protected
DMA Registers	0x00 1000 - 0x00 11FF	512	EALLOW protected

(1) Registers in Frame 0 support 16-bit and 32-bit accesses.
(2) If registers are EALLOW protected, then writes cannot be performed until the EALLOW instruction is executed. The EDIS instruction disables writes to prevent stray code or pointers from corrupting register contents.
(3) The Flash Registers are also protected by the Code Security Module (CSM).

Table 3-8. Peripheral Frame 1 Registers

NAME	ADDRESS RANGE	SIZE (×16)
ECAN-A Registers	0x0000 6000 - 0x0000 61FF	512
ECAN-B Registers	0x0000 6200 - 0x0000 63FF	512
EPWM1 + HRPWM1 Registers	0x0000 6800 - 0x0000 683F	64
EPWM2 + HRPWM2 Registers	0x0000 6840 - 0x0000 687F	64
EPWM3 + HRPWM3 Registers	0x0000 6880 - 0x0000 68BF	64
EPWM4 + HRPWM4 Registers	0x0000 68C0 - 0x0000 68FF	64
EPWM5 + HRPWM5 Registers	0x0000 6900 - 0x0000 693F	64
EPWM6 + HRPWM6 Registers	0x0000 6940 - 0x0000 697F	64
ECAP1 Registers	0x0000 6A00 - 0x0000 6A1F	32
ECAP2 Registers	0x0000 6A20 - 0x0000 6A3F	32
ECAP3 Registers	0x0000 6A40 - 0x0000 6A5F	32
ECAP4 Registers	0x0000 6A60 - 0x0000 6A7F	32
ECAP5 Registers	0x0000 6A80 - 0x0000 6A9F	32
ECAP6 Registers	0x0000 6AA0 - 0x0000 6ABF	32
EQEP1 Registers	0x0000 6B00 - 0x0000 6B3F	64
EQEP2 Registers	0x0000 6B40 - 0x0000 6B7F	64
GPIO Registers	0x0000 6F80 - 0x0000 6FFF	128

Table 3-9. Peripheral Frame 2 Registers

NAME	ADDRESS RANGE	SIZE (×16)
System Control Registers	0x0000 7010 - 0x0000 702F	32
SPI-A Registers	0x0000 7040 - 0x0000 704F	16
SCI-A Registers	0x0000 7050 - 0x0000 705F	16
External Interrupt Registers	0x0000 7070 - 0x0000 707F	16
ADC Registers	0x0000 7100 - 0x0000 711F	32
SCI-B Registers	0x0000 7750 - 0x0000 775F	16
SCI-C Registers	0x0000 7770 - 0x0000 777F	16
I2C-A Registers	0x0000 7900 - 0x0000 793F	64

Table 3-10. Peripheral Frame 3 Registers

NAME	ADDRESS RANGE	SIZE (×16)
McBSP-A Registers	0x0000 5000 - 0x0000 503F	64
McBSP-B Registers	0x0000 5040 - 0x0000 507F	64

3.4 Device Emulation Registers

These registers are used to control the protection mode of the C28x CPU and to monitor some critical device signals. The registers are defined in Table 3-11.

Table 3-11. Device Emulation Registers

NAME	ADDRESS RANGE	SIZE (x16)	DESCRIPTION
DEVICECNF	0x0880 0x0881	2	Device Configuration Register
PARTID	0x0882	1	Part ID Register 0x00F8(1) - F28332 0x00F9 - F28334 0x00FA - F28335
REVID	0x0883	1	Revision ID Register 0x0000 - Silicon Rev. 0 - TMX
PROTSTART	0x0884	1	Block Protection Start Address Register
PROTRANGE	0x0885	1	Block Protection Range Address Register

(1) The first byte (00) denotes flash devices. FF denotes ROM devices. Other values are reserved for future devices.

3.5 Interrupts

Figure 3-5 shows how the various interrupt sources are multiplexed within the 2833x devices.

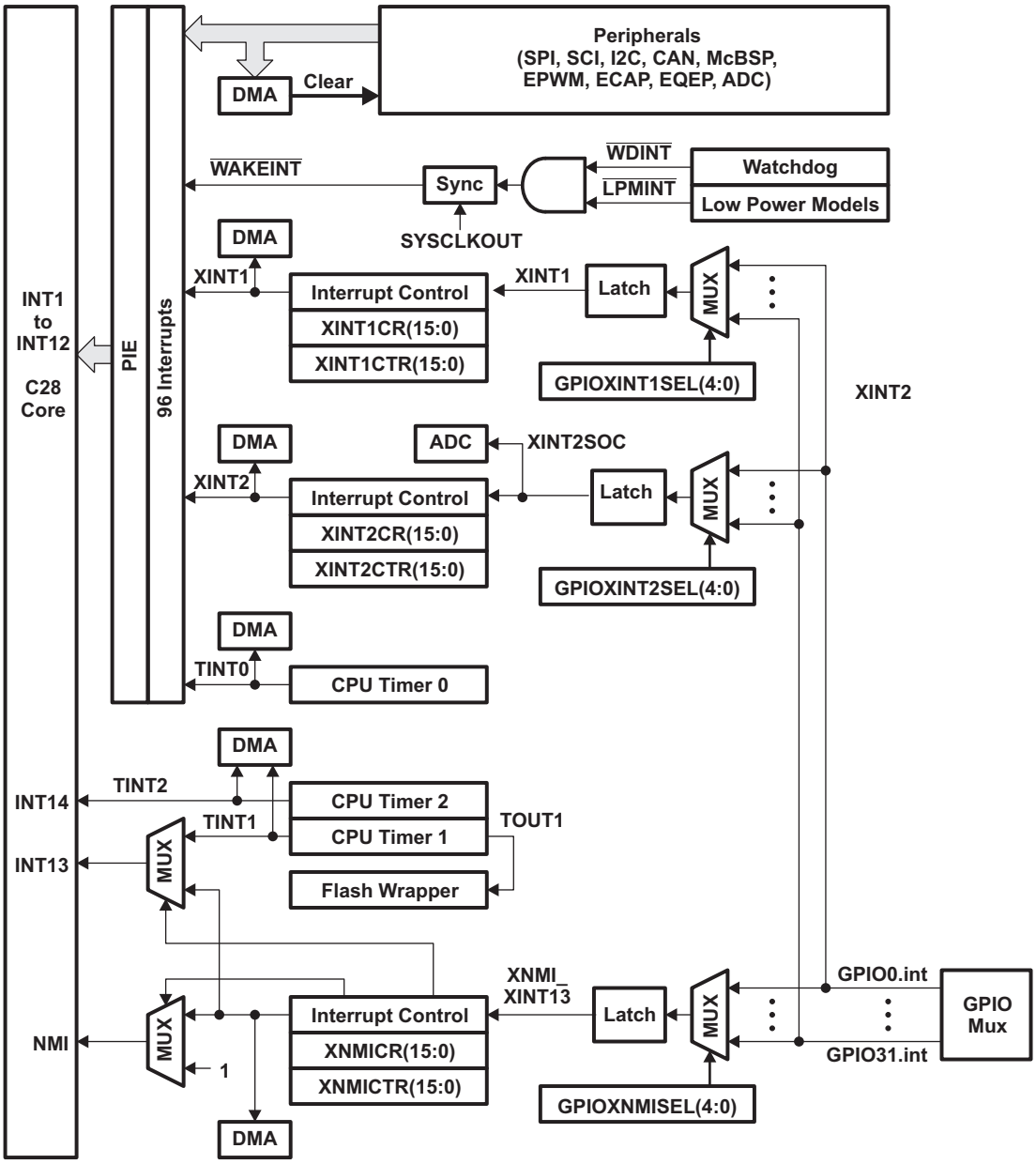

Figure 3-5. External and PIE Interrupt Sources

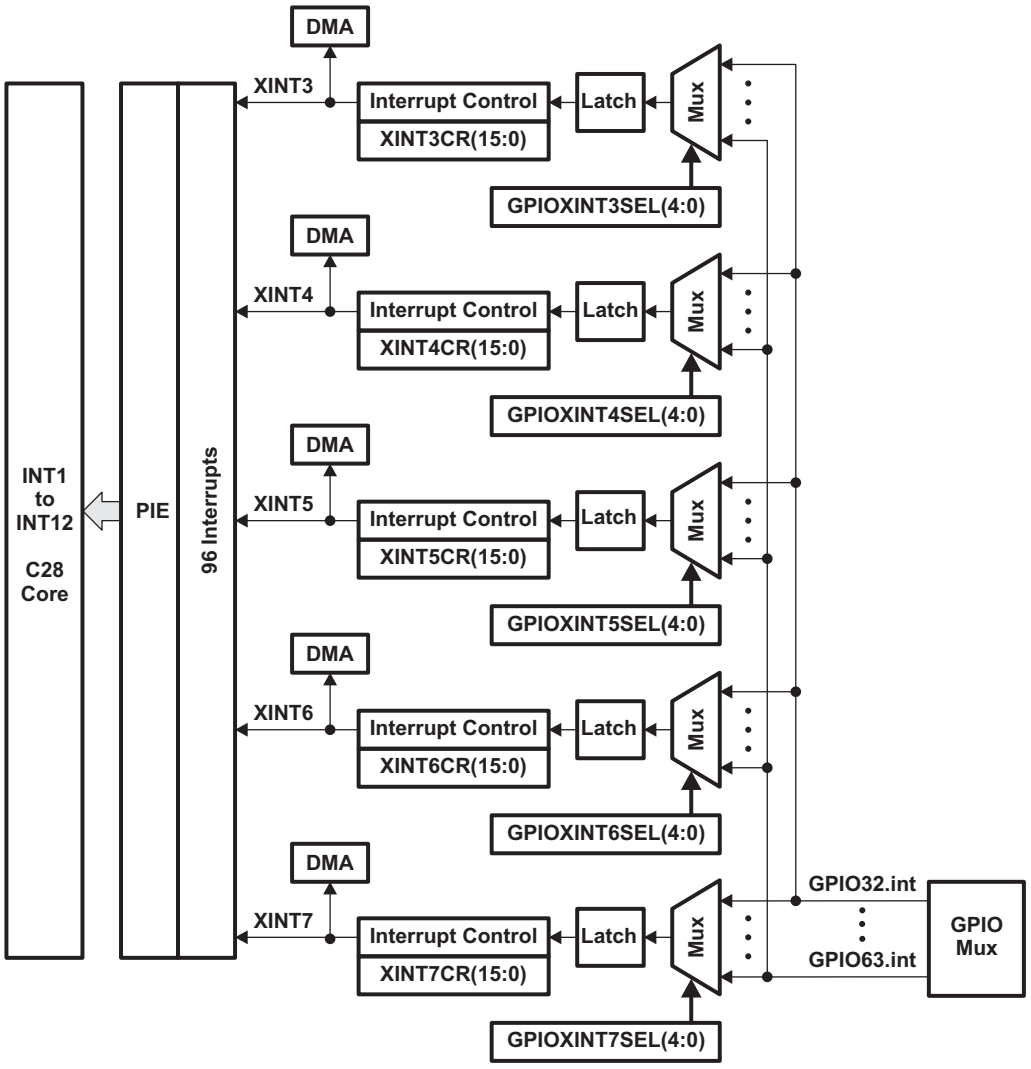

Figure 3-6. External Interrupts

Eight PIE block interrupts are grouped into one CPU interrupt. In total, 12 CPU interrupt groups, with 8 interrupts per group equals 96 possible interrupts. On the 2833x, 58 of these are used by peripherals as shown in Table 3-12.

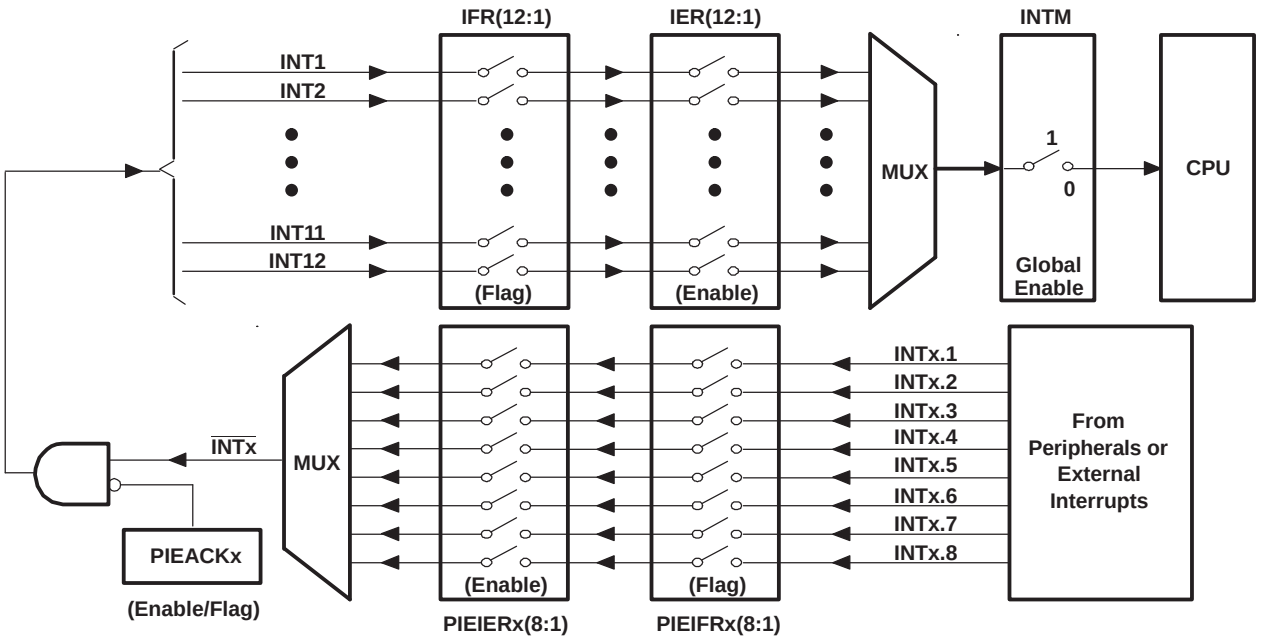

Figure 3-7. Multiplexing of Interrupts Using the PIE Block

Table 3-12. PIE Peripheral Interrupts(1)

CPU INTERRUPTS	PIE INTERRUPTS							
	INTx.8	INTx.7	INTx.6	INTx.5	INTx.4	INTx.3	INTx.2	INTx.1
INT1	WAKEINT (LPM/WD)	TINT0 (TIMER 0)	ADCINT (ADC)	XINT2	XINT1	reserved	SEQ2INT (ADC)	SEQ1INT (ADC)
INT2	reserved	reserved	EPWM6_TZINT (ePWM6)	EPWM5_TZINT (ePWM5)	EPWM4_TZINT (ePWM4)	EPWM3_TZINT (ePWM3)	EPWM2_TZINT (ePWM2)	EPWM1_TZINT (ePWM1)
INT3	reserved	reserved	EPWM6_INT (ePWM6)	EPWM5_INT (ePWM5)	EPWM4_INT (ePWM4)	EPWM3_INT (ePWM3)	EPWM2_INT (ePWM2)	EPWM1_INT (ePWM1)
INT4	reserved	reserved	ECAP6_INT (ECAP6)	ECAP5_INT (ECAP5)	ECAP4_INT (eCAP4)	ECAP3_INT (eCAP3)	ECAP2_INT (eCAP2)	ECAP1_INT (eCAP1)
INT5	reserved	reserved	reserved	reserved	reserved	reserved	EQEP2_INT (eQEP2)	EQEP1_INT (eQEP1)
INT6	reserved	reserved	MXINTA (McBSP-A)	MRINTA (McBSP-A)	MXINTB (McBSP-B)	MRXINTB (McBSP-B)	SPITXINTA (SPI-A)	SPIRXINTA (SPI-A)
INT7	reserved	reserved	DINTCH6 (DMA)	DINTCH5 (DMA)	DINTCH4 (DMA)	DINTCH3 (DMA)	DINTCH2 (DMA)	DINTCH1 (DMA)
INT8	reserved	reserved	SCITXINTC (SCI-C)	SCIRXINTC (SCI-C)	reserved	reserved	I2CINT2A (I2C-A)	I2CINT1A (I2C-A)
INT9	ECAN1_INTB (CAN-B)	ECAN0_INTB (CAN-B)	ECAN1_INTA (CAN-A)	ECAN0_INTA (CAN-A)	SCITXINTB (SCI-B)	SCIRXINTB (SCI-B)	SCITXINTA (SCI-A)	SCIRXINTA (SCI-A)
INT10	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
INT11	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
INT12	LUF (FPU)	LVF (FPU)	reserved	XINT7	XINT6	XINT5	XINT4	XINT3

(1) Out of the 96 possible interrupts, 58 interrupts are currently used. The remaining interrupts are reserved for future devices. These interrupts can be used as software interrupts if they are enabled at the PIEIFRx level, provided none of the interrupts within the group is being used by a peripheral. Otherwise, interrupts coming in from peripherals may be lost by accidentally clearing their flag while modifying the PIEIFR. To summarize, there are two safe cases when the reserved interrupts could be used as software interrupts:
1) No peripheral within the group is asserting interrupts.
2) No peripheral interrupts are assigned to the group (example PIE group 11).

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Table 3-13. PIE Configuration and Control Registers

NAME	ADDRESS	SIZE (X16)	DESCRIPTION(1)
PIECTRL	0x0CE0	1	PIE, Control Register
PIEACK	0x0CE1	1	PIE, Acknowledge Register
PIEIER1	0x0CE2	1	PIE, INT1 Group Enable Register
PIEIFR1	0x0CE3	1	PIE, INT1 Group Flag Register
PIEIER2	0x0CE4	1	PIE, INT2 Group Enable Register
PIEIFR2	0x0CE5	1	PIE, INT2 Group Flag Register
PIEIER3	0x0CE6	1	PIE, INT3 Group Enable Register
PIEIFR3	0x0CE7	1	PIE, INT3 Group Flag Register
PIEIER4	0x0CE8	1	PIE, INT4 Group Enable Register
PIEIFR4	0x0CE9	1	PIE, INT4 Group Flag Register
PIEIER5	0x0CEA	1	PIE, INT5 Group Enable Register
PIEIFR5	0x0CEB	1	PIE, INT5 Group Flag Register
PIEIER6	0x0CEC	1	PIE, INT6 Group Enable Register
PIEIFR6	0x0CED	1	PIE, INT6 Group Flag Register
PIEIER7	0x0CEE	1	PIE, INT7 Group Enable Register
PIEIFR7	0x0CEF	1	PIE, INT7 Group Flag Register
PIEIER8	0x0CF0	1	PIE, INT8 Group Enable Register
PIEIFR8	0x0CF1	1	PIE, INT8 Group Flag Register
PIEIER9	0x0CF2	1	PIE, INT9 Group Enable Register
PIEIFR9	0x0CF3	1	PIE, INT9 Group Flag Register
PIEIER10	0x0CF4	1	PIE, INT10 Group Enable Register
PIEIFR10	0x0CF5	1	PIE, INT10 Group Flag Register
PIEIER11	0x0CF6	1	PIE, INT11 Group Enable Register
PIEIFR11	0x0CF7	1	PIE, INT11 Group Flag Register
PIEIER12	0x0CF8	1	PIE, INT12 Group Enable Register
PIEIFR12	0x0CF9	1	PIE, INT12 Group Flag Register
Reserved	0x0CFA 0x0CFF	6	Reserved

(1) The PIE configuration and control registers are not protected by EALLOW mode. The PIE vector table is protected.

3.5.1 External Interrupts

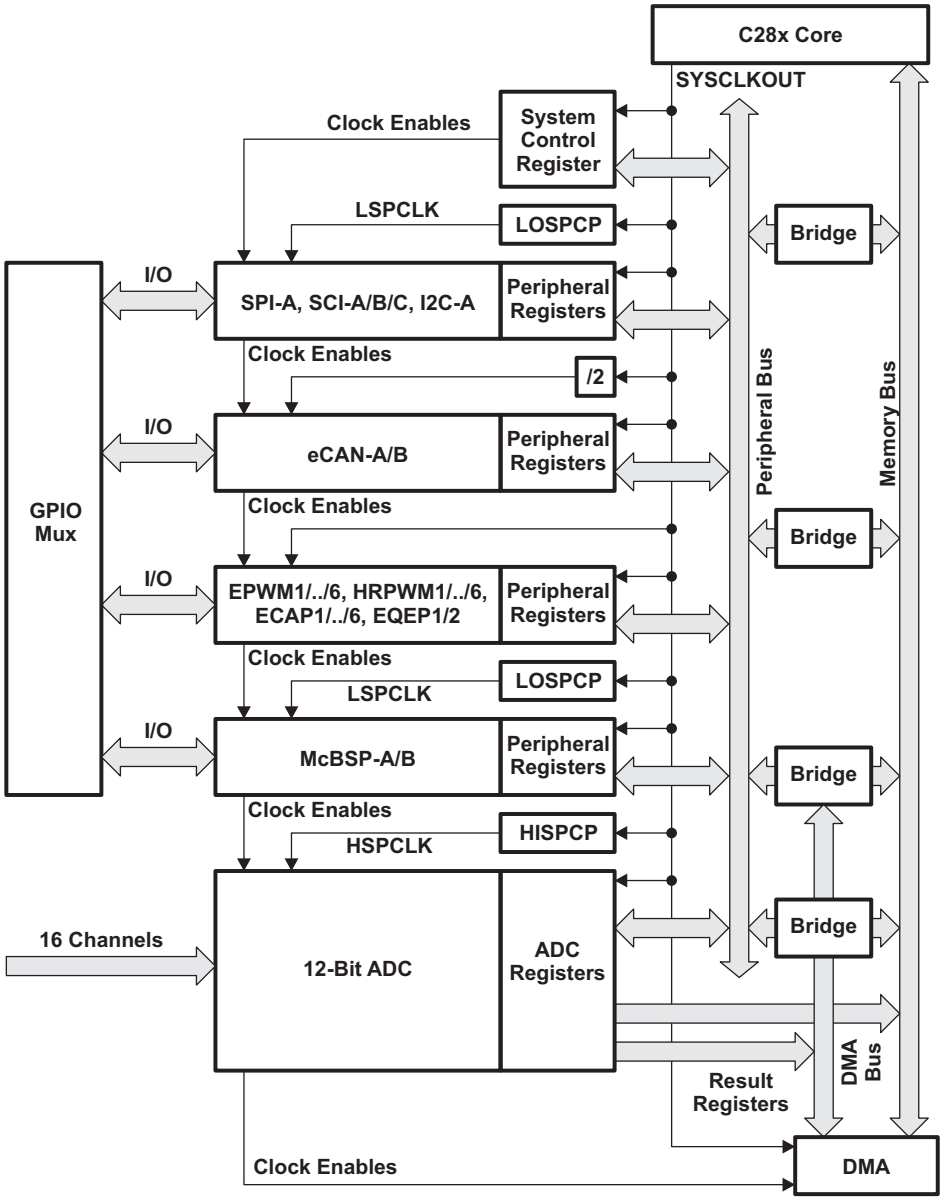
Table 3-14. External Interrupt Registers

Name	Address	Size (x16)	Description
XINT1CR	0x0000 7070	1	XINT1 configuration register
XINT2CR	0x0000 7071	1	XINT2 configuration register
XINT3CR	0x0000 7072	1	XINT3 configuration register
XINT4CR	0x0000 7073	1	XINT4 configuration register
XINT5CR	0x0000 7074	1	XINT5 configuration register
XINT6CR	0x0000 7075	1	XINT6 configuration register
XINT7CR	0x0000 7076	1	XINT7 configuration register
XNMICR	0x0000 7077	1	XNMI configuration register
XINT1CTR	0x0000 7078	1	XINT1 counter register
XINT2CTR	0x0000 7079	1	XINT2 counter register
reserved	0x0000 707A - 0x0000 707E	5	
XNMICTR	0x0000 707F	1	XNMI counter register

Each external interrupt can be enabled/disabled or qualified using positive, negative, or both positive and negative edge. For more information, see the *TMS320x280x, 2801x, 2804x System Control and Interrupts Reference Guide* (literature number SPRU712).

3.6 System Control

This section describes the 2833x oscillator, PLL and clocking mechanisms, the watchdog function and the low power modes. Figure 3-8 shows the various clock and reset domains in the 2833x devices that will be discussed.



A. CLKIN is the clock into the CPU. It is passed out of the CPU as SYSCLKOUT (that is, CLKIN is the same frequency as SYSCLKOUT).

Figure 3-8. Clock and Reset Domains

The PLL, clocking, watchdog and low-power modes, are controlled by the registers listed in Table 3-15.

Table 3-15. PLL, Clocking, Watchdog, and Low-Power Mode Registers

Name	Address	Size (x16)	Description
XCLK	0x0000-7010	1	XCLKOUT Pin Control and X1/XCLKIN Status Register
PLLSTS	0x0000-7011	1	PLL Status Register
reserved	0x0000-7012 - 0x0000-7018	7	
HISPCP	0x0000-701A	1	High-Speed Peripheral Clock Pre-Scaler Register
LOSPCP	0x0000-701B	1	Low-Speed Peripheral Clock Pre-Scaler Register
PCLKCR0	0x0000-701C	1	Peripheral Clock Control Register 0
PCLKCR1	0x0000-701D	1	Peripheral Clock Control Register 1
LPMCR0	0x0000-701E	1	Low Power Mode Control Register 0
reserved	0x0000-701F	1	Low Power Mode Control Register 1
PCLKCR3	0x0000-7020	1	Peripheral Clock Control Register 3
PLLCR	0x0000-7021	1	PLL Control Register
SCSR	0x0000-7022	1	System Control and Status Register
WDCNTR	0x0000-7023	1	Watchdog Counter Register
reserved	0x0000-7024	1	
WDKEY	0x0000-7025	1	Watchdog Reset Key Register
reserved	0x0000-7026 - 0x0000-7028	3	
WDCR	0x0000-7029	1	Watchdog Control Register
reserved	0x0000-702A - 0x0000-702F	6	

3.6.1 OSC and PLL Block

Figure 3-9 shows the OSC and PLL block on the 2833x.

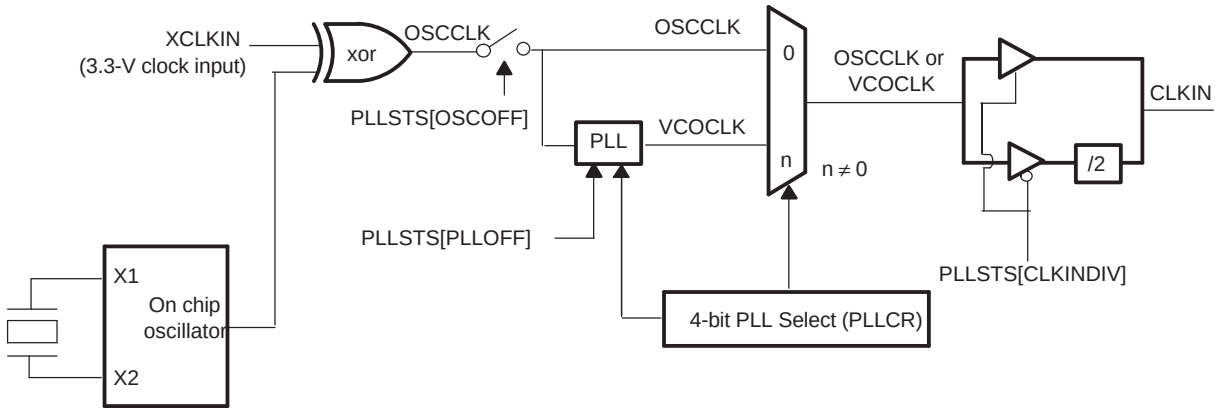


Figure 3-9. OSC and PLL Block Diagram

The on-chip oscillator circuit enables a crystal/resonator to be attached to the 2833x devices using the X1 and X2 pins. If the on-chip oscillator is not used, an external oscillator can be used in either one of the following configurations:

1. A 3.3-V external oscillator can be directly connected to the XCLKIN pin. The X2 pin should be left unconnected and the X1 pin tied low. The logic-high level in this case should not exceed V_{DDIO}.
2. A 1.8-V external oscillator can be directly connected to the X1 pin. The X2 pin should be left unconnected and the XCLKIN pin tied low. The logic-high level in this case should not exceed V_{DD}.

The three possible input-clock configurations are shown in Figure 3-10 through Figure 3-12

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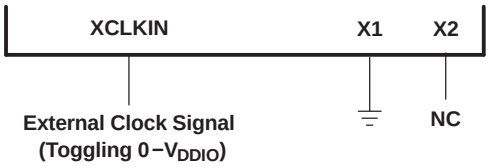

Figure 3-10. Using a 3.3-V External Oscillator

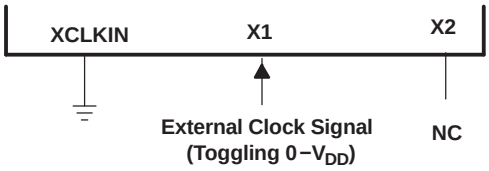

Figure 3-11. Using a 1.8-V External Oscillator

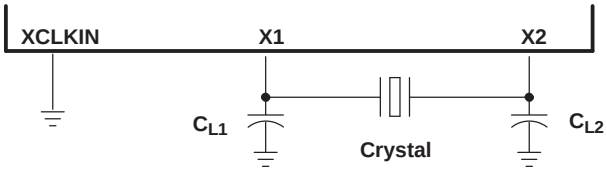

Figure 3-12. Using the Internal Oscillator

3.6.1.1 External Reference Oscillator Clock Option

The typical specifications for the external quartz crystal for a frequency of 20 MHz are listed below:

- Fundamental mode, parallel resonant
- C_L (load capacitance) = 12 pF
- $C_{L1} = C_{L2}$ = 24 pF
- C_{shunt} = 6 pF
- ESR range = 30 to 60 Ω

TI recommends that customers have the resonator/crystal vendor characterize the operation of their device with the DSC chip. The resonator/crystal vendor has the equipment and expertise to tune the tank circuit. The vendor can also advise the customer regarding the proper tank component values that will produce proper start up and stability over the entire operating range.

3.6.1.2 PLL-Based Clock Module

The 2833x devices have an on-chip, PLL-based clock module. This module provides all the necessary clocking signals for the device, as well as control for low-power mode entry. The PLL has a 4-bit ratio control PLLCR[DIV] to select different CPU clock rates. The watchdog module should be disabled before writing to the PLLCR register. It can be re-enabled (if need be) after the PLL module has stabilized, which takes 131072 OSCCLK cycles.

Table 3-16. PLLCR Register Bit Definitions

PLLCR[DIV](1)	SYSCLKOUT (CLKIN)(2)
0000 (PLL bypass)	OSCCLK/n
0001	(OSCCLK*1)/n
0010	(OSCCLK*2)/n
0011	(OSCCLK*3)/n
0100	(OSCCLK*4)/n
0101	(OSCCLK*5)/n
0110	(OSCCLK*6)/n
0111	(OSCCLK*7)/n
1000	(OSCCLK*8)/n
1001	(OSCCLK*9)/n
1010	(OSCCLK*10)/n
1011-1111	reserved

(1) This register is EALLOW protected.
(2) CLKIN is the input clock to the CPU. SYSCLKOUT is the output clock from the CPU. The frequency of SYSCLKOUT is the same as CLKIN. If CLKINDIV = 0, n = 2; if CLKINDIV = 1, n = 1.

Table 3-17. CLKIN Divide Options

PLLSTS [DIVSEL]	CLKIN DIVIDE
0	/4
1	/4
2	/2
3	/1

The PLL-based clock module provides two modes of operation:

- Crystal-operation - This mode allows the use of an external crystal/resonator to provide the time base to the device.
- External clock source operation - This mode allows the internal oscillator to be bypassed. The device clocks are generated from an external clock source input on the X1 or the XCLKIN pin.

Table 3-18. Possible PLL Configuration Modes

PLL MODE	REMARKS	PLLSTS[CLKINDIV]	SYSCLKOUT (CLKIN)
PLL Off	Invoked by the user setting the PLLOFF bit in the PLLSTS register. The PLL block is disabled in this mode. This can be useful to reduce system noise and for low power operation. The PLLCR register must first be set to 0x0000 (PLL Bypass) before entering this mode. The CPU clock (CLKIN) is derived directly from the input clock on either X1/X2, X1 or XCLKIN.	0	OSCCLK/2
		1	OSCCLK
PLL Bypass	PLL Bypass is the default PLL configuration upon power-up or after an external reset ($\overline{XRS}$). This mode is selected when the PLLCR register is set to 0x0000 or while the PLL locks to a new frequency after the PLLCR register has been modified. In this mode, the PLL itself is bypassed but the PLL is not turned off.	0	OSCCLK/2
		1	OSCCLK
PLL Enable	Achieved by writing a non-zero value n into the PLLCR register. Upon writing to the PLLCR the device will switch to PLL Bypass mode until the PLL locks.	0	OSCCLK*n/2

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3.6.1.3 Loss of Input Clock

In PLL-enabled and PLL-bypass mode, if the input clock OSCCLK is removed or absent, the PLL will still issue a limp-mode clock. The limp-mode clock continues to clock the CPU and peripherals at a typical frequency of 1-5 MHz. Limp mode is not specified to work from power-up, only after input clocks have been present initially. In PLL bypass mode, the limp mode clock from the PLL is automatically routed to the CPU if the input clock is removed or absent.

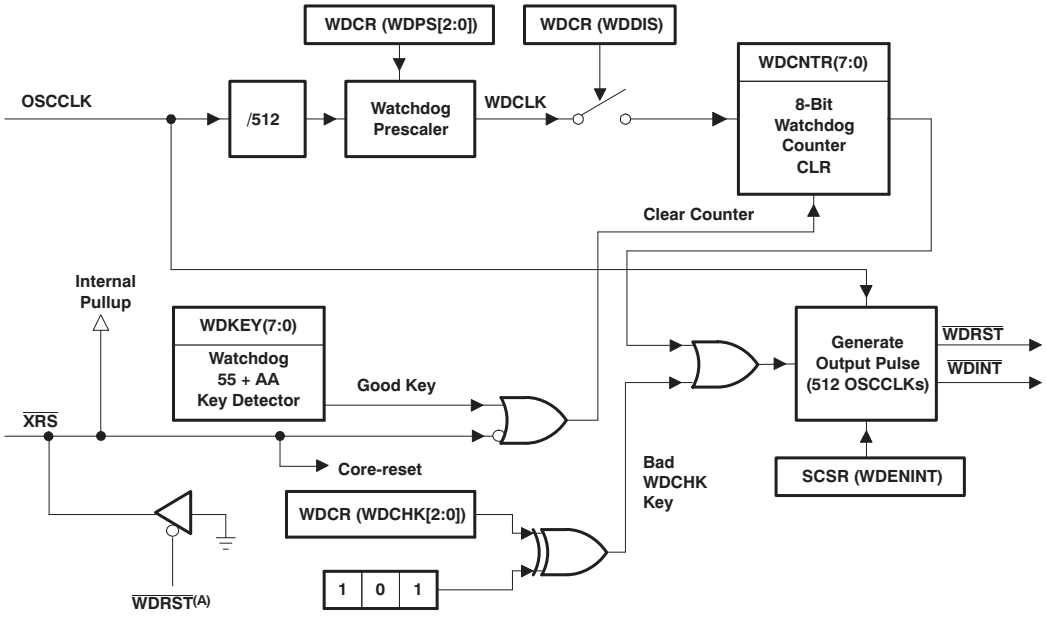
Normally, when the input clocks are present, the watchdog counter decrements to initiate a watchdog reset or WDINT interrupt. However, when the external input clock fails, the watchdog counter stops decrementing (i.e., the watchdog counter does not change with the limp-mode clock). In addition to this, the device will be reset and the “Missing Clock Status” (MCLKSTS) bit will be set. These conditions could be used by the application firmware to detect the input clock failure and initiate necessary shut-down procedure for the system.

NOTE

Applications in which the correct CPU operating frequency is absolutely critical should implement a mechanism by which the DSC will be held in reset, should the input clocks ever fail. For example, an R-C circuit may be used to trigger the $\overline{\text{XRS}}$ pin of the DSC, should the capacitor ever get fully charged. An I/O pin may be used to discharge the capacitor on a periodic basis to prevent it from getting fully charged. Such a circuit would also help in detecting failure of the flash memory and the V_{DD3VFL} rail.

3.6.2 Watchdog Block

The watchdog block on the 2833x is similar to the one used on the 240x and 281x devices. The watchdog module generates an output pulse, 512 oscillator clocks wide (OSCCLK), whenever the 8-bit watchdog up counter has reached its maximum value. To prevent this, the user disables the counter or the software must periodically write a 0x55 + 0xAA sequence into the watchdog key register which will reset the watchdog counter. Figure 3-13 shows the various functional blocks within the watchdog module.



A. The $\overline{\text{WDRST}}$ signal is driven low for 512 OSCCLK cycles.

Figure 3-13. Watchdog Module

The $\overline{\text{WDINT}}$ signal enables the watchdog to be used as a wakeup from IDLE/STANDBY mode.

In STANDBY mode, all peripherals are turned off on the device. The only peripheral that remains functional is the watchdog. The WATCHDOG module will run off OSCCLK. The $\overline{\text{WDINT}}$ signal is fed to the LPM block so that it can wake the device from STANDBY (if enabled). See Section Section 3.7, Low-Power Modes Block, for more details.

In IDLE mode, the $\overline{\text{WDINT}}$ signal can generate an interrupt to the CPU, via the PIE, to take the CPU out of IDLE mode.

In HALT mode, this feature cannot be used because the oscillator (and PLL) are turned off and hence so is the WATCHDOG.

3.7 Low-Power Modes Block

The low-power modes on the 2833x are similar to the 240x devices. Table 3-19 summarizes the various modes.

Table 3-19. Low-Power Modes

MODE	LPMCR0(1:0)	OSCCLK	CLKIN	SYSCLKOUT	EXIT(1)
IDLE	00	On	On	On(2)	$\overline{\text{XRS}}$, Watchdog interrupt, any enabled interrupt, XNMI
STANDBY	01	On (watchdog still running)	Off	Off	$\overline{\text{XRS}}$, Watchdog interrupt, GPIO Port A signal, debugger(3), XNMI
HALT	1X	Off (oscillator and PLL turned off, watchdog not functional)	Off	Off	$\overline{\text{XRS}}$, GPIO Port A signal, XNMI, debugger(3)

(1) The Exit column lists which signals or under what conditions the low power mode will be exited. A low signal, on any of the signals, will exit the low power condition. This signal must be kept low long enough for an interrupt to be recognized by the device. Otherwise the IDLE mode will not be exited and the device will go back into the indicated low power mode.
(2) The IDLE mode on the C28x behaves differently than on the 24x/240x. On the C28x, the clock output from the CPU (SYSCLKOUT) is still functional while on the 24x/240x the clock is turned off.
(3) On the C28x, the JTAG port can still function even if the CPU clock (CLKIN) is turned off.

The various low-power modes operate as follows:

IDLE Mode: This mode is exited by any enabled interrupt or an XNMI that is recognized by the processor. The LPM block performs no tasks during this mode as long as the LPMCR0(LPM) bits are set to 0,0.

STANDBY Mode: Any GPIO port A signal (GPIO[31:0]) can wake the device from STANDBY mode. The user must select which signal(s) will wake the device in the GPIOLPMSEL register. The selected signal(s) are also qualified by the OSCCLK before waking the device. The number of OSCCLKs is specified in the LPMCR0 register.

HALT Mode: Only the $\overline{\text{XRS}}$ and any GPIO port A signal (GPIO[31:0]) can wake the device from HALT mode. The user selects the signal in the GPIOLPMSEL register.

NOTE

The low-power modes do not affect the state of the output pins (PWM pins included). They will be in whatever state the code left them in when the IDLE instruction was executed. See the *TMS320x280x, 2801x, 2804x System Control and Interrupts Reference Guide* (literature number SPRU712) for more details.

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4 Peripherals

The integrated peripherals of the 2833x are described in the following subsections:

- Three 32-bit CPU-Timers
- Up to six enhanced PWM modules (ePWM1, ePWM2, ePWM3, ePWM4, ePWM5, ePWM6)
- Up to six enhanced capture modules (eCAP1, eCAP2, eCAP3, eCAP4, eCAP5, eCAP6)
- Up to two enhanced QEP modules (eQEP1, eQEP2)
- Enhanced analog-to-digital converter (ADC) module
- Up to two enhanced controller area network (eCAN) modules (eCAN-A, eCAN-B)
- Up to three serial communications interface modules (SCI-A, SCI-B, SCI-C)
- One serial peripheral interface (SPI) module (SPI-A)
- Inter-integrated circuit module (I2C)
- Up to two multichannel buffered serial port (McBSP-A, McBSP-B) modules
- Digital I/O and shared pin functions

4.1 DMA Overview

Features:

- 6 Channels with independent PIE interrupts
- Trigger Sources:
  - ADC Sequencer 1 and Sequencer 2
  - McBSP-A and McBSP-B transmit and receive logic
  - XINT1-7 and XINT13
  - CPU Timers
  - Software
- Data Sources/Destinations:
  - L4-L7 16k x 16 SARAM
  - All XINTF zones
  - ADC Memory Bus mapped RESULT registers
  - McBSP-A and McBSP-B transmit and receive buffers
- Word Size: 16-bit or 32-bit (McBSPs limited to 16-bit)
- Throughput: 4 cycles/word (5 cycles/word for McBSP reads)

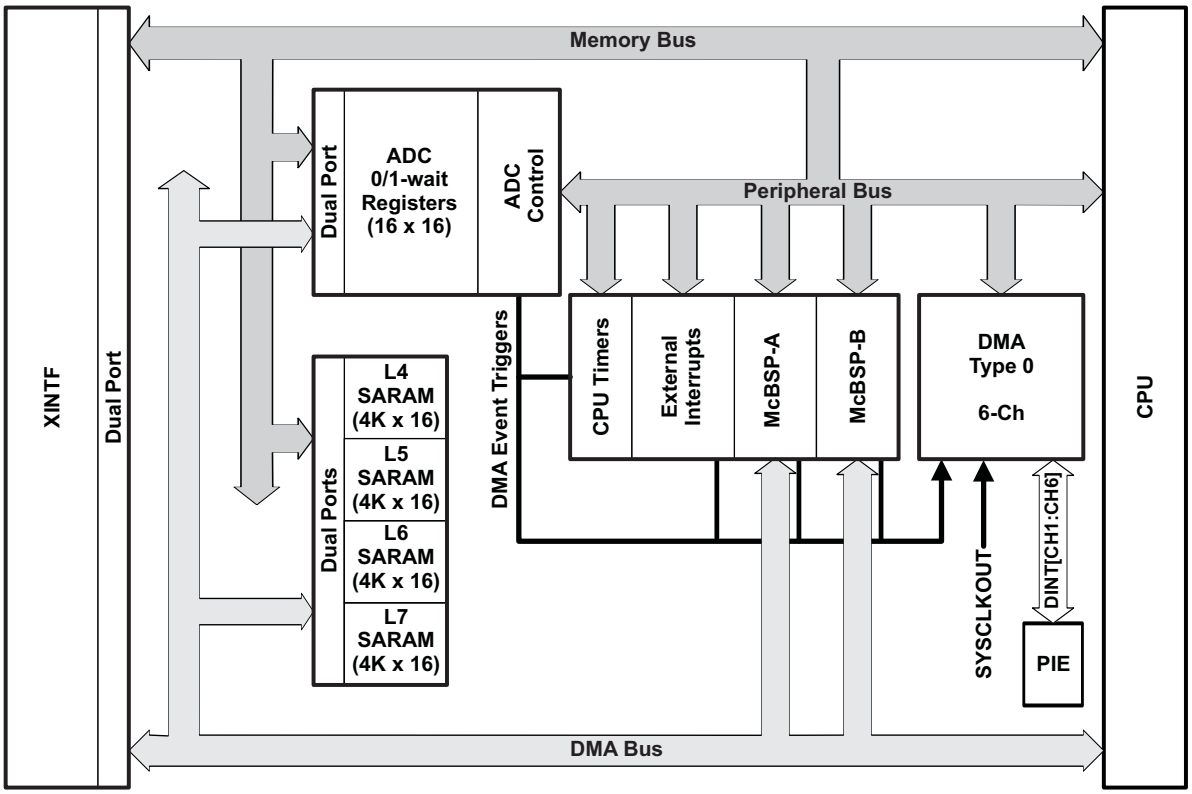


Figure 4-1. DMA Functional Block Diagram

4.2 32-Bit CPU-Timers 0/1/2

There are three 32-bit CPU-timers on the 2833x devices (CPU-TIMER0/1/2).

CPU-Timer 1 is reserved for TI system functions and Timer 2 is reserved for DSP/BIOS™. CPU-Timer 0 can be used in user applications. These timers are different from the timers that are present in the ePWM modules.

NOTE

NOTE: If the application is not using DSP/BIOS, then CPU-Timer 2 can be used in the application.

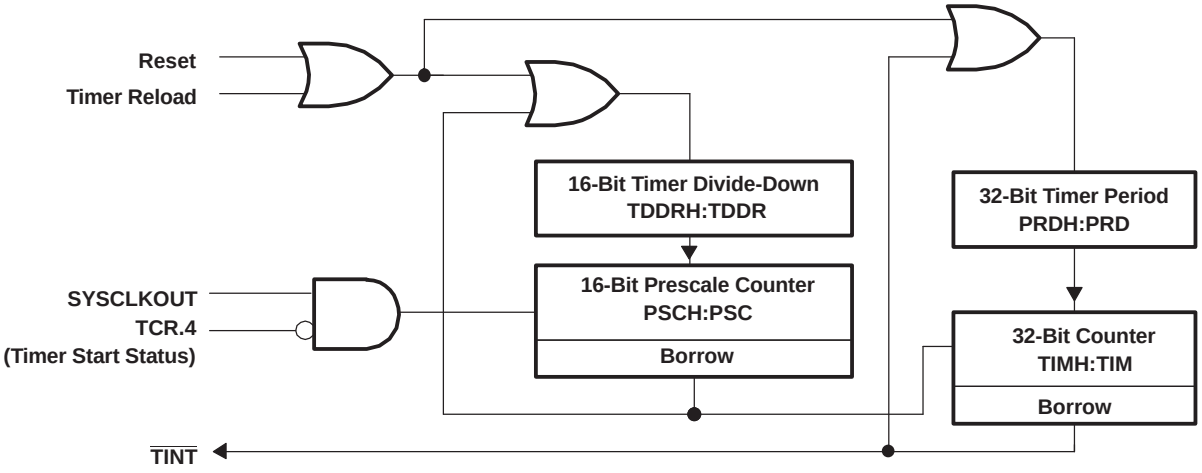
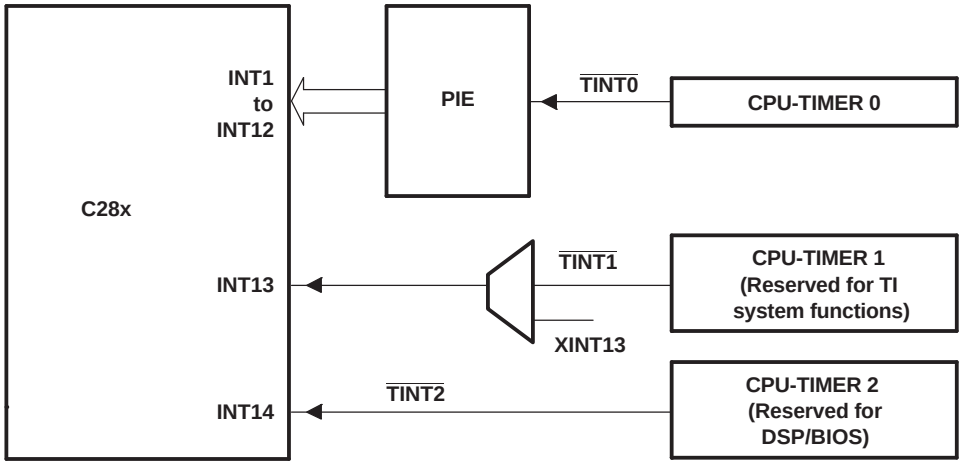


Figure 4-2. CPU-Timers

In the 2833x devices, the timer interrupt signals ($\overline{\text{TINT0}}$, $\overline{\text{TINT1}}$, $\overline{\text{TINT2}}$) are connected as shown in Figure 4-3.



A. The timer registers are connected to the memory bus of the C28x processor.

B. The timing of the timers is synchronized to SYSCLKOUT of the processor clock.

C. While TIMER1 is reserved, INT13 is not reserved and the user can use XINT13 connected to INT13.

Figure 4-3. CPU-Timer Interrupt Signals and Output Signal

The general operation of the timer is as follows: The 32-bit counter register "TIMH:TIM" is loaded with the value in the period register "PRDH:PRD". The counter register decrements at the SYSCLKOUT rate of the C28x. When the counter reaches 0, a timer interrupt output signal generates an interrupt pulse. The registers listed in Table 4-1 are used to configure the timers. For more information, see the *TMS320x280x, 2801x, 2804x System Control and Interrupts Reference Guide* (literature number SPRU712).

Table 4-1. CPU-Timers 0, 1, 2 Configuration and Control Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
TIMER0TIM	0x0C00	1	CPU-Timer 0, Counter Register
TIMER0TIMH	0x0C01	1	CPU-Timer 0, Counter Register High
TIMER0PRD	0x0C02	1	CPU-Timer 0, Period Register
TIMER0PRDH	0x0C03	1	CPU-Timer 0, Period Register High
TIMER0TCR	0x0C04	1	CPU-Timer 0, Control Register
reserved	0x0C05	1	
TIMER0TPR	0x0C06	1	CPU-Timer 0, Prescale Register
TIMER0TPRH	0x0C07	1	CPU-Timer 0, Prescale Register High
TIMER1TIM	0x0C08	1	CPU-Timer 1, Counter Register
TIMER1TIMH	0x0C09	1	CPU-Timer 1, Counter Register High
TIMER1PRD	0x0C0A	1	CPU-Timer 1, Period Register
TIMER1PRDH	0x0C0B	1	CPU-Timer 1, Period Register High
TIMER1TCR	0x0C0C	1	CPU-Timer 1, Control Register
reserved	0x0C0D	1	
TIMER1TPR	0x0C0E	1	CPU-Timer 1, Prescale Register
TIMER1TPRH	0x0C0F	1	CPU-Timer 1, Prescale Register High
TIMER2TIM	0x0C10	1	CPU-Timer 2, Counter Register
TIMER2TIMH	0x0C11	1	CPU-Timer 2, Counter Register High
TIMER2PRD	0x0C12	1	CPU-Timer 2, Period Register
TIMER2PRDH	0x0C13	1	CPU-Timer 2, Period Register High
TIMER2TCR	0x0C14	1	CPU-Timer 2, Control Register
reserved	0x0C15	1	
TIMER2TPR	0x0C16	1	CPU-Timer 2, Prescale Register
TIMER2TPRH	0x0C17	1	CPU-Timer 2, Prescale Register High
reserved	0x0C18 0x0C3F	40	

4.3 Enhanced PWM Modules (ePWM1/2/3/4/5/6)

The 2833x device contains up to six enhanced PWM Modules (ePWM). Figure 4-4 shows a block diagram of multiple ePWM modules. Figure 4-4 shows the signal interconnections with the ePWM. See the *TMS320x280x Enhanced Pulse Width Modulator (ePWM) Module Reference Guide* (literature number SPRU791) for more details.

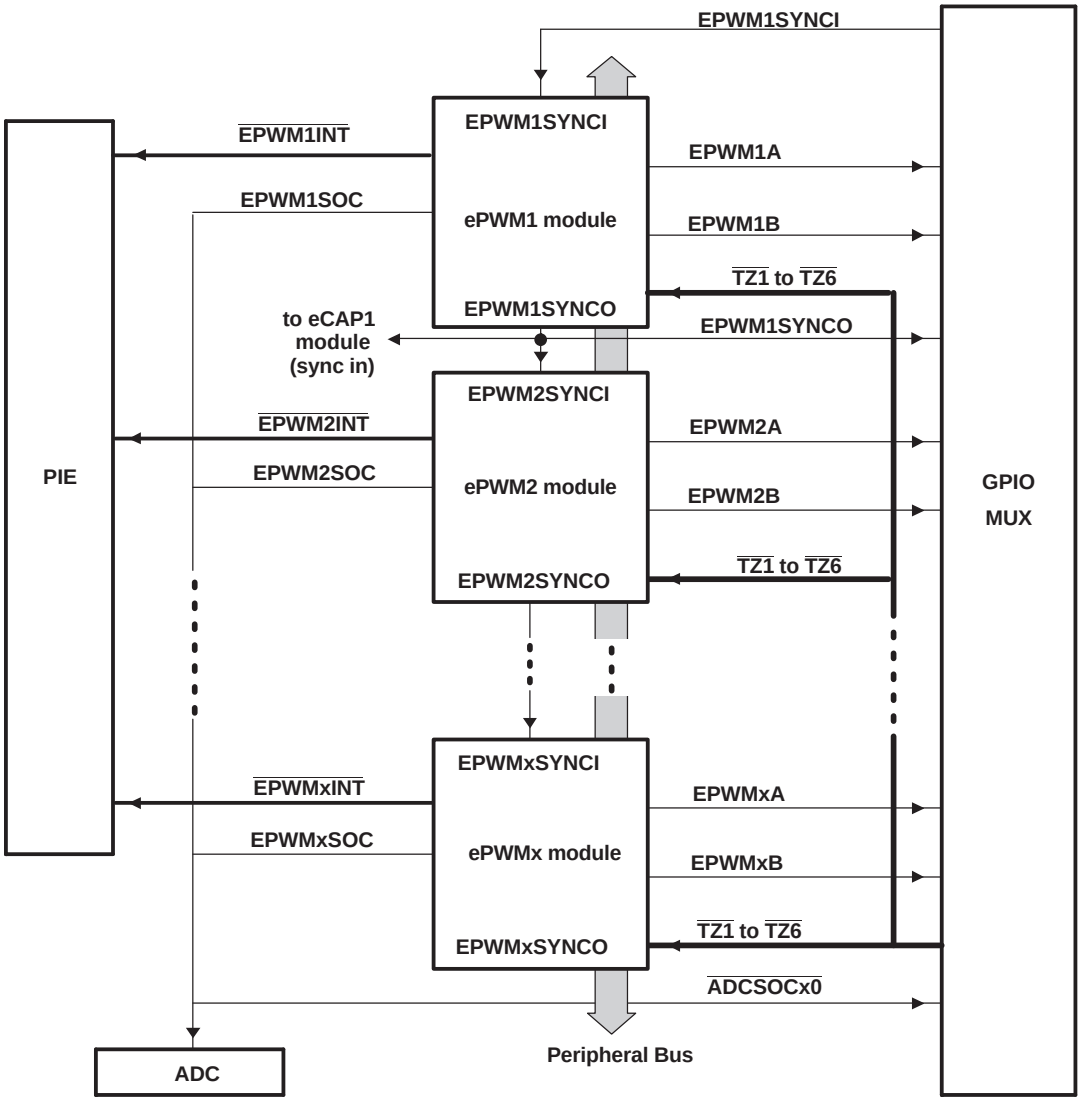


Figure 4-4. Multiple PWM Modules in a 2833x System

Table 4-2 shows the complete ePWM register set per module.

Table 4-2. ePWM Control and Status Registers

NAME	EPWM1	EPWM2	EPWM3	EPWM4	EPWM5	EPWM6	SIZE (x16) / #SHADOW	DESCRIPTION
TBCTL	0x6800	0x6840	0x6880	0x68C0	0x6900	0x6940	1 / 0	Time Base Control Register
TBSTS	0x6801	0x6841	0x6881	0x68C1	0x6901	0x6941	1 / 0	Time Base Status Register
TBPHSHR	0x6802	0x6842	0x6882	0x68C2	N/A	N/A	1 / 0	Time Base Phase HRPWM Register
TBPHS	0x6803	0x6843	0x6883	0x68C3	0x6903	0x6943	1 / 0	Time Base Phase Register
TBCTR	0x6804	0x6844	0x6884	0x68C4	0x6904	0x6944	1 / 0	Time Base Counter Register
TBPRD	0x6805	0x6845	0x6885	0x68C5	0x6905	0x6945	1 / 1	Time Base Period Register Set
CMPCTL	0x6807	0x6847	0x6887	0x68C7	0x6907	0x6947	1 / 0	Counter Compare Control Register
CMPAHR	0x6808	0x6848	0x6888	0x68C8	N/A	N/A	1 / 1	Time Base Compare A HRPWM Register
CMPA	0x6809	0x6849	0x6889	0x68C9	0x6909	0x6949	1 / 1	Counter Compare A Register Set
CMPB	0x680A	0x684A	0x688A	0x68CA	0x690A	0x694A	1 / 1	Counter Compare B Register Set
AQCTLA	0x680B	0x684B	0x688B	0x68CB	0x690B	0x694B	1 / 0	Action Qualifier Control Register For Output A
AQCTLB	0x680C	0x684C	0x688C	0x68CC	0x690C	0x694C	1 / 0	Action Qualifier Control Register For Output B
AQSFRC	0x680D	0x684D	0x688D	0x68CD	0x690D	0x694D	1 / 0	Action Qualifier Software Force Register
AQCSFRC	0x680E	0x684E	0x688E	0x68CE	0x690E	0x694E	1 / 1	Action Qualifier Continuous S/W Force Register Set
DBCTL	0x680F	0x684F	0x688F	0x68CF	0x690F	0x694F	1 / 1	Dead-Band Generator Control Register
DBRED	0x6810	0x6850	0x6890	0x68D0	0x6910	0x6950	1 / 0	Dead-Band Generator Rising Edge Delay Count Register
DBFED	0x6811	0x6851	0x6891	0x68D1	0x6911	0x6951	1 / 0	Dead-Band Generator Falling Edge Delay Count Register
TZSEL	0x6812	0x6852	0x6892	0x68D2	0x6912	0x6952	1 / 0	Trip Zone Select Register(1)
TZCTL	0x6814	0x6854	0x6894	0x68D4	0x6914	0x6954	1 / 0	Trip Zone Control Register(1)
TZEINT	0x6815	0x6855	0x6895	0x68D5	0x6915	0x6955	1 / 0	Trip Zone Enable Interrupt Register(1)
TZFLG	0x6816	0x6856	0x6896	0x68D6	0x6916	0x6956	1 / 0	Trip Zone Flag Register
TZCLR	0x6817	0x6857	0x6897	0x68D7	0x6917	0x6957	1 / 0	Trip Zone Clear Register(1)
TZFRC	0x6818	0x6858	0x6898	0x68D8	0x6918	0x6958	1 / 0	Trip Zone Force Register(1)
ETSEL	0x6819	0x6859	0x6899	0x68D9	0x6919	0x6959	1 / 0	Event Trigger Selection Register
ETPS	0x681A	0x685A	0x689A	0x68DA	0x691A	0x695A	1 / 0	Event Trigger Prescale Register
ETFLG	0x681B	0x685B	0x689B	0x68DB	0x691B	0x695B	1 / 0	Event Trigger Flag Register
ETCLR	0x681C	0x685C	0x689C	0x68DC	0x691C	0x695C	1 / 0	Event Trigger Clear Register
ETFRC	0x681D	0x685D	0x689D	0x68DD	0x691D	0x695D	1 / 0	Event Trigger Force Register
PCCTL	0x681E	0x685E	0x689E	0x68DE	0x691E	0x695E	1 / 0	PWM Chopper Control Register
HRCNFG	0x6820	0x6860	0x68A0	0x68E0	0x6920	0x6960	1 / 0	HRPWM Configuration Register(1)

(1) Registers that are EALLOW protected.

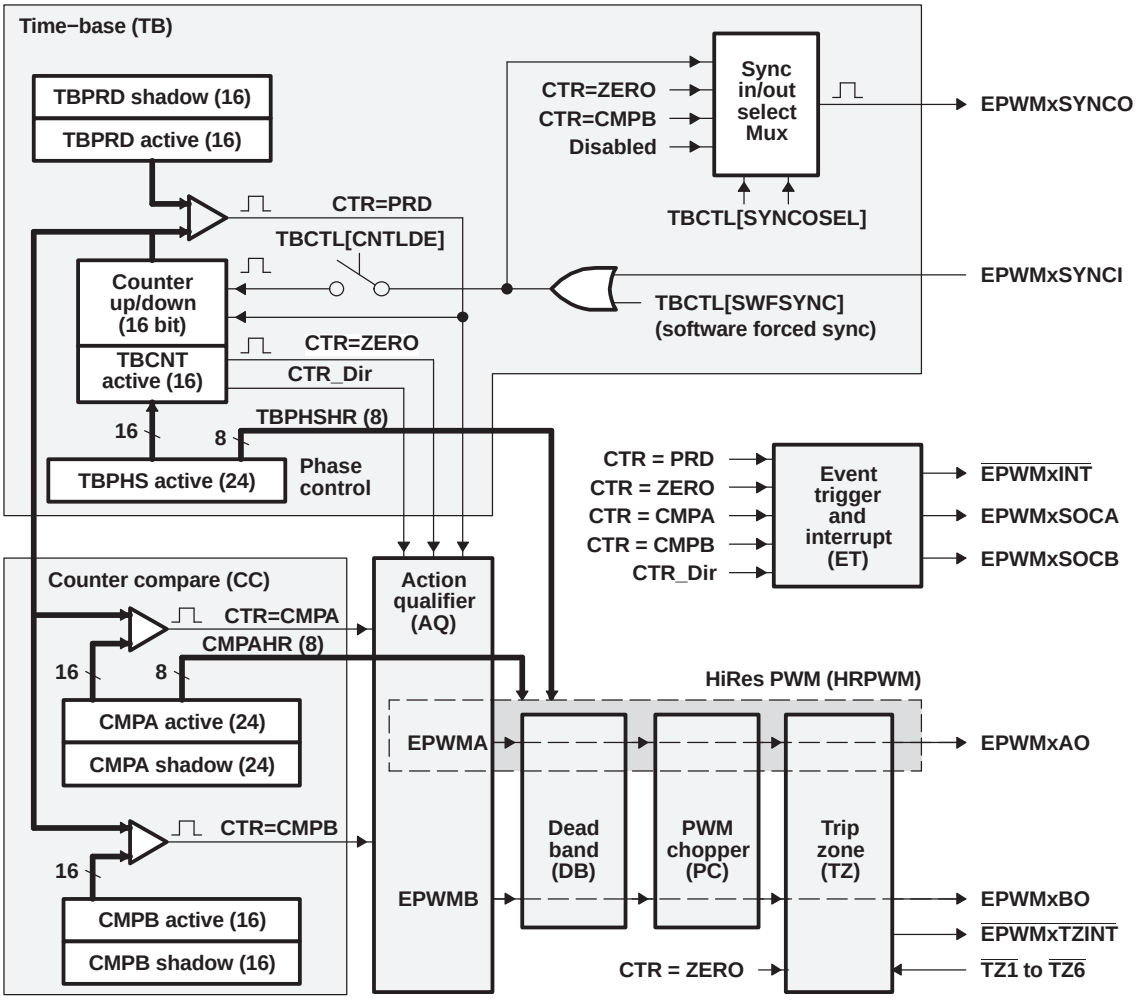


Figure 4-5. ePWM Sub-Modules Showing Critical Internal Signal Interconnections

4.4 High-Resolution PWM (HRPWM)

The HRPWM module offers PWM resolution (time granularity) which is significantly better than what can be achieved using conventionally derived digital PWM methods. The key points for the HRPWM module are:

- Significantly extends the time resolution capabilities of conventionally derived digital PWM
- Typically used when effective PWM resolution falls below ~ 9-10 bits. This occurs at PWM frequencies greater than ~200 KHz when using a CPU/System clock of 100 MHz.
- This capability can be utilized in both duty cycle and phase-shift control methods.
- Finer time granularity control or edge positioning is controlled via extensions to the Compare A and Phase registers of the ePWM module.
- HRPWM capabilities are offered only on the A signal path of an ePWM module (i.e., on the EPWMxA output). EPWMxB output has conventional PWM capabilities.

4.5 Enhanced CAP Modules (eCAP1/2/3/4/5/6)

The 2833x device contains up to six enhanced capture (eCAP) modules. Figure 4-6 shows a functional block diagram of a module. See the *TMS320x280x Enhanced Capture (eCAP) Module Reference Guide* (literature number SPRU807) for more details.

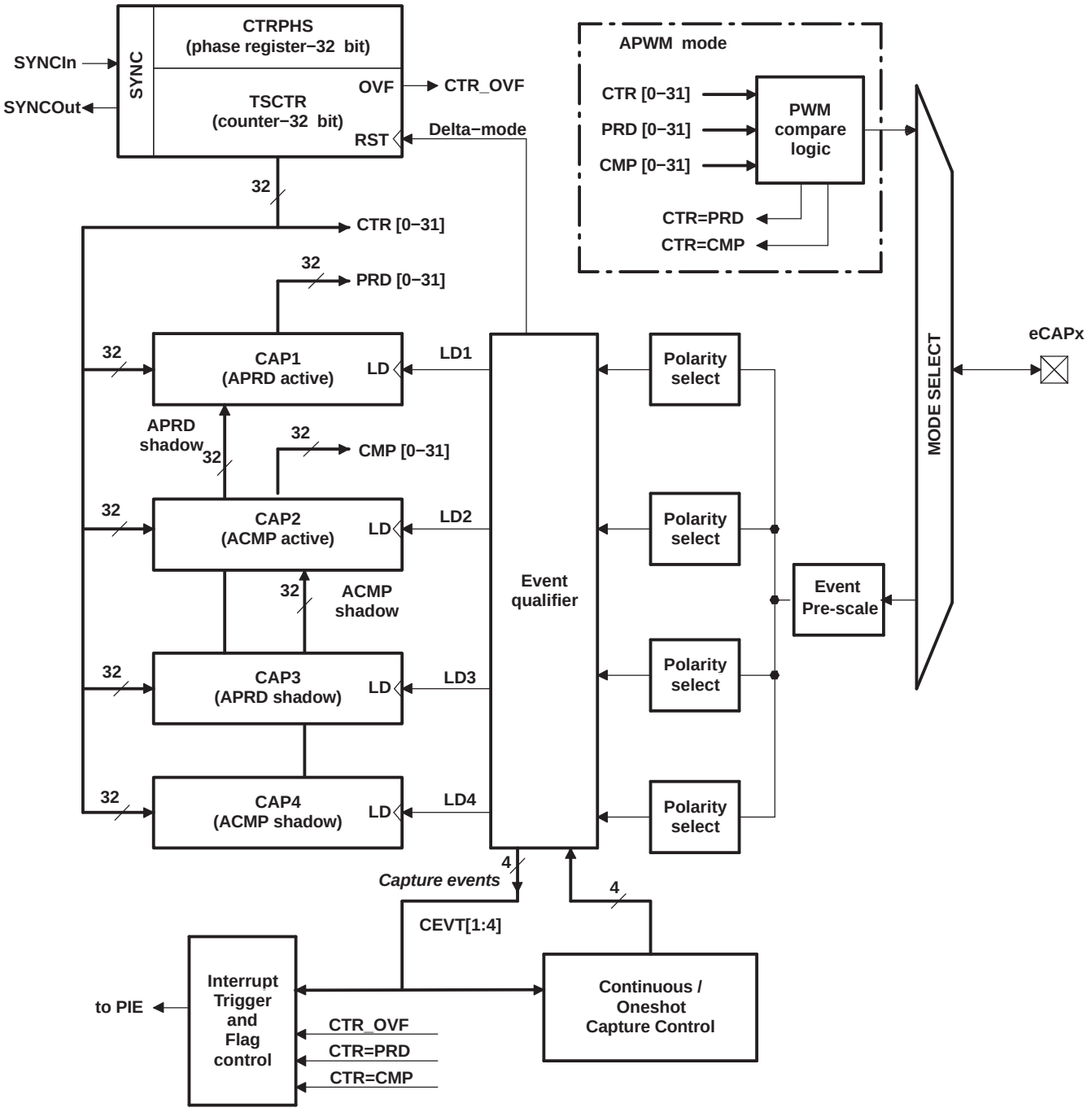


Figure 4-6. eCAP Functional Block Diagram

The eCAP modules are clocked at the SYSCLKOUT rate.

The clock enable bits (ECAP1/2/3/4/5/6ENCLK) in the PCLKCR1 register are used to turn off the eCAP modules individually (for low power operation). Upon reset, ECAP1ENCLK, ECAP2ENCLK, ECAP3ENCLK, ECAP4ENCLK, ECAP5ENCLK, and ECAP6ENCLK are set to low, indicating that the peripheral clock is off.

Table 4-3. eCAP Control and Status Registers

NAME	ECAP1	ECAP2	ECAP3	ECAP4	ECAP5	ECAP6	SIZE (x16)	DESCRIPTION
TSCTR	0x6A00	0x6A20	0x6A40	0x6A60	0x6A80	0x6AA0	2	Time-Stamp Counter
CTRPHS	0x6A02	0x6A22	0x6A42	0x6A62	0x6A82	0x6AA2	2	Counter Phase Offset Value Register
CAP1	0x6A04	0x6A24	0x6A44	0x6A64	0x6A84	0x6AA4	2	Capture 1 Register
CAP2	0x6A06	0x6A26	0x6A46	0x6A66	0x6A86	0x6AA6	2	Capture 2 Register
CAP3	0x6A08	0x6A28	0x6A48	0x6A68	0x6A88	0x6AA8	2	Capture 3 Register
CAP4	0x6A0A	0x6A2A	0x6A4A	0x6A6A	0x6A8A	0x6AAA	2	Capture 4 Register
Reserved	0x6A0C-0x6A12	0x6A2C-0x6A32	0x6A4C-0x6A52	0x6A6C-0x6A72	0x6A8C-0x6A92	0x6AAC-0x6AB2	8	Reserved
ECCTL1	0x6A14	0x6A34	0x6A54	0x6A74	0x6A94	0x6AB4	1	Capture Control Register 1
ECCTL2	0x6A15	0x6A35	0x6A55	0x6A75	0x6A95	0x6AB5	1	Capture Control Register 2
ECEINT	0x6A16	0x6A36	0x6A56	0x6A76	0x6A96	0x6AB6	1	Capture Interrupt Enable Register
ECFLG	0x6A17	0x6A37	0x6A57	0x6A77	0x6A97	0x6AB7	1	Capture Interrupt Flag Register
ECCLR	0x6A18	0x6A38	0x6A58	0x6A78	0x6A98	0x6AB8	1	Capture Interrupt Clear Register
ECFRC	0x6A19	0x6A39	0x6A59	0x6A79	0x6A99	0x6AB9	1	Capture Interrupt Force Register
Reserved	0x6A1A-0x6A1F	0x6A3A-0x6A3F	0x6A5A-0x6A5F	0x6A7A-0x6A7F	0x6A9A-0x6A9F	0x6ABA-0x6ABC	6	Reserved

4.6 Enhanced QEP Modules (eQEP1/2)

The 2833x device contains up to two enhanced quadrature encoder (eQEP) modules. See the *TMS320x280x Enhanced Quadrature Encoder (eQEP) Module Reference Guide* (literature number SPRU790) for more details.

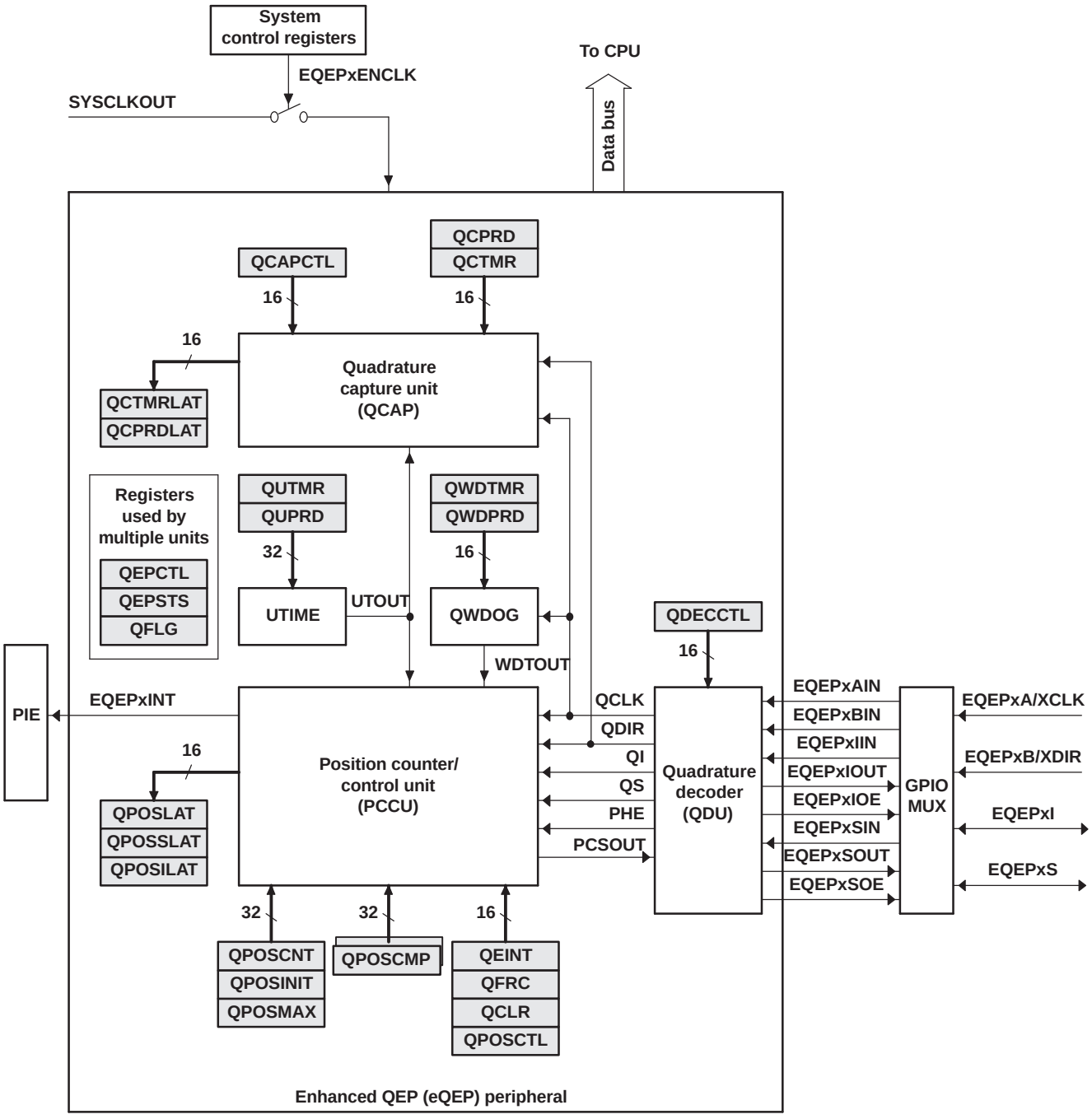


Figure 4-7. eQEP Functional Block Diagram

Table 4-4. eQEP Control and Status Registers

NAME	EQEP1 ADDRESS	EQEP2 ADDRESS	EQEP1 SIZE(x16)/ #SHADOW	REGISTER DESCRIPTION
QPOSCNT	0x6B00	0x6B40	2/0	eQEP Position Counter
QPOSINIT	0x6B02	0x6B42	2/0	eQEP Initialization Position Count
QPOSMAX	0x6B04	0x6B44	2/0	eQEP Maximum Position Count
QPOSCMP	0x6B06	0x6B46	2/1	eQEP Position-compare
QPOSILAT	0x6B08	0x6B48	2/0	eQEP Index Position Latch
QPOSSLAT	0x6B0A	0x6B4A	2/0	eQEP Strobe Position Latch
QPOSLAT	0x6B0C	0x6B4C	2/0	eQEP Position Latch
QUTMR	0x6B0E	0x6B4E	2/0	eQEP Unit Timer
QUPRD	0x6B10	0x6B50	2/0	eQEP Unit Period Register
QWDTMR	0x6B12	0x6B52	1/0	eQEP Watchdog Timer
QWDPRD	0x6B13	0x6B53	1/0	eQEP Watchdog Period Register
QDECCTL	0x6B14	0x6B54	1/0	eQEP Decoder Control Register
QEPCTL	0x6B15	0x6B55	1/0	eQEP Control Register
QCAPCTL	0x6B16	0x6B56	1/0	eQEP Capture Control Register
QPOSCTL	0x6B17	0x6B57	1/0	eQEP Position-compare Control Register
QEINT	0x6B18	0x6B58	1/0	eQEP Interrupt Enable Register
QFLG	0x6B19	0x6B59	1/0	eQEP Interrupt Flag Register
QCLR	0x6B1A	0x6B5A	1/0	eQEP Interrupt Clear Register
QFRC	0x6B1B	0x6B5B	1/0	eQEP Interrupt Force Register
QEPSTS	0x6B1C	0x6B5C	1/0	eQEP Status Register
QCTMR	0x6B1D	0x6B5D	1/0	eQEP Capture Timer
QCPRD	0x6B1E	0x6B5E	1/0	eQEP Capture Period Register
QCTMRLAT	0x6B1F	0x6B5F	1/0	eQEP Capture Timer Latch
QCPRDLAT	0x6B20	0x6B60	1/0	eQEP Capture Period Latch
Reserved	0x6B21-0x6B3F	0x6B61-0x6B7F	31/0	

4.7 Enhanced Analog-to-Digital Converter (ADC) Module

A simplified functional block diagram of the ADC module is shown in Figure 4-8. The ADC module consists of a 12-bit ADC with a built-in sample-and-hold (S/H) circuit. Functions of the ADC module include:

- 12-bit ADC core with built-in S/H
- Analog input: 0.0 V to 3.0 V (Voltages above 3.0 V produce full-scale conversion results.)
- Fast conversion rate: Up to 80 ns at 25-MHz ADC clock, 12.5 MSPS
- 16-channel, MUXed inputs
- Autosequencing capability provides up to 16 "autoconversions" in a single session. Each conversion can be programmed to select any 1 of 16 input channels
- Sequencer can be operated as two independent 8-state sequencers or as one large 16-state sequencer (i.e., two cascaded 8-state sequencers)
- Sixteen result registers (individually addressable) to store conversion values
  - The digital value of the input analog voltage is derived by:

$$\text{Digital Value} = 0, \quad \text{when input} \le 0\ \text{V}$$

$$\text{Digital Value} = 4096 \times \frac{\text{Input Analog Voltage} - \text{ADCLO}}{3}, \quad \text{when } 0\ \text{V} < \text{input} < 3\ \text{V}$$

$$\text{Digital Value} = 4095, \quad \text{when input} \ge 3\ \text{V}$$

A. All fractional values are truncated.

- Multiple triggers as sources for the start-of-conversion (SOC) sequence
  - S/W - software immediate start
  - ePWM start of conversion
  - XINT2 ADC start of conversion
- Flexible interrupt control allows interrupt request on every end-of-sequence (EOS) or every other EOS.
- Sequencer can operate in "start/stop" mode, allowing multiple "time-sequenced triggers" to synchronize conversions.
- SOCA and SOCB triggers can operate independently in dual-sequencer mode.
- Sample-and-hold (S/H) acquisition time window has separate prescale control.

The ADC module in the 2833x has been enhanced to provide flexible interface to ePWM peripherals. The ADC interface is built around a fast, 12-bit ADC module with a fast conversion rate of up to 80 ns at 25-MHz ADC clock. The ADC module has 16 channels, configurable as two independent 8-channel modules. The two independent 8-channel modules can be cascaded to form a 16-channel module. Although there are multiple input channels and two sequencers, there is only one converter in the ADC module. Figure 4-8 shows the block diagram of the ADC module.

The two 8-channel modules have the capability to autosequence a series of conversions, each module has the choice of selecting any one of the respective eight channels available through an analog MUX. In the cascaded mode, the autosequencer functions as a single 16-channel sequencer. On each sequencer, once the conversion is complete, the selected channel value is stored in its respective RESULT register. Autosequencing allows the system to convert the same channel multiple times, allowing the user to perform oversampling algorithms. This gives increased resolution over traditional single-sampled conversion results.

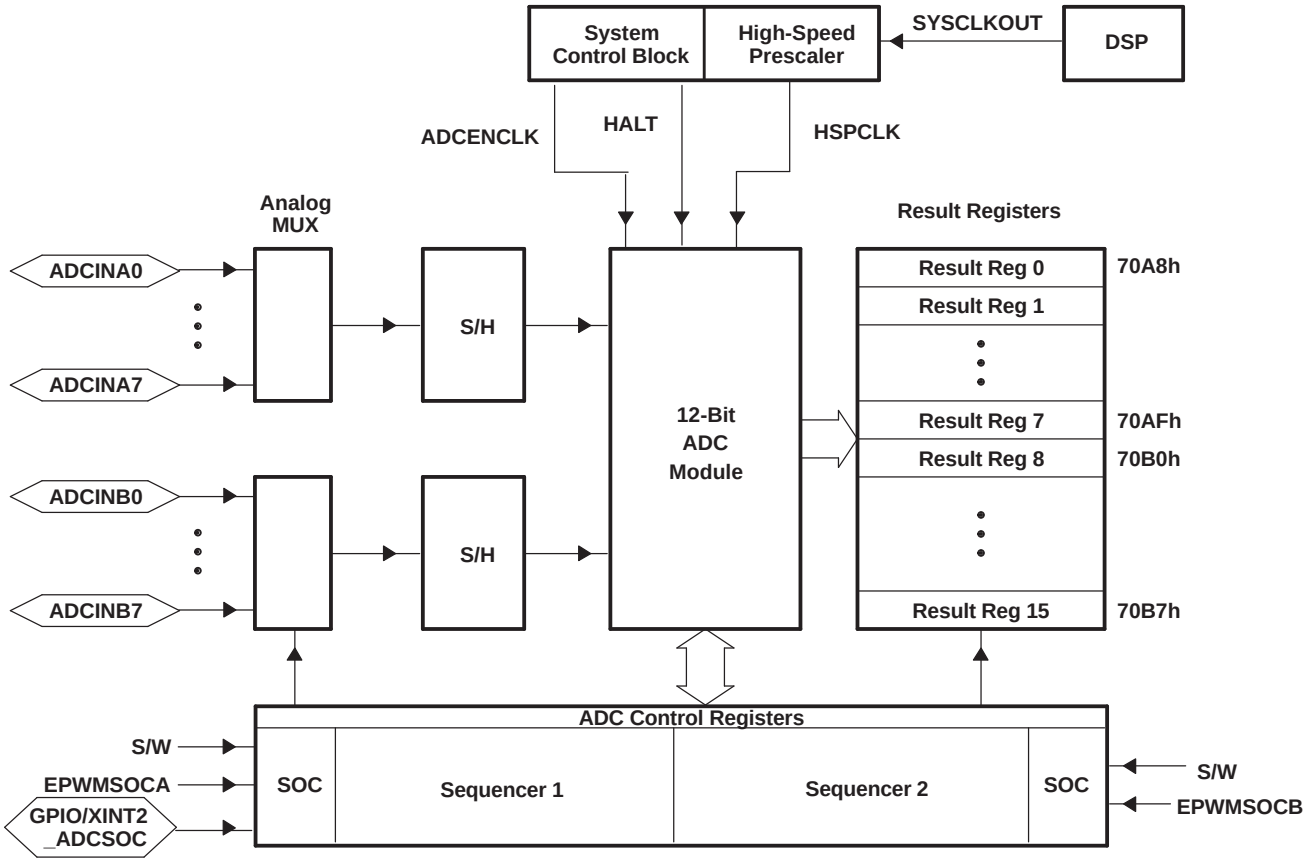


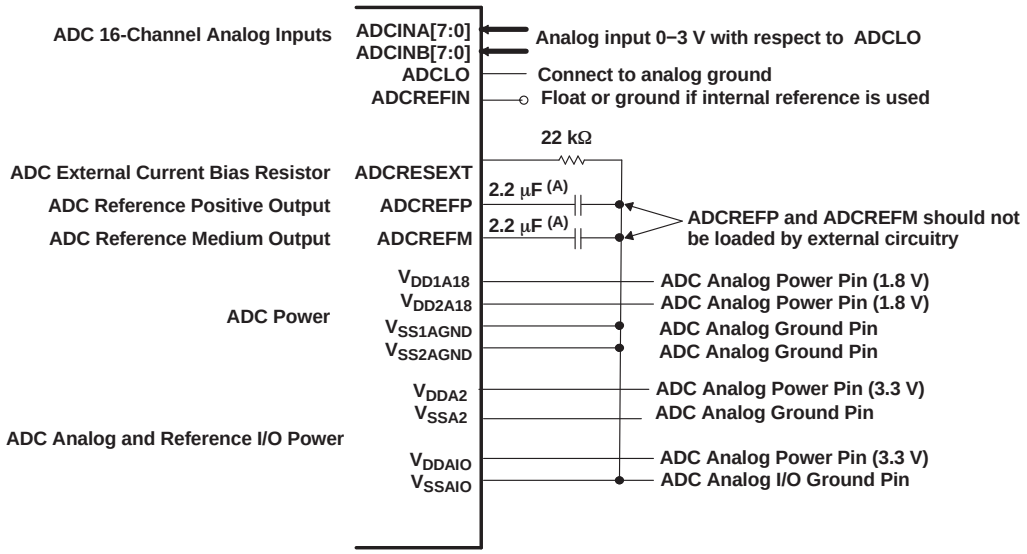
Figure 4-8. Block Diagram of the ADC Module

To obtain the specified accuracy of the ADC, proper board layout is very critical. To the best extent possible, traces leading to the ADCIN pins should not run in close proximity to the digital signal paths. This is to minimize switching noise on the digital lines from getting coupled to the ADC inputs. Furthermore, proper isolation techniques must be used to isolate the ADC module power pins (V_{DD1A18}, V_{DD2A18} , V_{DDA2}, V_{DDAIO}) from the digital supply.Figure 4-9 shows the ADC pin connections for the 2833x devices.

NOTE

1. The ADC registers are accessed at the SYSCLKOUT rate. The internal timing of the ADC module is controlled by the high-speed peripheral clock (HSPCLK).
2. The behavior of the ADC module based on the state of the ADCENCLK and HALT signals is as follows:
   - *ADCENCLK:* On reset, this signal will be low. While reset is active-low ($\overline{XRS}$) the clock to the register will still function. This is necessary to make sure all registers and modes go into their default reset state. The analog module, however, will be in a low-power inactive state. As soon as reset goes high, then the clock to the registers will be disabled. When the user sets the ADCENCLK signal high, then the clocks to the registers will be enabled and the analog module will be enabled. There will be a certain time delay (ms range) before the ADC is stable and can be used.
   - *HALT:* This mode only affects the analog module. It does not affect the registers. In this mode, the ADC module goes into low-power mode. This mode also will stop the clock to the CPU, which will stop the HSPCLK; therefore, the ADC register logic will be turned off indirectly.

Figure 4-9 shows the ADC pin-biasing for internal reference and Figure 4-10 shows the ADC pin-biasing for external reference.

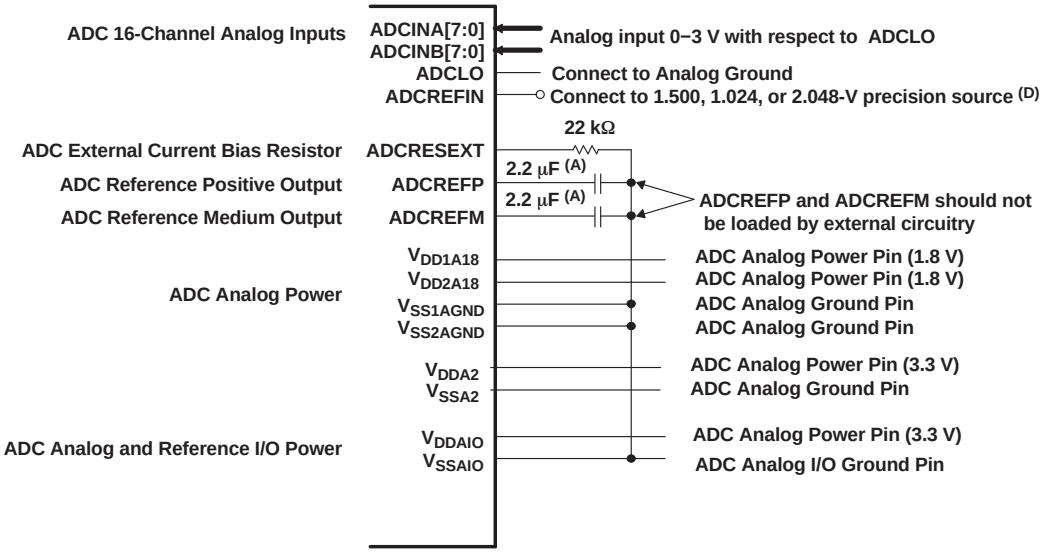


A. TAIYO YUDEN LMK212BJ225MG-T or equivalent

B. External decoupling capacitors are recommended on all power pins.

C. Analog inputs must be driven from an operational amplifier that does not degrade the ADC performance.

Figure 4-9. ADC Pin Connections With Internal Reference



A. TAIYO YUDEN LMK212BJ225MG-T or equivalent

B. External decoupling capacitors are recommended on all power pins.

C. Analog inputs must be driven from an operational amplifier that does not degrade the ADC performance.

D. External voltage on ADCREFIN is enabled by changing bits 15:14 in the ADC Reference Select register depending on the voltage used on this pin. TI recommends TI part REF3020 or equivalent for 2.048-V generation. Overall gain accuracy will be determined by accuracy of this voltage source.

Figure 4-10. ADC Pin Connections With External Reference

NOTE

The temperature rating of any recommended component must match the rating of the end product.

4.7.1 ADC Connections if the ADC Is Not Used

It is recommended to keep the connections for the analog power pins, even if the ADC is not used. Following is a summary of how the ADC pins should be connected, if the ADC is not used in an application:

- V_{DD1A18}/V_{DD2A18} – Connect to V_{DD}
- V_{DDA2}, V_{DDAIO} – Connect to V_{DDIO}
- $V_{SS1AGND}/V_{SS2AGND}$, V_{SSA2}, V_{SSAIO} – Connect to V_{SS}
- ADCLO – Connect to V_{SS}
- ADCREFIN – Connect to V_{SS}
- ADCREFP/ADCREFM – Connect a 100-nF cap to V_{SS}
- ADCRESEXT – Connect a 20-kΩ resistor (very loose tolerance) to V_{SS}.
- ADCINAn, ADCINBn - Connect to V_{SS}

When the ADC is not used, be sure that the clock to the ADC module is not turned on to realize power savings.

When the ADC module is used in an application, unused ADC input pins should be connected to analog ground ($V_{SS1AGND}/V_{SS2AGND}$)

4.7.2 ADC Registers

The ADC operation is configured, controlled, and monitored by the registers listed in Table 4-5.

Table 4-5. ADC Registers(1)

NAME	ADDRESS(1)	ADDRESS(2)	SIZE (x16)	DESCRIPTION
ADCTRL1	0x7100		1	ADC Control Register 1
ADCTRL2	0x7101		1	ADC Control Register 2
ADCMAXCONV	0x7102		1	ADC Maximum Conversion Channels Register
ADCCHSELSEQ1	0x7103		1	ADC Channel Select Sequencing Control Register 1
ADCCHSELSEQ2	0x7104		1	ADC Channel Select Sequencing Control Register 2
ADCCHSELSEQ3	0x7105		1	ADC Channel Select Sequencing Control Register 3
ADCCHSELSEQ4	0x7106		1	ADC Channel Select Sequencing Control Register 4
ADCASEQSR	0x7107		1	ADC Auto-Sequence Status Register
ADCRESULT0	0x7108	0x0B00	1	ADC Conversion Result Buffer Register 0
ADCRESULT1	0x7109	0x0B01	1	ADC Conversion Result Buffer Register 1
ADCRESULT2	0x710A	0x0B02	1	ADC Conversion Result Buffer Register 2
ADCRESULT3	0x710B	0x0B03	1	ADC Conversion Result Buffer Register 3
ADCRESULT4	0x710C	0x0B04	1	ADC Conversion Result Buffer Register 4
ADCRESULT5	0x710D	0x0B05	1	ADC Conversion Result Buffer Register 5
ADCRESULT6	0x710E	0x0B06	1	ADC Conversion Result Buffer Register 6
ADCRESULT7	0x710F	0x0B07	1	ADC Conversion Result Buffer Register 7
ADCRESULT8	0x7110	0x0B08	1	ADC Conversion Result Buffer Register 8
ADCRESULT9	0x7111	0x0B09	1	ADC Conversion Result Buffer Register 9

(1) The registers in this column are Peripheral Frame 2 Registers.
(2) The ADC result registers are dual mapped in the 2833x DSC. Locations in Peripheral Frame 2 (0x7108-0x7117) are 2 wait-states and left justified. Locations in Peripheral frame 0 space (0x0B00-0x0B0F) are 0 wait sates and right justified. During high speed/continuous conversion use of the ADC, use the 0 wait-state locations for fast transfer of ADC results to user memory.

Table 4-5. ADC Registers (continued)

NAME	ADDRESS(1)	ADDRESS(2)	SIZE (x16)	DESCRIPTION
ADCRESULT10	0x7112	0x0B0A	1	ADC Conversion Result Buffer Register 10
ADCRESULT11	0x7113	0x0B0B	1	ADC Conversion Result Buffer Register 11
ADCRESULT12	0x7114	0x0B0C	1	ADC Conversion Result Buffer Register 12
ADCRESULT13	0x7115	0x0B0D	1	ADC Conversion Result Buffer Register 13
ADCRESULT14	0x7116	0x0B0E	1	ADC Conversion Result Buffer Register 14
ADCRESULT15	0x7117	0x0B0F	1	ADC Conversion Result Buffer Register 15
ADCTRL3	0x7118		1	ADC Control Register 3
ADCST	0x7119		1	ADC Status Register
Reserved	0x711A 0x711B		2	
ADCREFSEL	0x711C		1	ADC Reference Select Register
ADCOFFTRIM	0x711D		1	ADC Offset Trim Register
Reserved	0x711E 0x711F		2	ADC Status Register

4.8 Multichannel Buffered Serial Port (McBSP) Module

The McBSP module has the following features:

- Compatible to McBSP in TMS320C54x™ /TMS320C55x™ DSC devices, except the DMA features
- Full–duplex communication
- Double–buffered data registers that allow a continuous data stream
- Independent framing and clocking for receive and transmit
- External shift clock generation or an internal programmable frequency shift clock
- A wide selection of data sizes including 8–, 12–, 16–, 20–, 24–, or 32–bits
- 8–bit data transfers with LSB or MSB first
- Programmable polarity for both frame synchronization and data clocks
- HIghly programmable internal clock and frame generation
- Support A–bis mode
- Direct interface to industry–standard CODECs, Analog Interface Chips (AICs), and other serially connected A/D and D/A devices
- Works with SPI–compatible devices

The following application interfaces can be supported on the McBSP:

- T1/E1 framers
- MVIP switching–compatible and ST–BUS–compliant devices including:
  - MVIP framers
  - H.100 framers
  - SCSA framers
  - IOM–2 compliant devices
  - AC97–compliant devices (the necessary multiphase frame synchronization capability is provided.)
  - IIS–compliant devices
- McBSP clock rate = $CLKG = \frac{CLKSRG}{(1 + CLKGDIV)}$ where CLKSRG source could be LSPCLK, CLKX, or CLKR. Serial port performance is limited by I/O buffer switching speed. Internal prescalers must be adjusted such that the peripheral speed is less than the I/O buffer speed limit—20–MHz maximum.

Figure 4-11 shows the block diagram of the McBSP module.

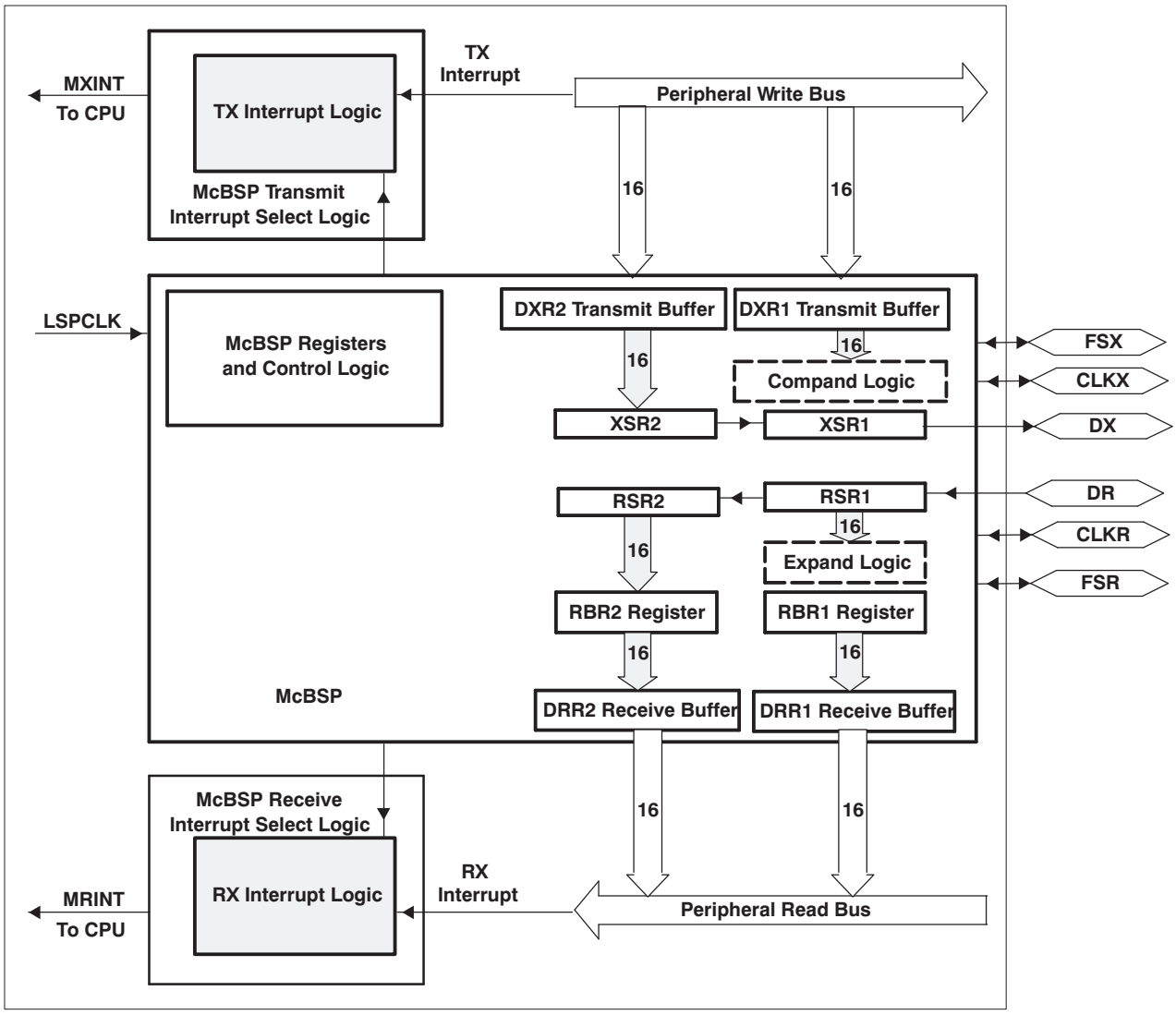


Figure 4-11. McBSP Module

Table 4-6 provides a summary of the McBSP registers.

Table 4-6. McBSP Register Summary

NAME	McBSP-A ADDRESS	McBSP-B ADDRESS	TYPE	RESET VALUE	DESCRIPTION
DATA REGISTERS, RECEIVE, TRANSMIT					
DRR2	0x5000	0x5040	R	0x0000	McBSP Data Receive Register 2
DRR1	0x5001	0x5041	R	0x0000	McBSP Data Receive Register 1
DXR2	0x5002	0x5042	W	0x0000	McBSP Data Transmit Register 2
DXR1	0x5003	0x5043	W	0x0000	McBSP Data Transmit Register 1
McBSP CONTROL REGISTERS					
SPCR2	0x5004	0x5044	R/W	0x0000	McBSP Serial Port Control Register 2
SPCR1	0x5005	0x5045	R/W	0x0000	McBSP Serial Port Control Register 1
RCR2	0x5006	0x5046	R/W	0x0000	McBSP Receive Control Register 2
RCR1	0x5007	0x5047	R/W	0x0000	McBSP Receive Control Register 1
XCR2	0x5008	0x5048	R/W	0x0000	McBSP Transmit Control Register 2
XCR1	0x5009	0x5049	R/W	0x0000	McBSP Transmit Control Register 1
SRGR2	0x500A	0x504A	R/W	0x0000	McBSP Sample Rate Generator Register 2
SRGR1	0x500B	0x504B	R/W	0x0000	McBSP Sample Rate Generator Register 1
MULTICHANNEL CONTROL REGISTERS					
MCR2	0x500C	0x504C	R/W	0x0000	McBSP Multichannel Register 2
MCR1	0x500D	0x504D	R/W	0x0000	McBSP Multichannel Register 1
RCERA	0x500E	0x504E	R/W	0x0000	McBSP Receive Channel Enable Register Partition A
RCERB	0x500F	0x504F	R/W	0x0000	McBSP Receive Channel Enable Register Partition B
XCERA	0x5010	0x5050	R/W	0x0000	McBSP Transmit Channel Enable Register Partition A
XCERB	0x5011	0x5051	R/W	0x0000	McBSP Transmit Channel Enable Register Partition B
PCR	0x5012	0x5052	R/W	0x0000	McBSP Pin Control Register
RCERC	0x5013	0x5053	R/W	0x0000	McBSP Receive Channel Enable Register Partition C
RCERD	0x5014	0x5054	R/W	0x0000	McBSP Receive Channel Enable Register Partition D
XCERC	0x5015	0x5055	R/W	0x0000	McBSP Transmit Channel Enable Register Partition C
XCERD	0x5016	0x5056	R/W	0x0000	McBSP Transmit Channel Enable Register Partition D
RCERE	0x5017	0x5057	R/W	0x0000	McBSP Receive Channel Enable Register Partition E
RCERF	0x5018	0x5058	R/W	0x0000	McBSP Receive Channel Enable Register Partition F
XCERE	0x5019	0x5059	R/W	0x0000	McBSP Transmit Channel Enable Register Partition E
XCERF	0x501A	0x505A	R/W	0x0000	McBSP Transmit Channel Enable Register Partition F
RCERG	0x501B	0x505B	R/W	0x0000	McBSP Receive Channel Enable Register Partition G
RCERH	0x501C	0x505C	R/W	0x0000	McBSP Receive Channel Enable Register Partition H
XCERG	0x501D	0x505D	R/W	0x0000	McBSP Transmit Channel Enable Register Partition G
XCERH	0x501E	0x505E	R/W	0x0000	McBSP Transmit Channel Enable Register Partition H
MFFINT	0x5023	0x5063	R/W	0x0000	McBSP Interrupt Enable Register
MFFST	0x5024	0x5064	R/W	0x0000	McBSP Pin Status Register

4.9 Enhanced Controller Area Network (eCAN) Modules (eCAN-A and eCAN-B)

The CAN module has the following features:

- Fully compliant with CAN protocol, version 2.0B
- Supports data rates up to 1 Mbps
- Thirty-two mailboxes, each with the following properties:
  - Configurable as receive or transmit
  - Configurable with standard or extended identifier
  - Has a programmable receive mask
  - Supports data and remote frame
  - Composed of 0 to 8 bytes of data
  - Uses a 32-bit time stamp on receive and transmit message
  - Protects against reception of new message
  - Holds the dynamically programmable priority of transmit message
  - Employs a programmable interrupt scheme with two interrupt levels
  - Employs a programmable alarm on transmission or reception time-out
- Low-power mode
- Programmable wake-up on bus activity
- Automatic reply to a remote request message
- Automatic retransmission of a frame in case of loss of arbitration or error
- 32-bit local network time counter synchronized by a specific message (communication in conjunction with mailbox 16)
- Self-test mode
  - Operates in a loopback mode receiving its own message. A "dummy" acknowledge is provided, thereby eliminating the need for another node to provide the acknowledge bit.

NOTE

For a SYSCLKOUT of 100 MHz, the smallest bit rate possible is 15.625 kbps.

For a SYSCLKOUT of 150 MHz, the smallest bit rate possible is 23.4 kbps.

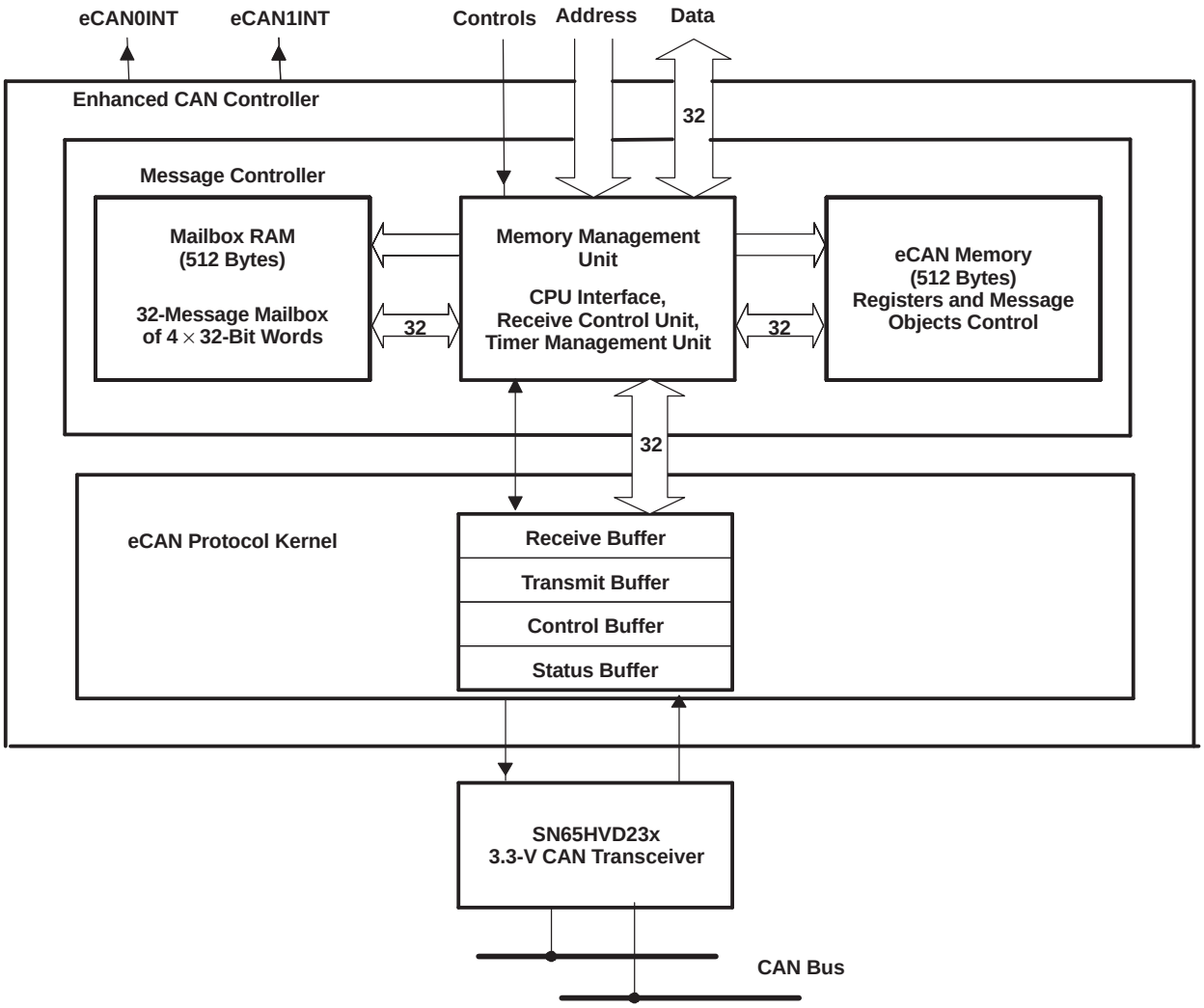


Figure 4-12. eCAN Block Diagram and Interface Circuit

Table 4-7. 3.3-V eCAN Transceivers

PART NUMBER	SUPPLY VOLTAGE	LOW-POWER MODE	SLOPE CONTROL	VREF	OTHER	T_A
SN65HVD230	3.3 V	Standby	Adjustable	Yes	–	-40°C to 85°C
SN65HVD230Q	3.3 V	Standby	Adjustable	Yes	–	-40°C to 125°C
SN65HVD231	3.3 V	Sleep	Adjustable	Yes	–	-40°C to 85°C
SN65HVD231Q	3.3 V	Sleep	Adjustable	Yes	–	-40°C to 125°C
SN65HVD232	3.3 V	None	None	None	–	-40°C to 85°C
SN65HVD232Q	3.3 V	None	None	None	–	-40°C to 125°C
SN65HVD233	3.3 V	Standby	Adjustable	None	Diagnostic Loopback	-40°C to 125°C
SN65HVD234	3.3 V	Standby and Sleep	Adjustable	None	–	-40°C to 125°C
SN65HVD235	3.3 V	Standby	Adjustable	None	Autobaud Loopback	-40°C to 125°C

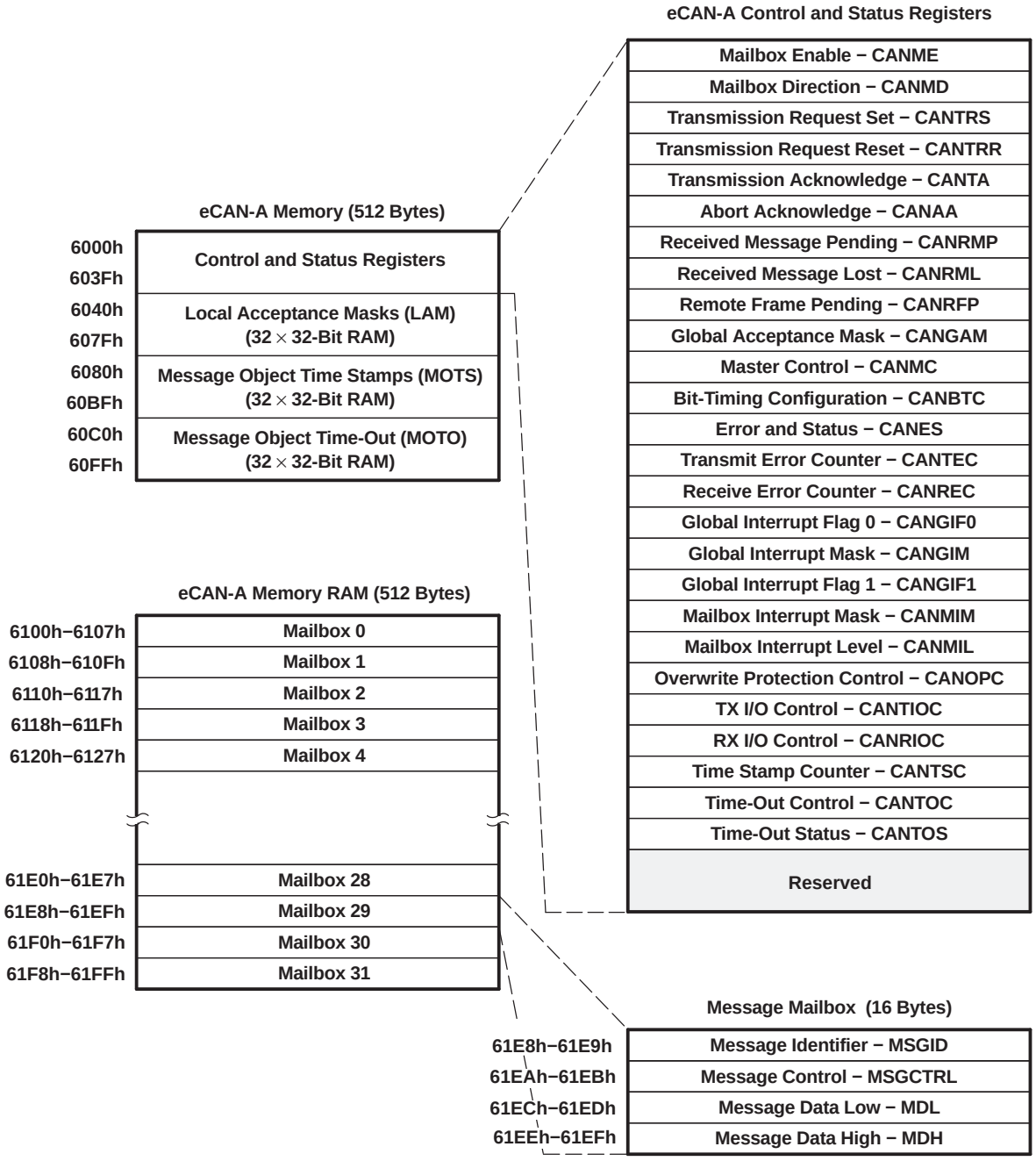


Figure 4-13. eCAN-A Memory Map

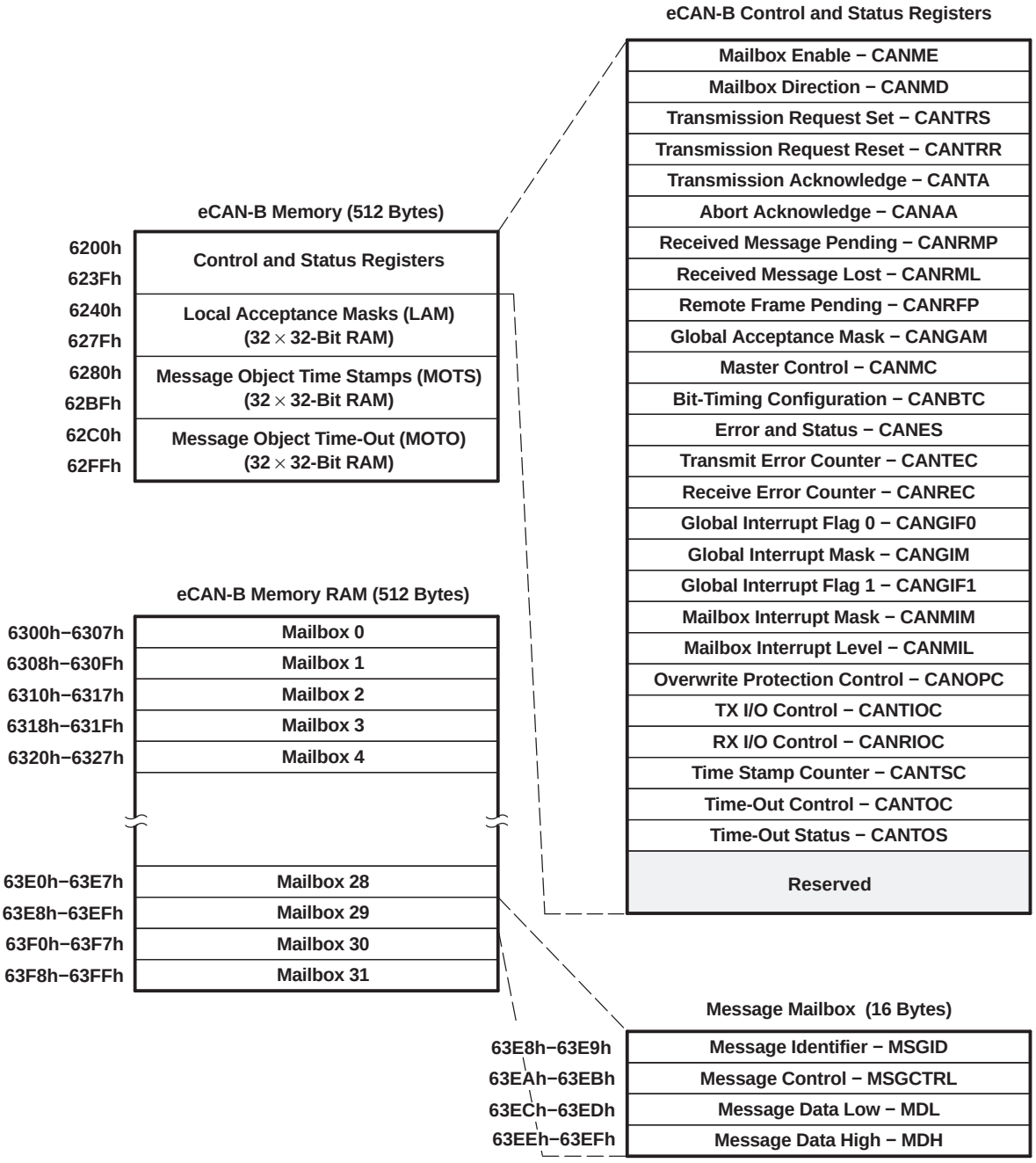


Figure 4-14. eCAN-B Memory Map

The CAN registers listed in Table 4-8 are used by the CPU to configure and control the CAN controller and the message objects. eCAN control registers only support 32-bit read/write operations. Mailbox RAM can be accessed as 16 bits or 32 bits. 32-bit accesses are aligned to an even boundary.

Table 4-8. CAN Register Map(1)

REGISTER NAME	ECAN-A ADDRESS	ECAN-B ADDRESS	SIZE (x32)	DESCRIPTION
CANME	0x6000	0x6200	1	Mailbox enable
CANMD	0x6002	0x6202	1	Mailbox direction
CANTRS	0x6004	0x6204	1	Transmit request set
CANTRR	0x6006	0x6206	1	Transmit request reset
CANTA	0x6008	0x6208	1	Transmission acknowledge
CANAA	0x600A	0x620A	1	Abort acknowledge
CANRMP	0x600C	0x620C	1	Receive message pending
CANRML	0x600E	0x620E	1	Receive message lost
CANRFP	0x6010	0x6210	1	Remote frame pending
CANGAM	0x6012	0x6212	1	Global acceptance mask
CANMC	0x6014	0x6214	1	Master control
CANBTC	0x6016	0x6216	1	Bit-timing configuration
CANES	0x6018	0x6218	1	Error and status
CANTEC	0x601A	0x621A	1	Transmit error counter
CANREC	0x601C	0x621C	1	Receive error counter
CANGIF0	0x601E	0x621E	1	Global interrupt flag 0
CANGIM	0x6020	0x6220	1	Global interrupt mask
CANGIF1	0x6022	0x6222	1	Global interrupt flag 1
CANMIM	0x6024	0x6224	1	Mailbox interrupt mask
CANMIL	0x6026	0x6226	1	Mailbox interrupt level
CANOPC	0x6028	0x6228	1	Overwrite protection control
CANTIOC	0x602A	0x622A	1	TX I/O control
CANRIOC	0x602C	0x622C	1	RX I/O control
CANTSC	0x602E	0x622E	1	Time stamp counter (Reserved in SCC mode)
CANTOC	0x6030	0x6230	1	Time-out control (Reserved in SCC mode)
CANTOS	0x6032	0x6232	1	Time-out status (Reserved in SCC mode)

(1) These registers are mapped to Peripheral Frame 1.

4.10 Serial Communications Interface (SCI) Modules (SCI-A, SCI-B, SCI-C)

The 2833x devices include three serial communications interface (SCI) modules. The SCI modules support digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format. The SCI receiver and transmitter are double-buffered, and each has its own separate enable and interrupt bits. Both can be operated independently or simultaneously in the full-duplex mode. To ensure data integrity, the SCI checks received data for break detection, parity, overrun, and framing errors. The bit rate is programmable to over 65000 different speeds through a 16-bit baud-select register.

Features of each SCI module include:

- Two external pins:
  - SCITXD: SCI transmit-output pin
  - SCIRXD: SCI receive-input pin

    NOTE: Both pins can be used as GPIO if not used for SCI.
  - Baud rate programmable to 64K different rates:

$$\text{Baud rate} = \frac{\text{LSPCLK}}{(\text{BRR} + 1) * 8} \quad \text{when BRR} \neq 0$$

$$\text{Baud rate} = \frac{\text{LSPCLK}}{16} \quad \text{when BRR} = 0$$

- Data-word format
  - One start bit
  - Data-word length programmable from one to eight bits
  - Optional even/odd/no parity bit
  - One or two stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wake-up multiprocessor modes: idle-line and address bit
- Half- or full-duplex operation
- Double-buffered receive and transmit functions
- Transmitter and receiver operations can be accomplished through interrupt-driven or polled algorithms with status flags.
  - Transmitter: TXRDY flag (transmitter-buffer register is ready to receive another character) and TX EMPTY flag (transmitter-shift register is empty)
  - Receiver: RXRDY flag (receiver-buffer register is ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR flag (monitoring four interrupt conditions)
- Separate enable bits for transmitter and receiver interrupts (except BRKDT)
- $\text{Max bit rate} = \frac{150\ \text{MHz}}{16} = 9.375 \times 10^6\ \text{b/s}$ (for 150-MHz devices)
- $\text{Max bit rate} = \frac{100\ \text{MHz}}{16} = 6.25 \times 10^6\ \text{b/s}$ (for 100-MHz devices)
- NRZ (non-return-to-zero) format
- Ten SCI module control registers located in the control register frame beginning at address 7050h

NOTE

All registers in this module are 8-bit registers that are connected to Peripheral Frame 2. When a register is accessed, the register data is in the lower byte (7-0), and the upper byte (15-8) is read as zeros. Writing to the upper byte has no effect.

Enhanced features:

- Auto baud-detect hardware logic

- 16-level transmit/receive FIFO

The SCI port operation is configured and controlled by the registers listed in Table 4-9, Table 4-10, and Table 4-11.

Table 4-9. SCI-A Registers(1)

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
SCICCRA	0x7050	1	SCI-A Communications Control Register
SCICTL1A	0x7051	1	SCI-A Control Register 1
SCIHBAUDA	0x7052	1	SCI-A Baud Register, High Bits
SCILBAUDA	0x7053	1	SCI-A Baud Register, Low Bits
SCICTL2A	0x7054	1	SCI-A Control Register 2
SCIRXSTA	0x7055	1	SCI-A Receive Status Register
SCIRXEMUA	0x7056	1	SCI-A Receive Emulation Data Buffer Register
SCIRXBUFA	0x7057	1	SCI-A Receive Data Buffer Register
SCITXBUFA	0x7059	1	SCI-A Transmit Data Buffer Register
SCIFFTXA(2)	0x705A	1	SCI-A FIFO Transmit Register
SCIFFRXA(2)	0x705B	1	SCI-A FIFO Receive Register
SCIFFCTA(2)	0x705C	1	SCI-A FIFO Control Register
SCIPRIA	0x705F	1	SCI-A Priority Control Register

(1) Registers in this table are mapped to Peripheral Frame 2 space. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.
(2) These registers are new registers for the FIFO mode.

Table 4-10. SCI-B Registers(1)(2)

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
SCICCRB	0x7750	1	SCI-B Communications Control Register
SCICTL1B	0x7751	1	SCI-B Control Register 1
SCIHBAUDB	0x7752	1	SCI-B Baud Register, High Bits
SCILBAUDB	0x7753	1	SCI-B Baud Register, Low Bits
SCICTL2B	0x7754	1	SCI-B Control Register 2
SCIRXSTB	0x7755	1	SCI-B Receive Status Register
SCIRXEMUB	0x7756	1	SCI-B Receive Emulation Data Buffer Register
SCIRXBUFB	0x7757	1	SCI-B Receive Data Buffer Register
SCITXBUFB	0x7759	1	SCI-B Transmit Data Buffer Register
SCIFFTXB(2)	0x775A	1	SCI-B FIFO Transmit Register
SCIFFRXB(2)	0x775B	1	SCI-B FIFO Receive Register
SCIFFCTB(2)	0x775C	1	SCI-B FIFO Control Register
SCIPRIB	0x775F	1	SCI-B Priority Control Register

(1) Registers in this table are mapped to peripheral bus 16 space. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.
(2) These registers are new registers for the FIFO mode.

Table 4-11. SCI-C Registers(1)(2)

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
SCICCRC	0x7770	1	SCI-C Communications Control Register
SCICTL1C	0x7771	1	SCI-C Control Register 1
SCIHBAUDC	0x7772	1	SCI-C Baud Register, High Bits
SCILBAUDC	0x7773	1	SCI-C Baud Register, Low Bits
SCICTL2C	0x7774	1	SCI-C Control Register 2
SCIRXSTC	0x7775	1	SCI-C Receive Status Register
SCIRXEMUC	0x7776	1	SCI-C Receive Emulation Data Buffer Register
SCIRXBUFC	0x7777	1	SCI-C Receive Data Buffer Register
SCITXBUFC	0x7779	1	SCI-C Transmit Data Buffer Register
SCIFFTXC(2)	0x777A	1	SCI-C FIFO Transmit Register
SCIFFRXC(2)	0x777B	1	SCI-C FIFO Receive Register
SCIFFCTC(2)	0x777C	1	SCI-C FIFO Control Register
SCIPRC	0x777F	1	SCI-C Priority Control Register

(1) Registers in this table are mapped to peripheral bus 16 space. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.
(2) These registers are new registers for the FIFO mode.

Figure 4-15 shows the SCI module block diagram.

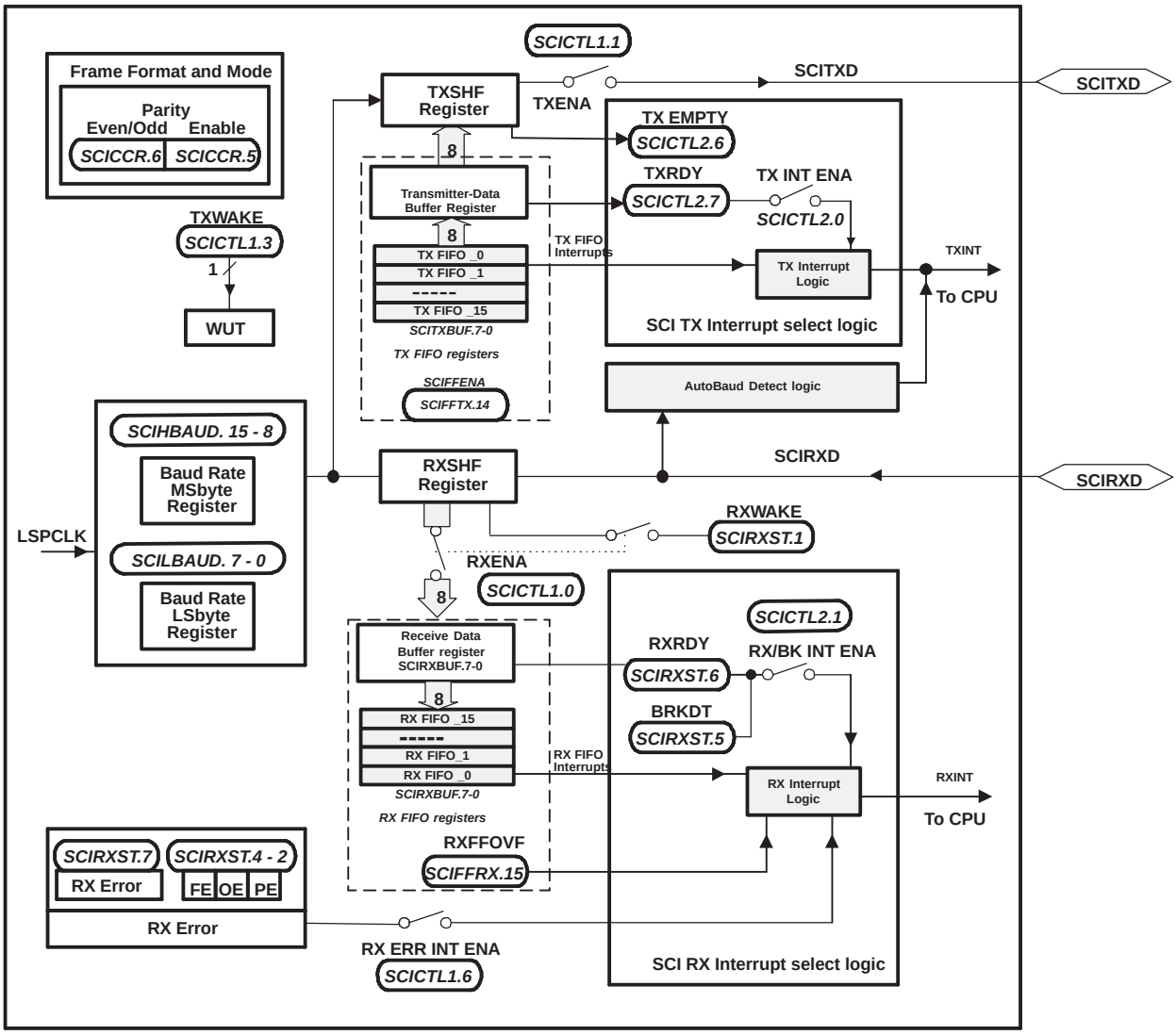


Figure 4-15. Serial Communications Interface (SCI) Module Block Diagram

4.11 Serial Peripheral Interface (SPI) Module (SPI-A)

The 2833x devices include the four-pin serial peripheral interface (SPI) module. One SPI module (SPI-A) is available. The SPI is a high-speed, synchronous serial I/O port that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmable bit-transfer rate. Normally, the SPI is used for communications between the DSC controller and external peripherals or another processor. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and ADCs. Multidevice communications are supported by the master/slave operation of the SPI.

The SPI module features include:

- Four external pins:
  - SPISOMI: SPI slave-output/master-input pin
  - SPISIMO: SPI slave-input/master-output pin
  - $\overline{\text{SPISTE}}$: SPI slave transmit-enable pin
  - SPICLK: SPI serial-clock pin

NOTE: All four pins can be used as GPIO, if the SPI module is not used.

- Two operational modes: master and slave

  Baud rate: 125 different programmable rates.

$$\text{Baud rate} = \frac{\text{LSPCLK}}{(\text{SPIBRR} + 1)} \quad \text{when SPIBRR = 3 to 127}$$

$$\text{Baud rate} = \frac{\text{LSPCLK}}{4} \quad \text{when SPIBRR = 0,1, 2}$$

- Data word length: one to sixteen data bits
- Four clocking schemes (controlled by clock polarity and clock phase bits) include:
  - Falling edge without phase delay: SPICLK active-high. SPI transmits data on the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
  - Falling edge with phase delay: SPICLK active-high. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge without phase delay: SPICLK inactive-low. SPI transmits data on the rising edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge with phase delay: SPICLK inactive-low. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
- Simultaneous receive and transmit operation (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt-driven or polled algorithms.
- Nine SPI module control registers: Located in control register frame beginning at address 7040h.

NOTE

All registers in this module are 16-bit registers that are connected to Peripheral Frame 2. When a register is accessed, the register data is in the lower byte (7-0), and the upper byte (15-8) is read as zeros. Writing to the upper byte has no effect.

Enhanced feature:

- 16-level transmit/receive FIFO
- Delayed transmit control

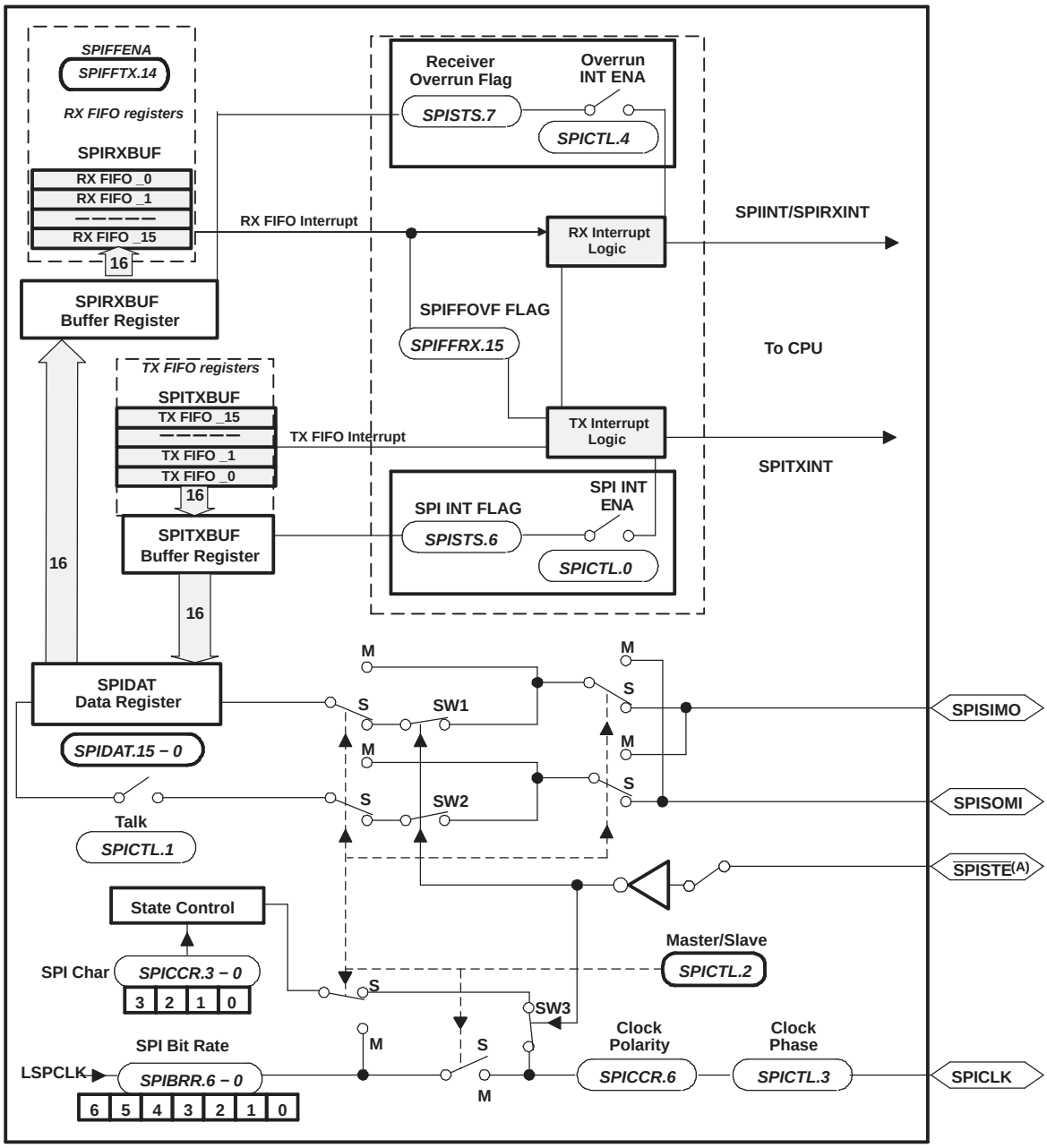
The SPI port operation is configured and controlled by the registers listed in Table 4-12.

Table 4-12. SPI-A Registers

NAME	ADDRESS	SIZE (X16)	DESCRIPTION(1)
SPICCR	0x7040	1	SPI-A Configuration Control Register
SPICTL	0x7041	1	SPI-A Operation Control Register
SPISTS	0x7042	1	SPI-A Status Register
SPIBRR	0x7044	1	SPI-A Baud Rate Register
SPIRXEMU	0x7046	1	SPI-A Receive Emulation Buffer Register
SPIRXBUF	0x7047	1	SPI-A Serial Input Buffer Register
SPITXBUF	0x7048	1	SPI-A Serial Output Buffer Register
SPIDAT	0x7049	1	SPI-A Serial Data Register
SPIFFTX	0x704A	1	SPI-A FIFO Transmit Register
SPIFFRX	0x704B	1	SPI-A FIFO Receive Register
SPIFFCT	0x704C	1	SPI-A FIFO Control Register
SPIPRI	0x704F	1	SPI-A Priority Control Register

(1) Registers in this table are mapped to Peripheral Frame 2. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.

Figure 4-16 is a block diagram of the SPI in slave mode.



A. $\overline{\text{SPISTE}}$ is driven low by the master for a slave device.

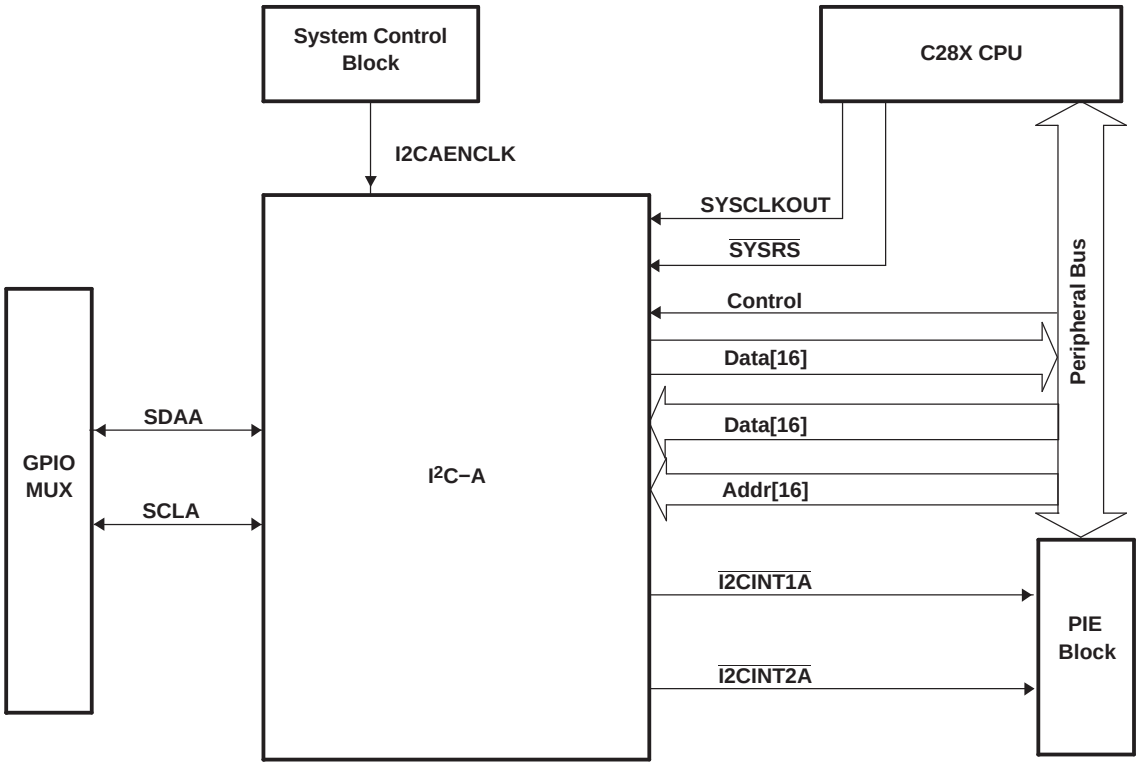
Figure 4-16. SPI Module Block Diagram (Slave Mode)

4.12 Inter-Integrated Circuit (I2C)

The 2833x device contains one I2C Serial Port. Figure 4-15 shows how the I2C peripheral module interfaces within the 2833x device.

The I2C module has the following features:

- Compliance with the Philips Semiconductors I2C-bus specification (version 2.1):
  - Support for 1-bit to 8-bit format transfers
  - 7-bit and 10-bit addressing modes
  - General call
  - START byte mode
  - Support for multiple master-transmitters and slave-receivers
  - Support for multiple slave-transmitters and master-receivers
  - Combined master transmit/receive and receive/transmit mode
  - Data transfer rate of from 10 kbps up to 400 kbps (Philips Fast-mode rate)
- One 16-bit receive FIFO and one 16-bit transmit FIFO
- One interrupt that can be used by the CPU. This interrupt can be generated as a result of one of the following conditions:
  - Transmit-data ready
  - Receive-data ready
  - Register-access ready
  - No-acknowledgment received
  - Arbitration lost
  - Stop condition detected
  - Addressed as slave
- An additional interrupt that can be used by the CPU when in FIFO mode
- Module enable/disable capability
- Free data format mode



A. The I2C registers are accessed at the SYSCLKOUT rate. The internal timing and signal waveforms of the I2C port are also at the SYSCLKOUT rate.

B. The clock enable bit (I2CAENCLK) in the PCLKCRO register turns off the clock to the I2C port for low power operation. Upon reset, I2CAENCLK is clear, which indicates the peripheral internal clocks are off.

Figure 4-17. I2C Peripheral Module Interfaces

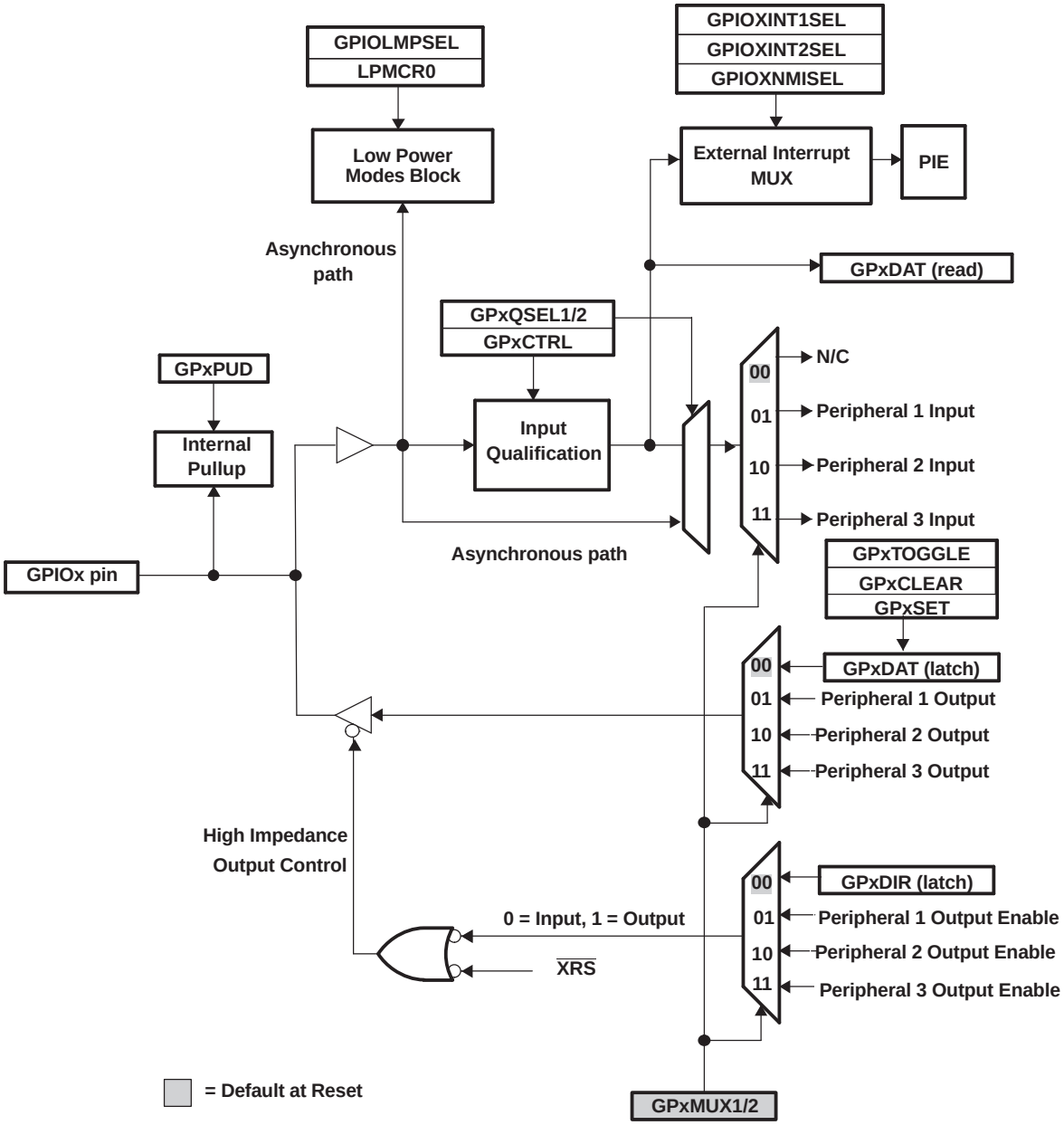
The registers in Table 4-13 configure and control the I2C port operation.

Table 4-13. I2C-A Registers

NAME	ADDRESS	DESCRIPTION
I2COAR	0x7900	I2C own address register
I2CIER	0x7901	I2C interrupt enable register
I2CSTR	0x7902	I2C status register
I2CCLKL	0x7903	I2C clock low-time divider register
I2CCLKH	0x7904	I2C clock high-time divider register
I2CCNT	0x7905	I2C data count register
I2CDRR	0x7906	I2C data receive register
I2CSAR	0x7907	I2C slave address register
I2CDXR	0x7908	I2C data transmit register
I2CMDR	0x7909	I2C mode register
I2CISRC	0x790A	I2C interrupt source register
I2CPSC	0x790C	I2C prescaler register
I2CFFTX	0x7920	I2C FIFO transmit register
I2CFFRX	0x7921	I2C FIFO receive register
I2CRSR	-	I2C receive shift register (not accessible to the CPU)
I2CXSR	-	I2C transmit shift register (not accessible to the CPU)

4.13 GPIO MUX

On the 2833x devices, the GPIO MUX can multiplex up to three independent peripheral signals on a single GPIO pin in addition to providing individual pin bit-banging IO capability. The GPIO MUX block diagram per pin is shown in Figure 4-18. Because of the open drain capabilities of the I2C pins, the GPIO MUX block diagram for these pins differ. See the *TMS320x280x, 2801x, 2804x System Control and Interrupts Reference Guide* (literature number SPRU712) for details.



A. x stands for the port, either A or B. For example, GPxDIR refers to either the GPADIR and GPBDIR register depending on the particular GPIO pin selected.

B. GPxDAT latch/read are accessed at the same memory location.

Figure 4-18. GPIO MUX Block Diagram

The 2833x supports 88 GPIO pins. The GPIO control and data registers are mapped to Peripheral Frame 1 to enable 32-bit operations on the registers (along with 16-bit operations). Table 4-14 shows the GPIO register mapping.

Table 4-14. GPIO Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
GPIO CONTROL REGISTERS (EALLOW PROTECTED)			
GPACTRL	0x6F80	2	GPIO A Control Register (GPIO0 to 31)
GPAQSEL1	0x6F82	2	GPIO A Qualifier Select 1 Register (GPIO0 to 15)
GPAQSEL2	0x6F84	2	GPIO A Qualifier Select 2 Register (GPIO16 to 31)
GPAMUX1	0x6F86	2	GPIO A MUX 1 Register (GPIO0 to 15)
GPAMUX2	0x6F88	2	GPIO A MUX 2 Register (GPIO16 to 31)
GPADIR	0x6F8A	2	GPIO A Direction Register (GPIO0 to 31)
GPAPUD	0x6F8C	2	GPIO A Pull Up Disable Register (GPIO0 to 31)
reserved	0x6F8E 0x6F8F	2	
GPBCTRL	0x6F90	2	GPIO B Control Register (GPIO32 to 35)
GPBQSEL1	0x6F92	2	GPIO B Qualifier Select 1 Register (GPIO32 to 35)
GPBQSEL2	0x6F94	2	reserved
GPBMUX1	0x6F96	2	GPIO B MUX 1 Register (GPIO32 to 35)
GPBMUX2	0x6F98	2	reserved
GPBDIR	0x6F9A	2	GPIO B Direction Register (GPIO32 to 35)
GPBPUD	0x6F9C	2	GPIO B Pull Up Disable Register (GPIO32 to 35)
reserved	0x6F9E 0x6F9F	2	reserved
reserved	0x6FA0 0x6FBF	32	
GPIO DATA REGISTERS (NOT EALLOW PROTECTED)			
GPADAT	0x6FC0	2	GPIO Data Register (GPIO0 to 31)
GPASET	0x6FC2	2	GPIO Data Set Register (GPIO0 to 31)
GPACLEAR	0x6FC4	2	GPIO Data Clear Register (GPIO0 to 31)
GPATOGGLE	0x6FC6	2	GPIO Data Toggle Register (GPIO0 to 31)
GPBDAT	0x6FC8	2	GPIO Data Register (GPIO32 to 35)
GPBSET	0x6FCA	2	GPIO Data Set Register (GPIO32 to 35)
GPBCLEAR	0x6FCC	2	GPIO Data Clear Register (GPIO32 to 35)
GPBTOGGLE	0x6FCE	2	GPIO Data Toggle Register (GPIO32 to 35)
reserved	0x6FD0 0x6FDF	16	
GPIO INTERRUPT AND LOW POWER MODES SELECT REGISTERS (EALLOW PROTECTED)			
GPIOXINT1SEL	0x6FE0	1	XINT1 GPIO Input Select Register (GPIO0 to 31)
GPIOXINT2SEL	0x6FE1	1	XINT2 GPIO Input Select Register (GPIO0 to 31)
GPIOXNMISEL	0x6FE2	1	XNMI GPIO Input Select Register (GPIO0 to 31)
reserved	0x6FE3 0x6FE7	5	
GPIOLPMSEL	0x6FE8	2	LPM GPIO Select Register (GPIO0 to 31)
reserved	0x6FEA 0x6FFF	22	

Table 4-15. GPIO-A Mux Peripheral Selection Matrix

REGISTER BITS		PERIPHERAL SELECTION				
GPADIR GPADAT GPASET GPACLR GPATOGGLE		**GPAMUX1 GPAQSEL1**	**GPIOx GPAMUX1=0,0**	**PER1 GPAMUX1 = 0, 1**	**PER2 GPAMUX1 = 1, 0**	**PER3 GPAMUX1 = 1, 1**
Q	0	1, 0	GPIO0 (I/O)	EPWM1A (O)		
U	1	3, 2	GPIO1 (I/O)	EPWM1B (O)	ECAP6 (I/O)	MFSRB (I/O)
A	2	5, 4	GPIO2 (I/O)	EPWM2A (O)		
L	3	7, 6	GPIO3 (I/O)	EPWM2B (O)	ECAP5 (I/O)	MCLKRB (I/O)
P	4	9, 8	GPIO4 (I/O)	EPWM3A (O)		
R	5	11, 10	GPIO5 (I/O)	EPWM3B (O)	MFSRA (I/O)	ECAP1 (I/O)
D	6	13, 12	GPIO6 (I/O)	EPWM4A (O)	EPWMSYNCI (I)	EPWMSYNCO (O)
0	7	15, 14	GPIO7 (I/O)	EPWM4B (O)	MCLKRA (I/O)	ECAP2 (I/O)
Q	8	17, 16	GPIO8 (I/O)	EPWM5A (O)	CANTXB (O)	$\overline{\text{ADCSOCAO}}$ (O)
U	9	19, 18	GPIO9 (I/O)	EPWM5B (O)	SCITXDB (O)	ECAP3 (I/O)
A	10	21, 20	GPIO10 (I/O)	EPWM6A (O)	CANRXB (I)	$\overline{\text{ADCSOCBO}}$ (O)
L	11	23, 22	GPIO11 (I/O)	EPWM6B (O)	SCIRXDB (I)	ECAP4 (I/O)
P	12	25, 24	GPIO12 (I/O)	$\overline{\text{TZ1}}$ (I)	CANTXB (O)	MDXB (O)
R	13	27, 26	GPIO13 (I/O)	$\overline{\text{TZ2}}$ (I)	CANRXB (I)	MDRB (I)
D	14	29, 28	GPIO14 (I/O)	$\overline{\text{TZ3}}$ (I)/$\overline{\text{XHOLD}}$ (I)	SCITXDB (O)	MCLKXB (I/O)
1	15	31, 30	GPIO15 (I/O)	$\overline{\text{TZ4}}$ (I)/$\overline{\text{XHOLDA}}$ (O)	SCIRXDB (I)	MFSXB (I/O)
		GPAMUX2				
		GPAQSEL2	**GPAMUX2 =0, 0**	**GPAMUX2 = 0, 1**	**GPAMUX2 = 1, 0**	**GPAMUX2 = 1, 1**
Q	16	1, 0	GPIO16 (I/O)	SPISIMOA (I/O)	CANTXB (O)	$\overline{\text{TZ5}}$ (I)
U	17	3, 2	GPIO17 (I/O)	SPISOMIA (I/O)	CANRXB (I)	$\overline{\text{TZ6}}$ (I)
A	18	5, 4	GPIO18 (I/O)	SPICLKA (I/O)	SCITXDB (O)	CANRXA (I)
L	19	7, 6	GPIO19 (I/O)	SPISTEA (I/O)	SCIRXDB (I)	CANTXA (O)
P	20	9, 8	GPIO20 (I/O)	EQEP1A (I)	MDXA (O)	CANTXB (O)
R	21	11, 10	GPIO21 (I/O)	EQEP1B (I)	MDRA (I)	CANRXB (I)
D	22	13, 12	GPIO22 (I/O)	EQEP1S (I/O)	MCLKXA (I/O)	SCITXDB (O)
2	23	15, 14	GPIO23 (I/O)	EQEP1I (I/O)	MFSXA (I/O)	SCIRXDB (I)
Q	24	17, 16	GPIO24 (I/O)	ECAP1 (I/O)	EQEP2A (I)	MDXB (O)
U	25	19, 18	GPIO25 (I/O)	ECAP2 (I/O)	EQEP2B (I)	MDRB (I)
A	26	21, 20	GPIO26 (I/O)	ECAP3 (I/O)	EQEP2I (I/O)	MCLKXB (I/O)
L	27	23, 22	GPIO27 (I/O)	ECAP4 (I/O)	EQEP2S (I/O)	MFSXB (I/O)
P	28	25, 24	GPIO28 (I/O)	SCIRXDA (I)	$\overline{\text{XZCS6}}$ (O)	
R	29	27, 26	GPIO29 (I/O)	SCITXDA (O)	XA19 (O)	
D	30	29, 28	GPIO30 (I/O)	CANRXA (I)	XA18 (O)	
3	31	31, 30	GPIO31 (I/O)	CANTXA (O)	XA17 (O)	

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Table 4-16. GPIO-B Mux Peripheral Selection Matrix

REGISTER BITS		PERIPHERAL SELECTION				
GPBDIR GPBDAT GPBSET GPBCLR GPBTOGGLE		**GPBMUX1 GPBQSEL1**	**GPIOx GPBMUX1=0, 0**	**PER1 GPBMUX1 = 0, 1**	**PER2 GPBMUX1 = 1, 0**	**PER3 GPBMUX1 = 1, 1**
Q	0	1, 0	GPIO32 (I/O)	SDAA (I/OC)(1)	EPWMSYNCI (I)	$\overline{\text{ADCSOCAO}}$ (O)
U	1	3, 2	GPIO33 (I/O)	SCLA (I/OC)(1)	EPWMSYNCO (O)	$\overline{\text{ADCSOCBO}}$ (O)
A	2	5, 4	GPIO34 (I/O)	ECAP1 (I/O)	XREADY (I)	
L	3	7, 6	GPIO35 (I/O)	SCITXDA (O)	XR/$\overline{\text{W}}$ (O)	
P	4	9, 8	GPIO36 (I/O)	SCIRXDA (I)	$\overline{\text{XZCS0}}$ (O)	
R	5	11, 10	GPIO37 (I/O)	ECAP2 (I/O)	$\overline{\text{XZCS7}}$ (O)	
D	6	13, 12	GPIO38 (I/O)		$\overline{\text{XWE0}}$ (O)	
0	7	15, 14	GPIO39 (I/O)		XA16 (O)	
Q	8	17, 16	GPIO40 (I/O)		XA0/$\overline{\text{XWE1}}$ (O)	
U	9	19, 18	GPIO41 (I/O)		XA1 (O)	
A	10	21, 20	GPIO42 (I/O)		XA2 (O)	
L	11	23, 22	GPIO43 (I/O)		XA3 (O)	
P	12	25, 24	GPIO44 (I/O)		XA4 (O)	
R	13	27, 26	GPIO45 (I/O)		XA5 (O)	
D	14	29, 28	GPIO46 (I/O)		XA6 (O)	
1	15	31, 30	GPIO47 (I/O)		XA7 (O)	
		GPBMUX2 GPBQSEL2	**GPBMUX2 =0, 0**	**GPBMUX2 = 0, 1**	**GPBMUX2 = 1, 0**	**GPBMUX2 = 1, 1**
Q	16	1, 0	GPIO48 (I/O)	ECAP5 (I/O)	XD31 (I/O)	
U	17	3, 2	GPIO49 (I/O)	ECAP6 (I/O)	XD30 (I/O)	
A	18	5, 4	GPIO50 (I/O)	EQEP1A (I)	XD29 (I/O)	
L	19	7, 6	GPIO51 (I/O)	EQEP1B (I)	XD28 (I/O)	
P	20	9, 8	GPIO52 (I/O)	EQEP1S (I/O)	XD27 (I/O)	
R	21	11, 10	GPIO53 (I/O)	EQEP1I (I/O)	XD26 (I/O)	
D	22	13, 12	GPIO54 (I/O)	SPISIMOA (I/O)	XD25 (I/O)	
2	23	15, 14	GPIO55 (I/O)	SPISOMIA (I/O)	XD24 (I/O)	
Q	24	17, 16	GPIO56 (I/O)	SPICLKA (I/O)	XD23 (I/O)	
U	25	19, 18	GPIO57 (I/O)	$\overline{\text{SPISTEA}}$ (I/O)	XD22 (I/O)	
A	26	21, 20	GPIO58 (I/O)	MCLKRA (I/O)	XD21 (I/O)	
L	27	23, 22	GPIO59 (I/O)	MFSRA (I/O)	XD20 (I/O)	
P	28	25, 24	GPIO60 (I/O)	MCLKRB (I/O)	XD19 (I/O)	
R	29	27, 26	GPIO61 (I/O)	MFSRB (I/O)	XD18 (I/O)	
D	30	29, 28	GPIO62 (I/O)	SCIRXDC (I)	XD17 (I/O)	
3	31	31, 30	GPIO63 (I/O)	SCITXDC (O)	XD16 (I/O)	

(1) Open drain

Table 4-17. GPIO-C Mux Peripheral Selection Matrix

REGISTER BITS		PERIPHERAL SELECTION		
GPCDIR GPCDAT GPCSET GPCCLR GPCTOGGLE		GPCMUX1	GPIOx or PER1 GPCMUX1 = 0, 0 or 0, 1	PER2 or PER3 GPCMUX1 = 1, 0 or 1, 1
no	0	1, 0	GPIO64 (I/O)	XD15 (I/O)
	1	3, 2	GPIO65 (I/O)	XD14 (I/O)
qu	2	5, 4	GPIO66 (I/O)	XD13 (I/O)
a	3	7, 6	GPIO67 (I/O)	XD12 (I/O)
l	4	9, 8	GPIO68 (I/O)	XD11 (I/O)
	5	11, 10	GPIO69 (I/O)	XD10 (I/O)
	6	13, 12	GPIO70 (I/O)	XD9 (I/O)
	7	15, 14	GPIO71 (I/O)	XD8 (I/O)
no	8	17, 16	GPIO72 (I/O)	XD7 (I/O)
	9	19, 18	GPIO73 (I/O)	XD6 (I/O)
qu	10	21, 20	GPIO74 (I/O)	XD5 (I/O)
a	11	23, 22	GPIO75 (I/O)	XD4 (I/O)
l	12	25, 24	GPIO76 (I/O)	XD3 (I/O)
	13	27, 26	GPIO77 (I/O)	XD2 (I/O)
	14	29, 28	GPIO78 (I/O)	XD1 (I/O)
	15	31, 30	GPIO79 (I/O)	XD0 (I/O)
		GPCMUX2	GPCMUX2 = 0, 0 or 0, 1	GPCMUX2 = 1, 0 or 1, 1
no	16	1, 0	GPIO80 (I/O)	XA8 (O)
	17	3, 2	GPIO81 (I/O)	XA9 (O)
qu	18	5, 4	GPIO82 (I/O)	XA10 (O)
a	19	7, 6	GPIO83 (I/O)	XA11 (O)
l	20	9, 8	GPIO84 (I/O)	XA12 (O)
	21	11, 10	GPIO85 (I/O)	XA13 (O)
	22	13, 12	GPIO86 (I/O)	XA14 (O)
	23	15, 14	GPIO87 (I/O)	XA15 (O)

The user can select the type of input qualification for each GPIO pin via the GPxQSEL1/2 registers from four choices:

- Synchronization To SYSCLKOUT Only (GPxQSEL1/2=0, 0): This is the default mode of all GPIO pins at reset and it simply synchronizes the input signal to the system clock (SYSCLKOUT).
- Qualification Using Sampling Window (GPxQSEL1/2=0, 1 and 1, 0): In this mode the input signal, after synchronization to the system clock (SYSCLKOUT), is qualified by a specified number of cycles before the input is allowed to change.

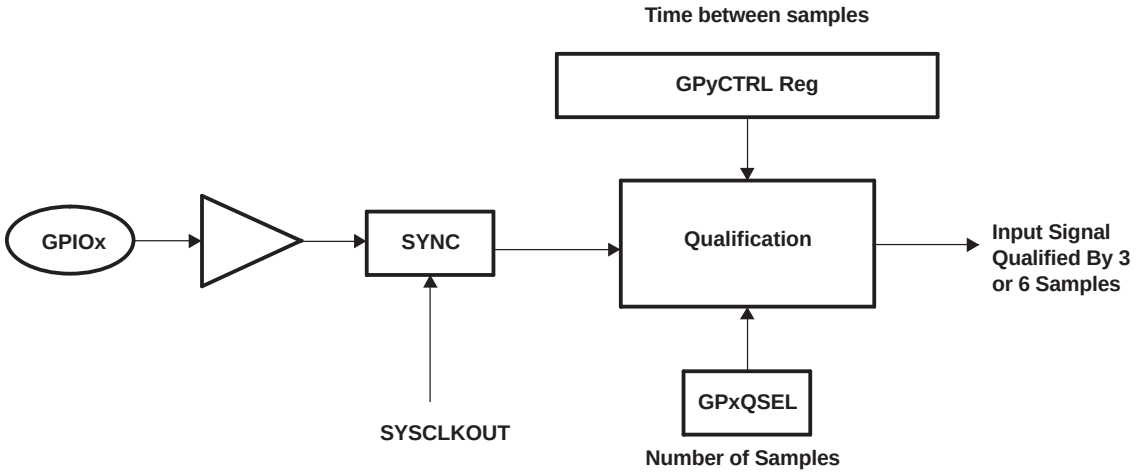


Figure 4-19. Qualification Using Sampling Window

- The sampling period is specified by the QUALPRD bits in the GPxCTRL register and is configurable in groups of 8 signals. It specifies a multiple of SYSCLKOUT cycles for sampling the input signal. The sampling window is either 3-samples or 6-samples wide and the output is only changed when ALL samples are the same (all 0s or all 1s) as shown in Figure 4-18 (for 6 sample mode).
- No Synchronization (GPxQSEL1/2=1,1): This mode is used for peripherals where synchronization is not required (synchronization is performed within the peripheral).

Due to the multi-level multiplexing that is required on the 2833x device, there may be cases where a peripheral input signal can be mapped to more then one GPIO pin. Also, when an input signal is not selected, the input signal will default to either a 0 or 1 state, depending on the peripheral.

5 Device Support

Texas Instruments (TI) offers an extensive line of development tools for the C28x™ generation of DSCs, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

The following products support development of 2833x-based applications:

Software Development Tools

- Code Composer Studio™ Integrated Development Environment (IDE)
  - C/C++ Compiler
  - Code generation tools
  - Assembler/Linker
  - Cycle Accurate Simulator
- Application algorithms
- Sample applications code

Hardware Development Tools

- 2833x development board
- Evaluation modules
- JTAG-based emulators - SPI515, XDS510PP, XDS510PP Plus, XDS510USB
- Universal 5-V dc power supply
- Documentation and cables

5.1 Device and Development Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all TMS320™ DSC devices and support tools. Each TMS320™ DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (e.g., **TMS**320F28335). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification

TMS Fully qualified production device

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing

TMDS Fully qualified development-support product

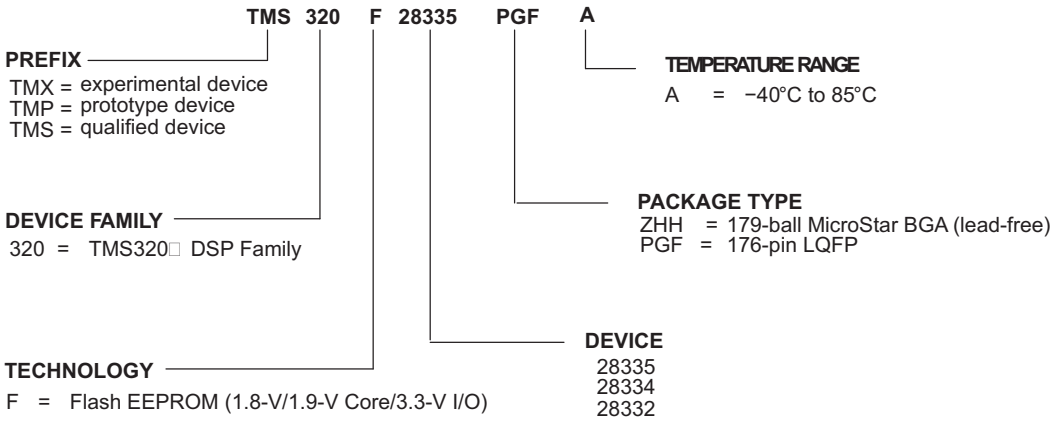
TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:
"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

PRODUCT PREVIEW

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PBK) and temperature range (for example, A). Figure 5-1 provides a legend for reading the complete device name for any family member.



BGA = Ball Grid Array
LQFP = Low-Profile Quad Flatpack

LQFP package not yet available lead (Pb)-free. For estimated conversion dates, go to www.ti.com/leadfree

Figure 5-1. Example of 2833x Device Nomenclature

5.2 Documentation Support

Extensive documentation supports all of the TMS320™ DSP family generations of devices from product announcement through applications development. The types of documentation available include: data sheets and data manuals, with design specifications; and hardware and software applications. Useful reference documentation includes:

CPU User's Guides

SPRU430 TMS320C28x DSP CPU and Instruction Set Reference Guide describes the central processing unit (CPU) and the assembly language instructions of the TMS320C28x fixed-point digital signal processors (DSPs). It also describes emulation features available on these DSPs.

SPRUEO2 TMS320C28x Floating Point Unit and Instruction Set Reference Guide describes the floating-point unit and includes the instructions for the FPU.

Peripheral Guides

SPRU566 TMS320x28xx, 28xxx Peripheral Reference Guide describes the peripheral reference guides of the 28x digital signal processors (DSPs).

SPRU716 TMS320x280x, 2801x, 2804x Analog-to-Digital Converter (ADC) Reference Guide describes how to configure and use the on-chip ADC module, which is a 12-bit pipelined ADC.

SPRU791 TMS320x28xx, 28xxx Enhanced Pulse Width Modulator (ePWM) Module Reference Guide describes the main areas of the enhanced pulse width modulator that include digital motor control, switch mode power supply control, UPS (uninterruptible power supplies), and other forms of power conversion

SPRU924 TMS320x28xx, 28xxx High-Resolution Pulse Width Modulator (HRPWM) describes the operation of the high-resolution extension to the pulse width modulator (HRPWM)

SPRU807 TMS320x28xx, 28xxx Enhanced Capture (eCAP) Module Reference Guide describes the enhanced capture module. It includes the module description and registers.

SPRU790 TMS320x28xx, 28xxx Enhanced Quadrature Encoder Pulse (eQEP) Reference Guide describes the eQEP module, which is used for interfacing with a linear or rotary incremental encoder to get position, direction, and speed information from a rotating machine in high performance motion and position control systems. It includes the module description and registers

SPRU074 TMS320x28xx, 28xxx Enhanced Controller Area Network (eCAN) Reference Guide describes the eCAN that uses established protocol to communicate serially with other controllers in electrically noisy environments.

SPRU051 TMS320x28xx, 28xxx Serial Communication Interface (SCI) Reference Guide describes the SCI, which is a two-wire asynchronous serial port, commonly known as a UART. The SCI modules support digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format.

SPRU059 TMS320x28xx, 28xxx Serial Peripheral Interface (SPI) Reference Guide describes the SPI - a high-speed synchronous serial input/output (I/O) port - that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmed bit-transfer rate.

SPRU721 TMS320x28xx, 28xxx Inter-Integrated Circuit (I2C) Reference Guide describes the features and operation of the inter-integrated circuit (I2C) module that is available on the TMS320x280x digital signal processor (DSP).

Tools Guides

SPRU513 TMS320C28x Assembly Language Tools User's Guide describes the assembly language tools (assembler and other tools used to develop assembly language code), assembler

directives, macros, common object file format, and symbolic debugging directives for the TMS320C28x device.

SPRU514 TMS320C28x Optimizing C Compiler User's Guide describes the TMS320C28x™ C/C++ compiler. This compiler accepts ANSI standard C/C++ source code and produces TMS320 DSP assembly language source code for the TMS320C28x device.

SPRU608 The TMS320C28x Instruction Set Simulator Technical Overview describes the simulator, available within the Code Composer Studio for TMS320C2000 IDE, that simulates the instruction set of the C28x™ core.

SPRU625 TMS320C28x DSP/BIOS Application Programming Interface (API) Reference Guide describes development using DSP/BIOS.

Application Reports

SPRAAM0 Getting Started With TMS320C28x™ Digital Signal Controllers is organized by development flow and functional areas to make your design effort as seamless as possible. Tips on getting started with C28x™ DSP software and hardware development are provided to aid in your initial design and debug efforts. Each section includes pointers to valuable information including technical documentation, software, and tools for use in each phase of design.

SPRAAD5 Power Line Communication for Lighting Apps using BPSK w/ a Single DSP Controller presents a complete implementation of a power line modem following CEA-709 protocol using a single DSP.

SPRAA85 Programming TMS320x28xx and 28xxx Peripherals in C/C++ explores a hardware abstraction layer implementation to make C/C++ coding easier on 28x DSPs. This method is compared to traditional #define macros and topics of code efficiency and special case registers are also addressed.

SPRA958 Running an Application from Internal Flash Memory on the TMS320F28xx DSP covers the requirements needed to properly configure application software for execution from on-chip flash memory. Requirements for both DSP/BIOS™ and non-DSP/BIOS projects are presented. Example code projects are included.

SPRAA91 TMS320F280x DSC USB Connectivity Using TUSB3410 USB-to-UART Bridge Chip presents hardware connections as well as software preparation and operation of the development system using a simple communication echo program.

SPRAA58 TMS320x281x to TMS320x280x Migration Overview describes differences between the Texas Instruments TMS320x281x and TMS320x280x DSPs to assist in application migration from the 281x to the 280x. While the main focus of this document is migration from 281x to 280x, users considering migrating in the reverse direction (280x to 281x) will also find this document useful.

SPRAAD8 TMS320280x and TMS320F2801x ADC Calibration describes a method for improving the absolute accuracy of the 12-bit ADC found on the TMS320280x and TMS3202801x devices. Inherent gain and offset errors affect the absolute accuracy of the ADC. The methods described in this report can improve the absolute accuracy of the ADC to levels better than 0.5%. This application report has an option to download an example program that executes from RAM on the F2808 EzDSP.

SPRAAI1 Using Enhanced Pulse Width Modulator (ePWM) Module for 0-100% Duty Cycle Control provides a guide for the use of the ePWM module to provide 0% to 100% duty cycle control and is applicable to the TMS320x280x family of processors.

SPRAA88 Using PWM Output as a Digital-to-Analog Converter on a TMS320F280x presents a method for utilizing the on-chip pulse width modulated (PWM) signal generators on the TMS320F280x family of digital signal controllers as a digital-to-analog converter (DAC).

SPRAAH1 Using the Enhanced Quadrature Encoder Pulse (eQEP) Module provides a guide for the use of the eQEP module as a dedicated capture unit and is applicable to the TMS320x280x, 28xxx family of processors.

SPRA820 Online Stack Overflow Detection on the TMS320C28x DSP presents the methodology for online stack overflow detection on the TMS320C28x™ DSP. C-source code is provided that contains functions for implementing the overflow detection on both DSP/BIOS™ and non-DSP/BIOS applications.

SPRA806 An Easy Way of Creating a C-callable Assembly Function for the TMS320C28x DSP provides instructions and suggestions to configure the C compiler to assist with understanding of parameter-passing conventions and environments expected by the C compiler.

A series of DSP textbooks is published by Prentice-Hall and John Wiley & Sons to support digital signal processing research and education. The TMS320 DSP newsletter, *Details on Signal Processing*, is published quarterly and distributed to update TMS320 DSP customers on product information.

Updated information on the TMS320 DSP controllers can be found on the worldwide web at: **http://www.ti.com**.

To send comments regarding this data manual (literature number SPRS230), use the *comments@books.sc.ti.com* email address, which is a repository for feedback. For questions and support, contact the Product Information Center listed at the **http://www.ti.com/sc/docs/pic/home.htm** site.

6 Electrical Specifications

This section provides the absolute maximum ratings and the recommended operating conditions.

6.1 Absolute Maximum Ratings[1][2]

Unless otherwise noted, the list of absolute maximum ratings are specified over operating temperature ranges.

Supply voltage range, V_{DDIO}, V_{DD3VFL}	with respect to V_{SS}	- 0.3 V to 4.6 V
Supply voltage range, V_{DDA2}, V_{DDAIO}	with respect to V_{SSA}	- 0.3 V to 4.6 V
Supply voltage range, V_{DD}	with respect to V_{SS}	- 0.3 V to 2.5 V
Supply voltage range, V_{DD1A18}, V_{DD2A18}	with respect to V_{SSA}	- 0.3 V to 2.5 V
Supply voltage range, V_{SSA2}, V_{SSAIO}, $V_{SS1AGND}$, $V_{SS2AGND}$	with respect to V_{SS}	- 0.3 V to 0.3 V
Input voltage range, V_{IN}		- 0.3 V to 4.6 V
Output voltage range, V_O		- 0.3 V to 4.6 V
Input clamp current, I_{IK} ($V_{IN} < 0$ or $V_{IN} > V_{DDIO}$)[3]		± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DDIO}$)		± 20 mA
Operating ambient temperature ranges,	T_A: A version [4]	- 40°C to 85°C
Junction temperature range, T_j[4]		- 40°C to 150°C
Storage temperature range, T_{stg}[4]		- 65°C to 150°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Section 6.2 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted.
(3) Continuous clamp current per pin is ± 2 mA. This includes the analog inputs which have an internal clamping circuit that clamps the voltage to a diode drop above V_{DDA2} or below V_{SSA2}.
(4) Long-term high-temperature storage and/or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see *IC Package Thermal Metrics Application Report* (literature number SPRA953) and *Reliability Data for TMS320LF24x and TMS320F281x Devices Application Report* (literature number SPRA963)

PRODUCT PREVIEW

6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Device supply voltage, I/O, V_{DDIO}		3.2	3.3	3.4	V
Device supply voltage CPU, V_{DD}		1.84	1.9	1.96	V
Supply ground, V_{SS}, V_{SSIO}			0		V
ADC supply voltage (3.3 V), V_{DDA2}, V_{DDAIO}		3.2	3.3	3.4	V
ADC supply voltage (1.8 V), V_{DD1A18}, V_{DD2A18}		1.84	1.9	1.96	V
Flash supply voltage, V_{DD3VFL}		3.2	3.3	3.4	V
Device clock frequency (system clock), $f_{SYSCLKOUT}$	150-MHz devices	2		150	MHz
	100-MHz devices	2		100	MHz
High-level input voltage, V_{IH}		2		V_{DDIO}	V
Low-level input voltage, V_{IL}				0.8	
High-level output source current, V_{OH} = 2.4 V, I_{OH}	All I/Os except Group 2			-4	mA
	Group 2(1)			-8	
Low-level output sink current, V_{OL} = V_{OL} MAX, I_{OL}	All I/Os except Group 2			4	mA
	Group 2(1)			8	
Ambient temperature, T_A	A version	-40		85	

(1) Group 2 pins are as follows: GPIO28, GPIO29, GPIO30, GPIO31, TDO, XCLKOUT, EMU0, EMU1, XINTF pins, GPIO35-87, $\overline{XRD}$.

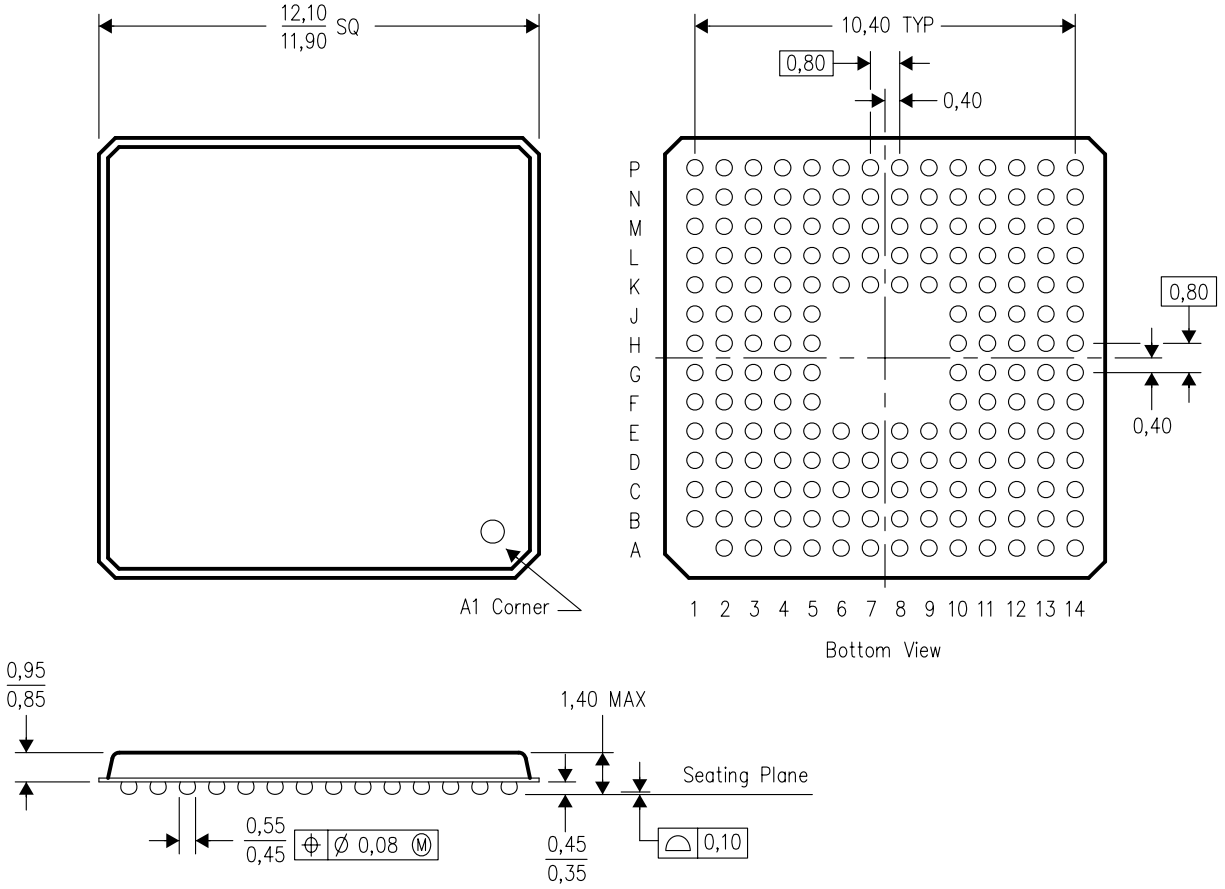
6.3 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = I_{OH}MAX		2.4			V
			I_{OH} = 50 µA		V_{DDIO} - 0.2			
V_{OL}	Low-level output voltage		I_{OL} = I_{OL}MAX				0.4	V
I_{IL}	Input current (low level)	Pin with pullup enabled	V_{DDIO} = 3.3 V, V_{IN} = 0 V	All I/Os (including $\overline{XRS}$)	-80	-140	-190	µA
		Pin with pulldown enabled	V_{DDIO} = 3.3 V, V_{IN} = 0 V				±2	
I_{IH}	Input current (high level)	Pin with pullup enabled	V_{DDIO} = 3.3 V, V_{IN} = V_{DDIO}				±2	µA
		Pin with pulldown enabled	V_{DDIO} = 3.3 V, V_{IN} = V_{DDIO}		28	50	80	
		Pin with pulldown enabled	V_{DDIO} = 3.3 V, V_{IN} = V_{DDIO}		80	140	190	
I_{OZ}	Output current, pullup or pulldown disabled		V_O = V_{DDIO} or 0 V				±2	µA
C_I	Input capacitance					2		pF

PRODUCT PREVIEW

ZHH (S–PBGA–N179) PLASTIC BALL GRID ARRAY

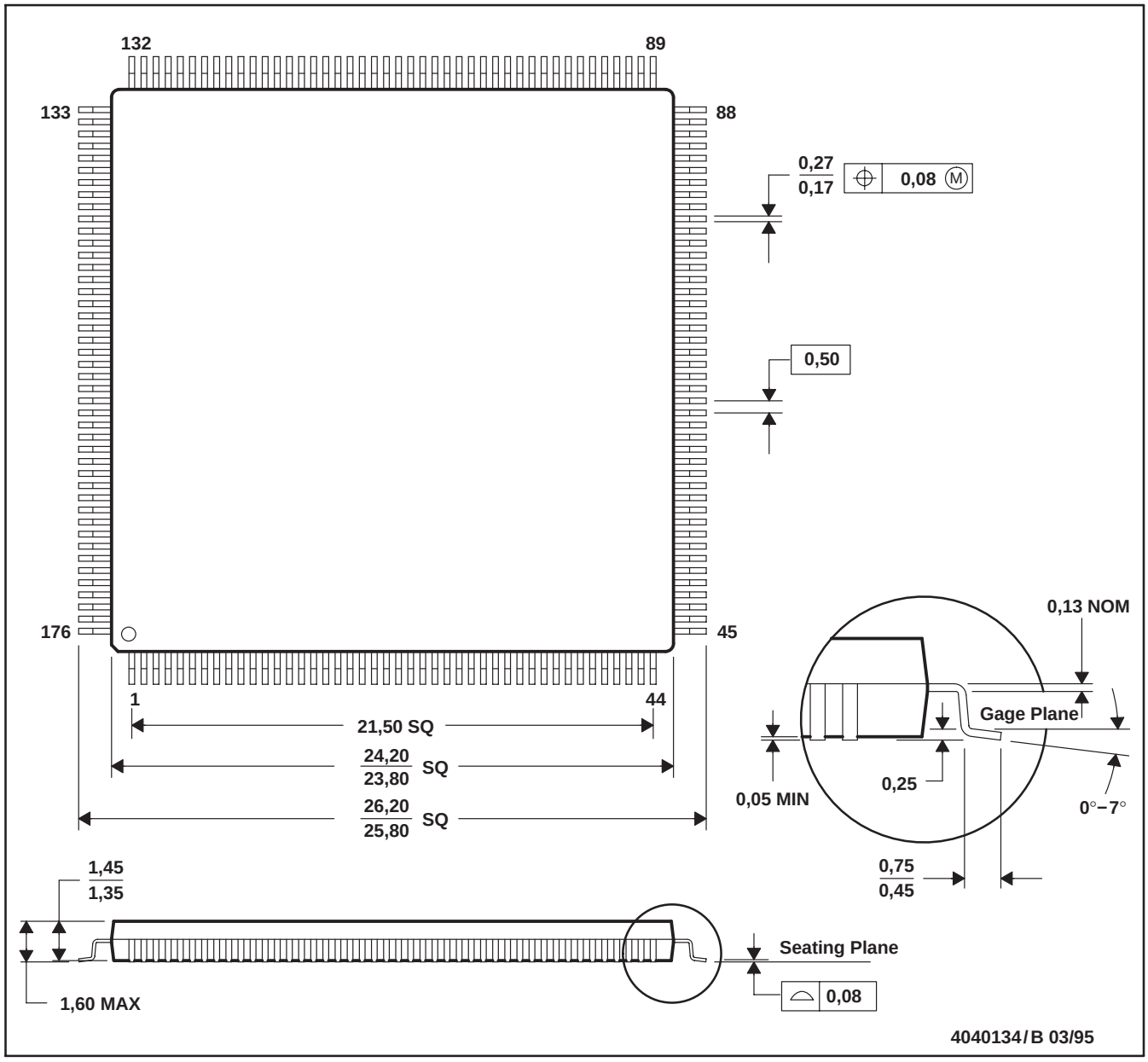


4204739–4/C 06/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Micro Star BGA configuration.
D. This is a lead–free solder ball design.

OCTOBER 1994

PGF (S-PQFP-G176) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

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Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
Low Power Wireless	www.ti.com/lpw	Video & Imaging	www.ti.com/video
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