NEC

**User's Manual** 

# 78K0/Kx2

# **8-Bit Single-Chip Microcontrollers**

# Flash Memory Self Programming

μ <b>PD78F0500</b>	$\mu$ PD78F0521	$\mu$ PD78F0544
μ <b>PD78F0501</b>	μ <b>PD78F0522</b>	μ <b>PD78F0545</b>
μ <b>PD78F0502</b>	μ <b>PD78F0523</b>	μ <b>PD78F0546</b>
μ <b>PD78F0503</b>	μ <b>PD78F0524</b>	μ <b>ΡD78F0547</b>
$\mu$ PD78F0503D	$\mu$ PD78F0525	μ <b>ΡD78F0547D</b>
μ <b>PD78F0511</b>	$\mu$ PD78F0526	
μ <b>PD78F0512</b>	$\mu$ PD78F0527	
μ <b>PD78F0513</b>	$\mu$ PD78F0527D	
μ <b>PD78F0513D</b>	μ <b>PD78F0531</b>	
μ <b>PD78F0514</b>	μ <b>PD78F0532</b>	
μ <b>PD78F0515</b>	μ <b>PD78F0533</b>	
μ <b>PD78F0515D</b>	μ <b>PD78F0534</b>	
	μ <b>PD78F0535</b>	
	μ <b>PD78F0536</b>	
	μ <b>PD78F0537</b>	
	μ <b>PD78F0537D</b>	

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### **1** VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (MAX) and  $V_{IH}$  (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (MAX) and  $V_{IH}$  (MIN).

### (2) HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

### **③** PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

#### **④** STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

#### **⑤** POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

#### **(6)** INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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### INTRODUCTION

Readers		or users who wish to understand the functions of the flash 78K0/Kx2 and design application systems using these
Purpose		to give users an understanding of the usage of the flash sample library which is used when rewriting the 78K0/Kx2
Organization	Description of flash envi	ally divided into the following sections. ronment nory self programming sample library
How to Read This Manual	electrical engineering, logi	ders of this manual have general knowledge in the fields of c circuits, and microcontrollers.
	To check the hardware fun → Refer to the user's mar	nual of each 78k0/Kx2 product.
Conventions	Data significance: Active low representation: <b>Note:</b> <b>Caution</b> : <b>Remark</b> : Numerical representation:	Footnote for item marked with <b>Note</b> in the text Information requiring particular attention Supplementary information

Hexadecimal ... xxxxH

Terminology

The following describes the meanings of certain terms used in this manual.

• Self programming

Self programming operations are flash memory write operations that are performed by user programs.

• Flash memory self programming sample library

This is the library that is provided by the 78K0/Kx2 for flash memory manipulation.

Flash environment

This is the environment that supports flash memory manipulations. It has restrictions that differ from those applied to ordinary program execution.

Block number

Block numbers indicate blocks in flash memory. They are used as units during manipulations such as erasures and blank checks.

Boot cluster

This is the area that is used for boot swapping. Boot cluster 0 and boot cluster 1 are provided and the cluster to be booted can be selected.

Entry RAM

This is the area in RAM that is used by the flash memory self programming sample library. The user program reserves this area and specifies the start address of the specific area to be used when the library is called.

Internal verification

After writing to flash memory, signal levels are checked internally to confirm correct reading of data. When an internal verification error occurs, the corresponding device is judged as faulty.

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# CHAPTER 1 GENERAL

### 1.1 Overview

The self programming sample library is firmware provided on the 78K0/Kx2, and is software which is used to rewrite data in the flash memory.

By calling the self programming sample library from a user program, the contents of the flash memory can be rewritten and, consequently, the period for software development can be substantially shortened.

- Cautions 1. Because the self programming sample library rewrites the contents of the flash memory by using the CPU, registers, and RAM of the 78K0/Kx2, a user program cannot be executed while processing of the self programming sample library is being executed.
  - 2. The self programming sample library uses the CPU (register bank 3) and a work area (100 bytes of entry RAM). Therefore, the user must save the data necessary for the user program in that area immediately before calling the self programming sample library.

# 1.2 Calling Self Programming Sample Library

The self programming sample library can be called by a user program in C or an assembly language.

If the -SM option (that uses an object as a static model) is specified when a file written in C is complied, use (link) the library for static models. If the -SM option is not specified, link the library for normal models.

If the file is written in an assembly language, use (link) the library for static models.

The following flowchart illustrates how to rewrite the contents of the flash memory by using the self programming sample library.

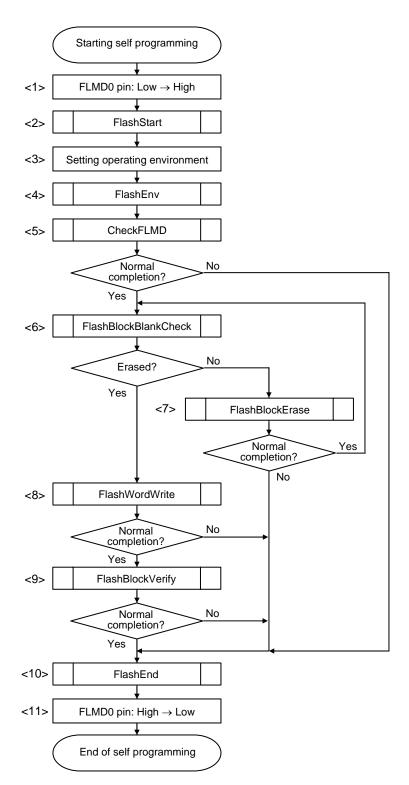


Figure 1-1. Flow of Self Programming (rewriting contents of flash memory)

- <1> Preprocessing (setting of hardware environment) As preprocessing, make the FLMD0 pin high (refer to **2.1 Hardware Environment**).
- <2> Preprocessing (declaring start of self programming) As preprocessing, call the self programming start library FlashStart to declare the start of self programming.
- <3> Preprocessing (setting of software environment) As preprocessing, save register bank 3 and specify a work area (refer to **2.2 Software Environment**).
- <4> Preprocessing (initializing entry RAM) As preprocessing, call the initialize library FlashEnv to initialize the entry RAM.
- <5> Preprocessing (checking voltage level) As preprocessing, call the mode check library CheckFLMD and check the voltage level.
- <6> Checking erasing of specified block (1 KB) Call the block blank check library FlashBlockBlankCheck to check if the specified block (1 KB) has been erased.
- <7> Erasing specified block (1 KB) Call the block erase library FlashBlockErase to erase a specified block (1 KB).
- <8> Writing data of 1 to 64 words to specified addresses Call the word write library FlashWordWrite to write data of 1 to 64 words to specified addresses.
- <9> Verifying specified block (1 KB) (internal verification) Call the block verify library FlashBlockVerify to verify a specified block (1 KB) (internal verification).
- <10> Post-processing (declaring end of self programming) As post-processing, call the self programming end library FlashEnd to declare the end of self programming.
- <11> Post-processing (setting of hardware environment) As post-processing, return the level of the FLMD0 pin to the low level.

### 1.3 Bank Number and Block Number

Products in the 78K0/Kx2 Series having flash memory of up to 60 KB have their flash memory divided into 1 KB blocks. Erasing, blank checking, and verification (internal verification) for self programming are performed in these block units. To call the self programming sample library, a block number is specified.

Addresses 0000H to 0FFFH and 1000H to 1FFFH of the 78K0/Kx2 are allocated for boot clusters. A boot cluster is an area that is used to prevent the vector table data and basic functions of the program from being destroyed, and to prevent the user program from being unable to start due to a power failure or because the device was reset while an area including a vector area was being rewritten. For details on the boot cluster, refer to **CHAPTER 4 BOOT SWAP FUNCTION**.

Figure 1-2 shows the block numbers and boot clusters of a flash memory of up to 60 KB.

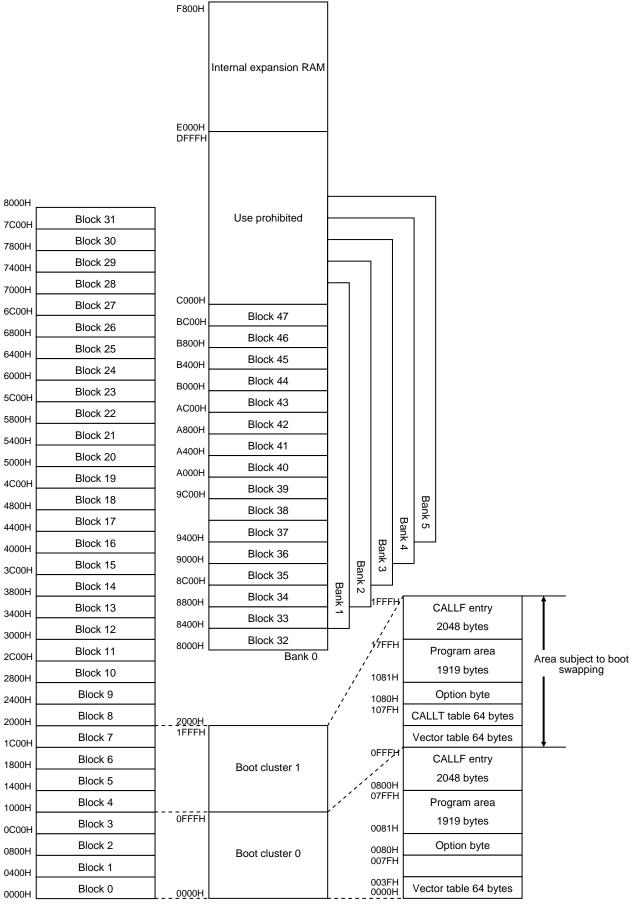
78K0/Kx2 products having flash memory of more than 96 KB have banks in an area that is larger than 32 KB. For these products, not only a block number but also a bank number must be specified to call the self programming sample library when performing erasing, blank checking, or verification (internal verification) in the area that is larger than 32 KB during self programming.

Figure 1-3 shows the block numbers and boot clusters of a flash memory of more than 96 KB.

Internal expansion RAM           Ecouri         Block 50           Ecouri         Block 50           Ecouri         Block 50           Ecouri         Block 50           Block 51         Block 55           Decori         Block 51           Coori         Block 52           Decori         Block 42           Block 28         Coori           Block 28         Block 42           Block 28         Block 43           Block 24         Block 43           Block 25         Block 43           Block 24         Block 43           Block 25         Block 43           Block 16         Block 43           Block 17         Block 43           Block 18         Block 35           Block 18         Block 35           Block 18         Block 35           Bl			F800H		]			
Block 58           E8004         Block 57           E8004         Block 56           D2004         Block 56           D2004         Block 53           Block 51         D2004           Block 52         C2004           Block 29         C2004           Block 21         Block 43           Block 21         Block 42           Block 21         A2004           Block 21         A2004           Block 31         Block 42           Block 10         Block 33           Block 11         Block 33           Block 12         A2004           Block 33         Block 34           Block 16         Block 33           Block 17         Block 33           Block 18         Block 33           Block 19         Block 33           Block 11         Block 33			F000H	Internal expansion RAM	-			
E4004         Block 57           E4004         Block 56           D0004         Block 55           D0004         Block 53           D0004         Block 53           D0004         Block 53           D0004         Block 51           C0004         Block 51           C0004         Block 53           Pacoba         Block 51           C0004         Block 53           Pacoba         Block 51           C0004         Block 52           C0004         Block 43           Block 28         Cocose           Block 27         Block 43           Block 23         Block 45           Block 24         Block 42           Block 23         Accose           Block 18         Block 41           Block 19         Accose           Block 11         Block 33           Block 11         Block 34           Block 11         Block 32           Accose         Block 32           Block 11         Block 33           Block 11         Block 32           Block 11         Block 32           Block 11         Block 32           Block 11 <td></td> <td></td> <td>EC00H</td> <td>Block 59</td> <td></td> <td></td> <td></td> <td></td>			EC00H	Block 59				
Block 56         E004         Block 55           B000H         Block 55           B000H         Block 53           9000H         Block 51           7000H         Block 20           Block 20         C400H           Block 21         C400H           Block 22         Block 41           6000H         Block 11           6000H         Block 12           6000H         Block 21           A400H         Block 42           6000H         Block 11           6000H         Block 11           6000H         Block 11           6000H         Block 11           6000H         Block 13           6000H         Block 33           6000H         Block 34           6000H         Block 35           6000H         Block 34           6000H         Block 35           6000H         Block 34           6000H         Block 35           6000H         Block 34           6000H			E800H	Block 58				
Lucasi         Block 55           Decom         Block 53           Block 31         Doore           70004         Block 52           70004         Block 30           70004         Block 29           Block 29         C4004           Block 20         Block 43           70004         Block 20           Block 20         C0004           Block 21         C0004           Block 22         Block 43           60004         Block 23           60004         Block 13           80004         Block 42           60004         Block 13           80004         Block 33           80004         Block 34           80004         Block 33           80004         Block 34           80004         Block 33           80004         Block 33           80004         Block 34           80004         Block 35           80004         Block 36           80004         Block 36 <td></td> <td></td> <td>E400H</td> <td>Block 57</td> <td></td> <td></td> <td></td> <td></td>			E400H	Block 57				
Block 31         Doon+         Block 53           8000H         Block 53         Doon+           7200H         Block 30         CCOH           7200H         Block 20         C600H           7400H         Block 20         C600H           7400H         Block 22         C600H           8000H         Block 48         C000H           6000H         Block 20         C600H           8000H         Block 43         Boon+           6000H         Block 21         B000H           Block 22         ACOH         Block 43           6000H         Block 23         ACOH           Block 23         ACOH         Block 43           6000H         Block 23         ACOH           Block 13         Boon+         Block 33           8000H         Block 33         Boon+           Block 12         Boon+         Block 33           8000H         Block 32         Boon+           8000H         Block 33         Boon+           8000H         Block 33         Boon+           8000H         Block 33         Boon+           8000H         Block 33         Boon+           8000Ck 11 </th <th></th> <th></th> <th>E000H</th> <th>Block 56</th> <th></th> <th></th> <th></th> <th></th>			E000H	Block 56				
Block 31         Block 53           9000H         Block 31         000H         Block 52           7800H         Block 30         CC00H         Block 51           7800H         Block 22         Ca0H         Block 48           6000H         Block 27         Block 48           6000H         Block 27         Block 48           6000H         Block 26         Block 47           6000H         Block 27         Block 46           6000H         Block 27         Block 46           6000H         Block 23         Block 43           6000H         Block 21         Ac00H         Block 41           6000H         Block 11         Block 33         Block 37           6000H         Block 13         9000H         Block 35           6000H         Block 13         8000H         Block 35           6000H         Block 5         6000H         1081H			DC00H	Block 55				
Block 31         Dooch         Block 52           7200H         Block 30         Ccooh         Block 51           7400H         Block 28         Ccooh         Block 49           7000H         Block 27         Ccooh         Block 47           6600H         Block 25         B800H         Block 46           6600H         Block 25         B600H         Block 42           6600H         Block 25         B600H         Block 42           6600H         Block 23         B000H         Block 43           6600H         Block 23         B000H         Block 43           6600H         Block 21         A600H         Block 41           5000H         Block 19         A000H         Block 33           6400H         Block 13         9600H         Block 33           6400H         Block 13         8600H         Block 34           7FFFH         CALLT entry         2048			D800H	Block 54				
Block 31         D000H         Block 52           7800H         Block 30         CC00H         Block 50           7400H         Block 29         C800H         Block 50           7400H         Block 28         C000H         Block 48           6000H         Block 26         BC00H         Block 47           6800H         Block 26         BC00H         Block 43           6000H         Block 22         B000H         Block 44           6000H         Block 22         B000H         Block 43           6000H         Block 21         A000H         Block 41           6000H         Block 11         Block 39         Block 36           6000H         Block 15         B000H         Block 36           6000H         Block 11         Block 36         Block 32           6000H         Block 11         Block 33         Block 34           6000H         Block 14         Block 32         Program area           6000H         Block 13         Block 33         Block 12           6000H         Block 32         Block 34         Block 34           6000H         Block 11         Block 32         Program area           6000H         Block			D400H	Block 53				
Lock         Block 30         CC00H         Block 50           7800H         Block 29         C400H         Block 40           7000H         Block 28         C000H         Block 47           6800H         Block 27         B000H         Block 47           6800H         Block 25         B800H         Block 44           6400H         Block 23         A00H         Block 43           6600H         Block 21         A00H         Block 43           5600H         Block 21         A00H         Block 43           5600H         Block 19         A00H         Block 39           5600H         Block 17         9800H         Block 33           6800H         Block 16         900H         Block 36           6800H         Block 16         900H         Block 37           9800H         Block 36         Block 37           9800H         Block 32         Program area           910ck 11         8800H         Block 32           910ck 12         800H         Block 32           910ck 13         8800H         Block 32           910ch 11         800H         Block 32           910ch 11         800H         Block 32 <td></td> <td>Plack 21</td> <td>D000H</td> <td>Block 52</td> <td></td> <td></td> <td></td> <td></td>		Plack 21	D000H	Block 52				
Noon         Block 29         C800H         Block 49           7400H         Block 28         C600H         Block 49           6C00H         Block 27         BC00H         Block 47           8600H         Block 26         BC00H         Block 46           6400H         Block 25         B600H         Block 43           6600H         Block 22         A600H         Block 44           6600H         Block 22         A600H         Block 42           6600H         Block 21         A800H         Block 42           6600H         Block 21         A800H         Block 42           6600H         Block 11         Block 30         Block 30           6600H         Block 17         B800H         Block 33           6600H         Block 16         9000H         Block 36           6700H         Block 16         9000H         Block 36           8000H         Block 36         Block 36           6100k 11         9000H         Block 33           6000H         Block 32         Program area           1900H         Block 10         Block 32           2000H         Block 5         Boot cluster 1           1000H <t< td=""><td>7C00H</td><td></td><td>СС00Н</td><td>Block 51</td><td></td><td></td><td></td><td></td></t<>	7C00H		СС00Н	Block 51				
Houris         Block 28         C-400H         Block 49           7000H         Block 27         Block 48           6C00H         Block 26         Block 47           6800H         Block 26         Block 46           6400H         Block 23         B000H           6600H         Block 23         B000H           6600H         Block 23         B000H           8000H         Block 43         Block 44           5000H         Block 22         A000H           Block 11         A000H         Block 43           5000H         Block 16         9400H           Block 18         9000H         Block 37           9000H         Block 36         9000H           Block 13         8000H         Block 34           9000H         Block 33         Block 34           9000H         Block 34         Block 34           9000H         Block 34     <	7800H		C800H	Block 50				
Note         Block 27         Cooper         Block 48           6C00H         Block 26         BC00H         Block 47           6600H         Block 25         B800H         Block 46           6600H         Block 22         B800H         Block 43           6600H         Block 23         Accoold         Block 43           5600H         Block 22         Accoold         Block 43           5600H         Block 21         A800H         Block 42           5400H         Block 11         Block 43           5600H         Block 13         9000H         Block 33           5800H         Block 16         9000H         Block 37           5800H         Block 16         9000H         Block 35           3800H         Block 13         8800H         Block 33           3800H         Block 12         8400H         Block 33           3800H         Block 11         8000H         Block 32           3400H         Block 11         8000H         Block 32           3400H         Block 11         8000H         Block 32           3400H         Block 11         800H         CALLF entry           2000H         Block 5         900	7400H		C400H	Block 49				
Block 25         BCO0H         Block 47           6800H         Block 25         B800H         Block 46           6400H         Block 23         B400H         Block 44           6000H         Block 23         B000H         Block 43           6000H         Block 22         AC00H         Block 43           6000H         Block 22         AC00H         Block 42           5400H         Block 21         A800H         Block 42           5400H         Block 20         A400H         Block 43           5600H         Block 19         9C00H         Block 39           8000H         Block 17         9800H         Block 36           9000H         Block 36         Block 36         Block 36           9000H         Block 13         8800H         Block 33           9000H         Block 13         800H         Block 32           9000H         Block 12         8000H         Block 32           9000H         Block 11         Block 32         Program area           91919 bytes         Program area         1919 bytes           9200H         Block 5         Boot cluster 1         000H           1000H         Block 4         0FFFH </td <td>7000H</td> <td></td> <td>Сооон</td> <td>Block 48</td> <td></td> <td></td> <td></td> <td></td>	7000H		Сооон	Block 48				
Block 25         BB00H         Block 45           6400H         Block 24         B400H         Block 45           6000H         Block 23         AC00H         Block 43           5300H         Block 22         AC00H         Block 43           5400H         Block 21         A800H         Block 42           5400H         Block 21         A800H         Block 42           5400H         Block 19         9000H         Block 39           4800H         Block 16         9400H         Block 33           4800H         Block 16         9400H         Block 33           4800H         Block 16         9400H         Block 33           9000H         Block 13         8600H         Block 33           9000H         Block 13         8600H         Block 33           9000H         Block 12         8000H         Block 33           9000H         Block 11         8000H         Block 32           9000H         Block 11         Block 32         Program area           91919 bytes         Option byte         CALLT entry           2000H         Block 5         Program area           9100K 5         Program area         1919 bytes	6C00H		всоон	Block 47				
6400H         Block 23         BaooH         Block 45           6000H         Block 23         Block 44         Block 44           5000H         Block 22         A800H         Block 42           5400H         Block 22         A800H         Block 42           5400H         Block 21         A800H         Block 42           5400H         Block 20         A400H         Block 41           5600H         Block 19         9000H         Block 33           6400H         Block 18         9000H         Block 36           6600H         Block 17         9400H         Block 36           6600H         Block 17         9400H         Block 36           6600H         Block 17         9400H         Block 36           6600H         Block 31         Block 33         Block 32           9000H         Block 11         Block 32         HFFH           2000H         Block 10         Block 32         Diors 32           9000H         Block 7         1FFFH         CALLF entry           2000H         Block 6         1919 bytes         CALLT table 64 bytes           1000H         Block 5         9000H         1FFFH         CALLF entry	6800H		B800H	Block 46				
Block 23         B000H         Block 44           6000H         Block 22         AC00H         Block 43           5800H         Block 21         A800H         Block 42           5400H         Block 20         A400H         Block 41           5000H         Block 19         Goodel         Block 40           5000H         Block 18         Goodel         Block 33           4000H         Block 16         Goodel         Block 37           9000H         Block 36         Block 36         Block 36           3000H         Block 15         Block 36         Block 36           3000H         Block 13         Block 33         Block 36           3000H         Block 13         Block 33         Block 34           3000H         Block 12         Block 32         IFFFH         CALLF entry 2048 bytes           2000H         Block 10         Block 32         IfFFH         Option byte           2000H         Block 7         - 2000H         IfFFH         Option byte           2000H         Block 6         - 2000H         OFFFH         OB00H         OPTH           1000H         Block 6         - 2000H         OFFFH         OB00H         OPTH	6400H		B400H	Block 45				
Block 12         ACO0H         Block 43           5600H         Block 21         A800H         Block 42           5400H         Block 20         A400H         Block 41           5000H         Block 19         9000H         Block 39           4400H         Block 17         9800H         Block 37           9400H         Block 36         9000H         Block 36           9300H         Block 32         17FFH         CALLF entry           1300H         Block 11         800H         Block 32           9400H         Block 32         107FH         2048 bytes           1081H         1919 bytes         Option byte         Swapping           1080H         Block 7         1FFFH         CALLF entry         2048 bytes           107FH         Block 6         1         1080H         Option byte         CALLF entry           2000H         Block 7         1FFFH         007FFH	6000H		вооон	Block 44				
S800H         Block 22         A800H         Block 42           5400H         Block 21         A400H         Block 41           5000H         Block 20         A400H         Block 40           6000H         Block 19         9C00H         Block 39           4800H         Block 18         9C00H         Block 37           4800H         Block 16         9400H         Block 36           4000H         Block 15         9000H         Block 36           3800H         Block 13         8800H         Block 36           3800H         Block 11         8000H         Block 32           3000H         Block 11         8000H         Block 32           3000H         Block 11         8000H         Block 32           3000H         Block 10         8000H         Block 32           2000H         Block 7         - 2000H         1081H           1080H         Block 5         - 2000H         107FH           1080H         Block 5         - 2000H         0FFFH           1080H         Block 6         - 2000H         0FFFH           1080H         Block 5         - 2000H         0FFFH           1000H         Block 5	5C00H		АСООН	Block 43	]			
S400H         Block 21         A400H         Block 41           5000H         Block 20         A400H         Block 40           400H         Block 19         9C00H         Block 39           4800H         Block 18         9C00H         Block 39           4400H         Block 17         9800H         Block 37           4000H         Block 16         9400H         Block 36           3000H         Block 13         8800H         Block 35           3800H         Block 11         8000H         Block 32           3000H         Block 10         8000H         Block 32           2400H         Block 5         900H         Block 32           2400H         Block 5         900H         1081H           1080H         Block 5         900H         1081H           1080H         Block 5         900H         107FH           2400H         Block 5         900H         900H           1000H         Block 5         900H	5800H			Block 42	]			
S000H         Block 20         A000H         Block 40           4C00H         Block 19         9C00H         Block 39           4800H         Block 18         9C00H         Block 38           4400H         Block 16         9400H         Block 37           9400H         Block 36         9000H         Block 36           3C00H         Block 15         9000H         Block 35           3800H         Block 13         8800H         Block 33           3000H         Block 11         8000H         Block 32           2000H         Block 10         8000H         Block 32           2000H         Block 10         8000H         Block 32           2000H         Block 6         - 2000H         1081H           2000H         Block 7         1FFFH         CALLF entry           2040H         Block 7         1FFFH         CALLT table 64 bytes           1000H         Block 6         - 2000H         1FFFH           1000H         Block 5         - 2000H         - 2000H           1400H         Block 5         - 2000H         - 2000H           1400H         Block 6         - 2000H         - 2000H           1400H         Bl	5400H			Block 41				
4C00H         Block 19         9C00H         Block 39           4800H         Block 18         99C00H         Block 38           4400H         Block 17         9800H         Block 38           4400H         Block 16         9400H         Block 36           3600H         Block 15         8000H         Block 36           3600H         Block 13         8800H         Block 33           3600H         Block 12         8400H         Block 33           3000H         Block 11         8000H         Block 32           2000H         Block 7         Program area           1081H         1919 bytes         Area subject to boot swapping           2000H         Block 7         1FFFH         CALLF entry           2000H         Block 7         1FFFH         Program area           1080H         Block 6	5000H			Block 40	1			
4800H         Block 18         9800H         Block 38           4400H         Block 17         9800H         Block 37           4000H         Block 16         9000H         Block 36           3C00H         Block 15         8000H         Block 35           3800H         Block 13         8000H         Block 33           3000H         Block 12         8000H         Block 33           3000H         Block 11         8000H         Block 32           2000H         Block 10         8000H         Block 32           2400H         Block 7         1         1           1000H         Block 7         1         1           1000H         Block 5         1         9           1000H         Block 5         1         1           1000H         Block 3         -         2000H         0           1400H         Block 5         -         2000H         0         0           1400H         Block 3         -         0         0         0           1400H         Block 4         -         0         0         0         0           1000H         Block 3         -         0         0	4C00H			Block 39	1			
4400H     Block 17     9400H       4000H     Block 16     9400H       3000H     Block 15     9000H       3800H     Block 13     8800H       3800H     Block 13     8800H       3000H     Block 13     8800H       3000H     Block 12     8400H       3000H     Block 12     8400H       3000H     Block 12     8400H       3000H     Block 11     Block 32       2000H     Block 10     1081H       2000H     Block 7     1FFFH       1000H     Block 6     -2000H       1000H     Block 5     -2000H       1000H     Block 5     -2000H       1000H     Block 3     -70FFFH       1000H     Block 3     0FFFH       1000H     Block 3     0FFFH       1000H     Block 3     0FFFH       1000H     Block 3     0FFFH       1000H     Block 1     0050H       1000H     Block 1     0050H       1000H     Block 3     0FFFH       1000H     Block 1     0050H       1000H     Block 1     0050H       1000H     Block 1     0050H       1000H     Block 3     0FFFH       1000H	4800H			Block 38	1			
4000H     Block 16       3C00H     Block 15       3C00H     Block 15       3C00H     Block 14       3C00H     Block 13       3C00H     Block 13       3C00H     Block 13       3C00H     Block 13       3C00H     Block 12       3C00H     Block 12       3C00H     Block 12       3C00H     Block 11       3C00H     Block 10       2C00H     Block 10       2C00H     Block 7       1C00H     Block 7       1C00H     Block 5       1C00H     Block 5       1000H     Block 3       1000H     Block 4       0C00H     Block 3       0FFFH     005FFH       0C00H     Block 1       0C00H     Block 3       0C00H     Block 4       0C00H     Block 1       0C00H     Block 1       0C00H     Block 1       0C00H     Block 1       0C00H     Block 1 </td <td>4400H</td> <td></td> <td></td> <td>Block 37</td> <td></td> <td></td> <td></td> <td></td>	4400H			Block 37				
Block 15       Block 35         3800H       Block 14       8000H         3400H       Block 13       8000H         3400H       Block 12       8400H         3000H       Block 12       8400H         3000H       Block 12       8400H         Block 11       Block 32       17FFH         2000H       Block 10       1081H         2400H       Block 9       1081H         2400H       Block 7       -2000H         1000H       Block 6       -2000H         11000H       Block 5       -2000H         11000H       Block 5       -2000H         11000H       Block 3       -2000H         11000H       Block 4       -2000H         11000H       Block 3       0FFFH         11000H       Block 4       0FFFH         11000H       Block 2       0FFFH         11000H       Block 1       0FFFH         11000H       Block 2       0FFFH <t< td=""><td>4000H</td><td></td><td></td><td>Block 36</td><td></td><td></td><td></td><td></td></t<>	4000H			Block 36				
Block 14     Block 34       3400H     Block 13     8800H       3000H     Block 12     8800H       3000H     Block 12     Block 33       2000H     Block 11     Block 32       2400H     Block 9     1081H       2400H     Block 7       1000H     Block 7       1000H     Block 5       1000H     Block 5       1000H     Block 3       000H     Block 1       1400H     Block 3       000H     OFFFH       1400H     Block 3       000H     OFFFH       1400H     Block 6       1400H     Block 1       1400H     Block 3       000H     OFFFH       1400H     Block 4       000H     OFFFH       1400H     Block 3       000H     OFFFH       1400H     Block 4       000H     OFFFH       1400H     Block 3       000H     OFFFH       1400H     Block 4       000H     Block 1       000H     OFFFH       000H     007FFH       000H     007FFH       000H     007FFH       000H     007FFH       000H     007FFH	3C00H			Block 35				
3400H       Block 13       Block 33       CALLF entry         3000H       Block 12       8400H       Block 33       1/7FFH       Program area         2000H       Block 10       Block 32       1/7FFH       Program area       Area subject to boot         2800H       Block 9       1081H       0091       1919 bytes       Area subject to boot         2400H       Block 7       1FFFH       CALLT table 64 bytes       Vector table 64 bytes         1000H       Block 5       1FFFH       CALLF entry       2048 bytes         1000H       Block 6       1FFFH       CALLF entry       2048 bytes         1000H       Block 7       1FFFH       Boot cluster 1       0600H       07FFH         1400H       Block 3       0FFFH       CALLF entry       2048 bytes         1000H       Block 3       0FFFH       0800H       07FFH       Program area         1000H       Block 3       0FFFH       0081H       1919 bytes       048 bytes         0400H       Block 1       0FFFH       0080H       007FH       CALLT table 64 bytes         0400H       Block 1       005FH       003FH       Vector table 64 bytes       0400FH	3800H			Block 34	]1F	FFH1		
3000H       Block 12       Block 32       17FFH       Program area       Area subject to boot swapping         2600H       Block 10       1081H       1919 bytes       Area subject to boot swapping         2400H       Block 9       1081H       000H       Option byte         2400H       Block 7       -2000H       CALLT table 64 bytes       Vector table 64 bytes         1000H       Block 6       -2000H       OFFFH       CALLF entry         1200H       Block 5       0800H       07FFH       Program area         1400H       Block 3       -0FFFH       Boot cluster 1       0800H       07FFH         1400H       Block 3       0FFFH       Boot cluster 1       0800H       0080H       009H         0400H       Block 1       0FFFH       Boot cluster 0       0080H       009H       0010 byte         0400H       Block 1       007FFH       Program area       003FH       Vector table 64 bytes       003FH	3400H			Block 33	]	/	-	
2C00H       Block 11       Program area       Area subject to boot swapping         2800H       Block 10       1081H       1081H       Option byte         2400H       Block 9       1081H       0000H       Option byte         2000H       Block 7       1FFFH       0000H       CALLT table 64 bytes         1000H       Block 6       1FFFH       0000H       CALLT table 64 bytes         1400H       Block 5       0FFFH       0800H       07FFH         1400H       Block 3       0FFFH       0800H       07FFH         1000H       Block 2       0FFFH       0081H       0080H         0000H       Block 1       0FFFH       0081H       001H         0000H       Block 2       0FFFH       0081H       0080H         0000H       Block 1       007FH       0080H       001H         0000H       Block 1       0001H       001H       001H         0000H       Block 2       0001H       001H       001H         0000H       Block 2       001H       001H       001H         0000H       Block 0       001H       001H       001H         0000H       Block 0       001H       001H <td< td=""><td>3000H</td><td></td><td></td><td>Block 32</td><td>/ 17</td><td>FFH</td><td>-</td><td></td></td<>	3000H			Block 32	/ 17	FFH	-	
2800H     Block 9       2400H     Block 9       2000H     Block 8       2000H     Block 7       1C00H     Block 7       1800H     Block 6       1800H     Block 5       1000H     Block 5       1000H     Block 3       0C00H     Block 3       0C00H     Block 2       0Block 1     0FFFH       0All H     OFFFH       0C00H     Block 2       0Block 1     0FFFH       0All H     OFFFH       0Block 2     0FFFH       0Block 1     0080H       0Block 2     0FFFH       0Block 3     0FFFH       0Block 4     0081H       0Block 5     0081H       0Block 1     0080H       0Block 1     0080H       0Block 1     003FH	2C00H		-		/		-	Area subject to boot
2400H     Block 8     - 2000H     CALLT table 64 bytes       2000H     Block 7     1FFFH     CALLT table 64 bytes       1C00H     Block 6     Block 6     Vector table 64 bytes       1800H     Block 5     Boot cluster 1     0FFFH     CALLF entry       1400H     Block 4     OFFFH     0800H     2048 bytes       1000H     Block 3     OFFFH     0800H     1919 bytes       0800H     Block 2     Boot cluster 0     0080H     Option byte       0400H     Block 0     Option byte     CALLT table 64 bytes	2800H		-		i		-	Gildpping
2000H       Block 7       1FFFH       Vector table 64 bytes         1C00H       Block 6       Block 6       Vector table 64 bytes         1800H       Block 5       Boot cluster 1       OFFFH       CALLF entry         1000H       Block 3       OFFFH       0800H       Program area         0C00H       Block 2       OFFFH       0081H       1919 bytes         0800H       Block 1       007FFH       OR80H       007FFH         0800H       Block 2       OFFFH       0081H       1919 bytes         0400H       Block 0       OVER 1       003FH       Vector table 64 bytes	2400H		-		, 10 , 10	80H 7FH		
ICODH     Block 7       1800H     Block 6       1800H     Block 5       1400H     Block 5       1000H     Block 4       0C00H     Block 3       0FFFH     0800H       07FFH     Program area       1919 bytes     080H       0800H     0081H       1919 bytes     080H       0800H     007FFH       Block 1     0080H       003FH     Vector table 64 bytes	2000H		<u>2000H</u> 1FFFH		í		-	
1800H     Block 6       1400H     Block 5       1000H     Block 4       0C00H     Block 3       0FFFH     0600H       0800H     07FFH       0800H     07FFH       0800H     0081H       0800H     0080H       0800H     Block 2       0400H     Block 0	1C00H		-		OF	FFH	,	<b>↓</b>
1400H     Block 2       000H     Block 3       000H     Block 3       000H     Block 2       0800H     Block 1       0400H     Block 0	1800H		-	Boot cluster 1		· ·		
Indext depicted with the second se	1400H		-				-	
0C00H     Block 3       0800H     Block 2       0400H     Block 1   Block 1 Block 0 Block	1000H				ł.		-	
0400H     Block 1       0400H     Block 0         Block 1         003FH         Voctor table 64 bytes	осоон		-		00	81H	-	
0400H Block 1 CALL I table 64 bytes	0800H		-	Boot cluster 0				
0000H Block 0 0000H 0000H Vector table 64 bytes	0400H		-				-	
	0000Н	Block 0	<u>0000H</u>			ЮОН	Vector table 64 bytes	

# Figure 1-2. Block Numbers and Boot Clusters (flash memory of up to 60 KB)





# 1.4 Processing Time and Acknowledging Interrupt

Table 1-1 and Table 1-2 show the processing time of the self programming sample library and whether interrupts can be acknowledged. Table 1-1 shows a case where an internal high-speed oscillator is used for the main system clock and Table 1-2 shows a case where an external system clock is used for the main system clock.

The self programming sample library that can acknowledge interrupts has a function to check if an interrupt is generated while processing of the self programming sample library is under execution, and a function to perform post-processing if an interrupt has been generated.

For details on interrupts, refer to CHAPTER 3 INTERRUPT SERVICING DURING SELF PROGRAMMING.

			Pro	cessing Time (u	unit: microsecon	ds)			
	Outside short direct addressing range				In short direct addressing range				Acknowledging
Library Name	Norma	l model	Static	model	Norma	l model	Static model		Interrupt
	Min	Max	Min	Max	Min	Max	Min	Max	
self programming start library				4.:	25				Not acknowledged
initialize library		977	<b>'</b> .75			44	3.5		Not acknowledged
mode check library	753	.875	753	.125	219	.625	218	.875	Not acknowledged
block blank check library	1277	0.875	1276	5.875	1223	6.625	1223	1.625	Acknowledged
block erase library	36909.5	356318	36904.5	356296.25	36363.25	355771.75	36358.25	355750	Acknowledged
word write library	1214 (1214.375)	2409 (2409.375)	1207 (1207.375)	2402 (2402.375)	679.75 (680.125)	1874.75 (1875.125)	672.75 (673.125)	1867.75 (1868.125)	Acknowledged
block verify library	2561	8.875	2561	3.875	2507	2.625	2506	7.625	Acknowledged
self programming end library				4.2	25				Not acknowledged
get information library (option value: 03H)	-	.25 .375)		66 .125)	-	37 .125)		1.75 .875)	Not acknowledged
get information library (option value: 04H)		.375 3.5)	858 (858	.125 3.25)		329.125 323.875 (239.25) (324)		Not acknowledged	
get information library (option value: 05H)	_	2.75 3.625)		37.5 3.375)	502.25 (503.125)			97 7.875)	Not acknowledged
set information library	105524.75	790809.375	105523.75	790808.375	104978.5	541143.125	104977.5	541142.125	Acknowledged
EEPROM write library	1496.5 (1496.875)	2691.5 (2691.875)	1489.5 (1489.875)	2684.5 (2684.875)	962.25 (962.625)	2157.25 (2157.625)	955.25 (955.625)	2150.25 (2150.625)	Acknowledged

### Table 1-1. Processing Time and Acknowledging Interrupt (with internal high-speed oscillator)

**Remark** Values in parentheses are when the write start address structure is placed outside of internal high-speed RAM.

	Processing Time (unit: microseconds)								
Librory Nomo	Outside short direct addressing range			In short direct addressing range				Acknowledging	
Library Name	Norma	model	Static	model	Norma	l model	Static model		Interrupt
	Min	Max	Min	Max	Min	Max	Min	Max	
self programming start library	34/fx <sup>Note</sup>					Not acknowledged			
initialize library		49x <sup>Note</sup> + 4	485.8125			49/fx <sup>Note</sup> +	224.6875		Not acknowledged
mode check library	35/fx <sup>Note</sup> -	+ 374.75	29/fx <sup>Note</sup> ·	+ 374.75	35/fx <sup>Note</sup> +	113.625	29/fx <sup>Note</sup> +	- 113.625	Not acknowledged
block blank check library	174/fx <sup>Note</sup> +	6382.0625	134/fx <sup>Note</sup> +	6382.0625	174/fx <sup>Note</sup> +	6120.9375	134/fx <sup>Note</sup> +	6120.9375	Acknowledged
block erase library	174/fx <sup>Note</sup> + 31093.875	174/fx <sup>Note</sup> + 298948.125	134/fx <sup>Note</sup> + 31093.875	134/fx <sup>Note</sup> + 298948.125	174/fx <sup>Note</sup> + 30820.75	174/fx <sup>Note</sup> + 298675	134/fx <sup>Note</sup> + 30820.75	134/fx <sup>Note</sup> + 298675	Acknowledged
word write library	318(321)/fx <sup>Note</sup> + 644.125	318(321)/fx <sup>Note</sup> + 1491.625	262(265)/fx <sup>Note</sup> + 644.125	262(265)/fx <sup>Note</sup> + 1491.625	318(321)/fx <sup>Note</sup> + 383	318(321)/fx <sup>Note</sup> + 1230.5	262(265)/fx <sup>Note</sup> + 383	262(265)/fx <sup>Note</sup> + 1230.5	Acknowledged
block verify library	174/fx <sup>Note</sup> +	13448.5625	134/fx <sup>Note</sup> +	13448.5625	174/fx <sup>Note</sup> +	13175.4375	134/fx <sup>Note</sup> +	13175.4375	Acknowledged
self programming end library				34	Note				Not acknowledged
get information library (option value: 03H)	171(172)/fx <sup>№</sup>	<sup>1e</sup> + 432.4375	129(130)/fx <sup>№</sup>	<sup>te</sup> + 432.4375	171(172)/fx <sup>№</sup>	™ + 171.3125	129(130)/fx <sup>№</sup>	** + 171.3125	Not acknowledged
get information library (option value: 04H)	181(182)/fx <sup>№</sup>	<sup>ote</sup> + 427.875	139(140)/f× <sup>№</sup>	<sup>ote</sup> + 427.875	181(182)/fx	181(182)/fx <sup>Note</sup> + 166.75 139(140)/fx <sup>Note</sup> + 166.75		<sup>Note</sup> + 166.75	Not acknowledged
get information library (option value: 05H)	404(411)/f× <sup>N</sup>	<sup>ote</sup> + 496.125	362(369)/f× <sup>N</sup>	<sup>ote</sup> + 496.125	404(411)/fx <sup>Note</sup> + 231.875 362(369)/fx <sup>Note</sup> + 231.875		<sup>lote</sup> + 231.875	Not acknowledged	
set information library	75/fx <sup>Note</sup> + 79157.6875	75/fx <sup>Note</sup> + 652400	67/fx <sup>Note</sup> + 79157.6875	67/fx <sup>Note</sup> + 652400	75/fx <sup>Note</sup> + 78884.5625			Acknowledged	
EEPROM write library	318(321)/fx <sup>Note</sup> + 799.875	318(321)/fx <sup>Note</sup> + 1647.375	262(265)/fx <sup>Note</sup> + 799.875	262(265)/fx <sup>Note</sup> + 1647.375	318(321)/fx <sup>Note</sup> + 538.75	318(321)/fx <sup>Note</sup> + 1386.25	262(265)/fx <sup>Note</sup> + 538.75	262(265)/fx <sup>Note</sup> + 1386.25	Acknowledged

CHAPTER 1 GENERAL

### Table 1-2. Processing Time and Acknowledging Interrupt (with external system clock used)

**Note** fx: Operating frequency of external system clock

**Remark** Values in parentheses are when the write start address structure is placed outside of internal high-speed RAM.

# CHAPTER 2 PROGRAMMING ENVIRONMENT

This chapter explains the hardware environment and software environment necessary for the user to rewrite flash memory by using the self programming sample library.

# 2.1 Hardware Environment

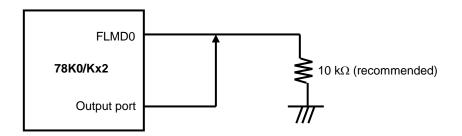
To execute self programming, a circuit that controls the voltage on the FLMD0 pin of the 78K0/Kx2 is necessary.

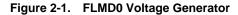
The voltage on the FLMD0 pin must be low while an ordinary user program is being executed (in normal operation mode) and high while self programming is being executed (in flash rewriting mode).

While the FLMD0 pin is low, the firmware and software for rewriting run, but the circuit for rewriting flash memory does not operate. Therefore, the flash memory is not actually rewritten.

A self programming sample library that makes the FLMD0 pin high is not provided. Therefore, to rewrite the flash memory, the voltage level of the FLMD0 pin must be made high by manipulating a port through user program, before calling the self programming start library.

Here is an example of the circuit that changes the voltage on the FLMD0 pin by manipulating a port.





# 2.2 Software Environment

The self programming sample library allocates its program to a user area and consumes about 500 bytes of the program area. The self programming sample library itself uses the CPU (register bank 3), work area (entry RAM), stack, and data buffer.

The following table lists the necessary software resources.

Item	Description	Restriction
CPU	Register bank 3	-
Work area	Entry RAM: 100 bytes	Internal high-speed RAM outside short addressing range or internal high-speed RAM in short direct addressing range with first address as FE20H (Refer to 2.2.1 Entry RAM.)
Stack	39 bytes max. <b>Remark</b> Use the same stack as for the user program.	Internal high-speed RAM other than FE20H to FE83H (Refer to 2.2.2 Stack and data buffer.)
Data buffer	1 to 256 bytes <b>Remark</b> The size of this buffer varies depending on the writing unit specified by the user program.	Internal high-speed RAM other than FE20H to FE83H (Refer to 2.2.2 Stack and data buffer.)
Program area	Normal model: 525 bytes Static model: 432 bytes <b>Remark</b> Supplied as an assembly-language source.	<ul> <li>Within 0000H to 7FFFH (32 KB)</li> <li>Caution The self programming sample library and the user program that calls the self programming sample library must always be located within the above range, because the firmware built into the product is allocated to addresses starting from 8000H.</li> </ul>

Table 2-1. Software Resources

- Cautions 1. The self programming operation is not guaranteed if the user manipulates the above resources. Do not manipulate these resources during a self programming operation.
  - 2. The user must release the above resources used by the self programming sample library before calling the self programming sample library.

### 2.2.1 Entry RAM

The self programming sample library uses a work area of 100 bytes. This area is called entry RAM.

As the entry RAM, 100 bytes are automatically allocated, starting from the first address that is specified when the initialize library is called. Therefore, the first address of the entry RAM can be specified in the range from FB00H to FE20H.

In addition, a data buffer used by the initialize library to actually write data to the flash memory must be allocated to an area that is within the range from 1 to 256 bytes and is other than the work area. For details on the data buffer, refer to 2.2.2 Stack and data buffer.

The range in which the entry RAM can be allocated is shown below.

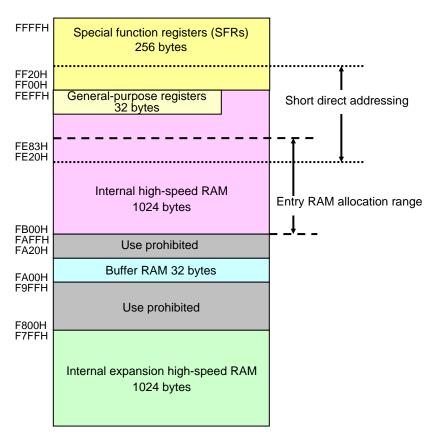


Figure 2-2. Allocation Range of Entry RAM

Caution The size of the internal expansion high-speed RAM varies depending on the product. For the size of the internal expansion high-speed RAM, refer to the user's manual of each product.

### 2.2.2 Stack and data buffer

The self programming sample library writes data to flash memory by using the CPU. Therefore, a self programming operation is performed by using the stack specified by the user program.

The stack must be allocated by stack processing of the self programming operation so that the entry RAM and the RAM used by the user are not cleared. Therefore, the stack can be allocated in the internal high-speed RAM at addresses other than FE20H to FE83H.

A data buffer is automatically allocated from the first address and by the number of data specified when the word write library is called. Therefore, the first address of the data buffer can be specified in the internal high-speed RAM at an address other than FE20H to FE83H, just as for the stack pointer.

Note that data to be written to the flash memory must be appropriately set and processed before the word write library is called.

The following figure shows the range in which the stack pointer and data buffer can be allocated.

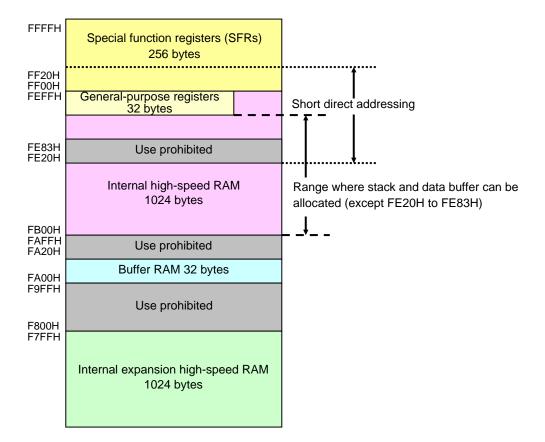


Figure 2-3. Allocatable Range for Stack Pointer and Data Buffer

Caution The size of the internal expansion high-speed RAM varies depending on the product. For the size of the internal expansion high-speed RAM, refer to the user's manual of each product.

# CHAPTER 3 INTERRUPT SERVICING DURING SELF PROGRAMMING

# 3.1 Overview

An interrupt can be generated, even while self programming is executed, in some self programming sample libraries of the 78K0/Kx2.

However, unlike the case for an ordinary interrupt, the user must decide whether the processing that has been interrupted should be resumed, by checking the return value from the self programming sample library.

The following figure illustrates the flow of processing if an interrupt is generated while processing of the self programming sample library is being executed.

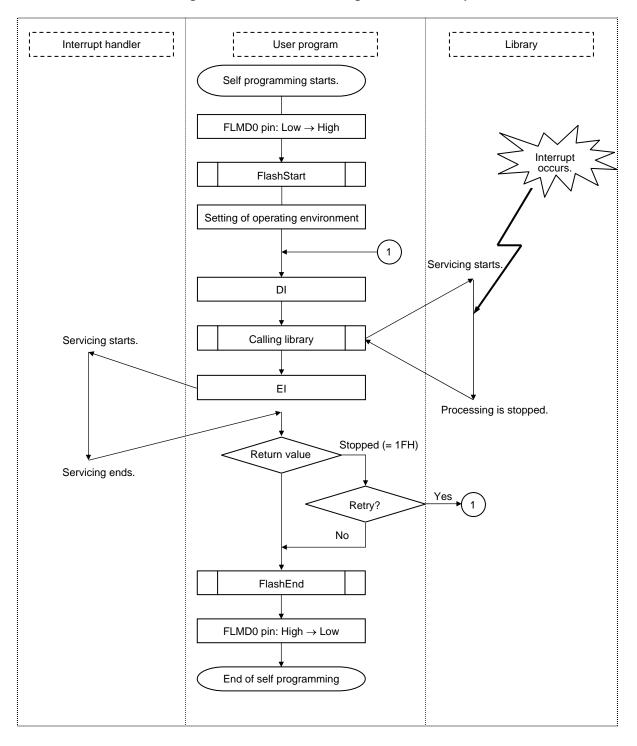


Figure 3-1. Flow of Processing in Case of Interrupt

The following table shows how the processing of the self programming sample libraries that acknowledge interrupts is resumed after the processing has been stopped by the occurrence of an interrupt.

Library Name	Resuming Method
block blank check library	Call the block blank check library FlashBlockBlankCheck to resume processing to check block erasure that has been stopped by the occurrence of an interrupt.
block erase library	To resume processing to erase blocks that was stopped by the occurrence of an interrupt, call the block blank check library FlashBlockBlankCheck and check whether blocks that should be erased have been erased. Then, call the block erase library FlashBlockErase.
word write library	Call the word write library FlashWordWrite to resume data write processing that was stopped by the occurrence of an interrupt.
block verify library	Call the block verify library FlashBlockVerify to resume block verify processing that was stopped by the occurrence of an interrupt.
set information library	Call the set information library FlashSetInfo to resume flash information setting processing that was stopped by the occurrence of an interrupt.
EEPROM write library	Call the EEPROM write library FlashEEPROMWrite to resume processing to write data during EEPROM emulation that was stopped by the occurrence of an interrupt.

 Table 3-1.
 Resume Processing Stopped by Interrupt

**Remark** An interrupt is not acknowledged until all of the processing of the above self programming sample libraries has been completed, because these libraries execute their processing with interrupts disabled.

# 3.2 Interrupt Response Time

Unlike the case for an ordinary interrupt, generation of an interrupt during execution of self programming is accomplished via post-interrupt servicing in the self programming sample library (such as setting 0x1F as the return value from the self programming sample library). Consequently, the response time is longer than that for an ordinary interrupt.

When an interrupt occurs during self programming execution, both the interrupt response time of the self programming sample library, as well as the interrupt response time of the device used, are necessary.

**Remark** For the response time of each device, refer to the user's manual of each device.

Table 3-2 and Table 3-3 show the interrupt response time of the self programming sample library. Table 3-2 is a case where the internal high-speed oscillator is used to generate the main system clock, and Table 3-3 is a case where an external system clock is used as the main system clock.

	Interrupt Response Time (Unit: Microseconds)						
Library Name	,	nort direct addressing	Entry RAM inside short direct addressing range (from FE20H)				
	Min	Max	Min	Мах			
block blank check library	391.25	1300.5	81.25	727.5			
block erase library	389.25	1393.5	79.25	820.5			
word write library	394.75	1289.5	84.75	716.5			
block verify library	390.25	1324.5	80.25	751.5			
set information library	387 852.5		77	279.5			
EEPROM write library	399.75	1395.5	89.75	822.5			

#### Table 3-2. Interrupt Response Time (with Internal High-Speed Oscillator)

**Remark** An interrupt is not acknowledged until all of the processing of the above self programming sample libraries has been completed, because these libraries execute their processing with interrupts disabled.

	Interrupt Response Time (Unit: Microseconds)						
Library Name	,	hort direct addressing	Entry RAM inside short direct addressing range (from FE20H)				
	Min	Max	Min	Max			
block blank check library	18/fx <sup>Note</sup> + 192	28/fx <sup>Note</sup> + 698	18/fx <sup>Note</sup> + 55	28/fx <sup>Note</sup> + 462			
block erase library	18/fx <sup>Note</sup> + 186	28/fx <sup>Note</sup> + 745	18/fx <sup>Note</sup> + 49	28/fx <sup>Note</sup> + 509			
word write library	22/fx <sup>Note</sup> + 189	28/fx <sup>Note</sup> + 693	22/fx <sup>Note</sup> + 52	28/fx <sup>Note</sup> + 457			
block verify library	18/fx <sup>Note</sup> + 192	28/fx <sup>Note</sup> + 709	18/fx <sup>№te</sup> + 55	28/fx <sup>Note</sup> + 473			
set information library	16/fx <sup>Note</sup> + 190	28/fx <sup>Note</sup> + 454	16/fx <sup>Note</sup> + 53	28/fx <sup>Note</sup> + 218			
EEPROM write library	22/fx <sup>Note</sup> + 191	28/fx <sup>Note</sup> + 783	22/fx <sup>Note</sup> + 54	28/fx <sup>Note</sup> + 547			

### Table 3-3. Interrupt Response Time (with External System Clock)

Note fx: Operating frequency of external system clock

**Remark** An interrupt is not acknowledged until all of the processing of the above self programming sample libraries has been completed, because these libraries execute their processing with interrupts disabled.

# 3.3 Description Example

This section shows an example of writing a user program that resumes erase processing that was stopped by the occurrence of an interrupt during execution of a self programming sample library (block erase library).

<pre></pre>	ERS RTRY:				
<pre>MOV A, #0 ; Sets 0 as the bank number of the block to be erased. MOV B, #10 ; Sets 10 as the block number of the block to be erased. DT ; Disables interrupts. CALL !_PlashBlockErase ; Calls the block erase library. EI ; Enables interrupts. CNP A, #1FH ; Checks whether a stop status is set. BZ \$BLN_RTRY ; If the stop status is set, ; jumps to resume processing BLN_RTRY. CMP A, #00H ; Checks whether execution has been correctly completed. BNZ \$ERS_FALSE_END ; Jumps to abnormal termination ERS_FALSE_END if execution has not been correctly completed. BR ERS_TRUE_END BLN_RTRY: ; Resume processing MOV A, #0 ; Sets 0 as the bank number of the block to be blank-checked. MOV B, #10 ; Sets 10 as the block number of the block to be blank-checked. DI ; Sats 10 as the block number of the block to be blank-checked. DI ; Sats 10 as the block number of the block to be blank-checked. DI ; Sats 10 as the block number of the block to be blank-checked. DI ; Sats 10 as the block number of the block to be blank-checked. DI ; Sats 10 as the block number of the block to be blank-checked. DI ; Sats 10 as the block blank check library. CALL !_FlachBlockBlankCheck EI ; Calls the block blank check library. CALL !_FlachBlockBlankCheck EI ; Checks whether a stop status is set. B2 \$BLN_RTRY ; If the stop status is set. B2 \$BLN_RTRY ; If the stop status is set. B1 ; Checks whether execution has been correctly completed. BNZ \$ERS_RTRY ; Retries the main processing. CMP A, #00H ; Checks whether execution has been correctly completed. BNZ \$ERS_RTRY ; Sats the first address of entry RAM. CALL !_FlashEnv ; Calls the initialize library. ERS_TRUE_END: ; Normal completion ERS_TRUE_END: ; Normal completion</pre>	_				
<pre>MOV B, #10 ; Sets 10 as the block number of the block to be erased. DI ; Disables interrupts. CALL !_FlashBlockErase ; Calls the block erase library. EI ; Enables interrupts. CMP A, #1FH ; Checks whether a stop status is set. EZ \$BLN_RTRY ; If the stop status is set, ; jumps to resume processing BLN_RTRY. CMP A, #00H ; Checks whether execution has been correctly completed. BNZ \$ERS_FALSE_END ; Jumps to abnormal termination ERS_FALSE_END if execution has not been correctly completed. BR ERS_TRUE_END ELN_RTRY: ; Resume processing MOV A, #0 ; Sets 0 as the bank number of the block to be blank-checked. MOV B, #10 ; Sets 10 as the block number of the block to be blank-checked. DI ; Disables interrupts. ; Calls the block blank check library. CALL !_FlashBlockBlankCheck EI ; Enables interrupts. ; retries the resume processing. CMP A, #10H ; Checks whether a stop status is set. BZ \$BLN_RTRY ; If the stop status is set. BZ \$BLN_RTRY ; If the stop status is set. BZ \$BLN_RTRY ; If the stop status is set. BZ \$BLN_RTRY ; Retries the main processing if execution has not been correctly completed. BNZ \$ERS_RTRY ; Retries the main processing if execution has not been correctly completed. BNZ \$ERS_RTRY ; Sats the first address of entry RAM. CALL !_FlashEnv ; Calls the initialize library. ERS_TRUE_END: ; Normal completion ERS_TRUE_END: ; Normal completion</pre>				; Sets 0 as the bank number of the block to be erased.	
CALL 1_FlashBlockErase ; Calls the block erase library. ET ; Enables interrupts. CMP A, 41FH ; Checks whether a stop status is set. BZ \$BLN_RTRY ; If the stop status is set. BZ \$BLN_RTRY ; If the stop status is set. BZ \$BLN_RTRY ; If the stop status is set. BZ \$ERS_FALSE_END ; Jumps to abnormal termination ERS_FALSE_END if execution has not been correctly completed. BR ERS_TRUE_END ELN_RTRY: ; Resume processing MOV A, 40 ; Sets 0 as the bank number of the block to be blank-checked. DI ; Disables interrupts. ; Calls the block blank check library. CALL 1_FlashBlockElankCheck EI ; Enables interrupts. CMP A, 400 ; Sets 0 has not been correctly completed. BZ \$BLN_RTRY ; ; CALL 1_FlashBlockBlankCheck EI ; Enables interrupts. CMP A, 41FH ; Checks whether a stop status is set. BZ \$BLN_RTRY ; If the stop status is set. BZ \$BLN_RTRY ; Retries the resume processing. CMP A, 400H ; Checks whether execution has been correctly completed. BNZ \$ERS_RTRY ; Retries the main processing if execution has not been correctly completed. ENZ \$ERS_RTRY ; Calls the initialize library. CALL 1_FlashBlock to the stop processing MOVW AX, #EntryRAM ; Sets the first address of entry RAM. CALL 1_FlashEnv ; Calls the initialize library. ERS_TRUE_END: ; Normal completion ERS_TRUE_END:		MOV	в, #10	; Sets 10 as the block number of the block to be erased.	
<pre>FI ; Enables interrupts. CMP A, #IFH ; Checks whether a stop status is set. BZ SBLM_RTRY ; If the stop status is set,</pre>		DI		; Disables interrupts.	
<pre>CMP A, #1FH ; Checks whether a stop status is set. BZ \$BLN_RTRY ; If the stop status is set, ; jumps to resume processing BLN_RTRY. CMP A, #00H ; Checks whether execution has been correctly completed. BNZ \$ERS_FALSE_END ; Jumps to abnormal termination ERS_FALSE_END if execution has not been correctly completed. BR ERS_TRUE_END ELN_RTRY: ; Resume processing MOV A, #0 ; Sets 0 as the bank number of the block to be blank-checked. MOV B, #10 ; Sets 10 as the block number of the block to be blank-checked. DI ; Disables interrupts. ; Calls the block blank check library. CALL !_FlashBlockBlankCheck EI ; Enables interrupts. BZ \$BLN_RTRY ; If the stop status is set. BZ \$BLN_RTRY ; If the stop status is set. BZ \$BLN_RTRY ; If the stop status is set. BZ \$BLN_RTRY ; Retries the main processing. CMP A, #OH ; Checks whether execution has been correctly completed. BNZ \$ERS_RTRY ; Retries the main processing if execution has not been correctly completed. ; Clears the internal status of the stop processing MOVW AX, #EntryRAM ; Sets the first address of entry RAM. CALL !_FlashEnv ; Calls the initialize library. ERS_TRUE_END: ERS_FALSE_END:</pre>		CALL	!_FlashBlockErase	; Calls the block erase library.	
<pre>BZ \$BLN_RTRY ; If the stop status is set,</pre>		ΕI		; Enables interrupts.	
<pre>; jumps to resume processing BLN_RTRY. CMP A, #00H ; Checks whether execution has been correctly completed. BNZ \$ERS_FALSE_END ; Jumps to abnormal termination ERS_FALSE_END if execution has not been correctly completed. BR ERS_TRUE_END BLN_RTRY: ; Resume processing MOV A, #0 ; Sets 0 as the bank number of the block to be blank-checked. MOV B, #10 ; Sets 10 as the block number of the block to be blank-checked. DI ; Disables interrupts. ; Calls the block blank check library. CALL !_FlashBlockBlankCheck EI ; Enables interrupts. CMP A, #1FH ; Checks whether a stop status is set. BZ \$BLN_RTRY ; If the stop status is set, ; retries the resume processing. CMP A, #00H ; Checks whether execution has been correctly completed. BNZ \$ERS_RTRY ; Retries the main processing if execution has not been correctly completed. ; Clears the internal status of the stop processing MOW AX, #EntryRAM ; Sets the first address of entry RAM. CALL !_FlashEnv ; Calls the initialize library. ERS_TRUE_END: ; Normal completion ERS_FALSE_END;</pre>		CMP	A, #1FH	; Checks whether a stop status is set.	
<pre>CMP A, #00H ; Checks whether execution has been correctly completed. ENZ \$ERS_FALSE_END ; Jumps to abnormal termination ERS_FALSE_END if execution has not been correctly completed. BR ERS_TRUE_END ELN_RTRY:</pre>		ΒZ	\$BLN_RTRY	; If the stop status is set,	
<pre>completed. BNZ \$ERS_FALSE_END ; Jumps to abnormal termination ERS_FALSE_END if execution has not been correctly completed. BR ERS_TRUE_END BLN_RTRY: ; Resume processing MOV A, #0 ; Sets 0 as the bank number of the block to be blank-checked. MOV B, #10 ; Sets 10 as the block number of the block to be blank-checked. DI ; Disables interrupts. ( alls the block blank check library. CALL !_FlashBlockBlankCheck EI ; Enables interrupts. (CMP A, #1FH ; Checks whether a stop status is set. BZ \$BLN_RTRY ; If the stop status is set, ; retries the resume processing. CMP A, #00H ; Checks whether execution has been correctly completed. BNZ \$ERS_RTRY ; Retries the main processing if execution has not been correctly completed. ; Clears the internal status of the stop processing MOVW AX, #EntryRAM ; Sets the first address of entry RAM. CALL !_FlashEnv ; Calls the initialize library. ERS_TRUE_END: ; Normal completion ERS_FALSE_END: ERS_FALSE_END: ERS_FALSE_END:</pre>				; jumps to resume processing BLN_RTRY.	
execution has not been correctly completed. BR ERS_TRUE_END BLN_RTRY:		CMP	А, #ООН	-	
<pre>BLM_RTRY: ; Resume processing MOV A, #0    ; Sets 0 as the bank number of the block to be</pre>		BNZ	\$ERS_FALSE_END		
<pre>-     ; Resume processing     MOV A, #0         ; Sets 0 as the bank number of the block to be         blank-checked.     MOV B, #10         ; Sets 10 as the block number of the block to be         blank-checked.     DI         ; Disables interrupts.         ; Calls the block blank check library.     CALL !_FlashBlockBlankCheck     EI         ; Enables interrupts.         CMP A, #1FH         ; Checks whether a stop status is set.         BZ \$BLN_RTRY         ; If the stop status is set,             ; retries the resume processing.     CMP A, #00H         ; Checks whether execution has been correctly             completed.     BNZ \$ERS_RTRY         ; Retries the main processing if execution has not been             correctly completed.     ; Clears the internal status of the stop processing     MOVW AX, #EntryRAM         ; Sets the first address of entry RAM.     CALL !_FlashEnv         ; Calls the initialize library.  ERS_TRUE_END:     ; Normal completion ERS_FALSE_END:</pre>		BR	ERS_TRUE_END		
<pre>MOV A, #0 ; Sets 0 as the bank number of the block to be blank-checked. MOV B, #10 ; Sets 10 as the block number of the block to be blank-checked. DI ; Disables interrupts. ; Calls the block blank check library. CALL !_FlashBlockBlankCheck EI ; Enables interrupts. CMP A, #1FH ; Checks whether a stop status is set. BZ \$BLN_RTRY ; If the stop status is set, ; retries the resume processing. CMP A, #00H ; Checks whether execution has been correctly completed. BNZ \$ERS_RTRY ; Retries the main processing if execution has not been correctly completed.</pre>	—				
<pre>blank-checked. MOV B, #10 ; Sets 10 as the block number of the block to be blank-checked. DI ; Disables interrupts. ; Calls the block blank check library. CALL !_FlashBlockBlankCheck EI ; Enables interrupts. CMP A, #1FH ; Checks whether a stop status is set. BZ \$BLN_RTRY ; If the stop status is set, ; retries the resume processing. CMP A, #00H ; Checks whether execution has been correctly completed. BNZ \$ERS_RTRY ; Retries the main processing if execution has not been correctly completed. ; Clears the internal status of the stop processing MOVW AX, #EntryRAM ; Sets the first address of entry RAM. CALL !_FlashEnv ; Calls the initialize library. ERS_TRUE_END: ; Normal completion ERS_FALSE_END:</pre>					
<pre>blank-checked. DI ; Disables interrupts. ; Calls the block blank check library. CALL !_FlashBlockBlankCheck EI ; Enables interrupts. CMP A, #IFH ; Checks whether a stop status is set. BZ \$BLN_RTRY ; If the stop status is set, ; retries the resume processing. CMP A, #00H ; Checks whether execution has been correctly completed. BNZ \$ERS_RTRY ; Retries the main processing if execution has not been correctly completed. ; Clears the internal status of the stop processing MOVW AX, #EntryRAM ; Sets the first address of entry RAM. CALL !_FlashEnv ; Calls the initialize library. ERS_TRUE_END: ; Normal completion ERS_FALSE_END:</pre>		MOV	A, #0		
<pre>; Calls the block blank check library. CALL !_FlashBlockBlankCheck EI : Enables interrupts. CMP A, #IFH : Checks whether a stop status is set. BZ \$BLN_RTRY : If the stop status is set,</pre>		MOV	B, #10		
CALL !_FlashBlockBlankCheck EI ; Enables interrupts. CMP A, #1FH ; Checks whether a stop status is set. BZ \$BLN_RTRY ; If the stop status is set, ; retries the resume processing. CMP A, #00H ; Checks whether execution has been correctly completed. BNZ \$ERS_RTRY ; Retries the main processing if execution has not been correctly completed. ; Clears the internal status of the stop processing MOVW AX, #EntryRAM ; Sets the first address of entry RAM. CALL !_FlashEnv ; Calls the initialize library. ERS_TRUE_END: ; Normal completion ERS_FALSE_END:		DI		; Disables interrupts.	
<pre>EI ; Enables interrupts. CMP A, #1FH ; Checks whether a stop status is set. BZ \$BLN_RTRY ; If the stop status is set, ; retries the resume processing. CMP A, #00H ; Checks whether execution has been correctly completed. BNZ \$ERS_RTRY ; Retries the main processing if execution has not been correctly completed. ; Clears the internal status of the stop processing MOVW AX, #EntryRAM ; Sets the first address of entry RAM. CALL !_FlashEnv ; Calls the initialize library. ERS_TRUE_END: ; Normal completion ERS_FALSE_END:</pre>				; Calls the block blank check library.	
<pre>CMP A, #1FH ; Checks whether a stop status is set. BZ \$BLN_RTRY ; If the stop status is set, ; retries the resume processing. CMP A, #00H ; Checks whether execution has been correctly completed. BNZ \$ERS_RTRY ; Retries the main processing if execution has not been correctly completed. ; Clears the internal status of the stop processing MOVW AX, #EntryRAM ; Sets the first address of entry RAM. CALL !_FlashEnv ; Calls the initialize library. ERS_TRUE_END: ; Normal completion ERS_FALSE_END:</pre>		CALL	!_FlashBlockBlankChe	ck	
<pre>BZ \$BLN_RTRY ; If the stop status is set, ; retries the resume processing. CMP A, #00H ; Checks whether execution has been correctly completed. BNZ \$ERS_RTRY ; Retries the main processing if execution has not been correctly completed. ; Clears the internal status of the stop processing MOVW AX, #EntryRAM ; Sets the first address of entry RAM. CALL !_FlashEnv ; Calls the initialize library. ERS_TRUE_END: ; Normal completion ERS_FALSE_END:</pre>		ΕI		; Enables interrupts.	
<pre>; retries the resume processing. ; retries the resume processing. CMP A, #00H ; Checks whether execution has been correctly completed. BNZ \$ERS_RTRY ; Retries the main processing if execution has not been correctly completed. ; Clears the internal status of the stop processing MOVW AX, #EntryRAM ; Sets the first address of entry RAM. CALL !_FlashEnv ; Calls the initialize library. ERS_TRUE_END: ; Normal completion ERS_FALSE_END:</pre>		CMP	A, #1FH	; Checks whether a stop status is set.	
<pre>CMP A, #00H ; Checks whether execution has been correctly</pre>		ΒZ	\$BLN_RTRY	-	
completed. BNZ \$ERS_RTRY ; Retries the main processing if execution has not been correctly completed. ; Clears the internal status of the stop processing MOVW AX, #EntryRAM ; Sets the first address of entry RAM. CALL !_FlashEnv ; Calls the initialize library. ERS_TRUE_END: ; Normal completion ERS_FALSE_END:					
correctly completed. ; Clears the internal status of the stop processing MOVW AX, #EntryRAM ; Sets the first address of entry RAM. CALL !_FlashEnv ; Calls the initialize library. ERS_TRUE_END: ; Normal completion ERS_FALSE_END:		CMP	А, #ООН		
<pre>MOVW AX, #EntryRAM ; Sets the first address of entry RAM. CALL !_FlashEnv ; Calls the initialize library. ERS_TRUE_END: ; Normal completion ERS_FALSE_END:</pre>		BNZ	\$ERS_RTRY		
CALL !_FlashEnv ; Calls the initialize library. ERS_TRUE_END: ; Normal completion ERS_FALSE_END:		; Clears the internal status of the stop processing			
ERS_TRUE_END: ; Normal completion ERS_FALSE_END:		MOVW	AX, #EntryRAM	; Sets the first address of entry RAM.	
: Normal completion ERS_FALSE_END:		CALL	!_FlashEnv	; Calls the initialize library.	
ERS_FALSE_END:	ERS_TRUE_END:				
		; Nor	mal completion		
; Abnormal termination	ERS_FALSE_END:				
		; Abn	ormal termination		

Caution It is assumed that the entry RAM has already been set.

# 3.4 Cautions

This section explains points to be noted during interrupt servicing.

- If processing related to self programming is performed or a setting related to it is changed during processing of an interrupt that has occurred during execution of self programming, then the operation is not guaranteed. Do not perform processing related to self programming and change settings related to it during interrupt servicing.
- Do not use register bank 3 during interrupt servicing, because self programming uses register bank 3.
- Save and restore registers used for interrupt servicing during interrupt servicing.
- If the set time of the watchdog timer is too short, processing of the set information library may not be completed. Therefore, do not set a time that is too short to the watchdog timer.
   If an interrupt successively occurs during a specific period while processing of the set information library is being executed, an infinite loop may occur if processing of the set information library is resumed after it has been stopped by the interrupt, because the processing is started from the beginning. Therefore, do not allow an interrupt to occur successively at an interval shorter than that within which processing of the set information library is to be completed.

Remark Processing time of set information library (at 8 MHz) Min.: 108 milliseconds Max.: 696 milliseconds

- If multiple interrupts occur during execution of self programming, then the operation is not guaranteed. Disable the acknowledging of multiple interrupts during execution of self programming.
- If processing of the self programming sample library that was stopped by the occurrence of an interrupt is not resumed and processing of another block is to be performed, then the initialize library must be called before the processing of another block is started.
  - **Example** To not resume erase processing of block 0 that was stopped and to execute erase processing of block 1, call the initialize library and then start the erase processing of block 1.
- Do not erase the entry RAM, stack, and data buffer until the series of processing tasks has been completed.
- Allocate an interrupt servicing program in an area other than that of the blocks to be rewritten, just as for the self programming program.

# **CHAPTER 4 BOOT SWAP FUNCTION**

If rewriting of the vector table data, the basic functions of the program, or the self programming area fails because of a momentary power failure or the occurrence of a reset due to an external cause, then the data being rewritten is lost, the user program cannot be restarted by a reset, and rewriting can no longer be performed. This problem can be avoided by using a boot swap function through self programming.

The boot swap function is to replace boot program area, boot cluster  $0^{Note}$ , with the boot swap target area, boot cluster  $1^{Note}$ .

Before rewrite processing is started, a new boot program is written to boot cluster 1. This boot cluster 1 and boot cluster 0 are swapped and boot cluster 1 is used as a boot program area.

As a result, even if a power failure occurs while the boot program area is rewritten, the program is executed correctly because the next reset start program is booted from boot cluster 1. After that, boot cluster 0 can be erased or written as necessary.

**Note** Boot cluster 0 (0000H to 0FFFH): Original boot program area Boot cluster 1 (1000H to 1FFFH): Boot swap target area

Figure 4-1 shows the flow of boot swapping by using the self programming sample library.

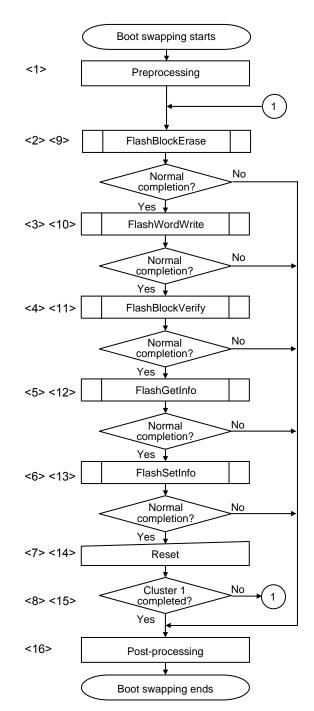


Figure 4-1. Flow of Boot Swapping

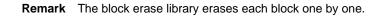
### <1> Preprocessing

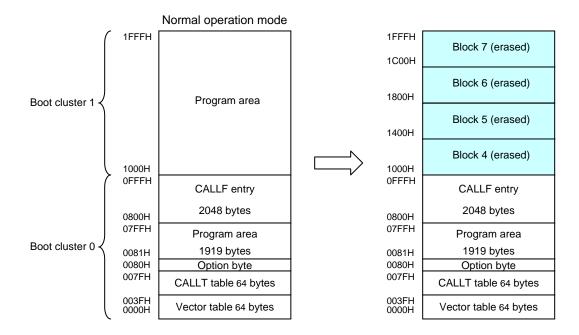
The following preprocessing of boot swapping is performed.

- Setting of hardware environment
- Declaring start of self programming
- Setting of software environment
- Initializing entry RAM
- Checking voltage level

### <2> Erasing boot cluster 1

Blocks 4 to 7 are erased by calling the block erase library FlashBlockErase.

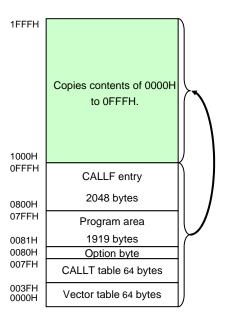




### <3> Copying boot cluster 0

The contents of 0000H to 0FFFH are written to 1000F to 1FFFH by calling the word write library FlashWordWrite.

Remark The word write library writes data in word units (256 bytes max.).



<4> Verifying boot cluster 1

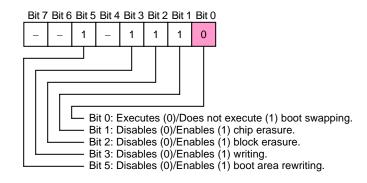
Blocks 4 to 7 are verified by calling the block verify library FlashBlockVerify.

Remark The block verify library verifies each block one by one.

<5> Reading set status of boot swapping The set status of boot swapping can be read by calling the get information library FlashGetInfo.

#### <6> Setting of boot swap bit

Set the boot swap bit to "execute boot swapping (0)" by calling the set information library FlashSetInfo.



#### <7> Occurrence of event

Boot cluster 1 is used as a boot program area when an external reset or overflow of the watchdog timer is generated.

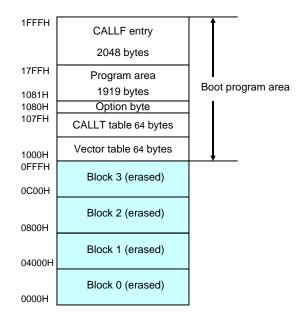
<8> End of swap processing (boot cluster 1)

Operations <2> to <7> complete the swap processing of boot cluster 1

#### <9> Erasing boot cluster 0

Blocks 0 to 3 are erased by calling the block erase library FlashBlockErase.

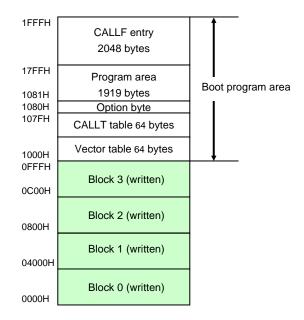
Remark The block erase library erases each block one by one.



#### <10> Writing new program to boot cluster 0

The contents of the new program are written to 0000H to 0FFFH by calling the word write library FlashWordWrite.

**Remark** The word write library writes the program in word units (256 bytes max.).



#### <11> Verifying boot cluster 0

Blocks 0 to 3 are verified by calling the block verify library FlashBlockVerify.

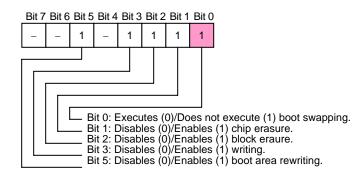
Remark The block verify library verifies each block one by one.

#### <12> Reading set status of boot swapping.

The set status of boot swapping is read by calling the get information library FlashGetInfo.

#### <13> Setting of boot swap bit

Set the boot swap bit to "not execute boot swapping (1)" by calling the set information library FlashSetInfo.



### <14> Occurrence of event

Boot cluster 0 is used as a boot program area when an external reset or overflow of the watchdog timer is generated.

#### <15> End of swap processing (boot cluster 0)

Operations <9> to <14> complete the swap processing of boot cluster 0.

#### <16> Post-processing

As post-processing of boot swapping, the following is performed.

- Declaring end of self programming
- Setting of hardware environment

## CHAPTER 5 SELF PROGRAMMING SAMPLE LIBRARY

This chapter explains details on the self programming sample library. For the source program of each library, refer to **APPENDIX A SAMPLE PROGRAM**.

## 5.1 Type of Self Programming Sample Library

The self programming sample library consists of the following libraries.

Library Marca	Call Example (C language)	Outline	
Library Name Call Example (assembly language)		Outline	
self programming start library	self programming start library FlashStart();		
	CALL !_FlashStart	programming.	
initialize library	<pre>FlashEnv( &amp;EntryRAM[0] );</pre>	Initializes entry RAM.	
	CALL !_FlashEnv		
mode check library	<pre>Status = CheckFLMD( );</pre>	Checks voltage level.	
	CALL !_CheckFLMD		
block blank check library	<pre>Status = FlashBlockBlankCheck(BlankCheckBANK, BlankCheckBlock);</pre>	Checks erasing of specified block (1 KB).	
	CALL !_FlashBlockBlankCheck		
block erase library	<pre>Status = FlashBlockErase( EraseBANK, EraseBlock );</pre>	Erases specified library (1	
	CALL !_FlashBlockErase	KB).	
word write library	Status = FlashWordWrite( &WordAddr, WordNumber, &DataBuffer );	Writes 1- to 64-word data to specified address.	
	CALL !_FlashWordWrite		
block verify library	<pre>Status = FlashBlockVerfy(VerifyBANK, VerifyBlock);</pre>	Verifies specified block (1	
CALL !_FlashBlockVerify		KB) (internal verification).	
self programming end library	FlashEnd( );	Declares end of self	
	CALL !_FlashEnd	programming.	
get information library	get information library Status = FlashGetInfo( &GetInfo, &DataBuffer );		
	CALL !_FlashGetInfo		
set information library	<pre>Status = FlashSetInfo( SetInfoData );</pre>	Changes setting of flash	
	CALL !_FlashSetInfo		
EEPROM write library Status = FlashEEPROMWrite( &WordAdder,		Writes 1- to 64-word data to	
	WordNumber, &DataBuffer );	specified address (during	
	CALL !_EEPROMWrite	EEPROM emulation).	

Table 5-1. Self programming sample library List

## 5.2 Explanation of Self Programming Sample Library

Each self programming sample library is explained in the following format.

## self programming sample library name

### [Outline]

Outlines the function of the self programming sample library.

#### [Format]

Indicates a format to call the self programming sample library from a user program described in C or an assembly language.

#### Caution In this manual, the data type name is defined as follows.

Definition Name	Data Type
UCHAR	unsigned char
USHORT	unsigned short

#### [Argument]

Indicates the argument of the self programming sample library.

#### [Return value]

Indicates the return value from the self programming sample library.

#### [Function]

Indicates the function details and points to be noted for the self programming sample library.

#### [Register status after calling]

Indicates the status of registers after the self programming sample library is called.

#### [Stack size]

Indicates the size of the stack used by the self programming sample library.

### [ROM capacity]

Indicates the ROM capacity necessary for self programming.

#### [Call example]

Indicates an example of calling the self programming sample library from a user program described in C or an assembly language.

#### [Supplement]

Indicates supplementary information on a self programming sample library other than the above.

## [Flow]

This indicates the program flow of the self programming sample library.

## self programming start library

#### [Outline]

Declares the start of self programming.

#### [Format]

```
<Clanguage>
void FlashStart(void)
```

#### <Assembly language>

```
CALL !_FlashStart
```

#### [Argument]

None

#### [Return value]

None

#### [Function]

This self programming sample library declares the start of self programming. Therefore, call this library first as a self programming operation.

Caution The operation is not guaranteed if this library is called with interrupts enabled. Before calling this library, execute the DI instruction, and execute the EI instruction after execution of this library is completed, so that acknowledgment of an interrupt is disabled while this library is executed.

#### [Register status after calling]

No register is cleared.

#### [Stack size]

0 bytes

#### [ROM capacity]

12 bytes

## [Call example]

<c language=""></c>	
di();	/* Disables interrupts. */
<pre>FlashStart();</pre>	<pre>/* Calls self programming start library. */</pre>
ei();	/* Enables interrupts. */

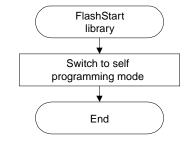
#### <Assembly language>

DI		; Disables interrupts.	
CALL	!_FlashStart	; Calls self programming start library.	
ΕI		; Enables interrupts.	

## [Flow]

Figure 5-1 shows the flow of the self programming start library.





## initialize library

#### [Outline]

Initializes entry RAM.

#### [Format]

<c langu<="" th=""><th>lage&gt;</th><th></th><th></th></c>	lage>		
void	FlashEnv( US	HORT EntryRAM	)

#### <Assembly language>

4 100011101	i i i gaage
CALL	!_FlashEnv

#### [Argument]

#### <C language>

Argument	Explanation
USHORT EntryRAM	First address of entry RAM <sup>Note</sup>

#### <Assembly language>

Argument	Explanation
AX	First address of entry RAM <sup>Note</sup>

Note For details on entry RAM, refer to 2.2.1 Entry RAM.

#### [Return value]

None

#### [Function]

This self programming sample library secures and initializes the entry RAM used for self programming.

As initialize processing, this library secures 100 bytes from an address specified by the parameter as a work area where the flash memory writing firmware operates, and sets the initial value to the first address +06H to +16H. The other areas are cleared to 0.

**Remark** Call this library after calling the self programming start library.

Also call this library to resume processing of a library executing self programming that was stopped by the occurrence of an interrupt.

#### [Register status after calling]

No register is cleared.

[Stack size]

30 bytes

## [ROM capacity]

11 bytes

<c language=""></c>				
USHORT EntryRAM;	/* Declares variable. */			
<pre>FlashEnv( &amp;EntryRAM[0] );</pre>	/* Calls initialize library. */			

#### <Assembly language>

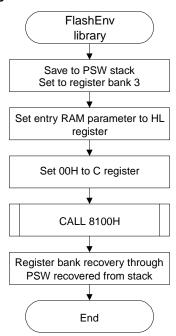
SELF_RAM	DSEG AT	OFDBCH	
EntryRAM: DS	100		
SELF_PROG	CSEG		
MOVW AX, #E	ntryRAM	; Sets firs	t address of entry RAM.
CALL !_Flas	hEnv	; Calls ini	tialize library.

Caution Allocate the entry RAM at any address of the internal high-speed RAM outside of the short direct addressing range.

To allocate it in the internal high-speed RAM in the short direct addressing range, the first address is set to FE20H.

#### [Flow]

Figure 5-2 shows the flow of the initialize library.



#### Figure 5-2. Flow of Initialize Library

## mode check library

#### [Outline]

Checks the voltage level.

#### [Format]

•	<c langua<="" th=""><th>age&gt;</th><th></th><th></th><th></th></c>	age>			
	UCHAR	CheckFLMD(	void	)	

#### <Assembly language>

	language/
CALL	_CheckFLMD

#### [Argument]

None

#### [Return value]

Status	Explanation	
00H	Normal completion – FLMD0 pin is at high level.	
01H	Abnormal termination – FLMD0 pin is at low level.	

**Remark** The status is the UCHAR type in C and is stored in the A register in an assembly language.

#### [Function]

This library checks the voltage level (high or low) of the FLMD0 pin.

- **Remark** Call this library after calling the self programming start library to check the voltage level of the FLMD0 pin.
- Caution If the FLMD0 pin is at low level, operations such as erasing and writing the flash memory cannot be performed. To manipulate the flash memory by self programming, it is necessary to call this library and confirm that the FLMD0 pin is at high level.

#### [Register status after calling]

Memory Model	Register Status	
Normal model	Registers cleared: A, BC Registers held: X, DE, HL	
Static model	Registers cleared: A Registers held: X, BC, DE, HL	

#### [Stack size]

28 bytes

## [ROM capacity]

Memory Model	ROM Capacity	
Normal model	14 bytes	
Static model	11 bytes	

## [Call example]

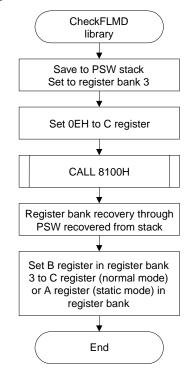
<c language=""></c>	
UCHAR Status;	/* Declares variable.*/
<pre>Status = CheckFLMD();</pre>	/* Calls mode check library and */ /* stores status information. */

#### <Assembly language>

SELF_RAM DSEG	
Status: DS 1	
SELF_PROG CSEG	
CALL !_CheckFLMD	; Calls mode check library.
MOV !Status, A	; Stores status information.

#### [Flow]

Figure 5-3 shows the flow of the mode check library.



#### Figure 5-3. Flow of Mode Check Library

## block blank check library

### [Outline]

Checks erasing of a specified block (1 KB).

## [Format]

4	<c langua<="" th=""><th>age&gt;</th><th></th><th></th><th></th><th></th></c>	age>				
	UCHAR	FlashBlockBlankCheck(	UCHAR	BlankCheckBANK,	UCHAR	BlankCheckBlock )

### <Assembly language>

#### [Argument]

### <C language>

Argument Explanation	
UCHAR BlankCheckBANK	Bank number of block to be blank-checked.
UCHAR BlankCheckBlock	Block number of block to be blank-checked.

#### <Assembly language>

Argument Explanation	
А	Bank number of block to be blank-checked.
В	Block number of block to be blank-checked.

**Remark** Set the bank number to 0 when a product with which no bank number has to be set is used.

#### [Return value]

Status	Explanation
00H	Normal completion Specified block is blank (erase processing has been completed).
05H	Parameter error Specified bank number or block number is outside the settable range.
1BH	Blank check error Specified block is not blank (erase processing has not been completed).
1FH	Processing is stopped because an interrupt occurs. An interrupt occurs while processing of this library is under execution.

**Remark** The status is the UCHAR type in C and is stored in the A register in an assembly language.

#### [Function]

This library checks if a specified block (1 KB) has been erased.

- **Remark** Because only one block is checked at a time, call this library as many times as required to check two or more blocks.
- Caution The operation is not guaranteed if this library is called with interrupts enabled. Before calling this library, execute the DI instruction, and execute the EI instruction after execution of this library is completed, so that acknowledgment of an interrupt is disabled while this library is executed.

#### [Register status after calling]

Memory Model	Register Status
Normal model	Registers cleared: AX, BC Registers held: DE, HL
Static model	Registers cleared: A, BC Registers held: X, DE, HL

#### [Stack size]

Memory Model	Stack Size	
Normal model	37 bytes	
Static model	35 bytes	

#### [ROM capacity]

Memory Model ROM Capacity		
Normal model	67 bytes (of which 30 bytes are common routine)	
Static model	54 bytes (of which 30 bytes are common routine)	

<c language=""></c>	
UCHAR Status;	/* Declares variable. */
UCHAR BlankCheckBA	NK; /* Declares variable. */
UCHAR BlankCheckBl	ock; /* Declares variable. */
BlankCheckBANK = 0;	/* Sets bank number of block to be blank-checked to 0. */
BlankCheckBlock = 1	10; /* Sets block number of block to be blank-checked to 10. */
	/* Calls block blank check library and */
	<pre>/* stores status information.*/</pre>
di();	/* Disables interrupts. */
Status = FlashBlock	<pre>KBlankCheck ( BlankCheckBANK, BlankCheckBlock );</pre>
ei();	/* Enables interrupts. */

## <Assembly language>

SELF_RAM	DSEG	
Status: DS	1	
SELF_PROG	CSEG	
MOV A, #	ŧO	; Sets bank number of block to be blank-checked to 0.
MOV B, #	ŧ10	; Sets block number of block to be blank-checked to 10.
		; Calls block blank check library.
DI		; Disables interrupts.
CALL !_Fl	ashBlockBlankCh	eck
MOV !Sta	atus, A	; Stores status information.
EI		; Enables interrupts.

## [Flow]

Figure 5-4 shows the flow of the block blank check library.

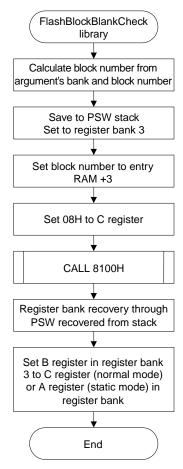


Figure 5-4. Flow of Block Blank Check Library

## block erase library

### [Outline]

Erases a specified block (1 KB).

## [Format]

•	<c language=""></c>						
	UCHAR	FlashBlockErase(	UCHAR	EraseBANK,	UCHAR	EraseBlock	)

#### <Assembly language>

CALL	! FlashBlockErase	

## [Argument]

### <C language>

Argument	Explanation	
UCHAR EraseBANK	Bank number of block to be erased	
UCHAR EraseBlock	Block number of block to be erased.	

#### <Assembly language>

Argument	Explanation
A Bank number of block to be erased	
B Block number of block to be erased.	

**Remark** Set the bank number to 0 when a product with which no bank number has to be set is used.

#### [Return value]

Status	Explanation
00H	Normal completion
05H	Parameter error Specified bank number or block number is outside the settable range.
10H	Protect error Specified block is included in the boot area and rewriting the boot area is disabled.
1AH	Erase error An error occurred during processing of this library.
1FH	Processing is stopped by the occurrence of an interrupt. An interrupt occurred while processing of this library was under execution.

**Remark** The status is the UCHAR type in C and is stored in the A register in an assembly language.

#### [Function]

This library erases a specified block (1 KB).

- **Remark** Because only one block is erased at a time, call this library as many times as required to erase two or more blocks.
- Caution The operation is not guaranteed if this library is called with interrupts enabled. Before calling this library, execute the DI instruction, and execute the EI instruction after execution of this library is completed, so that acknowledgment of an interrupt is disabled while this library is executed.

#### [Register status after calling]

Memory Model	Register Status	
Normal model	Registers cleared: AX, BC Registers held: DE, HL	
Static model	Registers cleared: A, BC Registers held: X, DE, HL	

#### [Stack size]

Memory Model	Stack Size	
Normal model	39 bytes	
Static model	37 bytes	

#### [ROM capacity]

Memory Model ROM Capacity		
Normal model	67 bytes (of which 30 bytes are common routine)	
Static model	54 bytes (of which 30 bytes are common routine)	

```
<C language>
                                 /* Declares variable. */
UCHAR Status;
UCHAR EraseBANK;
                                 /* Declares variable. */
UCHAR EraseBlock;
                                  /* Declares variable. */
EraseBANK = 0;
                                 /* Sets bank number of block to be erased to 0. */
EraseBlock = 10;
                                  /* Sets block number of block to be erased to 10. */
                                  /* Disables interrupts. */
di();
                                  /* Calls block erase library and stores status */
                                  /* information. */
Status = FlashBlockErase( EraseBANK, EraseBlock );
ei();
                                  /* Enables interrupts. */
```

#### <Assembly language>

SELF_RAM DSE	G	
Status: DS 1		
SELF_PROG CSE	G	
MOV A, #0	;	Sets bank number of block to be erased to 0.
MOV B, #10	;	Sets block number of block to be erased to 10.
DI	;	Disables interrupts.
CALL !_FlashBloc	kErase ;	Calls block erase library.
MOV !Status, A	· ;	Stores status information.
EI	;	Enables interrupts.

## [Flow]

Figure 5-5 shows the flow of the block erase library.

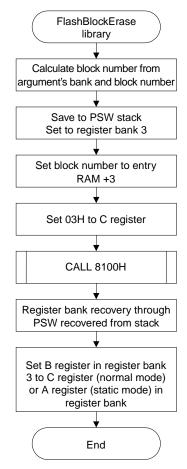


Figure 5-5. Flow of Block Erase Library

## word write library

#### [Outline]

Writes 1- to 64-word data to specified addresses.

#### [Format]

#### <Assembly language>

CALL ! FlashWordWrite

#### [Argument]

<C language>

Argument	Explanation
struct stWordAddress *ptr	First address of write start address structure (stWordAddress) <sup>Note 1</sup> . This structure must be 3 bytes in size and at a 4-byte boundary and must be secured by the user.
UCHAR WordNumber	Number of data to be written (1 to 64)
USHORT DataBufferAddress	First address of write data buffer <sup>Note 2</sup>

#### <Assembly language>

Argument	Explanation
АХ	First address of data having structure same as that of write start address structure <sup>Note 1</sup> in C (Refer to <b>APPENDIX A SAMPLE PROGRAM</b> .)
В	Number of data to be written (1 to 64)
HL	First address of write data buffer <sup>Note 2</sup>

#### Notes 1. Write start address structure

struct stWordAdd	lress{		
USHORT Wr	iteAddress; /*	Write start	address*/
UCHAR Wr	iteBank; /*	Bank number	of write start address*/
};			

Remarks 1. Specify the write start address as a multiple of 4 bytes.

2. Set the bank number to 0 when a product with which no bank number has to be set is used.

Caution Before calling this library, set a value to each member of this structure.

- 2. Before calling this library, set write data to the write data buffer (whose first address is indicated by DataBufferAddress).
- Caution Set the write start address and the number of data to be written so that they do not straddle over the boundary of each block.

#### [Return value]

Status	Explanation
00H	Normal completion
05H	<ul> <li>Parameter error</li> <li>Start address not is a multiple of 1 word (4 bytes).</li> <li>The number of data to be written is 0.</li> <li>The number of data to be written exceeds 64 words.</li> <li>Write end address (Start address + (Number of data to be written × 4 bytes)) exceeds the flash memory area.</li> </ul>
10H	Protect error – Specified range includes the boot area and rewriting the boot area is disabled.
1CH	Write error – Data is verified but does not match after execution of the processing of this library.
1FH	Processing is stopped by the occurrence of an interrupt. – An interrupt occurred while processing of this library was under execution.

**Remark** The status is the UCHAR type in C and is stored in the A register in an assembly language.

#### [Function]

This library writes the specified number of data from a specified address.

Set a RAM area containing the data to be written as a data buffer and call this library.

Data of up to 256 bytes can be written (in 4-byte units) at one time.

**Remark** Call this library as many times as required to write data of more than 256 bytes.

- Cautions 1. After writing data, execute verification (internal verification) of the block including the range in which the data has been written. If verification is not executed, the written data is not guaranteed.
  - 2. The operation is not guaranteed if this library is called with interrupts enabled. Before calling this library, execute the DI instruction, and execute the EI instruction after execution of this library is completed, so that acknowledgment of an interrupt is disabled while this library is executed.

#### [Register status after calling]

Memory Model	Register Status	
Normal model	Registers cleared: AX, BC, DE Registers held: HL	
Static model	Registers cleared: AX, C Registers held: B, DE, HL	

## [Stack size]

39 bytes

#### [ROM capacity]

Memory Model	ROM Capacity
Normal model	117 bytes (of which 57 bytes are common routine)
Static model	100 bytes (of which 57 bytes are common routine)

```
<C language>
UCHAR DataBuffer[4];
                             /* Declares variable. */
UCHAR WordNumber;
                             /* Declares variable. */
UCHAR Status;
                              /* Declares variable. */
                             /* Sets data to be written. */
DataBuffer[0] = 0x11;
DataBuffer[1] = 0x22;
                             /* Sets data to be written. */
                             /* Sets data to be written. */
DataBuffer[2] = 0x33;
DataBuffer[3] = 0x44;
                             /* Sets data to be written. */
WordNumber = 1;
                              /* Sets number of data to be written. */
WordAddr.WriteAddress = 0xA000; /* Sets 0xA000H as write start address. */
                              /* Sets bank number of write start address to 0. */
WordAddr.WriteBANK = 0;
                               /* Disables interrupts. */
di();
                               /* Calls word write library and stores status */
                               /* information. */
Status = FlashWordWrite( &WordAddr, WordNumber, &DataBuffer );
                              /* Enables interrupts. */
ei();
```

<assemt< th=""><th>oly language&gt;</th><th></th></assemt<>	oly language>		
SELF_H			
DataBu	DataBuffer: DS 4		
WordAd	ddr:		
Write	Address: DS 2		
Write	Bank: DS 1		
Status	s: DS 1		
SELF_I	PROG CSEG		
MOV	A, #11H		
-	P, #11n !DataBuffer, A	; Sets data to be written.	
	A, #22H	, Sets data to be willten.	
	!DataBuffer+1, A	; Sets data to be written.	
	A, #33H	, Sets data to be written.	
	!DataBuffer+2, A	; Sets data to be written.	
	A, #44H		
MOV	!DataBuffer+3, A	; Sets data to be written.	
MOTITAL	лу #0л000u		
MOVW MOVW	AX, #0A000H !WriteAddress, AX	; Sets 0xA000H as write start address.	
MOVW	:WIILEAUUIESS, AA	, Sets UXAUUUN as wille Start audiess.	
MOV	A, #0		
MOV	!WriteBANK, A	; Sets bank number of write start address to 0.	
MOVW	AX, #WordAddr	; Sets first address of write start address	
struct			
MOV	B, #1	; Sets number of data to be written.	
MOVW	HL, #DataBuffer	; First address of write data buffer	
DI		; Disables interrupts.	
CALL	!_FlashWordWrite	; Calls word write library.	
MOV	_ !Status, A	; Stores status information.	
ΕI		; Enables interrupts.	

## [Flow]

Figure 5-6 shows the flow of the word write library.

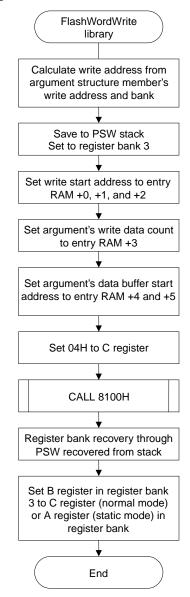


Figure 5-6. Flow of Word Write Library

## block verify library

### [Outline]

Verifies (internal verification) a specified block (1 KB).

Caution Verification (internal verification) is a function to check if data written to the flash memory is written at a sufficient level, and is different from verification that compares data.

## [Format]

<C language>
UCHAR FlashBlockVerify( UCHAR VerifyBANK, UCHAR VerifyBlock )

#### <Assembly language>

|--|

#### [Argument]

#### <C language>

Argument	Explanation
UCHAR VerifyBANK	Bank number of block to be verified
UCHAR VerifyBlock	Block number to be verified

#### <Assembly language>

Argument	Explanation
А	Bank number of block to be verified
В	Block number to be verified

**Remark** Set the bank number to 0 when a product with which no bank number has to be set is used.

#### [Return value]

Status	Explanation
00H	Normal completion
05H	Parameter error Specified bank number or block number is outside the settable range.
1BH	Verify (internal verify) error An error occurs during processing of this library.
1FH	Processing is stopped by the occurrence of an interrupt. An interrupt occurred while processing of this library was under execution.

**Remark** The status is the UCHAR type in C and is stored in the A register in an assembly language.

### [Function]

This library verifies (internal verification) a specified block (1 KB).

- **Remark** Call this library as many times as required to verify two or more blocks, because only one block is verified at a time.
- Cautions 1. After writing data, verify (internal verification) the block including the range in which the data has been written. If verification is not executed, the written data is not guaranteed.
  - 2. The operation is not guaranteed if this library is called with interrupts enabled. Before calling this library, execute the DI instruction, and execute the EI instruction after execution of this library is completed, so that acknowledgment of an interrupt is disabled while this library is executed.

#### [Register status after calling]

Memory Model	Register Status	
Normal model	Registers cleared: AX, BC Registers held: DE, HL	
Static model	Registers cleared: A, BC Registers held: X, DE, HL	

#### [Stack size]

Memory Model	Stack Size
Normal model	37 bytes
Static model	35 bytes

#### [ROM capacity]

Memory Model	ROM Capacity
Normal model	67 bytes (of which 30 bytes are common routine)
Static model	54 bytes (of which 30 bytes are common routine)

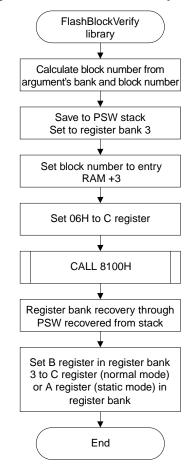
<c language=""></c>		
UCHAR Status;	/* Declares variable. */	
UCHAR VerifyBANK;	/* Declares variable. */	
UCHAR VerifyBlock;	/* Declares variable. */	
VerifyBANK = 0;	/* Sets bank number of block to be verified to 0. */	
<pre>VerifyBlock = 10;</pre>	/* Sets block number of block to be verified to 10. */	
di();	/* Disables interrupts. */	
	/* Calls block verify library and stores */	
	/* status information. */	
<pre>Status = FlashBlockVerify( VerifyBANK, VerifyBlock );</pre>		
ei();	/* Enables interrupts. */	

#### <Assembly language>

SELF\_RAM DSEG Status: DS 1 SELF\_PROG CSEG ; Sets bank number of block to be verified to 0. MOV A, #0 в**,** #10 MOV ; Sets block number of block to be verified to 10. DI ; Disables interrupts. CALL !\_FlashBlockVerify ; Calls block verify library. MOV !Status, A ; Stores status information. ΕI ; Enables interrupts.

## [Flow]

Figure 5-7 shows the flow of the block verify library.





## self programming end library

### [Outline]

Declares the end of self programming.

## [Format]

```
<C language>
void FlashEnd( void )
```

#### <Assembly language>

```
CALL !_FlashEnd
```

#### [Argument]

None

#### [Return value]

None

#### [Function]

This library declares the end of self programming.

It completes writing to the flash memory and restores the normal operation mode.

#### **Remarks 1.** Call this library at the end of the self programming operation.

- 2. After execution of this library is completed, the level of the FLMD0 pin is returned to low.
- Caution The operation is not guaranteed if this library is called with interrupts enabled. Before calling this library, execute the DI instruction, and execute the EI instruction after execution of this library is completed, so that acknowledgment of an interrupt is disabled while this library is executed

### [Register status after calling]

No register is cleared.

#### [Stack size]

0 bytes

### [ROM capacity]

12 bytes

<c language=""></c>	
di();	/* Disables interrupts. */
<pre>FlashEnd();</pre>	<pre>/* Calls self programming end library. */</pre>
ei();	/* Enables interrupts. */

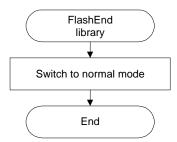
#### <Assembly language>

DI	· · ·	; Disables interrupts.	
CALL	!_FlashEnd	; Calls self programming end library.	
EI		; Enables interrupts.	

### [Flow]

Figure 5-8 shows the flow of the self programming end library.





## get information library

#### [Outline]

Reads flash information.

## [Format]

<C language>
UCHAR FlashGetInfo( struct stGetInfo \*ptr, USHORT DataBufferAddress )

#### <Assembly language>

CALL	!_FlashGetInfo	

### [Argument]

#### <C language>

Argument	Explanation
struct stGetInfo *ptr	First address of flash information acquisition structure (stGetInfo) <sup>№00</sup> . This structure is 3 bytes in size and must be secured by the user.
USHORT DataBufferAddress	First address of acquired data storage buffer

#### <Assembly language>

Argument	Explanation
АХ	First address of data having the same structure as flash information acquisition structure in C <sup>Note</sup> (Refer to <b>APPENDIX A SAMPLE PROGRAM</b> .)
BC	First address of acquired data storage buffer

#### **Note** Flash information acquisition structure

```
Struct stGetInfo{
    UCHAR OptionNumber; /* Option value<sup>Note</sup> */
    UCHAR GetInfoBank; /* Bank number (valid if option value is 05H) */
    UCHAR GetInfoBlock; /* Block number (valid if option value is 05H) */
};
```

#### Note Refer to [Supplement].

Remark Set the bank number to 0 when a product with which no bank number has to be set is used.

# Cautions 1. Setting of a bank number and a block number is invalid when security flag information and boot flag information are checked.

2. Before calling this library, set a value to each member of this structure.

#### [Return value]

Status	Explanation
00H	Normal completion
05H	Parameter error - Specified option value is outside the settable range.
20H	Read error - Security flag is read twice and different data are read when the option value is set to 03H.

Remark The status is the UCHAR type in C and is stored in the A register in an assembly language.

# Caution Flash information corresponding to a specified option value is stored in the data buffer. For details on the flash information, refer to [Supplement].

### [Function]

This library reads flash information.

It is used to check the set information (security flag, boot flag information, and last address of a specified block) of the flash memory.

Caution The operation is not guaranteed if this library is called with interrupts enabled. Before calling this library, execute the DI instruction, and execute the EI instruction after execution of this library is completed, so that acknowledgment of an interrupt is disabled while this library is executed.

#### [Register status after calling]

Memory Model	Register Status
Normal model	Registers cleared: AX, BC, DE Registers held: HL
Static model	Registers cleared: AX, BC, HL Registers held: DE

#### [Stack size]

38 bytes

#### [ROM capacity]

Memory Model	ROM Capacity
Normal model	161 bytes (of which 30 bytes are common routine)
Static model	148 bytes (of which 30 bytes are common routine)

<c language=""></c>		
Struct stGetInfo GetInfo;	/* Declares variable. */	
UCHAR DataBuffer[3];	/* Declares variable. */	
UCHAR Status;	/* Declares variable. */	
GetInfo.OptionNumber = 5;	/* Specifies option value to "get last address */	
	/* of specified block". */	
<pre>GetInfo.GetInfoBank = 0;</pre>	/* Sets bank number of block whose flash */	
	/* information is to be acquired to 0. */	
<pre>GetInfo.GetInfoBlock = 10;</pre>	/* Sets block number of block whose flash $\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \$	
	/* information is to be acquired to 10. */	
di();	/* Disables interrupts. */	
	/* Calls get information library and stores status */	
	/* information. */	
<pre>Status = FlashGetInfo( &amp;GetInfo, &amp;DataBuffer );</pre>		
ei();	/* Enables interrupts. */	

<Assembly language>

SELF_RAM DSE	EG	
DataBuffer: DS 3		
GetInfo:		
OptionNumber: DS	1	
GetInfoBank: DS	1	
GetInfoBlock: DS	1	
Status: DS 1		
SELF_PROG CSE	EG	
MOV A, #5		
MOV OptionNum	ber, A ;	Specifies option value to "get last address of
MOV A, #0	;	specified block".
MOV GetInfoBa	nk, A ;	Sets bank number of block whose flash
MOV A, #10	;	information is to be acquired to 0.
MOV GetIngoBlo	ock, A ;	Sets block number of block whose flash
	;	information is to be acquired to 10.
MOVW AX, #GetIn	nfo	
MOVW BC, #Data	Buffer	
DI	;	Disables interrupts.
CALL !_FlashGet	tInfo ;	Calls get information library.
MOV !Status,	A ;	Stores status information.
EI	;	Enables interrupts.

#### [Supplement]

The flash information that can be acquired differs depending on the option value specified by the flash information acquisition structure.

The information corresponding to each option value is shown below.

Option Value	Information Acquired
03H	Security flag information (2 bytes)
04H	Boot flag information (1 byte)
05H	Last address of specified block (3 bytes)

Each piece of information is detailed below.

#### (1) Security flag information (option value: 03H)

The setting status of the security flag is stored as data of 2 bytes in the data buffer from its beginning.

Offset	Contents
+0	Security flag information Note
+1	Last block number of boot area (fixed to 03H)

#### **Note** Details on security flag information

Security Flag	Contents
Bit 0	Chip erase enable flag 0: Disabled 1: Enabled
Bit 1	Block erase enable flag 0: Disabled 1: Enabled
Bit 2	Write enable flag 0: Disabled 1: Enabled
Bit 4	Boot area rewrite disable flag 0: Disabled 1: Enabled
Other than above	Always 1

#### (2) Boot flag information (option value: 04H)

The boot flag information (setting status of boot swapping) is stored in the data buffer as data of 1 byte.

Offset	Contents
+0	Boot flag information <sup>Note</sup>

#### Note Details on boot flag information

Offset	Contents
00H	Boot areas are not swapped. (Reset and started from address 0000H)
01H	Boot areas are swapped. (Reset and started from address 1000H)

#### (3) Last address of specified block (option value: 05H)

The last address of the specified block is stored in the data buffer from its beginning as data of 3 bytes.

Offset	Contents
+0	Block last address (Low)
+1	Block last address (High)
+2	Bank number

#### Example Where the last address for block of block number 00H is 0003FFH

	-	-	-	+05H		-			
<u>FFH</u>	03H	<u>00H</u>	ххх	ххх	ххх	ххх	ххх	ххх	

## [Flow]

Figure 5-9 shows the flow of the get information library.

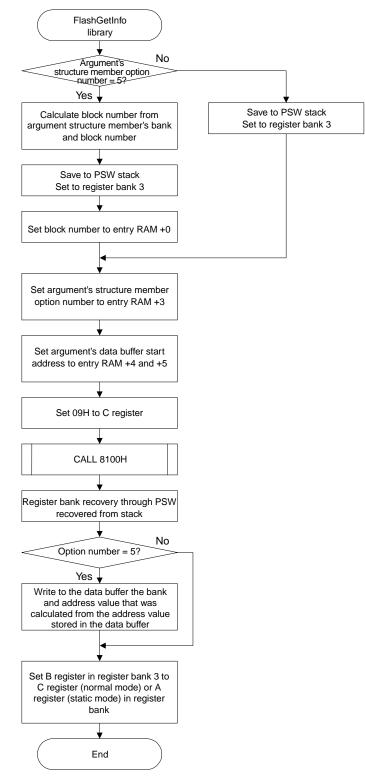


Figure 5-9. Flow of Get Information Library

## set information library

## [Outline]

Changes setting of flash information.

## [Format]

<c language=""></c>							
UCHAR	FlashSetInfo(	UCHAR	SetInfoData	)			

#### <Assembly language>

CALL	!_FlashSetInfo

## [Argument]

## <C language>

Argument	Explanation
UCHAR SetInfoData	Flash information data <sup>Note</sup>

### <Assembly language>

Argument	Explanation
А	Flash information data <sup>Note</sup>

#### Note Details on flash information data

Flash Information Data	Contents
Bit 0	0: Swaps boot areas. 1: Does not swap boot areas.
Bit 1	0: Disables chip erasure. 1: Enables chip erasure.
Bit 2	0: Disables block erasure. 1: Enables block erasure.
Bit 3	0: Disables writing. 1: Enables writing.
Bit 5	0: Disables writing boot area. 1: Enables writing boot area.
Other than above	Always 1

Status	Explanation
00H	Normal completion
05H	Parameter error Bit 0 of the information flag value was cleared to 0 for a product that does not support boot swapping.
10H	<ul><li>Protect error</li><li>Attempt was made to enable a flag that has already been disabled.</li><li>Attempt was made to change the boot area swap flag while rewriting of the boot area was disabled.</li></ul>
1AH	Erase error - An erase error occurred while processing of this library was under execution.
1BH	Verify (internal verify) error - A verify error occurred while processing of this library was under execution.
1CH	Write error - A write error occurred while processing of this library was under execution.
1FH	Processing is stopped by the occurrence of an interrupt. - An interrupt occurred while processing of this library was under execution.

**Remark** The status is the UCHAR type in C and is stored in the A register in an assembly language.

#### [Function]

This library changes the setting of the flash information.

It is used to change the set information (security flag and boot flag information) of the flash memory.

#### Cautions 1. A flag that has already disabled processing cannot be changed to enable the processing.

2. The operation is not guaranteed if this library is called with interrupts enabled. Before calling this library, execute the DI instruction, and execute the EI instruction after execution of this library is completed, so that acknowledgment of an interrupt is disabled while this library is executed.

#### [Register status after calling]

Memory Model	Register Status
Normal model	Registers cleared: A, BC Registers held: X, DE, HL
Static model	Registers cleared: A
	Registers held: X, BC, DE, HL

#### [Stack size]

37 bytes

#### [ROM capacity]

Memory Model	ROM Capacity	
Normal model	27 bytes	
Static model	23 bytes	

#### [Call example]

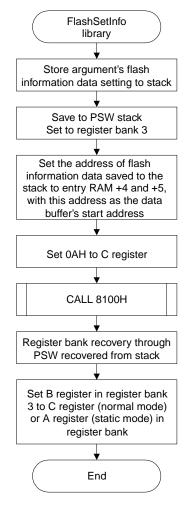
<c language=""></c>			
UCHAR	Status;	/*	Declares variable. */
UCHAR	SetInfoData;	/*	Declares variable. */
SetInf	oData = 0b11111101;	/*	Sets flash information data to "disable chip erase".*/
di();		/*	Disables interrupts. */
		/*	Calls set information library and stores status $^{\star/}$
		/*	information. */
Status	= FlashSetInfo( Set	Inf	oData );
ei();		/*	Enables interrupts. */

#### <Assembly language>

```
SELF_RAM DSEG
Status: DS 1
SELF_PROG CSEG
MOV A, #1111101B ; Sets flash information data to "disable chip erase".
DI ; Disables interrupts.
CALL !_FlashSetInfo ; Calls set information library.
MOV !Status, A ; Stores status information.
EI ; Enables interrupts.
```

#### [Flow]

Figure 5-10 shows the flow of the set information library.



#### Figure 5-10. Flow of Set Information Library

# **EEPROM** write library

#### [Outline]

Writes 1 to 64 word data to a specified address (during EEPROM emulation).

#### [Format]

#### 

#### <Assembly language>

CALL !\_EEPROMWrite

#### [Argument]

<C language>

Argument	Explanation
struct stWordAddress *ptr	First address of write start address structure (stWordAddress) <sup>Note 1</sup> . This structure must be 3 bytes in size and at a 4-byte boundary, and must be secured by the user.
UCHAR WordNumber	Number of data to be written (1 to 64)
USHORT DataBufferAddress	First address of write data buffer <sup>Note 2</sup>

#### <Assembly language>

Argument	Explanation	
AX	First address of data having the same structure as the write start address structure <sup>Note 1</sup> in C (Refer to <b>APPENDIX A SAMPLE PROGRAM</b> .)	
В	Number of data to be written (1 to 64)	
HL	First address of write data buffer <sup>Note 2</sup>	

#### Notes 1. Write start address structure

Struct stWordAddress{	
USHORT WriteAddress;	/* Write start address*/
UCHAR WriteBANK;	<pre>/* Bank number of write start address */</pre>
};	

Remarks 1. Set the write start address as a multiple of 4 bytes.

2. Set the bank number to 0 when a product with which no bank number has to be set is used.

#### Caution Set a value to each member of this structure before calling this library.

- 2. Set write data to the write data buffer (first address indicated by *DataBufferAddress*) before calling this library.
- Caution Set the write start address and the number of data to be written so that they do not straddle over the boundary of each block.

#### [Return value]

Status	Explanation	
00H	Normal completion	
05H	<ul> <li>Parameter error</li> <li>Start address is not a multiple of 1 word (4 bytes).</li> <li>The number of data to be written is 0.</li> <li>The number of data to be written exceeds 64 words.</li> <li>Write end address (Start address + (Number of data to be written x 4 bytes)) exceeds the flash memory area.</li> </ul>	
10H	<ul> <li>Protect error</li> <li>A boot area is included in the specified range and rewriting of the boot area is disabled.</li> </ul>	
1CH	Write error <ul> <li>Data cannot be written correctly.</li> </ul>	
1DH	Verify (MRG12) error – Data is verified but does not match after it has been written.	
1EH	Blank error – Area equal to the number of data to be written was not a vacant area.	
1FH	<ul><li>Processing is stopped by the occurrence of an interrupt.</li><li>An interrupt occurred while processing of this library was under execution.</li></ul>	

Remark The status is the UCHAR type in C and is stored in the A register in an assembly language.

#### [Function]

This library writes the specified number of data to the flash memory starting from a specified address during EEPROM emulation. Set a RAM area storing the data to be written as a data buffer and call this library. Data of up to 256 bytes can be written (in 4-byte units) at one time.

- **Remark** Call this library as many times as required to write data of more than 256 bytes.
- Caution The operation is not guaranteed if this library is called with interrupts enabled. Before calling this library, execute the DI instruction, and execute the EI instruction after execution of this library is completed, so that acknowledgment of an interrupt is disabled while this library is executed.

#### [Register status after calling]

Memory Model	Register Status
Normal model	Registers cleared: AX, BC, DE Registers held: HL
Static model	Registers cleared: AX, C Registers held: B, DE, HL

#### [Stack size]

36 bytes

## [ROM capacity]

Memory Model	ROM Capacity	
Normal model	117 bytes (of which 57 bytes are common routine)	
Static model	100 bytes (of which 57 bytes are common routine)	

## [Call example]

<C language>

Struct stWordAddress WordAddr;	/* Declares variable. */
<pre>UCHAR DataBuffer[4];</pre>	/* Declares variable. */
UCHAR WordNumber;	/* Declares variable. */
UCHAR Status;	/* Declares variable. */
<pre>DataBuffer[0] = 0x11;</pre>	/* Sets data to be written. */
DataBuffer[1] = 0x22; ;	/* Sets data to be written. */
DataBuffer[2] = $0x33;$ ;	/* Sets data to be written. */
DataBuffer[3] = 0x44; ;	/* Sets data to be written. */
WordNumber = 1;	/* Sets number of data to be written. */
WordAddr.WriteAddress = 0xA000;	/* Sets 0xA000 to write start address.* /
WordAddr.WriteBANK = 0;	/* Sets bank number of write start address to 0. */
di();	/* Disables interrupts. */
	/* Calls EEPROM write library and stores status */
	/* information.*/
<pre>Status = EEPROMWrite( &amp;WordAddr,</pre>	WordNumber, &DataBuffer );
ei();	/* Enables interrupts. */

```
<Assembly language>
```

SELF_F	RAM DSEG								
DataBu	affer: DS 4								
WordAd	ldr:								
WriteA	WriteAddress: DS 2								
WriteE	Bank: DS 1								
Status	: DS 1								
SELF_F	PROG CSEG								
MOV	A, #11H								
MOV	!DataBuffer, A	; Sets data to be written.							
MOV	A, #22H								
MOV	!DataBuffer+1, A	; Sets data to be written.							
MOV	А, #ЗЗН								
MOV	!DataBuffer+2, A	; Sets data to be written.							
MOV	A, #44H								
MOV	!DataBuffer+3, A	; Sets data to be written.							
MOVW	АХ, #ОАОООН								
MOVW	!WriteAddress, AX	; Sets A000H to write address.							
MOV	A, #0								
MOV	!WriteBANK, A	; Sets bank number of write start address to 0.							
	AX, #WordAddr	; Sets address of write start address structure.							
	B, #4	; Sets number of data to be written.							
MOVW	HL, #DataBuffer	; Sets first address of write data buffer.							
DT									
DI		; Disables interrupts.							
CALL	!_EEPROMWrite	; Calls EEPROM write library.							
MOV	!Status, A	; Stores status information.							
ΕI		; Enables interrupts.							

#### [Flow]

Figure 5-11 shows the flow of the EEPROM write library.

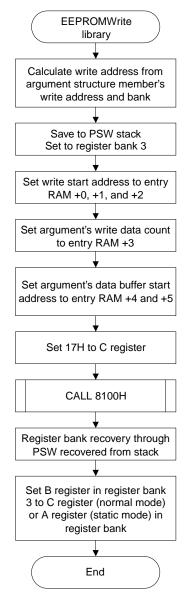


Figure 5-11. Flow of EEPROM Write Library

# CHAPTER 6 DETAILS OF SELF PROGRAMMING CONTROL

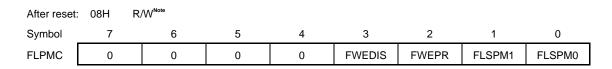
This chapter describes the registers that are used to control flash memory access, and the entry RAM.

## 6.1 Registers That Control Self Programming

### 6.1.1 Flash programming mode control register (FLPMC)

This register is used to enable/disable flash memory access (write, erase, etc.), and indicate the self programming operation mode.

A particular sequence must be used when writing to this register, in order to prevent inadvertent settings due to noise or manipulation errors. For the specific sequence, refer to 6.1.2 Flash protect command register (PFCMD).



Note Bit 2 is a read-only bit.

#### [FWEDIS]

This flag is used to control flash memory access (write, erase, etc.) enable/disable through software. The initial value of this flag is 1, and flash memory access is enabled by writing 0 to this flag.

FWEDIS	Function		
0	Enable write/erase		
1	Disable write/erase		

#### [FWEPR]

This flag is used to control flash memory access (write, erase, etc.) enable/disable through hardware. It directly reflects the voltage of the FLMD0 pin.

FLMD0 Pin Voltage	<b>FWEPR</b> <sup>Note</sup>	Function
Low level (Vss)	0	Disable write/erase
High level (VDD)	1	Enable write/erase

**Note** The FWEPR bit is a read-only bit. Its value cannot be changed by software. However, when using ICE, the value can be changed even by overwriting.

Flash memory access can be enabled through the combination of FWEDIS and FWEPR.

FWEDIS	FWEPR	Flash Memory Write/Erase Enable
0	1	Enable write/erase
Other than above		Disable write/erase

Cautions 1. When executing flash memory write/erase, be sure to set FWEDIS to 0.

2. In the normal mode, be sure to set FWEDIS to 1.

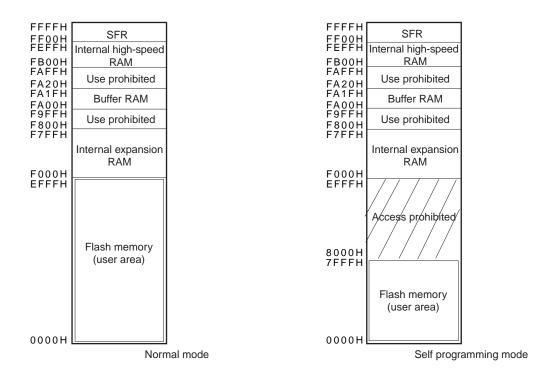
#### [FLSPM0 and FLSPM1]

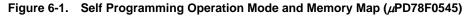
These control flags are used to select the self programming operation mode.

FLSPM1	FLSPM0	Mode Selection
0	0	<ul><li>Normal mode</li><li>Access (instruction fetch, data read) to the entire address range of flash memory is possible.</li></ul>
0	1	<ul> <li>Self programming mode</li> <li>Self programming by "CALL #8100H" is possible.</li> <li>Access (instruction fetch, data read) to flash memory (in products with 32 KB or more of ROM, 0000H to 7FFFH) is possible.</li> </ul>

Caution Setting FLSPM1, FLSPM0 = 1, 0 or 1, 1 is prohibited.

Figure 6-1 shows the self programming operation mode and memory map.







## 6.1.2 Flash protect command register (PFCMD)

To prevent erroneous flash memory write or erase caused by an inadvertent program loop, etc., protection is implemented by this register for flash programming mode control register (FLPMC) write.

The FLPMC register is a special register that is valid for write operations only when the write operations are performed via following special sequence.

- <1> Write a specified value (= A5H) to the PFCMD register.
- <2> Write the value to be set to the FLPMC register (writing is invalid at this step).
- <3> Write the inverted value of the value to be set to the FLPMC register (writing is invalid at this step).
- <4> Write the value to be set to the FLPMC register (writing is valid at this step).

#### Caution The above sequence must be executed every time the value of the FLPMC register is changed.

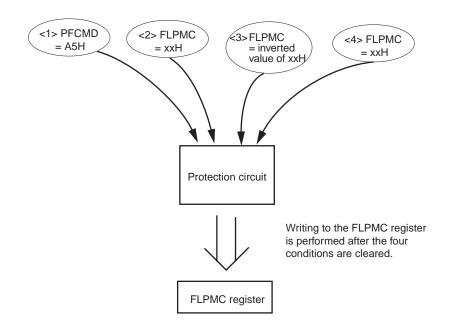
W After reset: Undefined Symbol 7 6 5 4 3 2 1 0 PFCMD REG7 REG6 REG5 REG4 REG3 REG2 REG1 REG0

<Coding example of special sequence>

When writing 05H to FLPMC register:

MOV PFCMD, #0A5H	; Writes A5H to PFCMD
MOV FLPMC, #05H	; Writes 05H to FLPMC
MOV FLPMC, #0FAH	; Writes 0FAH (inverted value of 05H) to FLPMC
MOV FLPMC, #05H	; Writes 05H to FLPMC





### 6.1.3 Flash status register (PFS)

If the flash programming mode control register (FLPMC) is not written in the correct sequence, the FLPMC register is not set and a protection error occurs. At this time, bit 0 (FPRERR) of the PFS register is set to 1.

This flag is a cumulative flag.

After reset:	00H F	R/W						
Symbol	7	6	5	4	3	2	1	0
PFS	0	0	0	0	0	0	0	FPRERR

The FPRERR flag's operation conditions are as follows.

<Setting conditions>

- When the PFCMD register is written to at a time when the store instruction's operation for the latest peripheral register was not a write operation to the PFCMD register using a specified value (A5H)
- When the first store instruction operation after <1> above is for a peripheral register other than the FLPMC register
- When the first store instruction operation after <2> above is for a peripheral register other than the FLPMC register
- When the first store instruction operation after <2> above writes a value other than the inverted value of the value to be set to the FLPMC register
- When the first store instruction operation after <3> above is for a peripheral register other than the FLPMC register
- When the first store instruction operation after <3> above writes a value other than the value (write value in <2>) to be set to the FLPMC register.
- **Remark** The numbers shown in angle brackets above correspond to the numbers shown in angle brackets in section 6.1.2 above.

<Reset conditions>

- When 0 is written to bit 0 (FPRERR) in the PFS register.
- When a system reset is performed.

#### 6.1.4 Self programming control parameters

The self programming operation includes setting the FLMD0 pin to 1, setting the required values to the FLPMC register, and setting up entry RAM, after which the function number (refer to Table 6-1) is set to register bank 3's C register and CALL8100H processing is performed.

The parameters involved in this operation are described below.

(1) Register bank 3's parameters

In the self programming sample library, register bank 3's C register is used to select functions to control self programming, while its B register is used to store execution results and the HL register is used to specify the start address of entry RAM.

Since settings to register bank 3 are all performed within a library, register bank 3 should be included in user programs.

Register C register Function Name Number		B Register Return Value	HL Register	AX/DE Register		
Initialize 00H		00H: Normal completion	Start address of	Not used		
Block erase	03H	00H: Normal completion 05H: Parameter error 10H: Protect error 1AH: Erase error 1FH: Stopped	entry RAM <sup>Note</sup>	(used by self programming sample library)		
Word write	04H	00H: Normal completion 05H: Parameter error 10H: Protect error 1CH: Write error 1FH: Stopped				
Block verify	06H	00H: Normal completion 05H: Parameter error 1BH: Verify (internal verify) error 1FH: Stopped				
Block blank check	08H	00H: Normal completion 05H: Parameter error 1BH: Blank check error 1FH: Stopped				
Get information	09H	00H: Normal completion 05H: Parameter error 20H: Read error				
Set information	0AH	00H: Normal completion 05H: Parameter error 10H: Protect error 1AH: Erase error 1BH: Verify (internal verify) error 1CH: Write error 1FH: Stopped				
Mode check	0EH	00H: Normal completion 01H: Error				
EEPROM write	17H	00H: Normal completion 05H: Parameter error 10H: Protect error 1CH: Write error 1DH: Verify (MRG12) error 1EH: Blank error 1FH: Stopped				

Table 6-1. Register Bank 3 Parameter Lis	st
--	----

**Note** Entry RAM can be allocated to any address in the internal high-speed RAM except in the short direct addressing area (entry RAM can be allocated to addresses in the internal high-speed RAM within the short direct addressing area only when the start address is FE20H).

(2) Entry RAM

Entry RAM is a 100-byte RAM area that is used for self programming. Parameters that control self programming are set six bytes from the start address of the entry RAM area. Once these parameters have been set, the self programming sample library is called to begin controlling self programming operations. The placement of the parameters for various functions relative to the start of the entry RAM area is listed in Table 6-2 below.

Allocate the Entry RAM to any address in the high-speed RAM area except in the short direct addressing area (it is possible to allocate the entry RAM to addresses in internal high-speed RAM within the short direct addressing area only when the start address is FE20H).

Entry RAM is used as a work area for self programming. Consequently, nothing in the entry RAM area except for parameters should be changed during self programming operations.

Offset Value Function Name	+00H	+01H	+02H	+03H	+04H, +05H	+06H to +99H
Initialize	-	-	-	_	_	_
Block erase	-	-	-	Block number	-	-
Word write	Start address lower bits	Start address higher bits	Start address MSB	Number of words	Data buffer start address	-
Block verify	-	-	-	Block number	-	-
Block blank check	-	-	-	Block number	-	-
Get information	Block number	-	-	Option value	Data buffer start address	-
Set information	-	-	-	-	Data buffer start address	-
Mode check	-	-	-	-	-	-
EEPROM write	Start address lower bits	Start address higher bits	Start address MSB	Number of words	Data buffer start address	-

Table 6-2. Entry RAM Parameter List

**Remark** Do not modify the content of any single description.

#### (3) Data buffer

The data buffer is used to pass data and setting-related information written to flash memory; its specific contents depend on the self programming function being used. The data buffer can be placed at any address in internal high-speed RAM, and its start address is specified in the entry RAM. The data buffer's size also depends on the function, but it must be in range from 1 to 256 bytes.

Function			Data Buffer Contents						
	Data Buffer Size (Bytes)		+00H	+01H	+02H	+03H	+04H to +FFH		
Initialize	-	-	Not used						
Block erase	-	-	Not used						
Word write	4 to 256	Write data	Write data						
Block verify	-	– Not used							
Block blank check	-	-	Not used						
Get information	1 to 8	Flash information	Flash information (refer to Table 6-4 for det	tails)					
Set information	1	Information flag	<ul> <li>Bit 0: Execute boot swap (0)/ Do not execute (1)</li> <li>Bit 1: Prohibit chip erase (0)/Enable (1)</li> <li>Bit 2: Prohibit block erase (0)/Enable (1)</li> <li>Bit 3: Prohibit write (0)/Enable (1)</li> <li>Bit 5: Prohibit boot area overwrite (0)/ Enable (1)</li> </ul>						
Mode check	-	-	- Not used						
EEPROM write	4 to 256	Write data	Write data						

Table 6-3. Data Buffer Parameter List

Remark If a function is used with an area marked as "not used", the area cannot be used as a data buffer.

	Data Buffer's Offset Value								
Value	+00H	+01H	+02H	+03H	+04H	+05H	+06H	+07H	
03H		flag final block information number							
	Bit 1: Chip e Bit 2: Block Bit 3: Write Bit 4: Boot a Bits 3, 5, 6,	Bit 1: Chip erase enable flag (0: Prohibit, 1: Enable) Bit 2: Block erase enable flag (0: Prohibit, 1: Enable) Bit 3: Write enable flag (0: Prohibit, 1: Enable) Bit 4: Boot area overwrite prohibit flag (0: Prohibit, 1: Enable) Bits 3, 5, 6, and 7 are always 1. <boot area's="" block="" final="" number=""></boot>							
04H	Boot flag information	Boot flag Not used information							
	00H: Boot a	<b>u</b>							
05H			MSB	Not used					
	04H	flag information <security fla<br="">Bit 1: Chip e Bit 2: Block Bit 3: Write Bit 4: Boot a Bits 3, 5, 6, <boot area'<br="">03H (fixed) 04H Boot flag information <boot flag="" i<br="">00H: Boot a 01H: Boot a</boot></boot></security>	flag       final block         information       number <security flag="" informatio<="" td="">         Bit 1: Chip erase enable         Bit 2: Block erase enable         Bit 3: Write enable flag (flag)         Bit 4: Boot area overwrite         Bits 3, 5, 6, and 7 are alw         <boot area's="" block="" final="" in<="" td="">         03H (fixed)         04H       Boot flag         information         <boot d<="" flag="" information:="" td="">         00H: Boot area is not be         01H: Boot area is being is         05H</boot></boot></security>	flag       final block information         flag       final block number <security details="" flag="" information:=""> Bit 1: Chip erase enable flag (0: Proh Bit 2: Block erase enable flag (0: Proh Bit 3: Write enable flag (0: Prohibit, 1: Bit 4: Boot area overwrite prohibit flag Bits 3, 5, 6, and 7 are always 1.         <boot area's="" block="" final="" number=""> 03H (fixed)         04H         Boot flag information         <boot details="" flag="" information:=""> 00H: Boot area is not being switched 01H: Boot area is being switched         05H</boot></boot></security>	flag       final block         information       number <security details="" flag="" information:="">         Bit 1: Chip erase enable flag (0: Prohibit, 1: Enable         Bit 2: Block erase enable flag (0: Prohibit, 1: Enable)         Bit 3: Write enable flag (0: Prohibit, 1: Enable)         Bit 4: Boot area overwrite prohibit flag (0: Prohibit, 1: Enable)         Bit 3: Write enable flag (0: Prohibit, 1: Enable)         Bit 4: Boot area overwrite prohibit flag (0: Prohibit, 1: Enable)         Bit 4: Boot area overwrite prohibit flag (0: Prohibit, 1: Enable)         Bit 4: Boot area overwrite prohibit flag (0: Prohibit, 1: Enable)         Bit 4: Boot area overwrite prohibit flag (0: Prohibit, 1: Enable)         Bit 4: Boot area overwrite prohibit flag (0: Prohibit, 1: Enable)         Bit 4: Boot area is final block number&gt;         03H (fixed)         04H       Boot flag information: details&gt;         00H: Boot area is not being switched         01H: Boot area is being switched         05H       Block's end address</security>	flag       final block information       final block number <security details="" flag="" information:=""> Bit 1: Chip erase enable flag (0: Prohibit, 1: Enable) Bit 2: Block erase enable flag (0: Prohibit, 1: Enable) Bit 3: Write enable flag (0: Prohibit, 1: Enable) Bit 4: Boot area overwrite prohibit flag (0: Prohibit, 1: Enable) Bits 3, 5, 6, and 7 are always 1. <boot area's="" block="" final="" number=""> 03H (fixed)         04H       Boot flag information       Not used information: details&gt; 00H: Boot area is not being switched 01H: Boot area is being switched         05H       Block's end address       Not used</boot></security>	flag       final block         information       number <security details="" flag="" information:="">         Bit 1: Chip erase enable flag (0: Prohibit, 1: Enable)         Bit 2: Block erase enable flag (0: Prohibit, 1: Enable)         Bit 3: Write enable flag (0: Prohibit, 1: Enable)         Bit 4: Boot area overwrite prohibit flag (0: Prohibit, 1: Enable)         Bit 3: Write enable flag (0: Prohibit, 1: Enable)         Bit 4: Boot area overwrite prohibit flag (0: Prohibit, 1: Enable)         Bit 3: 5, 6, and 7 are always 1.         <boot area's="" block="" final="" number="">         03H (fixed)         04H         Boot flag information: details&gt;         00H: Boot area is not being switched         01H: Boot area is being switched         05H       Block's end address</boot></security>	flag       final block         information       number <security details="" flag="" information:="">         Bit 1: Chip erase enable flag (0: Prohibit, 1: Enable)         Bit 2: Block erase enable flag (0: Prohibit, 1: Enable)         Bit 3: Write enable flag (0: Prohibit, 1: Enable)         Bit 4: Boot area overwrite prohibit flag (0: Prohibit, 1: Enable)         Bit 3: J, 5, 6, and 7 are always 1.         <boot area's="" block="" final="" number="">         03H (fixed)         04H         Boot flag information: details&gt;         00H: Boot area is not being switched         01H: Boot area is being switched         05H</boot></security>	

Table 6-4. Detailed Flash Information for Get Information Fun	ction
---	-------

**Remark** If a function is used with an area marked as "not used", the area cannot be used as a data buffer.

# APPENDIX A SAMPLE PROGRAM

This appendix shows the sample program provided.

Caution This sample program must be used at the user's own risk. Correct operation is not guaranteed if this sample program is used.

# A.1 User Program

<sample.c>

<sample.c></sample.c>			
/*++++++++	+++++++++++++++++++++++++++++++++++++++	+++++++++++++++++++++++++++++++++++++++	+++++++++++++++++++++++++++++++++++++++
* System	: Sample program t	hat uses sel:	f programming sample library
* File nam	ne : sample.c		
* Target (	CPU : 78K0/Kx2		
* Last upo	dated : 2005/02/25		
*+++++++++	+++++++++++++++++++++++++++++++++++++++	-++++++++++++++++++++++++++++++++++++++	+++++++++++++*/
/*			
	anded functions		
*			*/
#pragma	sfr		
#pragma	DI		
#pragma	EI		
#pragma	NOP		
/*			
* Type	e declarations		
*			*/
typedef un	signed char UCHAR;		
typedef un	signed short USHORT;		
/*			
	stant definitions		
*			*/
#define		(0x1F)	
#define		(0x00)	/* Normal completion */
#define	FLASHFIRM_ABNORMAL_END	(OxFF)	/* Abnormal completion */
#define	TRUE	(0x00)	
#define	FALSE	(OxFF)	/* Abnormal */
#define	PARAMETER_ERROR	(0x05)	/* Parameter error */
#define	BANKNUM	(5)	/* Bank number */
#define	BLOCK	(32)	/* Block number */
#define	ADDR	(0x8000)	/* Write Address */
" ACT THC	זעמני	(020000)	, WIICE AUGLESS /
etruct etw	ordAddress{		
SCIUCE SCW			

```
USHORT WriteAddress;
      UCHAR WriteBank;
};
struct stWordWriteData{
     UCHAR WordNumber;
     UCHAR WriteDataBuffer[256];
     USHORT WriteAddressData;
     UCHAR WriteBankData;
};
struct stGetInfo{
      UCHAR OptionNumber;
     UCHAR GetInfoBank;
     UCHAR GetInfoBlock;
};
struct stGetInfoData{
     UCHAR OptionNumberData;
     UCHAR GetInfoBankData;
     UCHAR GetInfoBlockData;
};
/*_____
     Prototype declarations
*-----*/
extern void FlashStart( void );
extern void FlashEnd( void );
extern void FlashEnv ( USHORT EntryRAM );
extern UCHAR FlashBlockErase( UCHAR EraseBank, UCHAR EraseBlock );
extern UCHAR FlashWordWrite( struct stWordAddress *ptr, UCHAR WordNumber, USHORT
DataBufferAddress );
extern UCHAR FlashBlockVerify( UCHAR VerifyBank, UCHAR VerifyBlock );
extern UCHAR FlashBlockBlankCheck( UCHAR BlankCheckBank, UCHAR BlankCheckBlock );
extern UCHAR FlashGetInfo( struct stGetInfo *ptr, USHORT DataBufferAddress );
extern UCHAR FlashSetInfo( UCHAR SetInfoData );
extern UCHAR CheckFLMD( void );
UCHAR FlashBlockErase Call( UCHAR EraseBank, UCHAR EraseBlock );
UCHAR FlashWordWrite_Call( struct stWordAddress *ptr1, USHORT DataBufferAddress,
struct stWordWriteData *ptr2 );
UCHAR FlashBlockVerify Call( UCHAR VerifyBank, UCHAR VerifyBlock );
UCHAR FlashBlockBlankCheck Call ( UCHAR BlankCheckBank, UCHAR BlankCheckBlock );
UCHAR FlashGetInfo Call( struct stGetInfo *ptr1, USHORT DataBufferAddress, struct
stGetInfoData *ptr2 );
UCHAR FlashGetInfo Call5( struct stGetInfo *ptr1, USHORT DataBufferAddress, struct
stGetInfoData *ptr2 );
UCHAR FlashSetInfo Call3( UCHAR SetInfoData, struct stGetInfo *ptr, USHORT
```

```
DataBufferAddress );
UCHAR FlashSetInfo_Call4( UCHAR SetInfoData, struct stGetInfo *ptr, USHORT
DataBufferAddress );
UCHAR CheckFLMD_Call( void );
/* FlashEnv */
sreg UCHAR EntryRAM[100];
/*_____
     Sample program
*-----*/
void main( void ) {
     USHORT i;
     UCHAR Status;
     /* FlashBlockErase */
     UCHAR EraseBank;
     UCHAR EraseBlock;
     /* FlashBlockVerify */
     UCHAR VerifyBank;
     UCHAR VerifyBlock;
      /* FlashBlockBlankCheck */
     UCHAR BlankCheckBank;
     UCHAR BlankCheckBlock;
     /* FlashWordWrite */
     struct stWordAddress WordAddr;
     UCHAR DataBuffer[256];
     struct stWordWriteData WordWriteData;
     DI();
     IMS = 0 \times CC;
     IXS = 0 \times 00;
      PCC = 0 \times 00;
                            /* Clock select( division ratio ) */
                             /* -> IN: 5MHZ = OUT: 5MHZ */
                            /* MOC.bit7:X1 oscillator operation */
     MSTOP = 0;
     OSTS = 0x05;
                            /* Oscillation stabilization time */
     while ( OSTC.0 == 0);
     MCM0 = 0;
     XSEL = 0;
```

while( MCS == 1 );

```
RSTOP = 1;
      LVIM = 0 \times 00;
                                 /* Prohibits low voltage detection */
      LVIS = 0 \times 00;
      EI();
      /* FlashStart( Self programming start library ) call processing */
      FlashStart();
      /* FlashEnv( Initialization library ) call processing */
      FlashEnv( ( USHORT )&EntryRAM );
      /* CheckFLMD( Mode check library ) call processing */
      Status = CheckFLMD Call();
      if ( Status == TRUE ) {
             while(1){
                     /* FlashBlockBlankCheck call processing */
                    BlankCheckBank = BANKNUM;
                    BlankCheckBlock = BLOCK;
                                                /* Block blank check library */
                    Status = FlashBlockBlankCheck_Call( BlankCheckBank,
BlankCheckBlock );
                    if( Status == TRUE ) {
                           break;
                     }else if ( Status == PARAMETER ERROR ) {
                           break;
                           /* Abnormal end */
                    }else{
                           /* FlashBlockErase call processing */
                           EraseBank = BANKNUM;
                           EraseBlock = BLOCK;
                                                /* Block erase library */
                           Status = FlashBlockErase Call( EraseBank, EraseBlock );
                           if( Status != TRUE ) {
                                  break;
                                  /* Abnormal end */
                           }
                    }
             }
       }
      if ( Status == TRUE ) {
             /* FlashWordWrite call processing */
             for( i=0; i<=255; i++ ) {</pre>
```

```
WordWriteData.WriteDataBuffer[i] = ( UCHAR )i;
            }
            WordWriteData.WordNumber = 64;
            WordWriteData.WriteAddressData = ADDR;
            WordWriteData.WriteBankData = BANKNUM;
            Status = FlashWordWrite Call( &WordAddr, ( USHORT )&DataBuffer,
&WordWriteData );
                                          /* Word write library */
            if ( Status == TRUE ) {
                  /* FlashBlockVerify call processing */
                  VerifyBank = BANKNUM;
                  VerifyBlock = BLOCK;
                                          /* Block verify library */
                  Status = FlashBlockVerify Call( VerifyBank, VerifyBlock );
            }
      }
      if ( Status == TRUE ) {
            /* FlashEnd( Self programming end library ) call processing */
            FlashEnd();
            /* Normal end */
      }else{
            /* FlashEnd( Self programming end library ) call processing */
            FlashEnd();
            /* Abnormal end */
      }
      while(1){
           NOP();
           NOP();
      }
}
/* Call processing in each library */
/*_____
* Function name : FlashBlockErase CALL
* Input :
                 EraseBank = Erase bank
                 EraseBlock = Erase block number
* Output :
                 Status = Return value from firm
                 ( When the retry time exceeds 10 times,
                 return PARAMETER ERROR from this function )
* Summary :
                 FlashBlockErase library call processing.
*-----*/
UCHAR FlashBlockErase Call( UCHAR EraseBank, UCHAR EraseBlock ) {
     UCHAR Status;
     UCHAR Counter;
```

```
/* Retry counter reset */
      Counter = 0;
      while(1){
            Counter++; /* When the retry time exceeds 10 times, it ends. */
            if (Counter \geq 10) {
                  Status = FLASHFIRM_ABNORMAL_END;
                  break;
            }
            DI();
                                            /* Erase library call */
            Status = FlashBlockErase( EraseBank, EraseBlock );
            EI();
            if( Status == STATE_OF_ABORT ) { /* State of abort?, YES */
                  while(1){
                         DI();
                                            /* Block blank check library call */
                         Status = FlashBlockBlankCheck( EraseBank, EraseBlock );
                         EI();
                                            /* State of abort?, NO */
                         if ( Status != STATE OF ABORT ) {
                              break;
                         }
                  }
                                            /* Normal completion?, YES */
                  if( Status == FLASHFIRM_NORMAL_END ) {
                                            /* Initialization library call */
                         FlashEnv( ( USHORT )&EntryRAM );
                         break;
                  }
            }else{
                  break;
            }
      }
                                           /* Return value = Status */
     return(Status);
}
                 _____
 Function name : FlashWordWrite CALL
```

```
*ptr1 = Address of writing beginning address structure
* Input :
*
                  DataBufferAddress = Address in writing data buffer
*
                  ptr2 = Address of writing beginning address structure
                  ( Member of structure ... Number of writing data
                                          Writing starting address
                                          Bank of writing starting address )
* Output :
                 Status = Return value from firm
                WordWrite library call processing.
* Summary :
*-----*/
UCHAR FlashWordWrite Call( struct stWordAddress *ptrl, USHORT DataBufferAddress,
struct stWordWriteData *ptr2 ){
     UCHAR Status;
     USHORT i;
     UCHAR *p;
      p = ( UCHAR * )DataBufferAddress;
                                    /* Writing data setting to data buffer. */
      for( i=0; i<=(ptr2->WordNumber) *4-1; i++) {
            *p = ptr2->WriteDataBuffer[i];
            p++;
      }
      /* Writing address and the bank are set to writing beginning address structure.
*/
      ptr1->WriteAddress = ptr2->WriteAddressData;
      ptr1->WriteBank = ptr2->WriteBankData;
      while(1){
            DI();
                                           /* Word write library call */
            Status = FlashWordWrite( ptr1, ptr2->WordNumber, DataBufferAddress );
            EI();
            if( Status != STATE OF ABORT ) { /* State of abort?, NO */
                 break;
            }
      }
                                         /* Return value = Status */
     return(Status);
}
   _____
* Function name : FlashBlockVerify CALL
* Input :
                 VerifyBank = Verify bank
                 VerifyBlock = Verify block number
```

```
* Output :
                Status = Return value from firm
* Summary :
              FlashBlockVerify library call processing.
*-----*/
UCHAR FlashBlockVerify Call( UCHAR VerifyBank, UCHAR VerifyBlock ) {
     UCHAR Status;
     while(1){
          DI();
                                       /* Block verify library call */
           Status = FlashBlockVerify(VerifyBank, VerifyBlock);
          EI();
           if( Status != STATE OF ABORT ) { /* State of abort?, NO */
                break;
           }
     }
     return(Status);
                                       /* Return value = Status */
}
/*_____
* Function name : FlashBlockBlankCheck CALL
               BlankCheckBank = Blank check bank
* Input :
                BlankCheckBlock = Blank check block number
* Output :
                Status = Return value from firm
* Summary :
               FlashBlockBlankCheck library call processing.
*_____*/
UCHAR FlashBlockBlankCheck Call( UCHAR BlankCheckBank, UCHAR BlankCheckBlock ) {
     UCHAR Status;
     while(1){
          DI();
                                       /* Block blank check library call */
           Status = FlashBlockBlankCheck( BlankCheckBank, BlankCheckBlock );
          EI();
           if( Status != STATE OF ABORT ) { /* State of abort?, NO */
                break;
           }
     }
                                      /* Return value = Status */
     return(Status);
}
```

```
/*_____
* Function name : FlashGetInfo CALL
* Input :
                 *ptr1 = Address of flash information acquisition structure
                 DataBufferAddress = The first address in buffer where get data is
stored
                 *ptr2 = Address of flash information acquisition structure
                 ( Member of structure ... Option number )
                 Status = Return value from firm
* Output :
* Summary :
                 FlashGetInfo library call processing.
                 ( When Security flag information or Boot flag information is
acquired )
*-----*/
UCHAR FlashGetInfo Call( struct stGetInfo *ptr1, USHORT DataBufferAddress, struct
stGetInfoData *ptr2 ) {
     UCHAR Status;
     /* Setting of option number of flash information acquisition structure */
     ptr1->OptionNumber = ptr2->OptionNumberData;
                                         /* Get information library call */
     Status = FlashGetInfo( ptr1, DataBufferAddress );
                                       /* Return value = Status */
     return(Status);
}
/*-----
* Function name : FlashGetInfo CALL5
           *ptr1 = Address of flash information acquisition structure
* Input :
           DataBufferAddress = The first address in buffer where get data is stored
           *ptr2 = Address of flash information acquisition structure
           ( Member of structure ... Option number
                                   Bank
                                   Block number)
           #Option Number=Only 05H#
* Output :
         Status = Return value from firm
* Summary : FlashGetInfo library call processing.
           (When block final address information is acquired)
   ----*/
UCHAR FlashGetInfo Call5( struct stGetInfo *ptr1, USHORT DataBufferAddress, struct
stGetInfoData *ptr2 ) {
     UCHAR Status;
           /* Setting of data of flash information acquisition structure */
     ptr1->OptionNumber = ptr2->OptionNumberData;
     ptr1->GetInfoBank = ptr2->GetInfoBankData;
     ptr1->GetInfoBlock = ptr2->GetInfoBlockData;
                                         /* Get information library call */
```

```
Status = FlashGetInfo( ptr1, DataBufferAddress );
     return(Status);
                                          /* Return value = Status */
}
/*-----
* Function name : FlashSetInfo CALL3
                 SetInfoData=Flash information data
* Input :
                 *ptr = Address of flash information acquisition structure( For
GetInfo )
                 DataBufferAddress=The first address in buffer where get data is
stored( For GetInfo )
* Output :
                 Status = Return value from firm
* Summary :
                 FlashSetInfo library call processing
                 (When security flag information is set )
*-----*/
UCHAR FlashSetInfo Call3( UCHAR SetInfoData, struct stGetInfo *ptr, USHORT
DataBufferAddress ) {
     UCHAR Status;
     UCHAR SecurityFlag;
     UCHAR *p;
     p = ( UCHAR * )DataBufferAddress;
      while(1){
           DI();
            while(1){
            ptr->OptionNumber = 0x03; /* Security flag information acquisition */
                                          /* Get information library call */
                  Status = FlashGetInfo( ptr, DataBufferAddress );
                  if ( Status == FLASHFIRM NORMAL END ) {
                        /* The state of a present security flag is maintained */
                        /* in the variable. */
                        SecurityFlag = *p;
                        break;
                  }
            }
                                          /* Set information library call */
            Status = FlashSetInfo( SetInfoData );
            EI();
            if( Status == STATE_OF_ABORT ) { /* State of abort?, YES */
                  while(1){
                        ptr->OptionNumber = 0x03;
```

```
/* Get information library call */
                        Status = FlashGetInfo( ptr, DataBufferAddress );
                                          /* Normal completion?, YES */
                        if ( Status == FLASHFIRM NORMAL END ) {
                             break;
                        }
                  }
                        /* Flash information rewriting completion?, YES */
                  if( SecurityFlag != *p ){
                       break;
                  }
            }else{
                 break;
            }
     }
     return( Status );
                                        /* Return value = Status */
}
/*_____
* Function name : FlashSetInfo CALL4
* Input :
                 SetInfoData = Flash information data
                 *ptr = Address of flash information acquisition structure (For
GetInfo )
                 DataBufferAddress = The first address in buffer where get data is
stored( For GetInfo )
                 Status = Return value from firm
* Output :
* Summary :
                 FlashSetInfo library call processing
                  (When boot flag information is set )
*-----*/
UCHAR FlashSetInfo Call4( UCHAR SetInfoData, struct stGetInfo *ptr, USHORT
DataBufferAddress ) {
      UCHAR Status;
     UCHAR BootFlag;
      UCHAR *p;
      p = ( UCHAR * )DataBufferAddress;
      while(1){
            DI();
            while(1){
                                   /* Boot flag information acquisition */
                  ptr->OptionNumber = 0x04;
                                          /* Get information library call */
                  Status = FlashGetInfo( ptr, DataBufferAddress );
```

```
if ( Status == FLASHFIRM NORMAL END ) {
                                  /* The state of a present boot flag */
                                  /* is maintained in the variable. */
                       BootFlag = *p;
                       break;
                 }
           }
                                        /* Set information library call */
           Status = FlashSetInfo( SetInfoData );
           EI();
           if( Status == STATE_OF_ABORT ) { /* State of abort ?, YES */
                 while( 1 ) {
                       ptr->OptionNumber = 0x04;
                                        /* Get information library call */
                       Status = FlashGetInfo( ptr, DataBufferAddress );
                                        /* Normal completion?, YES */
                       if( Status == FLASHFIRM_NORMAL_END ) {
                            break;
                       }
                 }
                 if( BootFlag != *p ){
                      break;
                 }
           }else{
                 break;
           }
     }
     return( Status );
                                       /* Return value = Status */
}
/*_____
* Function name : CheckFLMD CALL
* Input :
                None
                Status = Return value from firm
* Output :
              CheckFLMD library call processing.
* Summary :
*-----*/
UCHAR CheckFLMD Call( void ) {
     UCHAR Status;
     Status = CheckFLMD();
                                       /* Mode check library call */
```

return( Status );

}

/\* Return value = Status \*/

# A.2 Self Programming Library (Normal Model)

<SelfLibrary\_normal.asm>

```
; System :
             Self programming library (Normal model )
; File name :
            SelfLibrary_normal.asm
; Version :
             2.00
; Target CPU :
            78K0/Kx2
; Last updated : 2005/07/08
PUBLIC FlashStart
PUBLIC FlashEnd
PUBLIC FlashEnv
PUBLIC FlashBlockErase
PUBLIC FlashWordWrite
PUBLIC FlashBlockVerify
PUBLIC _FlashBlockBlankCheck
PUBLIC FlashGetInfo
PUBLIC FlashSetInfo
PUBLIC CheckFLMD
PUBLIC EEPROMWrite
EQU settings
;-----
FLASH ENV
                  EQU 00H ; Initialization
                 EQU 03H ; Block erace
FLASH BLOCK ERASE
                 EQU 04H ; Word write
FLASH_WORD WRITE
FLASH BLOCK VERIFY
                 EQU 06H ; Block verify
FLASH BLOCK BLANKCHECK EQU 08H ; Block blank check
                 EQU 09H ; Flash memory information read
FLASH GET INF
FLASH SET INF
                 EQU OAH ; Flash memory information setting
FLASH CHECK FLMD
                 EQU OEH ; Mode check
FLASH EEPROM WRITE EQU 17H ; EEPROM write
FLASHFIRM PARAMETER ERROR EQU 05H ; Parameter error
BANK BLC ERROR
                 EQU OFFH ; Bank number error( BLOCK )
BANK ADDR ERROR
                 EQU OFFFFH; Bank number error( ADDRESS )
SELF PROG
        CSEG
_FlashStart
; Function name :
; Input :
                  None
; Output :
                  None
```

```
; Destroyed register : None
; Summary :
                   Self programming start processing.
;------
FlashStart:
    MOV
         PFCMD, #0A5H
                       ; PFCMD register control
    MOV
        FLPMC, #001H
                       ; FLPMC register control ( set value )
                       ; FLPMC register control ( inverted set value )
         FLPMC, #0FEH
    MOV
        FLPMC, #001H ; FLPMC register control ( set value )
    MOV
    RET
; Function name :
                   FlashEnd
; Input :
                   None
; Output :
                  None
; Destroyed register : None
; Summary :
                   Self programming end processing.
;-----
FlashEnd:
        PFCMD, #0A5H
                      ; PFCMD register control
    MOV
    MOV
        FLPMC, #000H
                       ; FLPMC register control ( set value )
    MOV
        FLPMC, #OFFH
                       ; FLPMC register control ( inverted set value )
        FLPMC, #000H
    MOV
                       ; FLPMC register control ( set value )
    RET
;------
; Function name : ____FlashEnv
; Input :
                  AX = Entry RAM address
; Output :
                  None
; Destroyed register : None
; Summary :
                   Initialization processing of self programming.
;-----
FlashEnv:
; Initialization processing
    PUSH PSW
                       ; Save register bank in STACK.
    PUSH AX
    SEL RB3
                       ; Sets to register bank 3.
    POP HL
                       ; Sets Entry RAM address to HL register
    MOV C, #FLASH ENV
                       ; Sets function number to C register
    CALL !8100H
                        ; Calls flash firmware
    MOV A, #09H
                       ; Set Block Erase Retry Number
    MOV
         [HL+13H], A
        [HL+14H], A
    MOV
                       ; Set Chip Erase Retry Number
    POP
        PSW
                       ; Restores register bank from STACK.
    RET
;------
                  _FlashBlockErase
; Function name :
; Input :
                  AX = Erase bank
```

STACK = Erase block number ; ; Output : BC = Status ; Destroyed register : AX,BC ; Summary : Erases of specified block ( 1Kbyte ). ;-----FlashBlockErase: PUSH HL ; Calculate Erase block number from block number and bank. MOVW BC, AX MOVW AX, SP MOVW HL, AX MOV A, [HL+4] ; Read STACK data( = Erase block number ) MOV B, A MOV A, C ; A ... Erase bank, B ... Erase block number ; Block number is calculated from block number and bank. ; ( Return A = Erase block number after it calculates ) CALL !ExchangeBlockNum \$FBE PErr ; It is error if the bank number is outside the range. ΒZ ; Block erase processing PUSH PSW ; Save register bank in STACK. PUSH AX SEL RB3 ; Sets to register bank 3. POP AX ; Sets entry RAM+3 to Erase block number MOV [HL+3], A ; after it calculates MOV C, #FLASH BLOCK ERASE ; Sets function number to C register CALL !8100H ; Calls flash firmware ; Restores register bank from STACK. POP PSW ; Get flash firmware error information MOV A, OFEE3H ; Sets flash firmware error information to return value ; ( OFEE3H = B register of Bank 3 ) FlashBlockErase00 BR ; Parameter error FBE PErr: MOV A, #FLASHFIRM\_PARAMETER\_ERROR ; Sets parameter error to ; return value FlashBlockErase00: MOV C, A MOV B, #00H POP HL RET 

```
; Function name : _FlashWordWrite
; Input :
                         AX = Address of writing beginning address structure
                         ( Member of structure ...
;
                                      Writing starting address
;
                                      Bank of writing starting addres )
;
                                      STACK1 = Number of writing data
;
                                      STACK2 = Address in writing data buffer
;
                         BC = Status
; Output :
; Destroyed register :
                       AX, BC, DE
; Summary :
                         Data on RAM is written in the flash memory.
                         256 bytes or less ( Every 4 bytes ) are written at a time.
;
;------
FlashWordWrite:
      PUSH HL
; Calculate Writing address from writing address and bank.
      MOVW
            DE, AX
      MOVW AX, SP
           HL, AX
      MOVW
      MOV
            A, [HL+4]
                            ; Read STACK data( =Number of writing data )
      MOV
            в, А
            A, [HL+6]
                              ; Read STACK data ( =Address in writing data buffer )
      MOV
      XCH
            Α, Χ
            A, [HL+7]
      MOV
      MOVW HL, AX
      MOVW
            AX, DE
                               ; AX ...
                                           Address of writing beginning address
                                            structure address,
                                ;
                                ; B ...
                                           Number of writing data,
                                            Address in writing data buffer
                                ; HL ...
                              ; Writing address is calculated from structure
      CALL !ExchangeAddress
                                ; member's writing address and bank
                                ; ( Return AX=Writing address )
      ΒZ
            $FWW PErr ; It is error if the bank number is outside the range.
; Word write processing
      PUSH
            PSW
                         ; Save register bank in STACK.
      PUSH
            AX
      PUSH
            ВC
      PUSH
            ΗL
            RB3
      SEL
                        ; Sets to register bank 3.
      POP
            AX
      MOV
            [HL+5], A ; Sets entry RAM+5 to higher address in writing data buffer
            Α, Χ
      MOV
      MOV
            [HL+4], A
                        ; Sets entry RAM+4 to lower address in writing data buffer
      POP
            ΑX
      MOV
            [HL+3], A
                        ; Sets entry RAM+3 to Number of writing data
      MOV
            A.X
      MOV
            [HL+0], A
                         ; Sets entry RAM+0 to Writing address lower bytes
```

```
POP
           AX
     MOV
         [HL+2], A ; Sets entry RAM+2 to Writing address most higher bytes
     MOV
         Α, Χ
          [HL+1], A
                      ; Sets entry RAM+1 to Writing address higher bytes
     MOV
     MOV C, #FLASH WORD WRITE ; Sets function number to C register
     CALL !8100H
                      ; Calls flash firmware
     POP
           PSW
                      ; Restores register bank from STACK.
; Get flash firmware error information
     MOV A, OFEE3H
                      ; Sets flash firmware error information to return value
                      ; ( OFEE3H = B register of Bank 3 )
     BR
          FlashWordWrite00
; Parameter error
FWW PErr:
     MOV
         A, #FLASHFIRM PARAMETER ERROR ; Sets parameter error to
                                       ; return value
FlashWordWrite00:
     MOV C, A
     MOV B, #00H
         HL
     POP
     RET
; Function name :
                      FlashBlockVerify
; Input :
                      AX = Verify bank
                      STACK = Verify block number
;
           :
                      BC = Status
; Output
; Destroyed register :
                     AX, BC
                      Internal verify of specified block ( 1Kbyte ).
; Summary :
;-----
FlashBlockVerify:
     PUSH HL
; Calculate Verify block number from block number and bank.
     MOVW BC, AX
     MOVW AX, SP
     MOVW HL, AX
         A, [HL+4]
                           ; Read STACK data( =Verify block number )
     MOV
         в, А
     MOV
         A, C
                            ; A ... Verify bank, B ... Verify block number
     MOV
     CALL !ExchangeBlockNum ; Block number is calculated from block number
                            ; and bank.
                            ; (Return A=Verify block number after
                            ; it calculates)
     ΒZ
          $FBV PErr
                            ; It is error if the bank number is outside
                            ; the range.
```

```
; Block verify processing
     PUSH
           PSW
                                        ; Save register bank in STACK.
     PUSH
          AX
     SEL
           RB3
                                        ; Sets to register bank 3.
     POP
         AX
     MOV
                                        ; Sets entry RAM+3 to Verify block
           [HL+3], A
                                        ; number after it calculates
           C, #FLASH BLOCK VERIFY
                                       ; Sets function number to C register
     MOV
     CALL
           !8100H
                                        ; Calls flash firmware
     POP
           PSW
                                        ; Restores register bank from STACK.
; Get flash firmware error information
     MOV
          A, OFEE3H
                      ; Sets flash firmware error information to return value
                       ; ( OFEE3H = B register of Bank 3 )
          FlashBlockVerify00
     BR
; Parameter error
FBV PErr:
     MOV
          A, #FLASHFIRM PARAMETER ERROR ; Sets parameter error to return
                                        ; value
FlashBlockVerify00:
     MOV
          С, А
          в, #00н
     MOV
     POP
          HL
     RET
;------
; Function name :
                    _FlashBlockBlankCheck
                      AX = Blank check bank
; Input :
                     STACK = Blank check block number
; Output :
                      BC = Status
; Destroyed register : AX, BC
; Summary :
                      Blank check of specified block ( 1Kbyte ).
FlashBlockBlankCheck:
     PUSH HL
; Calculate Blank check block number from block number and bank.
     MOVW
          BC, AX
     MOVW AX, SP
     MOVW HL, AX
     MOV
           A, [HL+4] ; Read STACK data( =Blank check block number )
           в, А
     MOV
     MOV
          A, C
                      ; A ... Blank check bank, B ... Blank check block number
     CALL !ExchangeBlockNum
                                  ; Block number is calculated from block
                                   ; number and bank.
```

```
; (Return A = Blank check block number after it calculates)
     ΒZ
           $FBBC PErr ; It is error if the bank number is outside the range.
; Block blank check processing
     PUSH
          PSW
                                        ; Save register bank in STACK.
     PUSH AX
     SEL
         RB3
                                        ; Sets to register bank 3.
     POP AX
     MOV
         [HL+3], A
                                        ; Sets entry RAM+3 to Blank check
block number after it calculates
     MOV
         C, #FLASH BLOCK BLANKCHECK
                                       ; Sets function number to C register
     CALL !8100H
                                        ; Calls flash firmware
     POP PSW
                                         ; Restores register bank from STACK.
; Get flash firmware error information
     MOV A, OFEE3H
                      ; Sets flash firmware error information to return value
                       ; ( OFEE3H = B register of Bank 3 )
     BR
          FlashBlockBlankCheck00
; Parameter error
FBBC PErr:
     MOV A, #FLASHFIRM PARAMETER ERROR ; Sets parameter error to return
                                         ; value
FlashBlockBlankCheck00:
     MOV
          C, A
     MOV B, #00H
     POP HL
     RET
_FlashGetInfo
; Function name :
; Input :
                       AX = Address of flash information acquisition structure
                       (Member of structure ... Option number
;
                                              Bank
;
                                              Block number)
;
                       STACK = The first address in buffer where get data is stored
; Output :
                       BC = Status
; Destroyed register :
                     AX,BC,DE
; Summary :
                       The set up information of the flash memory is read.
FlashGetInfo:
     PUSH HL
; Check of Option number
     MOVW BC, AX
     MOVW AX, SP
     MOVW HL, AX
```

```
MOV
             A, [HL+4]
                                 ; Read STACK data( =The first address in buffer
                                 ; where get data is stored )
      XCH
             Α, Χ
      MOV
             A, [HL+5]
      XCHW
            AX, BC
                                 ; AX ... Address of flash information
                                 ; acquisition structure
                                 ; BC ... The first address in buffer where get data
                                 ; is stored
      MOVW
             HL, AX
      MOVW
             AX, BC
             DE, AX
      MOVW
                                ; Read data from flash information acquisition
      MOV
             A, [HL+0]
                                 ; structure ( = Option number )
      CMP
             A, #05H
                                 ; Option number = 5 ?
      BNZ
             $FlashGetInfo10
                               ; NO
; Calculate Block number from block number and bank.
      MOV
             Х, А
             A, [HL+2]
                                ; Read data from flash information acquisition
      MOV
                                ; structure ( =Block number )
      MOV
             в, А
             A, [HL+1]
      MOV
                                ; Read data from flash information acquisition
                                 ; structure (=Bank)
                                 ; A...Bank, B...Block number
            !ExchangeBlockNum ; Block number is calculated from block number
      CALL
                                 ; and bank.
                                 ; ( Return A = Block number after it calculates )
             $FlashGetInfo20
                                 ; It is error if the bank number is outside
      BZ
                                 ; the range.
      XCH
                                 ; A...Option number, X...Block number
             Α, Χ
; Get info processing (When Option number = 5 )
      PUSH
             PSW
                                 ; Save register bank in STACK.
      PUSH
             DE
      PUSH
           AX
      SEL
             RB3
                                 ; Sets to register bank 3.
      POP
             AX
      XCH
            Α, Χ
      MOV
             [HL+0],A
                                ; Sets entry RAM+0 to Block number
             Α, Χ
                                ; A...Option number
      MOV
             FlashGetInfo40
      BR
; Check of Option number error
FlashGetInfo10:
                                 ; Option number = 3 ?
      CMP
             A, #03H
      ΒZ
             $FlashGetInfo30
                               ; YES
                                 ; Option number = 4?
      CMP
             A, #04H
      ΒZ
             $FlashGetInfo30
                                 ; YES
```

```
FlashGetInfo20:
      MOV
           A, #FLASHFIRM PARAMETER ERROR
                                          ; The parameter error is returned,
                                             ; except when option NO is 3, 4,
                                             ; and 5.
      BR
            FlashGetInfo50
; Get info processing (When Option number = 3, 4 )
FlashGetInfo30:
      PUSH PSW
                               ; Save register bank in STACK.
      PUSH DE
      PUSH AX
      SEL
          RB3
                                ; Sets to register bank 3.
      POP
            AX
FlashGetInfo40:
      MOV
                               ; Sets entry RAM+3 to Option number
           [HL+3], A
      POP
           AX
      MOV
          [HL+5], A
                               ; Sets entry RAM+5 to Storage buffer higher address
      MOV
           Α, Χ
            [HL+4], A
                               ; Sets entry RAM+4 to Storage buffer lower address
      MOV
      MOV
          C, #FLASH GET INF ; Sets function number to C register
      CALL !8100H
                                ; Calls flash firmware
      POP
           PSW
                                ; Restores register bank from STACK.
; Calculate Address from Storage buffer and bank. Nothing to do
; when Option number = 3or4 or Bank = 0 or Block number( Previous ) < 32
; or Block number( Previous ) >= 48.
; A = Option number, B = Bank, C ... Block number (Previous),
; DE = Storage buffer first address of get data
            A, #05H
      CMP
                                      ; Option number = 5?
      BNZ
           $ReturnAddress end
                                     ; NO
      MOV
          А, В
      CMP
          A, #0
                                      ; Bank = 0 ?
            $ReturnAddress end
                                     ; YES
      ΒZ
      XCH
          A, C
      CMP A, #32
                                     ; Block number( Previous ) < 32?
      BC
           $ReturnAddress end
                                      ; YES
      CMP
          A, #48
                                     ; Block number( Previous ) >= 48?
      BNC
            $ReturnAddress end
                                      ; YES
      MOV
            A, C
; Calculation of address( 40H*Bank is pulled from address in two high rank bytes.
; Lower address is the state as it is. )
      XCHW AX, DE
      MOVW HL, AX
           A, [HL+1]
      MOV
      MOV
           Χ, Α
      MOV
            A, [HL+2]
                               ; A ... Most higher address, X ... Higher address
      XCHW AX, DE
                                ; A ... Bank, D ... Most higher address,
```

```
; E ... Higher address
     MOV
           [HL+2], A
                            ; Sets Storage buffer+2 to Bank.
     MOV
           X, #0
           A, 1
     ROL
     ROL
           A, 1
     ROL
          A, 1
     ROL
           A, 1
     ROL
         A, 1
         A, 1
     ROLC
     XCH
           Α, Χ
     ROLC
          A, 1
                          ; AX = 40H*Bank
     XCHW AX, DE
     XCH
           A, X
     SUB
         Α, Ε
          А, Х
     XCH
     SUBC A, D
     MOV
           Α, Χ
     MOV
           [HL+1], A
                          ; Sets Storage buffer+1 to Calculated
                           ; address(higher).
ReturnAddress end:
; Get flash firmware error information
     MOV
         A, OFEE3H
                          ; Sets flash firmware error information to
                           ; return value
                           ; ( OFEE3H = B register of Bank 3 )
FlashGetInfo50:
         С, А
     MOV
     MOV
         в, #00н
     POP
         HL
     RET
; Function name :
                     FlashSetInfo
                     AX = Flash information data
; Input :
                     BC = Status
; Output :
; Destroyed register : A, BC
; Summary :
                     Setting of flash information.
FlashSetInfo:
; Set infomation processing
     MOV
           Α, Χ
     PUSH AX
                           ; Save Flash information data in STACK.
     PUSH PSW
                           ; Save register bank in STACK.
     SEL
           RB3
                           ; Sets to register bank 3.
     MOVW AX, SP
     ADDW AX, #2
     MOV
           [HL+5], A
                           ; Sets entry RAM+5 to higher address of flash
                            ; information data secured for stack
```

```
MOV
          Α, Χ
     MOV
         [HL+4], A
                          ; Sets entry RAM+4 to lower address of flash
                            ; information data secured for stack
           C, #FLASH_SET_INF ; Sets function number to C register
     MOV
          !8100H
                           ; Calls flash firmware
     CALL
     POP
           PSW
                           ; Restores register bank from STACK.
     POP
           AX
; Get flash firmware error information
     MOV
         A, OFEE3H ; Sets flash firmware error information to return value
                      ; ( OFEE3H = B register of Bank 3 )
         С, А
     MOV
         в, #00н
     MOV
     RET
; Function name :
                      CheckFLMD
; Input :
                      None
                     BC = Status
; Output :
; Destroyed register : A, BC
; Summary :
                      Checks voltage level of FLMD pin.
CheckFLMD:
; Set infomation processing
     PUSH PSW
                                 ; Save register bank in STACK.
     SEL
         RB3
                                ; Sets to register bank 3.
                                ; Sets function number to C register
     MOV C, #FLASH CHECK FLMD
     CALL !8100H
                                 ; Calls flash firmware
     POP
         PSW
                                 ; Restores register bank from STACK.
; Get flash firmware error information
     MOV
         A, OFEE3H ; Sets flash firmware error information to return value
                      ; ( OFEE3H = B register of Bank 3 )
     MOV
         С, А
         в, #00н
     MOV
     RET
; Function name :
                      EEPROMWrite
                      : AX = Address of writing beginning address structure
; Input
                      ( Member of structure ... Writing starting address
;
                      Bank of writing starting address)
;
                      STACK1 = Number of writing data
:
                      STACK2 = Address in writing data buffer
; Output :
                      BC=Status
; Destroyed register :
                      AX,BC,DE
; Summary :
                      Data on RAM is written in the flash memory.
                      256 bytes or less ( Every 4 bytes ) are written at a time.
```

```
EEPROMWrite:
      PUSH HL
; Calculate Writing address from writing address and bank.
      MOVW
            DE, AX
      MOVW
            AX, SP
           HL, AX
      MOVW
            A, [HL+4]
      MOV
                            ; Read STACK data( =Number of writing data )
      MOV
            В, А
      MOV
            A, [HL+6]
                            ; Read STACK data ( = Address in writing data buffer )
            Α, Χ
      XCH
      MOV
            A, [HL+7]
      MOVW
           HL, AX
            AX, DE
      MOVW
                              ; AX ... Address of writing beginning address
                               ; structure address,
                               ; B ... Number of writing data,
                               ; HL ... Address in writing data buffer
                               ; Writing address is calculated from structure
      CALL
            !ExchangeAddress
                               ; member's writing address and bank
                               ; ( Return AX = Writing address )
                               ; It is error if the bank number is outside
            $EW PErr
      ΒZ
                               ; the range.
; EEPROM write processing
      PUSH
            PSW
                        ; Save register bank in STACK.
      PUSH
            AX
      PUSH
            BC
      PUSH HL
                       ; Sets to register bank 3.
      SEL
            RB3
      POP
            AX
      MOV
            [HL+5], A ; Sets entry RAM+5 to higher address in writing data buffer
      MOV
            Α, Χ
      MOV
            [HL+4], A
                        ; Sets entry RAM+4 to lower address in writing data buffer
      POP
            AX
      MOV
            [HL+3], A ; Sets entry RAM+3 to Number of writing data
      MOV
            A, X
      MOV
            [HL+0], A ; Sets entry RAM+0 to Writing address lower bytes
      POP
            AX
            [HL+2], A ; Sets entry RAM+2 to Writing address most higher bytes
      MOV
      MOV
            Α, Χ
            [HL+1], A
                        ; Sets entry RAM+1 to Writing address higher bytes
      MOV
            C, #FLASH EEPROM WRITE
                                   ; Sets function number to C register
      MOV
      CALL
            !8100H
                         ; Calls flash firmware
      POP
            PSW
                         ; Restores register bank from STACK.
; Get flash firmware error information
      MOV
            A,OFEE3H
                        ; Sets flash firmware error information to return value
```

```
; ( OFEE3H = B register of Bank 3 )
     BR
         EEPROMWrite00
; Parameter error
EW PErr:
     MOV
         A, #FLASHFIRM_PARAMETER_ERROR ; Sets parameter error to return
                                     ; value
EEPROMWrite00:
     MOV
         C, A
     MOV B, #00H
     POP HL
     RET
;-----
; Function name : ExchangeBlockNum
; Input :
               A = Bank
               B = Block number
;
               A = Block number( New )
; Output :
               B = Bank
;
                C = Block number ( Previous )
;
               Block number is converted into the real address
; Summary :
;
               from bank information.
;------
ExchangeBlockNum:
; It calculates from 32 to 47 block number.
     XCH
         А, В
     CMP A, #32
     BC
         $EBN end
         A, #48
     CMP
     BNC $EBN_end
; Calculation of block number( Bank*16 is added to block number. )
     XCH
         А, В
     MOV
         C, A
                          ; C ... Bank
     CMP
         A, #6
     BNC $EBN_error_end
     ROL
         A, 1
         A, 1
     ROL
     ROL A, 1
     ROL A, 1
                           ; A = 16*Bank
     ADD A, B
     XCH A, C
     XCH A, B
     XCH A, C
                           ; A = Block number after it calculates, B = Bank,
                           ; C = Block number before it calculates
     BR
          EBN_end
```

```
; Bank error
EBN error_end:
     MOV
           A, #BANK BLC ERROR ; Return error number
EBN end:
     CMP
          A, #BANK BLC ERROR ; Bank error?
     RET
;------
; Function name : ExchangeAddress
; Input :
                 AX = Address of writing beginning address structure
                 ( Member of structure ... Writing starting address
;
                                         Bank of writing starting address )
;
; Output
                AX = Writing starting address (Address in two high rank bytes )
          :
                 C = Writing starting address ( Lower address )
;
                 Writing starting address of structure is converted
; Summary :
                 into the real address from bank information.
;
;------
ExchangeAddress:
     PUSH HL
; It calculates from 8000H to BFFFH address.
     MOVW
           HL, AX
     MOV
           A, [HL+0] ; Read data from writing beginning address
                             ; structure(=Write address)
           Χ, Α
     MOV
           A, [HL+1]
     MOV
     CMPW
          AX, #8000H
     BC
           $EA end
           AX, #0C000H
     CMPW
     BNC
           $EA end
; Calculation of address( Bank*40H is added to address in two high rank bytes.
; Lower address is the state as it is. )
     MOV
           D, A
      ХСН
           Α, Χ
           C, A
     MOV
     MOV
           X, #0
           A, [HL+2] ; Read data from writing beginning address structure
      MOV
                       ; ( =Bank of writing starting address )
           A, #6
     CMP
      BNC
           $EA error end
      ROL
           A, 1
      ROL
           A, 1
           A, 1
     ROL
      ROL
           A, 1
      ROL
           A, 1
           A, 1
      ROLC
```

```
XCH
            Α, Χ
      ROLC A, 1
                         ; AX=40H*Bank
      XCH
          Α, Χ
      ADD
           A, D
                         ; Addition of Higher address
      XCH A, X
      ADDC A, #0
                         ; Addition of Most higher address
                         ; A ... Most higher address after it calculates
                         ; X ... higher address after it calculates,
                         ; C ... Lower address
      BR
            EA_normal_end
; Bank error
EA_error_end:
      MOVW AX, #BANK_ADDR_ERROR
      BR
           EA normal end
EA_end:
           Α, Χ
      XCH
          C, A
      MOV
      MOV
            A, #0
                         ; A ... Most higher address after it calculates
                         ; X ... higher address after it calculates,
                         ; C ... Lower address
EA_normal_end:
      POP
            ΗL
      CMPW AX, #BANK_ADDR_ERROR ; Bank error?
      RET
      END
```

# A.3 Self Programming Library (Static Model)

```
<SelfLibrary_static.asm>
```

```
; System :
             Self programming library(Static model)
            SelfLibrary static.asm
; File name :
; Version :
             2.00
; Target CPU :
             78K0/Kx2
; Last updated : 2005/07/08
PUBLIC FlashStart
PUBLIC FlashEnd
PUBLIC FlashEnv
PUBLIC FlashBlockErase
PUBLIC FlashWordWrite
PUBLIC FlashBlockVerify
PUBLIC _FlashBlockBlankCheck
PUBLIC FlashGetInfo
PUBLIC FlashSetInfo
PUBLIC CheckFLMD
PUBLIC EEPROMWrite
;
   EQU settings
;-----
                 EQU 00H ; Initialization
FLASH ENV
FLASH BLOCK ERASE
                 EQU 03H ; Block erace
                 EQU 04H ; Word write
FLASH_WORD WRITE
FLASH BLOCK VERIFY
                 EQU 06H ; Block verify
FLASH_BLOCK_BLANKCHECK EQU 08H ; Block blank check
                 EQU 09H ; Flash memory information read
FLASH GET INF
FLASH SET INF
                 EQU OAH ; Flash memory information setting
FLASH CHECK FLMD
                 EQU OEH ; Mode check
FLASH EEPROM WRITE EQU 17H ; EEPROM write
FLASHFIRM PARAMETER ERROR EQU 05H ; Parameter error
BANK BLC ERROR
                 EQU OFFH ; Bank number error(BLOCK)
                 EQU OFFFFH; Bank number error(ADDRESS)
BANK ADDR ERROR
SELF PROG
        CSEG
;------
                  _FlashStart
; Function name :
; Input :
                  None
; Output :
                  None
```

```
; Destroyed register : None
; Summary :
                   Self programming start processing.
;-----
FlashStart:
    MOV
         PFCMD, #0A5H
                       ; PFCMD register control
    MOV FLPMC, #001H
                       ; FLPMC register control ( set value )
                       ; FLPMC register control ( inverted set value )
    MOV FLPMC, #0FEH
    MOV FLPMC, #001H ; FLPMC register control ( set value )
    RET
:------
; Function name :
                   FlashEnd
; Input :
                   None
; Output :
                   None
; Destroyed register : None
; Summary :
                   Self programming end processing.
;-----
FlashEnd:
    MOV PFCMD, #0A5H
                       ; PFCMD register control
    MOV FLPMC, #000H
                       ; FLPMC register control ( set value )
    MOV FLPMC, #0FFH
                       ; FLPMC register control ( inverted set value )
    MOV FLPMC, #000H
                       ; FLPMC register control ( set value )
    RET
;------
; Function name :
                   FlashEnv
; Input :
                   AX = Entry RAM address
; Output :
                  None
; Destroyed register : None
; Summary :
                   Initialization processing of self programming.
;------
FlashEnv:
; Initialization processing
                       ; Save register bank in STACK.
    PUSH PSW
    PUSH AX
    SEL RB3
                        ; Sets to register bank 3.
    POP HL
                       ; Sets Entry RAM address to HL register
    MOV C, #FLASH ENV
                       ; Sets function number to C register
    CALL !8100H
                        ; Calls flash firmware
    MOV A, #09H
    MOV [HL+13H], A
                       ; Set Block Erase Retry Number
    MOV [HL+14H], A
                       ; Set Chip Erase Retry Number
    POP PSW
                       ; Restores register bank from STACK.
    RET
;-----
                  _FlashBlockErase
; Function name :
                  A = Erase bank
; Input :
```

B = Erase block number ; ; Output : A = Status ; Destroyed register : A, BC ; Summary : Erases of specified block ( 1Kbyte ). FlashBlockErase: ; Calculate Erase block number from block number and bank. ; Block number is calculated from block CALL !ExchangeBlockNum ; number and bank. ; ( Return A = Erase block number after it calculates ) ΒZ \$FBE PErr ; It is error if the bank number is outside the range. ; Block erase processing PUSH PSW ; Save register bank in STACK. PUSH AX ; Sets to register bank 3. SEL RB3 POP AX MOV [HL+3], A ; Sets entry RAM+3 to Erase block number after ; it calculates MOV C, #FLASH BLOCK ERASE ; Sets function number to C register CALL !8100H ; Calls flash firmware POP PSW ; Restores register bank from STACK. ; Get flash firmware error information A, OFEE3H MOV ; Sets flash firmware error information to return value ; ( OFEE3H = B register of Bank 3 ) BR FlashBlockErase00 ; Parameter error FBE PErr: A, #FLASHFIRM\_PARAMETER\_ERROR ; Sets parameter error to return MOV ; value FlashBlockErase00: RET ;-----; Function name : FlashWordWrite ; Input : AX = Address of writing beginning address structure ( Member of structure ... ; Writing starting address ; Bank of writing starting address ) ; B = Number of writing data ; HL = Address in writing data buffer ; ; Output : A = Status ; Destroyed register : AX, C ; Summary : Data on RAM is written in the flash memory. 256 bytes or less ( Every 4 bytes ) are written at a time.

```
;-----
FlashWordWrite:
      PUSH DE
; Calculate Writing address from writing address and bank.
      CALL !ExchangeAddress ; Writing address is calculated from structure
                               ; member's writing address and bank
                               ; ( Return AX = Writing address )
                               ; It is error if the bank number is outside
      ΒZ
            $FWW PErr
                               ; the range.
; Word write processing
      PUSH
           PSW
                              ; Save register bank in STACK.
      PUSH
           AX
      PUSH BC
      PUSH HL
      SEL
           RB3
                              ; Sets to register bank 3.
      POP
          AX
                              ; Sets entry RAM+5 to higher address in writing
      MOV [HL+5],A
                               ; data buffer
      MOV
           A,X
      MOV
           [HL+4],A
                              ; Sets entry RAM+4 to lower address in writing
                               ; data buffer
      POP
            AX
      MOV
           [HL+3],A
                              ; Sets entry RAM+3 to Number of writing data
      MOV
            A,X
      MOV
           [HL+0],A
                             ; Sets entry RAM+0 to Writing address lower bytes
            AX
      POP
           [HL+2],A
                              ; Sets entry RAM+2 to Writing address most
      MOV
                               ; higher bytes
          A,X
      MOV
      MOV
           [HL+1],A
                              ; Sets entry RAM+1 to Writing address higher bytes
            C,#FLASH WORD WRITE ; Sets function number to C register
      MOV
      CALL !8100H
                               ; Calls flash firmware
      POP
            PSW
                               ; Restores register bank from STACK.
; Get flash firmware error information
      MOV
           A,OFEE3H
                               ; Sets flash firmware error information to
                               ; return value
                              ; ( OFEE3H = B register of Bank 3 )
      BR
           FlashWordWrite00
; Parameter error
FWW PErr:
      MOV A, #FLASHFIRM PARAMETER ERROR ; Sets parameter error to return
                                           ; value
FlashWordWrite00:
```

```
POP
          DE
     RET
;-----
; Function name : ____FlashBlockVerify
; Input :
                     A = Verify bank
                     B = Verify block number
;
                     A = Status
; Output :
; Destroyed register : A, BC
; Summary :
                      Internal verify of specified block ( 1Kbyte ).
;-----
FlashBlockVerify:
; Calculate Verify block number from block number and bank.
     CALL !ExchangeBlockNum ; Block number is calculated from block number
                           ; and bank.
                            ; ( Return A = Verify block number after it
                           ; calculates )
                          ; It is error if the bank number is outside
     ΒZ
          $FBV PErr
                           ; the range.
; Block verify processing
     PUSH PSW
                                 ; Save register bank in STACK.
     PUSH AX
     SEL
          RB3
                                 ; Sets to register bank 3.
     POP
          AX
                                ; Sets entry RAM+3 to Verify block number
     MOV
         [HL+3], A
                                 ; after it calculates
     MOV
          C, #FLASH_BLOCK_VERIFY ; Sets function number to C register
     CALL !8100H
                                ; Calls flash firmware
     POP
          PSW
                                 ; Restores register bank from STACK.
; Get flash firmware error information
     MOV A, OFEE3H ; Sets flash firmware error information to return value
                      ; ( OFEE3H = B register of Bank 3 )
     BR FlashBlockVerify00
; Parameter error
FBV PErr:
     MOV A, #FLASHFIRM_PARAMETER_ERROR ; Sets parameter error to return
                                       ; value
FlashBlockVerify00:
    RET
;-----
; Function name : _FlashBlockBlankCheck
; Input :
                     A = Blank check bank
                     B = Blank check block number
;
```

; Output : A = Status ; Destroyed register : A, BC Blank check of specified block ( 1Kbyte ). ; Summary : FlashBlockBlankCheck: ; Calculate Blank check block number from block number and bank. CALL !ExchangeBlockNum ; Block number is calculated from block number ; and bank. ; ( Return A = Blank check block number after ; it calculates ) ΒZ \$FBBC PErr ; It is error if the bank number is outside ; the range. ; Block blank check processing PUSH PSW ; Save register bank in STACK. PUSH AX SEL RB3 ; Sets to register bank 3. POP AX MOV [HL+3], A ; Sets entry RAM+3 to Blank check ; block number after it calculates MOV C, #FLASH BLOCK BLANKCHECK ; Sets function number to C register CALL !8100H ; Calls flash firmware POP PSW ; Restores register bank from STACK. ; Get flash firmware error information MOV A, OFEE3H ; Sets flash firmware error information to return value ; ( OFEE3H = B register of Bank 3 ) FlashBlockBlankCheck00 BR ; Parameter error FBBC\_PErr: MOV A, #FLASHFIRM PARAMETER ERROR ; Sets parameter error to return ; value FlashBlockBlankCheck00: RET ; Function name : FlashGetInfo AX = Address of flash information acquisition structure ; Input : ( Member of structure ... Option number ; Bank ; Block number ) : BC = The first address in buffer where get data is stored ; Output : A = Status ; Destroyed register : AX, BC, HL ; Summary : The set up information of the flash memory is read. 

FlashGetInfo: PUSH DE ; Check of Option number MOVW HL, AX AX, BC MOVW MOVW DE, AX A, [HL+0] ; Read data from flash information acquisition MOV ; structure( =Option number ) ; Option number = 5 ? CMP A, #05H BNZ \$FlashGetInfo10 ; NO ; Calculate Block number from block number and bank. MOV Χ, Α MOV A, [HL+2] ; Read data from flash information acquisition structure(=Block number) MOV в, А A, [HL+1] ; Read data from flash information acquisition MOV structure(=Bank) ; A ... Bank, B ... Block number CALL !ExchangeBlockNum ; Block number is calculated from block number ; and bank. ; ( Return A=Block number after it calculates ) \$FlashGetInfo20 ; It is error if the bank number is outside ΒZ ; the range. XCH Α, Χ ; A ... Option number, X ... Block number ; Get info processing (When Option number = 5 ) PUSH PSW ; Save register bank in STACK. PUSH DE PUSH AX SEL RB3 ; Sets to register bank 3. POP AX Α, Χ XCH ; Sets entry RAM+0 to Block number MOV [HL+0], A MOV ; A ... Option number Α, Χ FlashGetInfo40 BR ; Check of Option number error FlashGetInfo10: CMP А, #ОЗН ; Option number = 3? \$FlashGetInfo30 ΒZ ; YES CMP A, #04H ; Option number = 4? ΒZ \$FlashGetInfo30 ; YES FlashGetInfo20: A, #FLASHFIRM PARAMETER ERROR ; The parameter error is returned, MOV ; except when option NO is 3, 4, ; and 5.

```
BR
            FlashGetInfo50
; Get info processing (When Option number = 3, 4 )
FlashGetInfo30:
      PUSH
           PSW
                                ; Save register bank in STACK.
      PUSH DE
      PUSH AX
            RB3
                                ; Sets to register bank 3.
      SEL
      POP
            AX
FlashGetInfo40:
      MOV
            [HL+3], A
                               ; Sets entry RAM+3 to Option number
      POP
           AX
      MOV
           [HL+5], A
                               ;S ets entry RAM+5 to Storage buffer higher address
      MOV
           Α, Χ
                               ; Sets entry RAM+4 to Storage buffer lower address
      MOV
           [HL+4], A
            C, #FLASH GET INF ; Sets function number to C register
      MOV
      CALL !8100H
                                ; Calls flash firmware
            PSW
                                ; Restores register bank from STACK.
      POP
; Calculate Address from Storage buffer and bank.Nothing to do
; when Option number = 3or4 or Bank = 0 or Block number( Previous ) < 32
; or Block number(Previous) >= 48.
; A = Option number, B = Bank, C ... Block number( Previous ),
; DE = Storage buffer first address of get data
                                ; Option number = 5?
      CMP
            A, #05H
      BNZ
            $ReturnAddress end ; NO
      MOV
           А, В
      CMP
          A, #0
                                ; Bank = 0 ?
            $ReturnAddress end ; YES
      ΒZ
            A, C
      XCH
      CMP A, #32
                                ; Block number( Previous ) < 32?
      BC
            $ReturnAddress end ; YES
            A, #48
                                ; Block number( Previous ) >= 48?
      CMP
      BNC
           $ReturnAddress_end ; YES
      MOV
            A, C
; Calculation of address( 40H*Bank is pulled from address in two high rank bytes.
; Lower address is the state as it is. )
      XCHW AX, DE
      MOVW HL, AX
      MOV
           A, [HL+1]
            Χ, Α
      MOV
      MOV
           A, [HL+2]
                               ; A ... Most higher address, X ... Higher address
      XCHW AX, DE
                                ; A ... Bank, D ... Most higher address,
                                ; E ... Higher address
      MOV
            [HL+2], A
                               ; Sets Storage buffer+2 to Bank.
      MOV
            X, #0
            A, 1
      ROL
```

ROL A, 1 A, 1 ROL ROL A, 1 A, 1 ROL ROLC A, 1 XCH Α, Χ ROLC A, 1 ; AX = 40H\*Bank XCHW AX, DE XCH Α, Χ SUB Α, Ε XCH Α, Χ SUBC A, D MOV Α, Χ MOV [HL+1], A ; Sets Storage buffer+1 to Calculated address ; ( higher ). ReturnAddress end: ; Get flash firmware error information A, OFEE3H ; Sets flash firmware error information to return value MOV ; ( OFEE3H = B register of Bank 3 ) FlashGetInfo50: DE POP RET ;-------; Function name : \_\_\_\_FlashSetInfo ; Input : A = Flash information data A = Status ; Output : ; Destroyed register : A ; Summary : Setting of flash information. ;-----FlashSetInfo: ; Set infomation processing PUSH AX ; Save Flash information data in STACK. PUSH PSW ; Save register bank in STACK. SEL RB3 ; Sets to register bank 3. MOVW AX, SP ADDW AX, #2 [HL+5], A ; Sets entry RAM+5 to higher address of flash MOV ; information data secured for stack MOV Α, Χ MOV [HL+4], A ; Sets entry RAM+4 to lower address of flash ; information data secured for stack MOV C, #FLASH SET INF ; Sets function number to C register CALL !8100H ; Calls flash firmware POP PSW ; Restores register bank from STACK. POP AX

```
; Get flash firmware error information
     MOV A, OFEE3H ; Sets flash firmware error information to return value
                      ; ( OFEE3H = B register of Bank 3 )
     RET
; Function name :
                      _CheckFLMD
; Input :
                     None
                    A = Status
; Output :
; Destroyed register :
                     А
; Summary :
                      Checks voltage level of FLMD pin.
;------
CheckFLMD:
; Set infomation processing
     PUSH PSW
                                ; Save register bank in STACK.
     SEL
         RB3
                                ; Sets to register bank 3.
     MOV C, #FLASH CHECK FLMD
                               ; Sets function number to C register
     CALL !8100H
                                ; Calls flash firmware
         PSW
     POP
                                 ; Restores register bank from STACK.
; Get flash firmware error information
     MOV A, OFEE3H
                     ; Sets flash firmware error information to return value
                      ; ( OFEE3H = B register of Bank 3 )
     RET
;-----
; Function name :
                     _EEPROMWrite
; Input :
                     AX = Address of writing beginning address structure
                      ( Member of structure ...
;
                                      Writing starting address
                                      Bank of writing starting address )
                      B = Number of writing data
                      HL = Address in writing data buffer
;
; Output :
                     A = Status
; Destroyed register :
                     AX, C
; Summary :
                      Data on RAM is written in the flash memory.
                     256 bytes or less (Every 4 bytes ) are written at a time.
EEPROMWrite:
    PUSH DE
; Calculate Writing address from writing address and bank.
     CALL !ExchangeAddress ; Writing address is calculated from structure
                           ; member's writing address and bank
                           ; ( Return AX = Writing address )
     ΒZ
           $EW PErr
                     ; It is error if the bank number is outside the range.
; EEPROM write processing
```

PUSH PSW ; Save register bank in STACK. PUSH AX PUSH BC PUSH HL SEL RB3 ; Sets to register bank 3. POP AX MOV ; Sets entry RAM+5 to higher address in writing data [HL+5], A buffer MOV A,X MOV [HL+4], A ; Sets entry RAM+4 to lower address in writing data buffer POP AX MOV [HL+3], A ; Sets entry RAM+3 to Number of writing data MOV A,X MOV [HL+0], A ; Sets entry RAM+0 to Writing address lower bytes POP AX [HL+2], A ; Sets entry RAM+2 to Writing address most higher bytes MOV MOV Α, Χ [HL+1], A MOV ; Sets entry RAM+1 to Writing address higher bytes C, #FLASH EEPROM WRITE ; Sets function number to C register MOV !8100H ; Calls flash firmware CALL POP PSW ; Restores register bank from STACK. ;Get flash firmware error information MOV A,OFEE3H ;Sets flash firmware error information to return value ; (OFEE3H = B register of Bank 3) BR EEPROMWrite00 ; Parameter error EW PErr: MOV A, #FLASHFIRM PARAMETER ERROR ; Sets parameter error to return ; value EEPROMWrite00: POP DE RET ; Function name : ExchangeBlockNum ; Input : A=Bank B = Block number ; A = Block number( New ) ; Output B = Bank ; C = Block number ( Previous ) Block number is converted into the real address from bank ; Summary : ; information. \_\_\_\_\_

```
ExchangeBlockNum:
; It calculates from 32 to 47 block number.
     XCH
         А, В
         A, #32
     CMP
     BC $EBN_end
     CMP A, #48
     BNC
          $EBN end
; Calculation of block number( Bank*16 is added to block number. )
     XCH
          А, В
         С, А
     MOV
                          ; C ... Bank
         A, #6
     CMP
     BNC
          $EBN error end
     ROL
         A, 1
     ROL A, 1
     ROL A, 1
     ROL A, 1
                           ; A = 16*Bank
     ADD A, B
     XCH A, C
     XCH A, B
                           ; A = Block number after it calculates, B = Bank,
     XCH A, C
                             ; C = Block number before it calculates
     BR
          EBN end
; Bank error
EBN error end:
     MOV
         A, #BANK_BLC_ERROR ; Return error number
EBN end:
         A, #BANK BLC ERROR ;Bank error ?
     CMP
     RET
;------
; Function name : ExchangeAddress
               AX = Address of writing beginning address structure
; Input :
;
                 ( Member of structure ... Writing starting address
                                        Bank of writing starting address )
;
               AX = Writing starting address (Address in two high rank bytes )
; Output :
                 C = Writing starting address ( Lower address )
;
               Writing starting address of structure is converted into the
; Summary :
                 real address from bank information.
;
;------
ExchangeAddress:
     PUSH HL
; It calculates from 8000H to BFFFH address.
     MOVW HL, AX
          A, [HL+0]
     MOV
                           ; Read data from writing beginning address
```

```
; structure( =Write address )
      MOV
             X, A
      MOV
             A, [HL+1]
             AX, #8000H
      CMPW
      ВC
             $EA end
      CMPW
             AX, #0C000H
      BNC
             $EA_end
; Calculation of address( Bank*40H is added to address in two high rank bytes.
; Lower address is the state as it is. )
      MOV
             D, A
             Α, Χ
      XCH
      MOV
             C, A
      MOV
             X, #0
             A, [HL+2]
                                ; Read data from writing beginning address
      MOV
structure
                                  ; ( =Bank of writing starting address )
             A, #6
      CMP
      BNC
             $EA error end
      ROL
             A, 1
             A, 1
      ROL
      ROL
             A, 1
      ROL
             A, 1
      ROL
             A, 1
             A, 1
      ROLC
      XCH
             Α, Χ
      ROLC
             A, 1
                                ; AX = 40H*Bank
      XCH
             A, X
      ADD
             A, D
                                 ; Addition of Higher address
      XCH
             Α, Χ
             A, #0
                                  ; Addition of Most higher address
      ADDC
                                  ; A ... Most higher address after it calculates
                                  ; X ... higher address after it calculates,
                                  ; C ... Lower address
      BR
             EA normal end
; Bank error
EA error end:
      MOVW
             AX, #BANK ADDR ERROR
      BR
             EA normal end
EA end:
      XCH
             A, X
             C, A
      MOV
      MOV
             A, #0
                                  ; A ... Most higher address after it calculates
                                  ; X ... higher address after it calculates,
                                  ; C...Lower address
EA normal end:
```

```
POP HL
CMPW AX, #BANK_ADDR_ERROR ; Bank error?
RET
END
```

# A.4 Boot Swap

.....

boot.asm>					
	+++++++++++++++++++++++++++++++++++++++	++++++	+++++	+++	+++++++++++++++++++++++++++++++++++++++
; System :	Sampl	e progra	m that	us	es self programming library
;	( Воо	tswap )			
; File name	: boot.	asm			
; Target CPU	: 78K0/	Kx2			
; Last update	ed: 2005/	04/04			
;++++++++++++++++++++++++++++++++++++++	+++++++++++++++++++++++++++++++++++++++	++++++	++++++	+++	+++++++++++++++++++++++++++++++++++++++
EXTRN _Flash	IStart				
EXTRN _Flash	ıEnd				
EXTRN _Flash	ıEnv				
EXTRN _Flash	BlockErase				
EXTRN _Flash	WordWrite				
EXTRN _Flash	GetInfo				
EXTRN _Flash	SetInfo				
EXTRN _Chec}	FLMD				
;					
; EQU se	ettings				
;					
STATE_OF_ABO	RT	EQU	1FH	;	State of abort
FLASHFIRM_NO	RMAL_END	EQU	00H	;	Normal completion
TRUE		EQU	00H	;	Normal
FALSE		EQU	OFFH	;	Abnormal
PARAMETER_ER	ROR	EQU	05H	;	Parameter error
BANKNUMBER		EQU	0	;	Bank number
BLOCK		EQU	32	;	Block number
;					
; Stores	s stack				
;					
DSTACK DSEG	AT OFB00	Н			
	DS 80H	; STAC	K AREA		
STACKINI:					
;					
	nterrupt vec				
;					
VCTTBL	CSEG AT	0000H			
			; addr		
DW	MAIN		; 00H		

<pre>FPlashEnv EntryRAM: DS 100 S_RAM2 DSEG AF 0FC00H : FlashMordWrite : FlashMordWrite DataBuffer: DS 128 S_RAM3 DSEG : FlashWordWrite WordAddr: WriteAddress: DS 2 WriteBank: DS 1 : FlashGetInfo GetInfo: OptionNumber: DS 1 FlashGetInfoData: DS 1 : FlashGetInfoData: DS 1 : FlashGetInfoData: DS 1 : FlashGetInfoData: DS 1 A_PROC CSEC AT 0400H : Sample program MAIN: DI SEL RE0 ; Sets to register bank 0. MOVW AX, #STACKINI MOVW SP, AX ; Sets stack pointer MOV IMS, #OCCH MOV IMS, #OCCH MOV STS, #05H AAIN_00: NOP EF 0STC.0, \$MAIN_00 CLR1 MCM0 CLR1 MCM0 CLR1 MCM0 CLR1 XSEL AAIN_01: NOP</pre>	;Flash				
<pre>S_RAM2 DEEG AT OFCOOH FlashWordWrite FlashGetInfo DataBuffer: DS 128 S_RAM3 DEEG : FlashGetInfo WordAddr: WriteBank: DS 1 : FlashGetInfo GetInfo: OptionNumber: DS 1 FlashGetInfoData: DS 1 : FlashGetInfoData: DS 1 : FlashGetInfoData: DS 1 4_PROC CSEG AT 0400H : Sample program MAIN: DI SEL RB0 ; Sets to register bank 0. MOVW AX, #STACKINI MOVW SP, AX ; Sets stack pointer MOV IMS, #OCCH MOV IMS, #OCCH MOV IXS, #00H MOV FCC, #00H CLR1 MSTOP MOV OSTS, #05H AAIN_00: NOP BF OSTC.0, SMAIN_00 CLR1 MCM0 CLR1 MCM0 C</pre>		ıEnv			
<pre>FlashWordWrite FlashGetInfo DataBuffer: DS 128 S_RAM3 DSEG FlashWordWrite WordAddr: WriteBank: DS 1 FlashGetInfo GetInfo: OptionNumber: DS 1 FlashGetInfoData: DS 1 FlashGetInfoData: DS 1 FlashGetInfoData: DS 1 FlashBlockErase EraseBlock: DS 1 4_PROG CSEG AT 0400H SEL RB0 ; Sets to register bank 0. MOVW AX, #STACKINI MOVW SP, AX ; Sets stack pointer MOV IMS, #0CH MOV IXS, #00H MOV PCC, #00H CLR1 MSTOP MOV OSTS, #05H AAIN_00: NOP BF OSTC.0, \$MAIN_00 CLR1 MSEL ANN_01:</pre>		EntryF	RAM:	DS	100
<pre>FlashWordWrite FlashGetInfo DataBuffer: DS 128 S_RAM3 DSEG FlashWordWrite WordAddr: WriteBank: DS 1 FlashGetInfo GetInfo: OptionNumber: DS 1 FlashGetInfoData: DS 1 FlashGetInfoData: DS 1 FlashGetInfoData: DS 1 FlashBlockErase EraseBlock: DS 1 4_PROG CSEG AT 0400H SEL RB0 ; Sets to register bank 0. MOVW AX, #STACKINI MOVW SP, AX ; Sets stack pointer MOV IMS, #0CH MOV IXS, #00H MOV PCC, #00H CLR1 MSTOP MOV OSTS, #05H AAIN_00: NOP BF OSTC.0, \$MAIN_00 CLR1 MSEL ANN_01:</pre>					
: FlashGetInfo DataBuffer: DS 128 S_RAM3 DSEG : FlashWordWrite WordAddr: WriteAddress: DS 2 WriteBank: DS 1 : FlashGetInfo GetInfo: OptionNumber: DS 1 FlashGetInfoData: DS 1 : FlashBlockErase EraseBlock: DS 1 4_PROG CSEG AT 0400H 	_			H	
DataBuffer: DS 128 S_RAM3 DSEG : FlashWordWrite WordAddr: WriteAddress: DS 2 WriteBank: DS 1 : FlashGetInfo GetInfo: OptionNumber: DS 1 FlashGetInfoData: DS 1 : FlashBlockErase EraseBlock: DS 1 4_PROG CSEG AT 0400H : Sample program ALIN: DI SEL RB0 ; Sets to register bank 0. MOVW AX, #STACKINI MOVW AX, #STACKINI MOVW SP, AX ; Sets stack pointer MOV IMS, #OCH MOV IXS, #OOH MOV PCC, #OOH CLR1 MSTOP MOV OSTS, #05H HAIN_00: NOP BF OSTC.0, SMAIN_00 CLR1 MSMO CLR1 MSMO	; Flas	hWordW:	rite		
<pre>s_RAM3 DSEG : FlashWordWrite WordAddr: WriteAddress: DS 2 WriteBank: DS 1 : FlashGetInfo GetInfo: OptionNumber: DS 1 FlashGetInfoData: DS 1 FlashGetInfoData: DS 1 : FlashBlockErase EraseBlock: DS 1 4_PROG CSEG AT 0400H</pre>	; Flas	hGetIn	fo		
<pre></pre>		DataBu	iffer:	DS	128
<pre></pre>					
<pre>WordAddr: WriteAddress: DS 2 WriteBank: DS 1 : FlashGetInfo GetInfo: OptionNumber: DS 1 FlashGetInfoData: DS 1 : FlashGetInfoData: DS 1 4_PROG CSEG AT 0400H : Sample program AIN: DI SEL RB0 ; Sets to register bank 0. MOVW AX, #STACKINI MOVW SP, AX ; Sets stack pointer MOV IMS, #OCCH MOV IMS, #OCCH MOV IXS, #OOH MOV PCC, #OOH CLR1 MSTOP MOV OSTS, #05H MAIN_00: NOP BF OSTC.0, \$MAIN_00 CLR1 MCM0 CLR1 MCM0 CLR1 MCM0 CLR1 XSEL MAIN_01:</pre>	S_RAM3	B DSEG			
<pre>WordAddr: WriteAddress: DS 2 WriteBank: DS 1 : FlashGetInfo GetInfo: OptionNumber: DS 1 FlashGetInfoData: DS 1 : FlashGetInfoData: DS 1 4_PROG CSEG AT 0400H : Sample program AIN: DI SEL RB0 ; Sets to register bank 0. MOVW AX, #STACKINI MOVW SP, AX ; Sets stack pointer MOV IMS, #OCCH MOV IMS, #OCCH MOV IXS, #OOH MOV PCC, #OOH CLR1 MSTOP MOV OSTS, #05H MAIN_00: NOP BF OSTC.0, \$MAIN_00 CLR1 MCM0 CLR1 MCM0 CLR1 MCM0 CLR1 XSEL MAIN_01:</pre>					
<pre>WriteAddress: DS 2 WriteBank: DS 1 FlashGetInfo GetInfo: OptionNumber: DS 1 FlashGetInfoData: DS 1 FlashBlockErase EraseBlock: DS 1 4_PROG CSEG AT 0400H Sample program AAIN: DI SEL RB0 ; Sets to register bank 0. MOVW AX, #STACKINI MOVW SP, AX ; Sets stack pointer MOV IMS, #OCCH MOV IMS, #OCCH MOV IXS, #OOH CLR1 MSTOP MOV OSTS, #O5H AAIN_00: NOP BF OSTC.0, \$MAIN_00 CLR1 MCM0 CLR1 MCM0 CLR1 MCM0 CLR1 XSEL AAIN_01:</pre>	; Flas				
<pre>WriteBank: DS 1  FlashGetInfo GetInfo: OptionNumber: DS 1 FlashGetInfoData: DS 1 FlashBlockErase EraseBlock: DS 1  4_PROG CSEG AT 0400H  Sample program AIN: DI SEL RB0 ; Sets to register bank 0. MOVW AX, #STACKINI MOVW SP, AX ; Sets stack pointer MOV IMS, #OCH MOV IMS, #OCH MOV IXS, #O0H  CLR1 MSTOP MOV OSTS, #05H AAIN_00: NOP BF OSTC.0, \$MAIN_00 CLR1 MCM0 CLR1 MCM0 CLR1 MCM0 CLR1 MCM0 CLR1 MSEL AAIN_01:</pre>		WordAc	ldr:		
<pre>FlashGetInfo GetInfo: OptionNumber: DS 1 FlashGetInfoData: DS 1 FlashBlockErase EraseBlock: DS 1 4_PROG CSEG AT 0400H Sample program AIN: DI SEL RB0 ; Sets to register bank 0. MOVW AX, #STACKINI MOVW SP, AX ; Sets stack pointer MOV IMS, #OCCH MOV IMS, #OCCH MOV IXS, #O0H CLR1 MSTOP MOV OSTS, #05H AAIN_00: NOP BF OSTC.0, \$MAIN_00 CLR1 MCM0 CLR1 XSEL AAIN_01:</pre>					
GetInfo: OptionNumber: DS 1 FlashGetInfoData: DS 1 FlashBlockErase EraseBlock: DS 1 4_PROG CSEG AT 0400H Sample program TAIN: DI SEL RB0 ; Sets to register bank 0. MOVW AX, #STACKINI MOVW SP, AX ; Sets stack pointer MOV IMS, #OCCH MOV IMS, #OCCH MOV IXS, #00H MOV PCC, #00H CLR1 MSTOP MOV OSTS, #05H MAIN_00: NOP BF OSTC.0, \$MAIN_00 CLR1 MCM0 CLR1 MCM0 CLR1 MSEL		WriteE	Bank:	DS	1
GetInfo: OptionNumber: DS 1 FlashGetInfoData: DS 1 FlashBlockErase EraseBlock: DS 1 4_PROG CSEG AT 0400H Sample program TAIN: DI SEL RB0 ; Sets to register bank 0. MOVW AX, #STACKINI MOVW SP, AX ; Sets stack pointer MOV IMS, #OCCH MOV IMS, #OCCH MOV IXS, #00H MOV PCC, #00H CLR1 MSTOP MOV OSTS, #05H MAIN_00: NOP BF OSTC.0, \$MAIN_00 CLR1 MCM0 CLR1 MCM0 CLR1 MSEL					
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AAIN: DI SEL RB0 ; Sets to register bank 0. MOVW AX, #STACKINI MOVW SP, AX ; Sets stack pointer MOV IMS, #OCCH MOV IMS, #OCCH MOV IXS, #OOH MOV PCC, #OOH CLR1 MSTOP MOV OSTS, #O5H MAIN_00: NOP BF OSTC.0, \$MAIN_00 CLR1 MCM0 CLR1 XSEL MAIN_01:					
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AAIN: DI SEL RB0 ; Sets to register bank 0. MOVW AX, #STACKINI MOVW SP, AX ; Sets stack pointer MOV IMS, #OCCH MOV IXS, #OOH MOV PCC, #OOH CLR1 MSTOP MOV OSTS, #05H AAIN_00: NOP BF OSTC.0, \$MAIN_00 CLR1 MCM0 CLR1 MCM0 CLR1 XSEL AAIN_01:					
AAIN: DI SEL RB0 ; Sets to register bank 0. MOVW AX, #STACKINI MOVW SP, AX ; Sets stack pointer MOV IMS, #OCCH MOV IMS, #OCCH MOV IXS, #OOH MOV PCC, #OOH CLR1 MSTOP MOV OSTS, #05H AAIN_00: NOP BF OSTC.0, \$MAIN_00 CLR1 MCM0 CLR1 MCM0 CLR1 XSEL					
DI SEL RBO ; Sets to register bank 0. MOVW AX, #STACKINI MOVW SP, AX ; Sets stack pointer MOV IMS, #OCCH MOV IXS, #OOH MOV PCC, #OOH CLR1 MSTOP MOV OSTS, #O5H AAIN_0: NOP BF OSTC.0, \$MAIN_00 CLR1 MCM0 CLR1 MCM0 CLR1 XSEL					
<pre>SEL RB0 ; Sets to register bank 0. MOVW AX, #STACKINI MOVW SP, AX ; Sets stack pointer MOV IMS, #OCCH MOV IXS, #OOH MOV PCC, #OOH CLR1 MSTOP MOV OSTS, #O5H MAIN_00: NOP BF OSTC.0, \$MAIN_00 CLR1 MCM0 CLR1 MCM0 CLR1 XSEL</pre>	MAIN:				
MOVW AX, #STACKINI MOVW SP, AX ; Sets stack pointer MOV IMS, #OCCH MOV IXS, #OOH MOV PCC, #OOH CLR1 MSTOP MOV OSTS, #05H MAIN_00: NOP BF OSTC.0, \$MAIN_00 CLR1 MCM0 CLR1 MCM0 CLR1 XSEL MAIN_01:		D T			
MOVW SP, AX ; Sets stack pointer MOV IMS, #OCCH MOV IXS, #OOH MOV PCC, #OOH CLR1 MSTOP MOV OSTS, #05H MAIN_00: NOP BF OSTC.0, \$MAIN_00 CLR1 MCM0 CLR1 MCM0 CLR1 XSEL MAIN_01:					
MOVW SP, AX ; Sets stack pointer MOV IMS, #OCCH MOV IXS, #OOH MOV PCC, #OOH CLR1 MSTOP MOV OSTS, #05H MAIN_00: NOP BF OSTC.0, \$MAIN_00 CLR1 MCM0 CLR1 MCM0 CLR1 XSEL MAIN_01:			RBO		; Sets to register bank 0.
MOV IMS, #0CCH MOV IXS, #00H MOV PCC, #00H CLR1 MSTOP MOV OSTS, #05H MAIN_00: NOP BF OSTC.0, \$MAIN_00 CLR1 MCM0 CLR1 XSEL MAIN_01:		SEL		_	; Sets to register bank 0.
MOV IXS, #00H MOV PCC, #00H CLR1 MSTOP MOV OSTS, #05H MAIN_00: NOP BF OSTC.0, \$MAIN_00 CLR1 MCM0 CLR1 MCM0 CLR1 XSEL MAIN_01:		SEL MOVW	AX, #STACKIN	I	
MOV IXS, #00H MOV PCC, #00H CLR1 MSTOP MOV OSTS, #05H MAIN_00: NOP BF OSTC.0, \$MAIN_00 CLR1 MCM0 CLR1 MCM0 CLR1 XSEL MAIN_01:		SEL MOVW	AX, #STACKIN	I	
MOV PCC, #00H CLR1 MSTOP MOV OSTS, #05H MAIN_00: NOP BF OSTC.0, \$MAIN_00 CLR1 MCM0 CLR1 XSEL MAIN_01:		SEL MOVW MOVW	AX, #STACKIN SP, AX	I	
CLR1 MSTOP MOV OSTS, #05H MAIN_00: NOP BF OSTC.0, \$MAIN_00 CLR1 MCM0 CLR1 XSEL MAIN_01:		SEL MOVW MOVW MOV	AX, #STACKIN SP, AX IMS, #OCCH	I	
CLR1 MSTOP MOV OSTS, #05H MAIN_00: NOP BF OSTC.0, \$MAIN_00 CLR1 MCM0 CLR1 XSEL MAIN_01:		SEL MOVW MOVW MOV	AX, #STACKIN SP, AX IMS, #OCCH	I	
MOV OSTS, #05H MAIN_00: NOP BF OSTC.0, \$MAIN_00 CLR1 MCM0 CLR1 XSEL MAIN_01:		SEL MOVW MOVW MOV	AX, #STACKIN SP, AX IMS, #OCCH IXS, #OOH	I	
MOV OSTS, #05H MAIN_00: NOP BF OSTC.0, \$MAIN_00 CLR1 MCM0 CLR1 XSEL MAIN_01:		SEL MOVW MOVW MOV	AX, #STACKIN SP, AX IMS, #OCCH IXS, #OOH	I	
MAIN_00: NOP BF OSTC.0, \$MAIN_00 CLR1 MCM0 CLR1 XSEL MAIN_01:		SEL MOVW MOVW MOV MOV	AX, #STACKIN SP, AX IMS, #OCCH IXS, #OOH PCC, #OOH	I	
NOP BF OSTC.0, \$MAIN_00 CLR1 MCM0 CLR1 XSEL MAIN_01:		SEL MOVW MOVW MOV MOV CLR1	AX, #STACKIN SP, AX IMS, #OCCH IXS, #OOH PCC, #OOH MSTOP	I	
BF OSTC.0, \$MAIN_00 CLR1 MCM0 CLR1 XSEL MAIN_01:		SEL MOVW MOVW MOV MOV MOV CLR1 MOV	AX, #STACKIN SP, AX IMS, #OCCH IXS, #OOH PCC, #OOH MSTOP	I	
CLR1 MCM0 CLR1 XSEL MAIN_01:	MAIN_(	SEL MOVW MOVW MOV MOV MOV CLR1 MOV	AX, #STACKIN SP, AX IMS, #OCCH IXS, #OOH PCC, #OOH MSTOP	I	
CLR1 XSEL MAIN_01:	MAIN_(	SEL MOVW MOVW MOV MOV MOV CLR1 MOV	AX, #STACKIN SP, AX IMS, #OCCH IXS, #OOH PCC, #OOH MSTOP OSTS, #05H		
MAIN_01:	MAIN_(	SEL MOVW MOVW MOV MOV MOV CLR1 MOV 00: NOP	AX, #STACKIN SP, AX IMS, #OCCH IXS, #OOH PCC, #OOH MSTOP OSTS, #05H		
_	MAIN_(	SEL MOVW MOV MOV MOV MOV CLR1 MOV O: NOP BF	AX, #STACKIN SP, AX IMS, #OCCH IXS, #OOH PCC, #OOH MSTOP OSTS, #O5H		
NOP	MAIN_0	SEL MOVW MOVW MOV MOV CLR1 MOV O: NOP BF CLR1	AX, #STACKIN SP, AX IMS, #OCCH IXS, #OOH PCC, #OOH MSTOP OSTS, #O5H OSTC.0, \$MAI MCMO		
	_	SEL MOVW MOVW MOV MOV CLR1 MOV O: NOP BF CLR1 CLR1	AX, #STACKIN SP, AX IMS, #OCCH IXS, #OOH PCC, #OOH MSTOP OSTS, #O5H OSTC.0, \$MAI MCMO		

```
MCS, $MAIN_01
    ΒT
    CLR1
        RSTOP
        LVIM, #00H
    MOV
    MOV
       LVIS, #00H
    ΕI
    CALL ! FlashStart ; FlashStart( Self programming start library )
                     ; call processing
;FlashEnv( Initialization library ) call processing
;-----
    MOVW AX, #EntryRAM
    CALL ! FlashEnv
                    ; Initialization library call
;CheckFLMD(Mode check library) call processing
;------
    CALL ! CheckFLMD ; Mode check library call
       A,#TRUE
    CMP
                    ; Normal completion?
    BZ $MAIN 02
                    ; YES
    BR
       MAIN 09
MAIN 02:
;0000H-OFFFH data is copied to 1000H-1FFFH.
;( Block4-7 is first erased, and 0000H-OFFFH data is written afterwards. )
A, #4
   MOV
    MOV !EraseBlock, A
MAIN 03:
; Erase Block4-Block7
   DI
        A, !EraseBlock
    MOV
    MOV
       в, А
    MOV
       A, #0
                        ; A ... Erase bank, B ... Erase block number
    CALL ! FlashBlockErase ; Erase library call
    ΕI
    CMP
       A, #TRUE
                        ; Normal completion?
    BNZ
        $MAIN 09
                         ; NO
```

```
A, !EraseBlock
     MOV
     INC
          А
     MOV
         !EraseBlock,A
     CMP
          A, #8
     ВC
          $MAIN 03
; Write 0000H-OFFFH data to Block4-Block7
         AX, #1000H
     MOVW
     MOVW !WriteAddress, AX
     MOV
          A, #0
     MOV !WriteBank, A
     MOVW HL, #0000H
MAIN 04:
     MOV
         в, #32*4
     MOVW DE, #DataBuffer
MAIN 05:
     MOV
         A, [HL]
         [DE], A
     MOV
     INCW HL
     INCW
         DE
     DBNZ B, $MAIN 05
     PUSH HL
     DI
         A, #32
     MOV
          в, А
     MOV
     MOVW AX, #WordAddr
     MOVW HL, #DataBuffer
     CALL
         ! FlashWordWrite ; Word write library call
     ΕI
         A, #TRUE
                         ; Normal completion?
     CMP
          $MAIN 09
                          ; NO
     BNZ
     POP
          HL
     MOVW AX, !WriteAddress
         AX, #128
     ADDW
     MOVW
         !WriteAddress,AX
         AX, #2000H
     CMPW
          $MAIN 04
     BC
MAIN 06:
;-----
;FlashGetInfo call processing( Boot flag information )
;-----
     MOV
          A, #04H
```

```
!OptionNumber, A
     MOV
          AX, #GetInfo
     MOVW
     MOVW
          BC, #DataBuffer
                         ; AX ... Address of flash information
                          ; acquisition structure,
                           ; BC ... The first address in buffer where get data
                          ; is stored
     CALL ! FlashGetInfo
                         ; Get information library call
          A, #TRUE
                         ; Normal completion ?
     CMP
     BNZ
          $MAIN 09
                          ; NO
          HL, #DataBuffer ; Get boot flag information
     MOVW
     MOV
          A, [HL]
     MOV
         !FlashGetInfoData, A
MAIN 07:
;FlashSetInfo call processing
DI
     MOV
          A, #OFEH
     CALL !_FlashSetInfo ; Set information library call
     ΕI
         A, #TRUE
                      ; Normal completion ?
     CMP
                          ; NO
     BNZ
         $MAIN 09
MAIN_08:
     CALL !_FlashEnd
                         ; FlashEnd( Self programming end library )
                          ; call processing
     ; Normal end
         MAIN LOOP
     BR
MAIN 09:
    CALL ! FlashEnd
                         ; FlashEnd( Self programming end library )
                           ; call processing
     ; Abnormal end
MAIN LOOP:
     NOP
     NOP
     BR
          MAIN LOOP
     END
```

# A.5 Compiling the Flash Self Programming Sample Library and Sample Program

Use the static model sample library and compile options only when using a static model. Otherwise, use the normal model.

- <1> Normal model compile method and options for C
  - ra78K0.exe -cF054780 -yC:¥NECTools32¥DEV SelfLibrary\_normal.asm
  - cc78k0.exe -cF054780 -yC:¥NECTools32¥DEV EEPROMCtrl.c
  - cc78k0.exe -cF054780 -yC:¥NECTools32¥DEV Main.c
  - Ik78K0.exe -yC:¥NECTools32¥DEV -oMain.lmf C:¥NECTools32¥LIB78K0¥s0l.rel -bcl0.lib -s Main.rel SelfLibrary\_normal.rel EEPROMCtrl.rel
  - oc78K0.exe -yC:¥NECTools32¥DEV Main.lmf
- <2> Static model compile method and options for C
  - ra78K0.exe -cF054780 -yC:¥NECTools32¥DEV SelfLibrary\_static.asm
  - cc78k0.exe -sm0 -cF054780 -yC:¥NECTools32¥DEV EEPROMCtrl.c
  - cc78k0.exe -sm0 -cF054780 -yC:¥NECTools32¥DEV Main.c
  - Ik78K0.exe -yC:¥NECTools32¥DEV -oMain.Imf C:¥NECTools32¥LIB78K0¥s0sml.rel -bcl0sm.lib -s Main.rel SelfLibrary\_static.rel EEPROMCtrl.rel
  - oc78K0.exe -yC:¥NECTools32¥DEV Main.lmf
- <3> Normal model compile method and options for assembler
  - ra78K0.exe -cF054780 -yC:¥NECTools32¥DEV USER\_MAIN.asm
  - ra78K0.exe -cF054780 -yC:¥NECTools32¥DEV EEPROM.asm
  - ra78K0.exe -cF054780 -yC:¥NECTools32¥DEV SelfLibrary\_normal.asm
  - Ik78K0.exe -yC:¥NECTools32¥DEV USER\_MAIN.rel EEPROM.rel SelfLibrary\_normal.rel
  - oc78K0.exe -yC:¥NECTools32¥DEV USER\_MAIN.lmf
- <4> Static model compile method and options for assembler
  - ra78K0.exe -cF054780 -yC:¥NECTools32¥DEV USER\_MAIN.asm
  - ra78K0.exe -cF054780 -yC:¥NECTools32¥DEV EEPROM.asm
  - ra78K0.exe -cF054780 -yC:¥NECTools32¥DEV SelfLibrary\_static.asm
  - Ik78K0.exe -yC:¥NECTools32¥DEV USER\_MAIN.rel EEPROM.rel SelfLibrary\_static.rel
  - oc78K0.exe -yC:¥NECTools32¥DEV USER\_MAIN.lmf

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