MC3301 LM2900
MC3401 LM3900

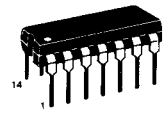
QUAD
OPERATIONAL AMPLIFIERS

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**

Quad Single Supply Operational Amplifiers

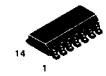
These internally compensated Norton operational amplifiers are designed specifically for single positive power supply applications found in industrial control systems and automotive electronics. Each device contains four independent amplifiers — making it ideal for applications such as active filters, multi-channel amplifiers, tachometers, oscillators and other similar usage.

- Single Supply Operation
- Internally Compensated
- Wide Unity Gain Bandwidth: 4.0 MHz Typical
- Low Input Bias Current: 50 nA Typical
- High Open-Loop Gain: 1000 V/V Minimum
- Large Output Voltage Swing: (V_{CC} — 1) V_{p-p}

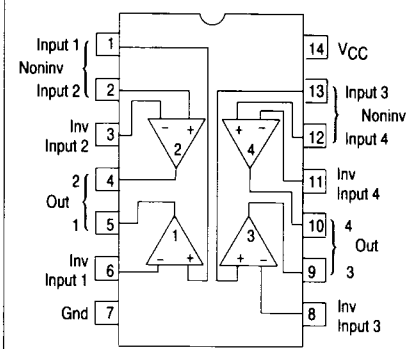


N, P SUFFIX
PLASTIC PACKAGE
CASE 646

D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)



PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS

Rating	Symbol	LM2900/ LM3900	MC3301	MC3401	Unit
Supply Voltage	V_{CC}	+32	+28	+18	V
Input Current (I_{in} + or I_{in} –)	I_{in}	5.0			mA
Output Current	I_O	50			mA
Power Dissipation (T_A = +25°C) Derate above T_A = +25°C	P_D $1/R_{\theta JA}$	625 5.0			mW mW/°C
Ambient Temperature Range LM2900 LM3900	T_A	 –40 to +85 0 to +70	 –40 to +85	 0 to +70	°C
Storage Temperature Range	T_{stg}	–65 to +150			°C

ORDERING INFORMATION

Device	Temperature Range	Package
LM3900D MC3401D	0° to +70°C	SO-14
LM3900N MC3401P	0° to +70°C	Plastic DIP
LM2900N MC3301P	–40° to +85°C	Plastic DIP

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, R_L = 5.0 kΩ, T_A = +25°C [each amplifier], unless otherwise noted.)

Characteristics	Symbol	LM2900			LM3900			MC3301			MC3401			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Open-Loop Voltage Gain f = 100 Hz, R_L = 5.0 k $T_A = T_{low}$ to T_{high} (Notes 1, 2)	A_{VOL}	1.2 —	2.0 —	— —	1.2 —	2.0 —	— —	1.2 —	2.0 —	— —	1.2 0.8	2.0 —	— —	V/mV
Input Resistance (Inverting Input)	r_i	—	1.0	—	—	1.0	—	—	1.0	—	0.1	1.0	—	MΩ
Output Resistance	r_o	—	8.0	—	—	8.0	—	—	8.0	—	—	8.0	—	kΩ
Input Bias Current (Inverting Input) $T_A = T_{low}$ to T_{high} (Note 1)	I_{IB}	— —	50 —	200 —	— —	50 —	200 —	— —	50 —	300 —	— —	50 —	300 500	nA
Slew Rate (C_L = 100 pF, R_L = 2.0 k) Positive Output Swing Negative Output Swing	SR	— —	0.5 20	— —	— —	0.5 20	— —	— —	0.5 20	— —	— —	0.5 20	— —	V/μs
Unity Gain Bandwidth	BW	—	4.0	—	—	4.0	—	—	4.0	—	—	4.0	—	MHz
Output Voltage Swing (Note 7) V_{CC} = +15 V, R_L = 2.0 k V_{out} High (I_{in}^- = 0, I_{in}^+ = 0) V_{out} Low (I_{in}^- = 10 μA, I_{in}^+ = 0) V_{CC} = Maximum Rating, R_L = ∞ V_{out} High (I_{in}^- = 0, I_{in}^+ = 0)	 V_{OH} V_{OL} V_{OH}	 13.5 — —	 14.2 0.03 29.5	 — 0.2 —	 13.5 — —	 14.2 0.03 29.5	 — 0.2 —	 13.5 — —	 14.2 0.03 25.5	 — 0.2 —	 13.5 — —	 14.2 0.03 15.5	 — 0.2 —	V
Output Current Source Sink (Note 3) Low Level Output Current I_{in}^- = 5.0 μA, V_{OL} = 1.0 V	 I_{Source} I_{Sink} I_{OL}	 6.0 0.5 —	 10 0.87 5.0	 — — —	 6.0 0.5 —	 10 0.87 5.0	 — — —	 5.0 0.5 —	 10 0.87 5.0	 5.0 0.5 —	 5.0 0.5 —	 10 0.87 5.0	 — — —	mA
Supply Current (All Four Amplifiers) Noninverting Inputs Open Noninverting Inputs Grounded	 I_{DO} I_{DG}	 — —	 6.9 7.8	 10 14	 — —	 6.9 7.8	 10 14	 — —	 6.9 7.8	 10 14	 — —	 6.9 7.8	 10 14	mA
Power Supply Rejection (f = 100 Hz)	PSR	—	55	—	—	55	—	—	55	—	—	55	—	dB
Mirror Gain ($T_A = T_{low}$ to T_{high}; Notes 1, 4) I_{in}^+ = 20 μA I_{in}^+ = 200 μA	A_i	 0.90 0.90	 1.0 1.0	 1.1 1.1	 0.90 0.90	 1.0 1.0	 1.1 1.1	 0.90 0.90	 1.0 1.0	 1.1 1.1	 0.90 0.90	 1.0 1.0	 1.1 1.0	μA
Δ Mirror Gain ($T_A = T_{low}$ to T_{high}; Notes 1, 4) 20 μA ≤ I_{in}^+ ≤ 200 μA	ΔA_i	—	2.0	5.0	—	2.0	5.0	—	2.0	5.0	—	2.0	5.0	%
Mirror Current ($T_A = T_{low}$ to T_{high}; Notes 1, 5)		—	10	500	—	10	500	—	10	500	—	10	500	μA
Negative Input Current (Note 6)		—	1.0	—	—	1.0	—	—	1.0	—	—	1.0	—	mA

NOTES: 1. T_{low} = −40°C for LM2900, MC3301; T_{high} = +85°C for LM290, MC3301
= 0°C for LM3900, MC3401 = +70°C for LM3900, MC3401

2. Open-Loop voltage gain is defined as voltage gain from the inverting input to the output.
3. Sink current is specified for linear operation. When the device is used as a comparator (non-linear operation) where the inverting input is overdriven, the sink current (low level output current) capability is typically 5.0 mA.
4. This specification indicates the current gain of the current mirror which is used as the noninverting input.
5. Input V_{BE} match between the noninverting and inverting inputs occurs for a mirror current (noninverting input current) of approximately 10 μA.
6. Clamp transistors are included to prevent the input voltages from swinging below ground more than approximately −0.3 V. The negative input currents that may result from large signal overdrive with capacitive input coupling must be limited externally to values of approximately 1.0 mA. If more than one of the input terminals are simultaneously driven negative, maximum currents are reduced. Common mode biasing can be used to prevent negative input voltages.
7. When used as a noninverting amplifier, the minimum output voltage is the V_{BE} of the inverting input transistor.

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Figure 1. Open-Loop Voltage Gain versus Frequency

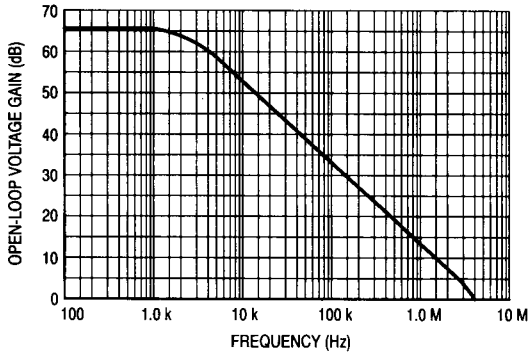


Figure 2. Open-Loop Voltage Gain versus Supply Voltage

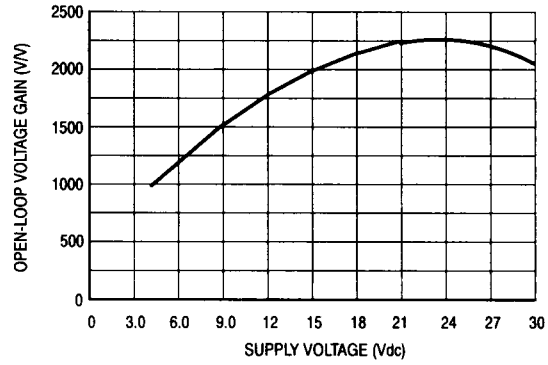


Figure 3. Output Resistance versus Frequency

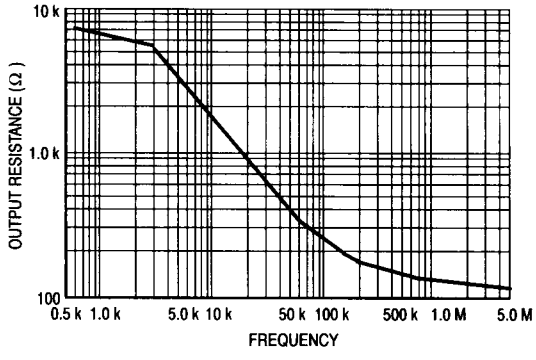


Figure 4. Supply Current versus Supply Voltage

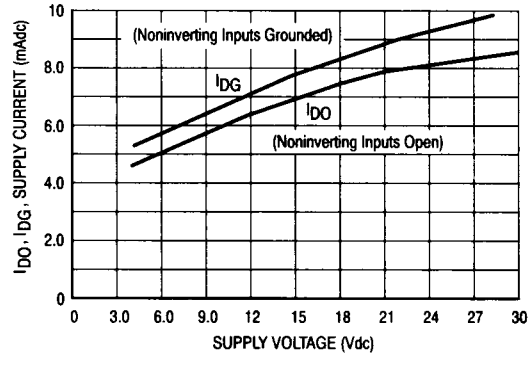


Figure 5. Linear Source Current versus Supply Voltage

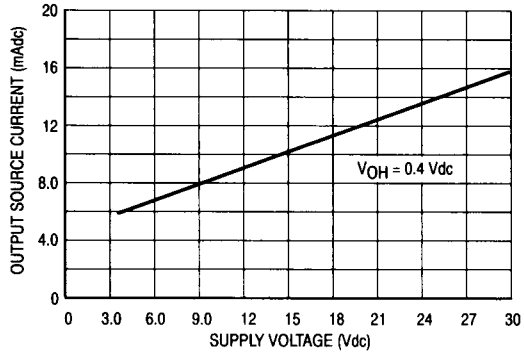
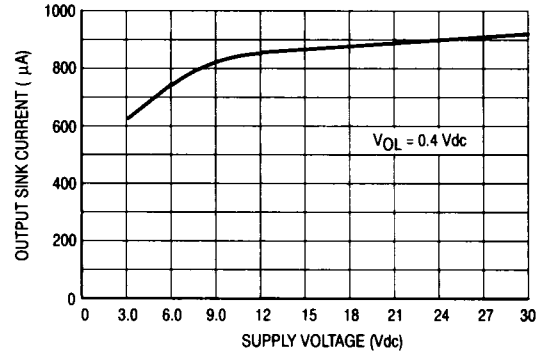


Figure 6. Linear Sink Current versus Supply Voltage

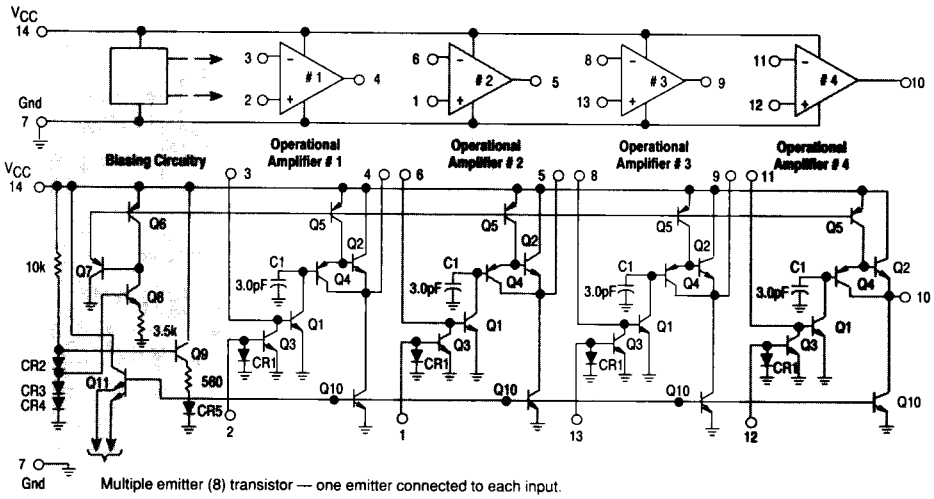


OPERATION AND APPLICATIONS

Basic Amplifier

The basic amplifier is the common emitter stage shown in Figures 7 and 8. The active load I_1 is buffered from the input transistor by a PNP transistor, Q4, and from the output by an NPN transistor, Q2. Q2 is biased Class A by the current source I_2. The magnitude of I_2 (specified I_{sink}) is a limiting factor in capacitively coupled linear operation at the output. The sink of the device can be forced to exceed the specified level by keeping the output dc voltage above ≈ 1.0 V resulting in an increase in the distortion appearing at the output. Closed-loop stability is maintained by an on-the-chip 3-pF capacitor shown in Figure 10 on the following page. No external compensation is required.

Figure 7. Block Diagram



Multiple emitter (8) transistor — one emitter connected to each input.

A noninverting input obtained by adding a current mirror as shown in Figure 9. Essentially all current which enters the noninverting input, I_{in}^+, flows through the diode CR1. The voltage drop across CR1 corresponds to this input current magnitude and this same voltage is applied to a matched device, Q3. Thus Q3 is biased to conduct an emitter current equal to I_{in}^+. Since the alpha current gain of Q3 ≈ 1, its collector current is approximately equal to I_{in}^+ also. In operation this current flows through an external feedback resistor which generates the output voltage signal. For inverting applications, the noninverting input is often used to set the dc quiescent level at the output. Techniques for doing this are discussed in the "Normal Design Procedure" section.

Figure 8. A Basic Gain Stage

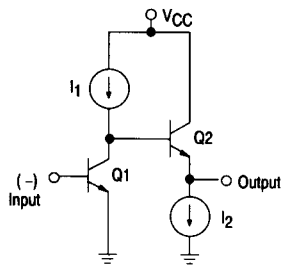
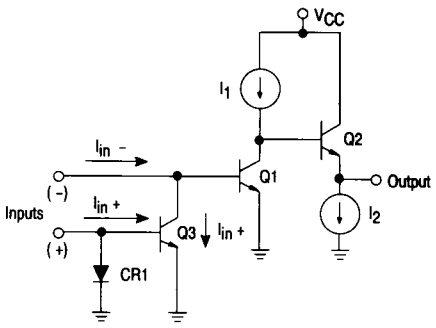


Figure 9. Obtaining A Noninverting Input



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Biasing Circuitry

The circuitry common to all four amplifiers is shown in Figure 11. The purpose of this circuity is to provide biasing voltage for the PNP and NPN current sources used in the amplifiers.

The voltage drops across diodes CR2, CR3 and CR4 are used as references. The voltage across resistor R1 is the sum of the drops across CR4 and CR3 minus the V_{BE} of Q8. The PNP current sources (Q5, ect.) are set to the magnitude V_{BE}/R1 by transistor Q6. Transistor Q7 reduces base current loading. The voltage across resistor R_2 is the sum of the voltage drops across CR2, CR3 and CR4, minus the V_{BE} drops of transistor Q9 and diode CR5 thus the current set is established by CR5 in all the NPN current sources (Q10, ect.). This technique results in current source magnitudes which are relatively independent of the supply voltage. Q11 (Figure 7) provides circuit protection from signals that are negative with respect to ground.

Figure 10. A Basic Operational Amplifier

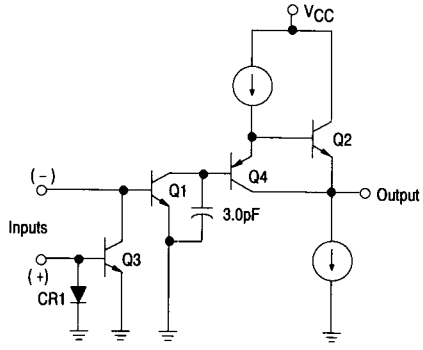
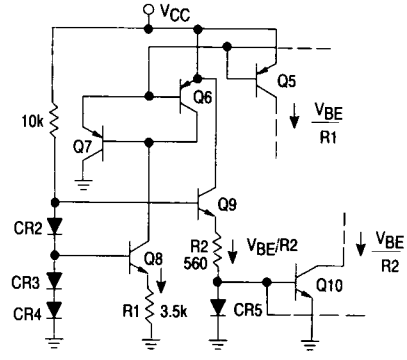


Figure 11. Biasing Circuitry



NORMAL DESIGN PROCEDURE

1. Output Q-Point Biasing
   A. A number of techniques may be devised to bias the quiescent output voltage to an acceptable level. However, in terms of loop gain considerations it is usually desirable to use the noninverting input to effect the biasing, as shown in Figures 12 and 13. The high impedance of the collector of the noninverting "current mirror" transistor helps to achieve the maximum loop gain for any particular configuration. It is desirable that the noninverting input current be in the 10 μA to 200 μA range.

   B. V_{CC} Reference Voltage (see Figures 12 and 13)
   The noninverting input is normally returned to the V_{CC} voltage (which should be well filtered) through a resistor (R_f) allowing the input current, (I_{in}^+) to be within the range of 10 μA to 200 μA. Choosing the feedback resistor (R_f) to be equal to $^1/_2 R_r$ will now bias the amplifier output DC level to approximately $V_{CC}/2$. This allows the maximum dynamic range of the output voltage.

   C. Reference Voltage other than V_{CC} (see Figure 14)
   The biasing resistor (R_r) may be returned to a voltage(V_r) other than V_{CC}. By setting $R_f = R_r$, (still keeping I_{in} +between 10 μA and 200 μA) the output DC level will be equal to V_r. The expression for determining V_{Odc} is:

$$V_{Odc} = \frac{(A_i)(V_r)(R_f)}{R_r} + \left(1 - \frac{R_f}{R_r}\ A_i\right)\phi$$

   where ϕ is the V_{BE} drop of the input transistors (approximately 0.6 Vdc @ +25°C and assumed equal). A_i is the current mirror gain.

Figure 12. Inverting Amplifier

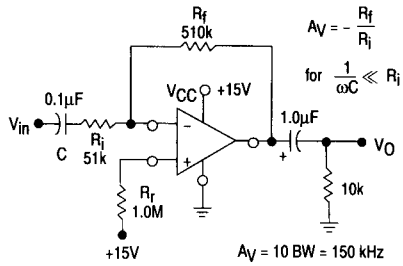
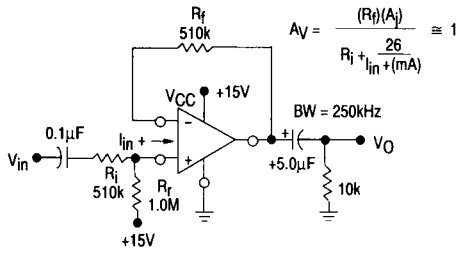


Figure 13. Noninverting Amplifier



2. Gain Determination

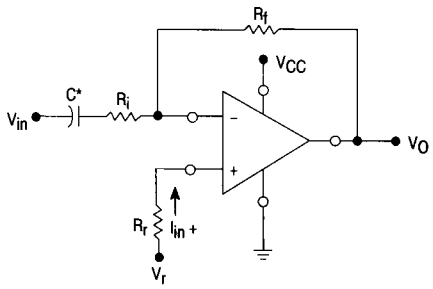
A. Inverting Amplifier

The amplifier is normally used in the inverting mode. The input may be capacitively coupled to avoid upsetting the dc bias and the output is normally capacitively coupled to eliminate the dc voltage across the load. Note that when the output is capacitively coupled to the load, the value of I_{sink} becomes a limitation with respect to the load driving capabilities of the device is direct coupled. In this configuration, the ac gain is determined by the ratio of R_f to R_i, in the same manner as for a conventional operational amplifier:

$$A_V = \frac{R_f}{R_i}$$

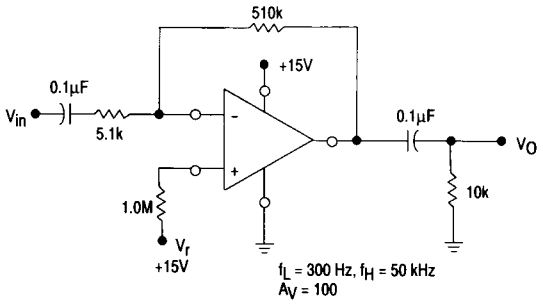
The lower corner frequency is determined by the coupling capacitors to the input and load resistors. The upper corner frequency will usually be determined by the amplifier internal compensation. The amplifier unity gain bandwidth is typically be 400 kHz with 20 dB of closed-loop gain or 40 kHz with 40 dB of closed-loop gain. The exception to this occurs at low gains where the input resistor selected is large. The pole formed by the amplifier input capacitance, stray capacitance and the input resistor may occur before the closed-loop gain intercepts the open-loop response curve. The inverting input capacity is typically 3.0 pF.

Figure 14. Inverting Amplifier with Arbitrary Reference



*Select for low frequency response.

Figure 15. Inverting Amplifier with $A_V = 100$ and $V_r = V_{CC}$



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B. Noninverting Amplifier

These devices may be used in the noninverting mode (see Figure 13). The amplifier gain in this configuration is subject to the current mirror gain. In addition, the resistance of the input diode must be included in the value of the input resistor. This resistance is approximately $\frac{26}{I_{in+}}\ \Omega$, where I_{in+} is input current in milliamperes. The noninverting AC gain expression is given by:

$$A_V = \frac{(R_f)(A_i)}{R_i + \frac{26}{I_{in+}(mA)}}$$

The bandwidth of the noninverting configuration for a given R_f value is essentially independent of the gain chosen. For $R_f = 510\ k\Omega$ the bandwidth will be in excess of 200 kHz for noninverting of 1, 10, or 100. This is a result of the loop gain remaining constant for these gains since the the input resistor is effectively isolated from the feedback loop.

Figure 16. Tachometer Circuit

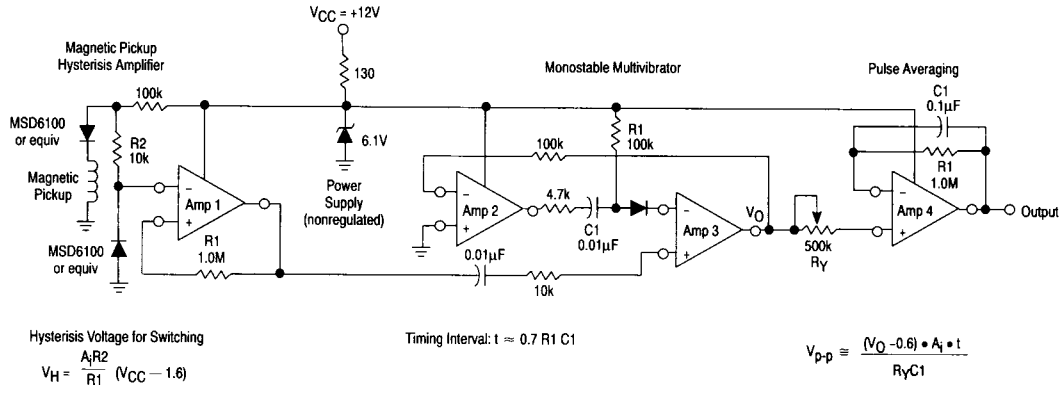
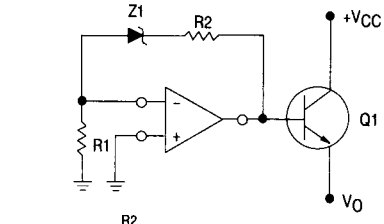


Figure 17. Voltage Regulator



$V_O = V_{Z1} + 0.6\ (1 + \frac{R2}{R1}) - V_{BE_{Q1}}$

Note: For positive T_C zeners R2 and R1 can be selected to give T_C output.

Figure 18. Logic "OR" Gate

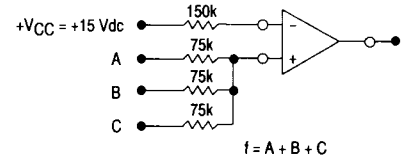


Figure 19. Logic "NAND" Gate (Large Fan-In)

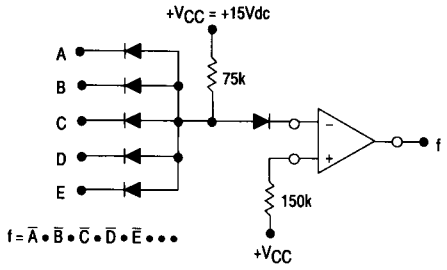


Figure 20. Logic "NOR" Gate

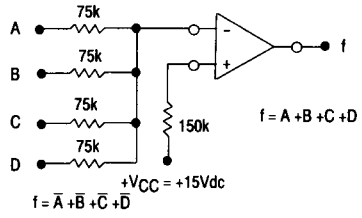


Figure 21. R-S Flip-Flop

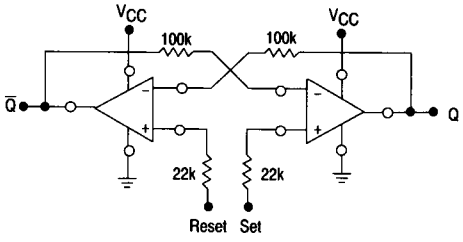


Figure 22. Astable Multivibrator

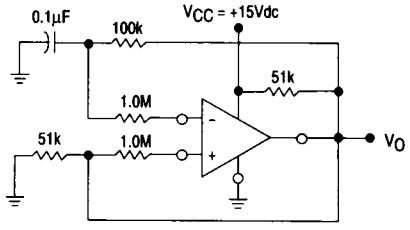


Figure 23. Positive-Edge Differentiator

Output Rise Time ≈ 0.22 ms
Input Change Time Constant ≈ 1.0 ms

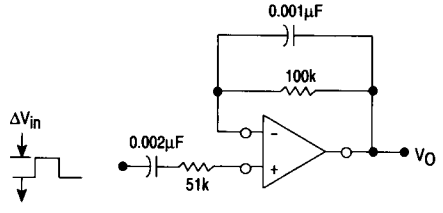
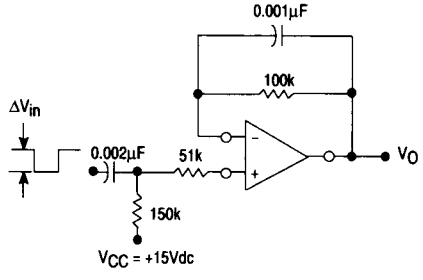


Figure 24. Negative-Edge Differentiator



VO(dc) ≈ 7.0 Vdc
Output Rise Time ≈ 0.22 ms
Input Change Time Constant ≈ 1.0 ms

2

Figure 25. Amplifier and Driver for a 50 Ω Line

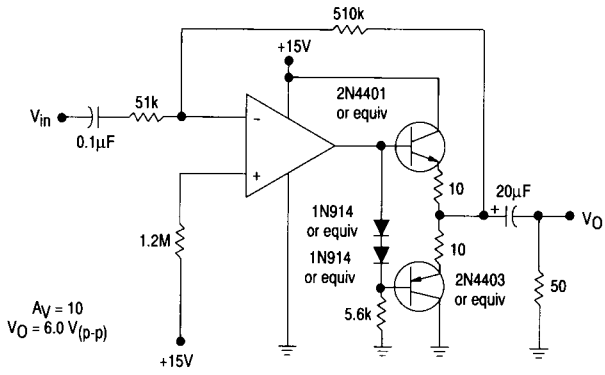


Figure 26. Basic Bandpass and Notch Filter

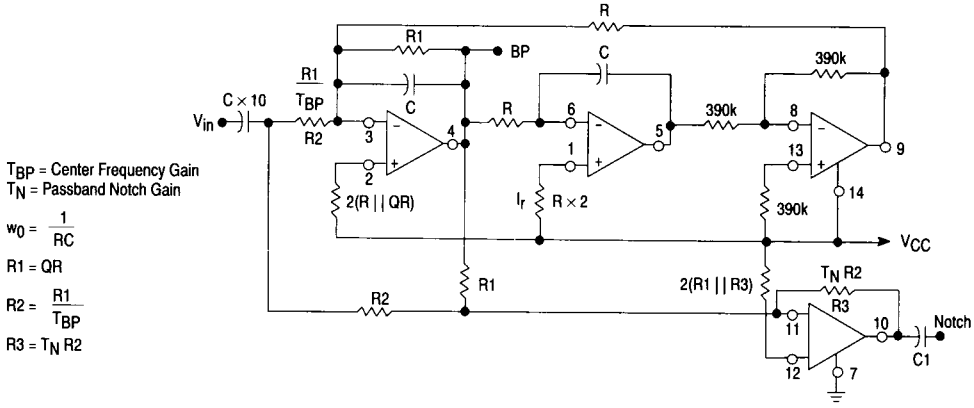


Figure 27. Bandpass and Notch Filter

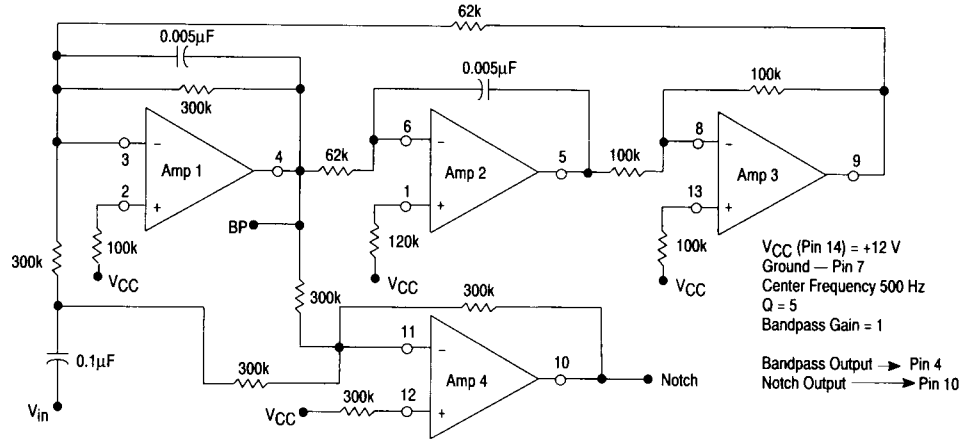
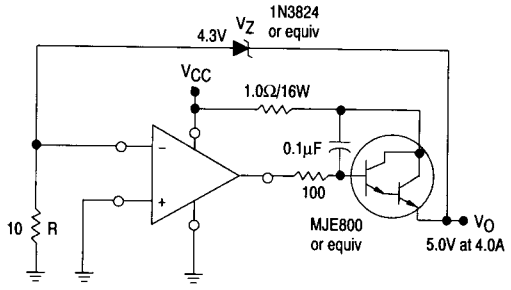


Figure 28. Voltage Regulator



$V_O = V_Z + 0.6$ Vdc

NOTES:
1. R is used to bias the zener.
2. If the zener TC is positive, and equal in magnitude to the negative TC of the input to the operational amplifier (≈2.0 mV/°C), the output is zero-TC. A 7.0 V zener will give approximately zero-TC.

Figure 29. Zero Crossing Detector