AN-6756

Applying FAN6756 to Control a Flyback Power Supply with Ultra-Low Standby Power

1. Introduction

Requirements for low standby power consumption are increasing due to the environmental impact of the energy wasted by idle electronic devices. Fairchild's new-generation green-mode PWM controller, FAN6756, incorporates innovative mWSaver™ technology, which dramatically reduces the standby and no-load power consumption of a power supply with minimum external components.

The AX-CAP™ innovation, one of the mWSaver™ technologies, removes the X-capacitor bleeder resistor and its loss in EMI filter stage through intelligent detection and discharge methods. At no-load or extremely light-load conditions, Standby Mode dramatically reduces the switching losses by minimizing the switching frequency while maintaining the controller supply voltage at the minimum level. Combined with ultra-low operation current in Standby Mode, the power consumption of PWM controller itself is also minimized.

This application note presents the step-by-step design with an example of applying FAN6756 to a flyback power supply. It covers designing of the transformer and selecting the external components.

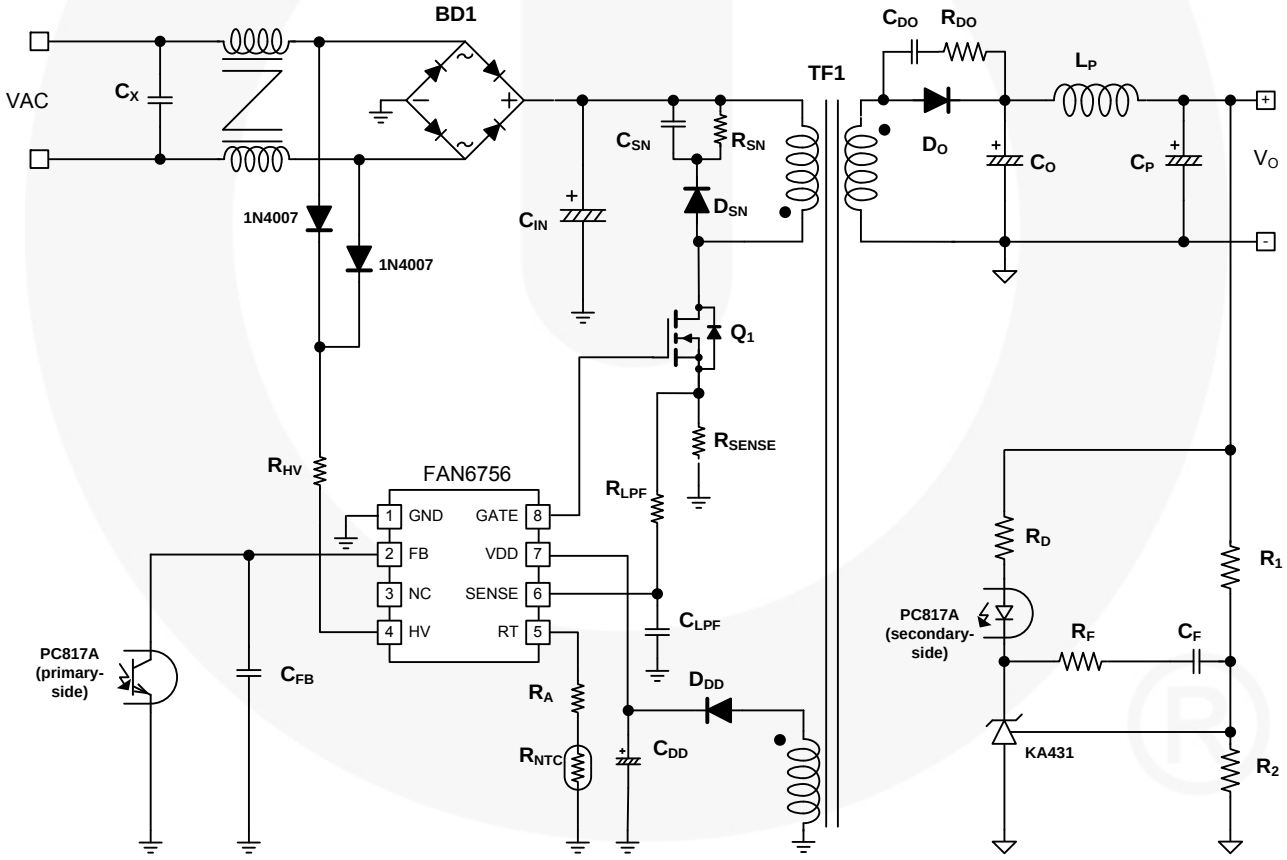

Figure 1. Typical Application

2. Design Consideration

In this section, a design procedure is presented using the schematic of Figure 1 as a reference. An offline flyback Switched Mode Power Supply (SMPS) with 65W / 19V output power has been selected as a design example. *For detailed explanation for flyback transformer design, refer to AN-4140 — Transformer Design Consideration for Offline Flyback Converters Using Fairchild Power Switch (FPS™).*

Step 1 - Estimate Rated Input Power (P_{IN})

Define Parameter:

- Nominal output power: P_O^{NOM}
- Estimated efficiency for maximum load: η

Design Tips:

- If no reference data is available, set η = 0.7-0.75 for low-voltage output applications and η = 0.8-0.85 for high-voltage output applications.

Design Example:

- P_O^{NOM}= 65W (19V / 3.42A)
- η = 0.85

$$P_{IN} = \frac{P_O^{NOM}}{\eta} = \frac{65}{0.85} = 76.5\,(\mathrm{W})$$

Step 2 - Determine the Input Capacitor (C_{IN}) and the Input Voltage Range (V_{IN}^{MIN}, V_{IN}^{MAX})

Define Parameter:

- Line voltage range: V_{LINE}^{MIN} and V_{LINE}^{MAX}
- Line frequency: f_L
- Ripple factor of line voltage (D_{CH}), as defined in Figure 2.

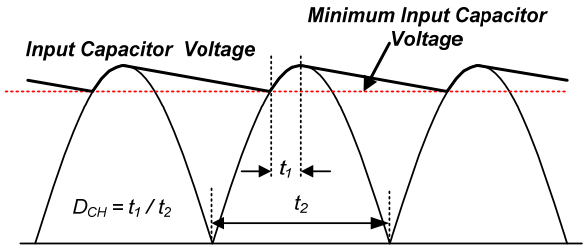

Figure 2. Input Capacitor Voltage Waveform

Design Tips:

- It is typical to select the input capacitor as 1.5-2μF per wattage of peak input power for universal input range (85 - 265 V_{RMS}) and 0.7-0.8μF per watt of peak input power for European input range (195 - 265 V_{RMS}).
- D_{CH} is related with selection of input capacitor. It is typical to set as 0.2.

Design Example:

- V_{LINE}^{MIN} = 90 V_{RMS}, V_{LINE}^{MAX} = 264 V_{RMS}
- f_L = 60Hz
- D_{CH}= 0.2
- C_{IN}=120μF

$$V_{IN}^{MIN} = \sqrt{2 \cdot \left(V_{LINE}^{MIN}\right)^2 - \frac{P_{IN} \cdot (1 - D_{CH})}{C_{IN} \cdot f_L}}$$

$$= \sqrt{2 \cdot (90)^2 - \frac{76.5 \cdot (1 - 0.2)}{120 \times 10^{-6} \cdot 60}} = 88V$$

$$V_{IN}^{MAX} = \sqrt{2} \cdot V_{LINE}^{MAX} = \sqrt{2} \cdot 264 = 373V$$

Step 3 - Determine the Maximum Duty Ratio (D_{MAX}) and Nominal MOSFET Voltage (V_{DS}^{NOM})

Define Parameter:

- The reflected voltage of output to the primary-side winding (V_{RO}), as illustrated in Figure 3.

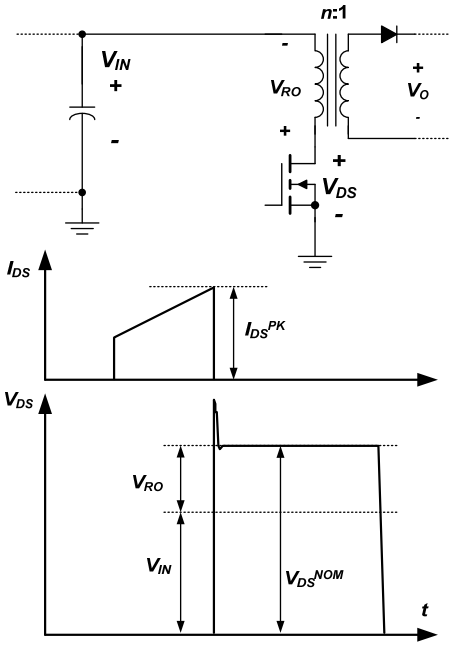

Figure 3. Typical MOSFET V_{DS} Waveform

Design Tips:

- V_{RO} should be determined by trade-offs between the voltage stress on MOSFET and output rectifier diode.
- It is typical to select a 650V MOSFET for applications with universal input range. Since V_{IN}^{MAX} is 373V, V_{RO} should be set around 70-100V so that V_{DS}^{NOM} is 440 - 470V for 68 - 72% of MOSFET voltage rating.
- Reducing leakage inductance helps reduce the voltage spike on V_{DS} since the voltage spike is proportional to the leakage inductance of the transformer.

Design Example:

- $V_{RO} = 95\text{V}$

$$D_{MAX} = \frac{V_{RO}}{V_{RO} + V_{IN}^{MIN}} = \frac{95}{95+88} = 0.52$$

$$V_{DS}^{NOM} = V_{IN}^{MAX} + V_{RO} = 373 + 95 = 468\,(\text{V})$$

Step 4 - Determine the Transformer Primary-Side Inductance (L_M)

Define Parameter:

- Ripple factor of primary switching current: K_{RF}, as defined in Figure 4.
- Switching frequency at the maximum load: f_S^{MAX}

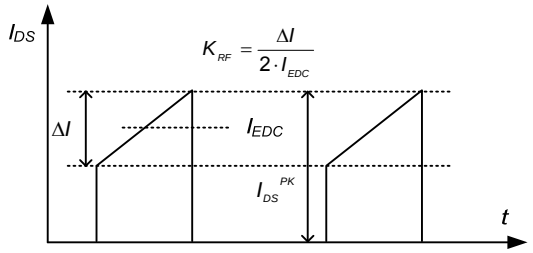

Figure 4. Typical MOSFET Current Waveform

Design Tips:

- Ripple factor K_{RF} is closely related to the transformer size and the RMS value of the MOSFET current.
- Smaller K_{RF} leads to lower RMS current and reduces the conduction loss; however, too small K_{RF} increases transformer size.
- From a practical point of view, it is reasonable to set K_{RF} = 0.3-0.6 for the universal input range and K_{RF} = 0.4-0.8 for the European input range.

Design Example:

- $K_{RF} = 0.41$
- $f_S^{MAX} = 65\text{kHz}$

$$L_M = \frac{(V_{IN}^{MIN} \cdot D_{MAX})^2}{2 \cdot P_{IN} \cdot f_S^{MAX} \cdot K_{RF}} = \frac{(88 \cdot 0.52)^2}{2 \cdot 76.5 \cdot 65 \times 10^3 \cdot 0.41} = 513\,(\mu\text{H})$$

Step 5 - Calculate the RMS Current of MOSFET (I_{DS}^{RMS})

Define Parameter:

- Average current of MOSFET current: I_{EDC}
- Ripple of MOSFET current: ΔI, illustrated in Figure 4.

Design Example:

$$I_{EDC} = \frac{P_{IN}}{V_{IN}^{MIN} \cdot D_{MAX}} = \frac{76.5}{88 \cdot 0.52} = 1.67\,(\text{A})$$

$$\Delta I = \frac{V_{IN}^{MIN} \cdot D_{MAX}}{L_M \cdot f_S^{MAX}} = \frac{88 \cdot 0.52}{513 \times 10^{-6} \cdot 65 \times 10^3} = 1.372\,(\text{A})$$

$$I_{DS}^{RMS} = \sqrt{\left[3 \cdot (I_{EDC})^2 + \left(\frac{\Delta I}{2}\right)^2\right] \cdot \frac{D_{MAX}}{3}} = \sqrt{\left[3 \cdot (1.67)^2 + (0.686)^2\right] \cdot \frac{0.52}{3}} = 1.24\,(\text{A})$$

Step 6 - Determine the Sense Resistor Value (R_{SENSE})

Since the determination of R_{SENSE} is related to the current limit level, V_{LIMIT}; it is necessary to understand the characteristic of V_{LIMIT}. As Figure 5 shows, V_{LIMIT} is determined by the detected AC line peak voltage, V_{LINE}^{PK}. The line voltage is sampled by R_{HV} and an internal resistor R_{LS}. The equation of V_{LIMIT} is given by:

$$V_{LIMIT} = \frac{V_{LIMIT-H} - V_{LIMIT-L}}{2} \cdot \frac{R_{LS}}{R_{HV}} \cdot V_{LINE}^{PK} + \frac{3 \cdot V_{LMIT-L} - V_{LIMIT-H}}{2} \quad (1)$$

where $V_{LIMIT-H}$ and $V_{LIMIT-L}$ is the current limit level when V_{LIMIT}^{PK} is 366V and 122V, respectively.

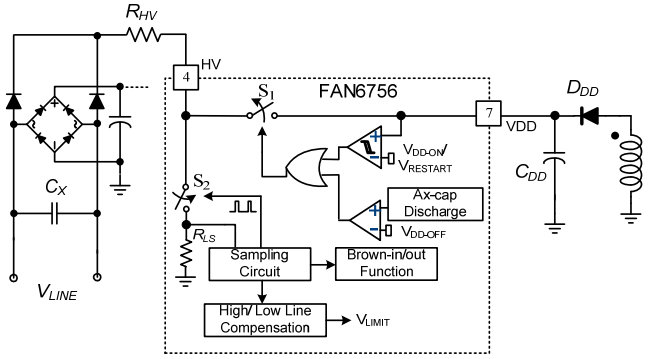

Figure 5. HV Pin Functional Block Diagram

Define Parameter:

- Peak value of input voltage: V_{LINE}^{PK}
- Current-limit level when V_{LINE}^{PK} is 366V: $V_{LIMIT-H}$
- Current-limit level when V_{LINE}^{PK} is 122V: $V_{LIMIT-L}$
- HV pin resistor: R_{HV}
- Internal sampling resistor: R_{LS}
- Switching frequency: f_S
- MOSFET peak current: I_{DS}^{PK}
- MOSFET peak current at over-power protection (OPP): I_{DS-OPP}^{PK}
- Output power at OPP: P_{O-OPP}

Design Tips:

- R_{SENSE} is determined by considering the pulse-by-pulse current-limit threshold.
- Set P_O^{OPP} as 115-135% of nominal output load. Start with the minimum input voltage and 200kΩ R_{HV} resistor, then check the over-power protection level for the entire line voltage range. Last, fine-tune R_{SENSE} to make P_O^{OPP} within 115-135% of P_O^{NOM}.
- Figure 6 shows the frequency modulation curve of FAN6756. If the system operates in frequency reduction region (from V_{FB-N} to V_{FB-G}), estimation of the peak current becomes more complex since the switching frequency varies with feedback voltage, V_{FB}. Therefore, make sure that V_{FB} is over V_{FB-N} when output power is closed to P_O^{OPP}. In addition, the high/low line compensation is more accurate since the switching frequency is identical in high/low line when V_{FB} is over V_{FB-N}.

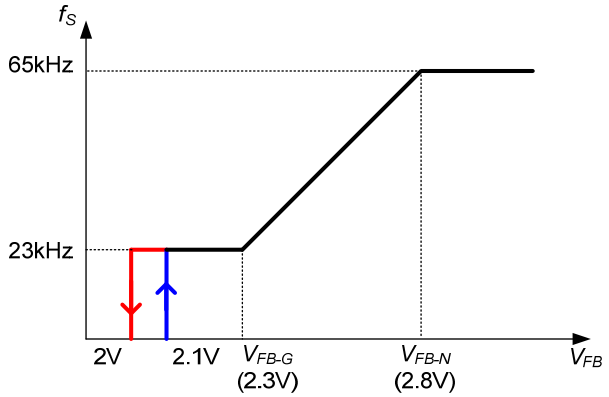

Figure 6. V_{FB} vs. PWM Switching Frequency

Design Example:

- $V_{LIMIT-H}$= 0.39V
- $V_{LIMIT-L}$= 0.46V
- R_{LS}= 1.6kΩ
- R_{HV}= 200kΩ
- V_{LINE}^{PK}= 127V
- P_O^{OPP}= 74.8W

R_{SENSE} is determined by

$$R_{SENSE} = \frac{V_{LIMIT}}{I_{DS-OPP}^{PK}} \quad (2)$$

As given in Equation 1, consider the input voltage is V_{LINE}^{MIN}:

$$V_{LIMIT} = \frac{0.39-0.46}{2}\cdot\frac{1.6\times10^3}{200\times10^3}\cdot127+\frac{3\cdot0.46-0.39}{2} = 0.46\,(\text{V})$$

In CCM,

$$I_{DS}^{PK} = \frac{P_{IN}\cdot(V_{IN}+V_{RO})}{V_{IN}\cdot V_{RO}} + \frac{V_{IN}\cdot V_{RO}}{2\cdot L_M\cdot f_S\cdot(V_{IN}+V_{RO})} \quad (3)$$

In DCM,

$$I_{DS}^{PK} = \sqrt{\frac{2\cdot P_{IN}}{f_S\cdot L_M}} \quad (4)$$

Whether the converter operates in CCM or DCM at minimum input voltage, nominal load condition is determined by:

CCM: $\sqrt{2\cdot P_{IN}\cdot L_M\cdot f_S}\cdot\frac{V_{IN}^{MIN}+V_{RO}}{V_{IN}^{MIN}\cdot V_{RO}} > 1$

DCM: $\sqrt{2\cdot P_{IN}\cdot L_M\cdot f_S}\cdot\frac{V_{IN}^{MIN}+V_{RO}}{V_{IN}^{MIN}\cdot V_{RO}} < 1$

It is recommended to design the power supply such that it operates in CCM when OPP occurs. Take:

$P_{IN} = \frac{P_O^{OPP}}{\eta}$ and $f_S = f_S^{MAX}$ into (3):

$$I_{DS-OPP}^{PK} = \frac{74.8}{0.85\cdot0.52\cdot88}+\frac{0.52\cdot88}{2\cdot513\times10^{-6}\cdot65\times10^3} = 2.61\,(\text{A})$$

$$R_{SENSE} = \frac{V_{LIMIT}}{I_{DS-OPP}^{PK}} = \frac{0.46}{2.61} = 0.176\,(\Omega)$$

Step 7 - Determine Number of Turns for the Minimum Primary-Side Winding (N_P^{MIN})

Define Parameter:

- The maximum flux density of L_M: B_{SAT}
- Effective cross-sectional area of L_M: A_e

Design Tips:

- A small number of turns reduces wire conduction loss; however, too small a number of turns can cause core saturation. Therefore, the number of turns should be determined by the trade-off between core saturation and conduction loss.

Design Example:

- B_{SAT}= 0.33 Tesla
- A_e = 98mm^2

Take $P_{IN} = \frac{P_O^{NOM}}{\eta}$ into (3),

$$I_{DS}^{PK} = 2.36\ \text{A}$$

$$N_P^{MIN} = \frac{L_M\cdot I_{DS}^{PK}}{B_{SAT}\cdot A_e}\times10^6 = \frac{513\times10^{-6}\cdot2.36}{0.33\cdot98}\times10^6 = 37.4\ (\text{Turns})$$

Since N_P should be an integer, it is selected as 38 turns.

Step 8 - Determine Number of Turns for the Secondary-side Winding (N_S) and Auxiliary Winding (N_A)

Define Parameter:

- The turn ratio of N_P to N_S: n
- Output diode forward-voltage drop: V_F
- Forward-voltage drop of V_{DD} rectifier diode: V_{FA}
- Nominal V_{DD} level: $V_{DD\text{-}OP}$

Design Tips:

- Select an integer for N_P and N_S such that N_P is larger than N_P^{MIN}.
- Allowable $V_{DD\text{-}OP}$ is 11-22V; typically set to 16V.

Design Example:

- V_F= 1V
- V_{FA}= 1V
- $V_{DD\text{-}OP}$= 16V

$$n = \frac{N_P}{N_S} = \frac{V_{RO}}{V_O + V_F} = \frac{95}{19+1} = 4.75$$

$$N_S = \frac{N_P}{n} = \frac{38}{4.75} = 8\ (\text{turns})$$

$$N_A = \frac{V_{DD-OP} + V_{FA}}{V_O + V_F} \cdot N_S = \frac{16+1}{19+1} \cdot 8 = 6.8\ (\text{turns})$$

Since N_A should be an integer, it is finally determined to be 7 turns. Then $V_{DD\text{-}OP}$ is changed to 16.5V, which is still within the operation voltage range.

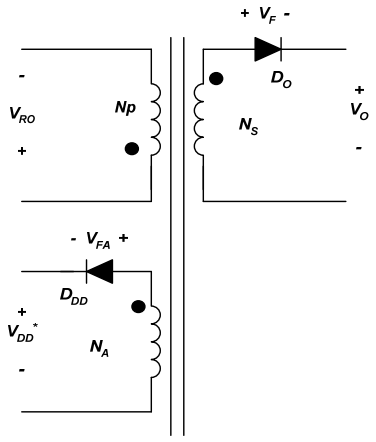

Figure 7. Simplified Transformer Diagram

Step 9 - Determine the Wire Diameter for Each Winding Based on the RMS Current

Define Parameter:

- Secondary-side RMS current: I_{SEC}^{RMS}

Design Tips:

- The current density is typically 6-10A/mm^2 when the wire is long (>1m).
- When the wire is short with a small number of turns, a current density of 8-14A/mm^2 is also acceptable.
- The whole layer should be filled with windings to get better coupling with small leakage inductance between primary and secondary sides.

Design Example:

$$I_{SEC}^{RMS} = n \cdot I_{DS}^{RMS} \cdot \sqrt{\frac{1-D_{MAX}}{D_{MAX}}}$$

$$= 4.75 \cdot 1.24 \cdot \sqrt{\frac{1-0.52}{0.52}} = 5.66\ (\text{A})$$

where D_{MAX} and I_{DS}^{RMS} are derived from Step 3 and Step 5, respectively.

As a result, 0.5mm (6.3A/mm^2) and 0.9mm (8.9A/mm^2) diameter wires are selected for primary and secondary windings, respectively.

Step 10 - Select Output Rectifier Diode

Define Parameter:

- The calculated maximum repetitive reverse voltage of output rectifier diode: V_{DO}.
- The specification for maximum repetitive reverse voltage of selected output diode: V_{RRM}.
- The specification for maximum rectified forward current of selected output diode: I_F.

Design Tips:

- When selecting the output diode, check the specification for V_{RRM} and I_F. V_{RRM} should be no less than 1.3 times V_{DO} and I_F should be no less than 1.5 times I_{SEC}^{RMS}.

Design Example:

$$V_{DO} = V_O + \frac{V_{IN}^{MAX}}{n} = 19 + \frac{373}{4.75} = 98\ (\text{V})$$

$$V_{RRM} > 1.3 \times V_{DO} = 127\ (\text{V})$$

$$I_F > 1.5 \times I_{SEC}^{RMS} = 8.5\ (\text{A})$$

As a result, a 150V-20A diode is selected.

Step 11 - Feedback Circuit Design

FAN6756 employs current-mode control, as shown in Figure 8. An opto-coupler (such as H11A817A) and a shunt regulator (such as KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the sensed current signal makes it possible to control the switching duty cycle. The feedback circuit design relates to the analysis of frequency response, which has been addressed in many of Fairchild's application notes. Since the entry/exit power level for Standby Mode operation depends on the feedback voltage, this section discusses how the loop response affects Standby Mode.

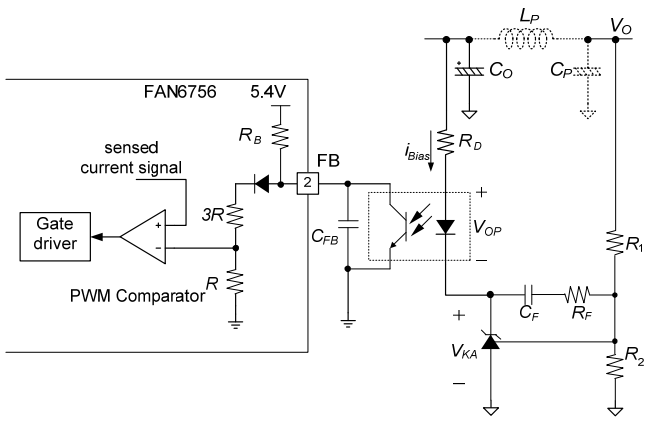

Figure 8. Feedback Compensation Network

At no-load or extremely light-load condition, FAN6756 enters Standby Mode to further reduce power consumption, which is initiated when the non-switching state of Burst Mode persists longer than 10ms for three consecutive burst switching operations, as Figure 9 shows. If FAN6756 does not enter Standby Mode; even at no load due to high burst frequency, increase C_{FB} or R_D to reduce the burst frequency by decreasing control bandwidth.

To prevent entering Standby Mode during dynamic load changes, there is a 900ms delay. During this period, if there are more than 104 consecutive switching pulses, FAN6756 does not enter Standby Mode.

If FAN6756 exits Standby Mode unexpectedly (for example, at no load) by V_{FB} exceeding 0.75V during the non-switching state of Burst Mode, try to increase the sourcing current of opto-coupler in the primary side. One way is to use opto-coupler with higher Current-Transfer Ratio (CTR). Another is to avoid using shunt-regulators with extra-low minimum cathode current for regulation. In addition, increase or remove the resistors connected from the output to the cathode of shunt-regulator.

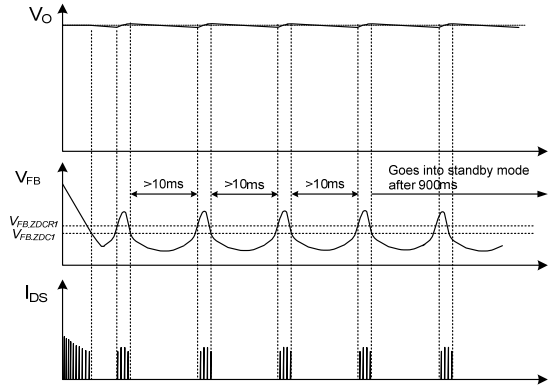

Figure 9. Timing Diagram for Entering Standby Mode

Step 12 - Design the Snubber

When the MOSFET turns off, a high-voltage spike occurs on the drain to source due to resonance between the transformer leakage inductor (L_{lk}) and MOSFET output capacitor (C_{OSS}). To protect the MOSFET from avalanche breakdown, a snubber circuit is necessary. The traditional RCD snubber circuit is shown in Figure 10. *For detailed snubber design and analysis, refer to AN-4147 — "Design Guidelines for RCD Snubber of Flyback Converters".*

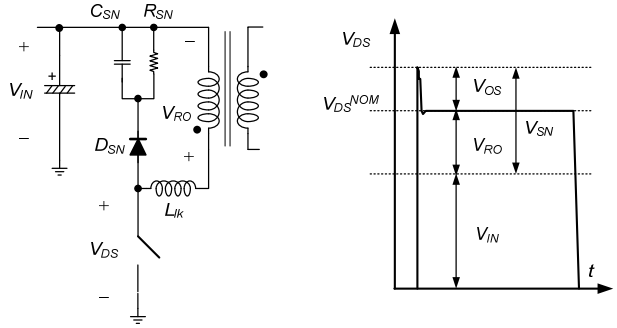

Figure 10. Typical RCD Snubber Circuit and V_{DS} Waveform

With an RCD snubber circuit, the energy stored in leakage inductor is absorbed and dissipated on R_{SN}. The power dissipation can be derived as:

$$P_{SN} = \frac{1}{2} \cdot f_S \cdot L_{lk} \cdot (I_{DS}^{PK})^2 \cdot \frac{V_{SN}}{V_{OS}} \quad (5)$$

To reduce the power loss, the effective way is to reduce the leakage inductance by proper transformer structure and shorten the layout trace in power loop. One tip for low standby power design is replacing R_{SN} and C_{SN} with a TVS, ZD_{SN}, as shown in Figure 11. For RCD snubber, the snubber voltage changes with the drain current. However, TVS keeps the snubber voltage constant regardless of the drain current. Thus, TVS has less power consumption than RCD snubber at light load condition.

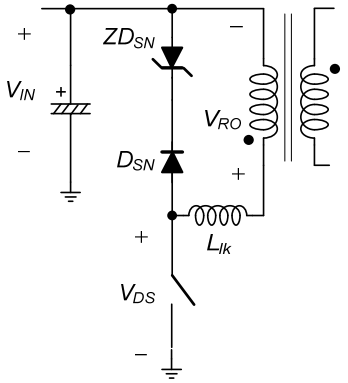

Figure 11.TVS Snubber Circuitry

Define Parameter:

- Breakdown voltage of ZD_{SN}: V_{BR}

Design Tips:

- For universal input Flyback power supply, a 650V MOSFET is generally used.
- The maximum of V_{DS} is generally under 80-85% of MOSFET rating.

Design Example:

$$V_{BR} = 0.8 \cdot 650 - V_{IN}^{MAX} = 520 - 373 = 147\ (V)$$

Therefore, a 150V or 200V TVS is selected.

Step 13 - Determine the HV Resistor (R_{HV}) and V_{DD} Hold-up Capacitor (C_{DD})

As shown in Figure 5, the HV pin functions include startup, brown-in/out, high/low line compensation, and AX-CAP™ discharge. When determining R_{HV}, the brown-in/out level and high/low line compensation should be considered.

Brown-in/out Consideration

The HV pin detects the AC line voltage using a switched voltage divider that consists of an external resistor (R_{HV}) and an internal resistor (R_{LS}). An internal peak detector identifies the peak value and holds it up in a DC level. Based on the detected voltage, the brown-in and brown-out threshold are determined as:

$$V_{BROWN-IN} = \frac{R_{HV}}{200 \times 10^3} \cdot \frac{V_{AC-ON}}{\sqrt{2}}\ (\text{RMS}) \quad (6)$$

$$V_{BROWN-OUT} = \frac{R_{HV}}{200 \times 10^3} \cdot \frac{V_{AC-OFF}}{\sqrt{2}}\ (\text{RMS}) \quad (7)$$

where V_{AC-ON} and V_{AC-OFF} are 110V and 100V, respectively. Typically, the brown-in level is set around $80V_{AC}$; therefore, R_{HV} is recommended to be 200kΩ. The brownout level then can be calculated by Equation 7, which results in $70V_{AC}$. The relationship between brown-in/out level and R_{HV} is shown in Figure 12.

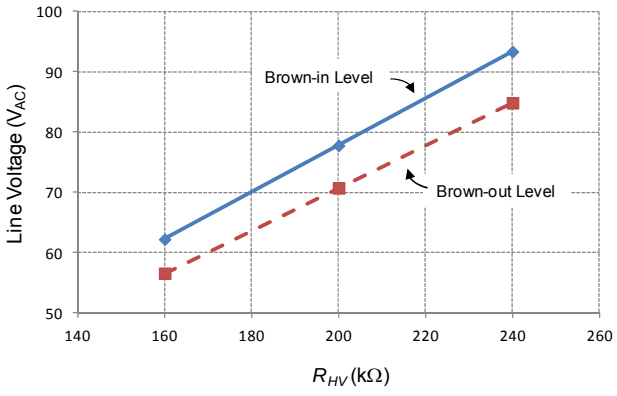

Figure 12. Brown-in/out Level with Different R_{HV}

Though the brown-in/out level can be adjusted by R_{HV}, R_{HV} is recommended to be from 150kΩ to 250kΩ to guarantee linear line compensation. Besides, smaller R_{HV} results in higher sampling loss, while larger R_{HV} resistance prolongs the startup time and the X-capacitor discharge time. Note that brownout function is disabled in Standby Mode.

High/ Low Line Compensation Consideration

Note that R_{HV} also affects the peak current limit level, V_{LIMIT}, as shown in Equation 1. Therefore, when determining R_{HV}, both brown-in/out and OPP level must be taken into consideration. R_{HV} shifts the V_{LIMIT} level as shown in Figure 13. Once the V_{LIMIT} level is determined, R_{SENSE} can be calculated by OPP level, as explained in Step 6.

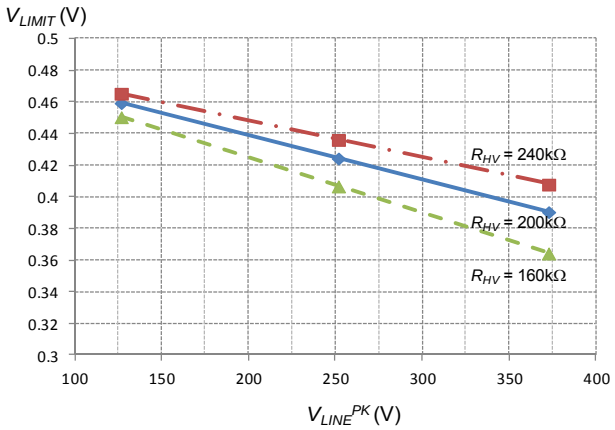

Figure 13. Current Limit vs. Line Voltage

Startup Consideration

As shown in Figure 14, when the AC line is applied to the power supply, the internal high-voltage current source charges the hold-up capacitor C_{DD} through a startup resistor R_{HV}. When V_{DD} voltage reaches turn-on threshold V_{DD-ON}, the PWM controller is enabled. Then the high-voltage current source is switched off and the supply current is drawn from the auxiliary winding of the main transformer.

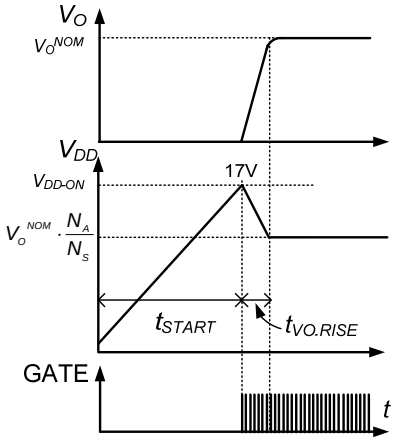

Figure 14. Typical Startup Waveform

Define Parameter:

- V_{DD} hold-up capacitor: C_{DD}.
- Delay time for HV charges C_{DD} to V_{DD-ON}: t_{START}.
- Output rising time: $t_{VO.RISE}$.

Design Tips:

- C_{DD} should be as large as possible to prevent V_{DD} from dropping below 6.5V during startup. As shown in Figure 15; if V_{DD} drops to 6.5V, FAN6756 enters UVLO shutting down the gate drive output.
- Larger C_{DD} also reduces the Burst Mode frequency in Standby Mode, since the burst frequency is controlled by V_{DD}, as shown in Figure 16. The benefit of low Burst Mode frequency is reduced switching loss in Standby Mode. However, the lower Burst Mode frequency is larger output ripple in Standby Mode.
- Typically, the startup time, estimated by t_{START}, is 2-3 seconds. C_{DD} should be properly selected to meet the startup time specification.

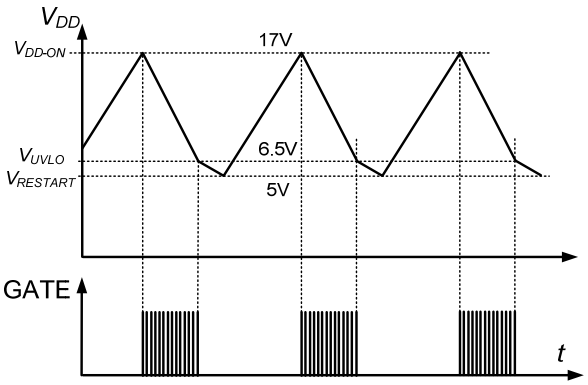

Figure 15. V_{DD} UVLO at Normal Mode

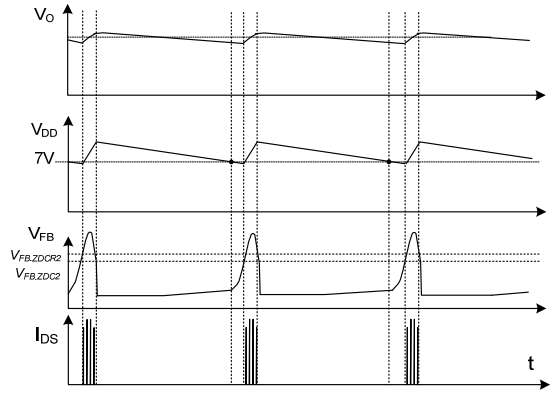

Figure 16. Deep Burst Operation in Standby Mode

Design Example:

$$C_{DD} < \left[\frac{R_{HV}}{t_{START}} \cdot \ln \frac{V_{ILINE}^{MIN} \cdot 2\sqrt{2}/\pi}{V_{LINE}^{MIN} \cdot 2\sqrt{2}/\pi - V_{DD-ON}} \right]^{-1}$$

$$= \left(\frac{200 \times 10^3}{3} \cdot \ln \frac{90 \cdot 2\sqrt{2}/\pi}{90 \cdot 2\sqrt{2}/\pi - 17} \right)^{-1} = 64 \times 10^{-6} \text{ (F)}$$

To have margin for startup time, C_{DD} is selected as 47 μF.

Estimate the X-Capacitor Discharge Time

FAN6756 detects the line voltage to determine when to activate AX-CAP™ discharge. Figure 17 shows the timing for discharging the X-capacitor. At light-load condition, to reduce the sampling loss; the HV sampler stops sampling for a period of time, t_{S-REST}. The maximum of t_{S-REST} is around 160ms. The maximum discharge time for the X-capacitor to be discharged to 37% of V_{LINE}^{PK} after being unplugged from power outlet, can be estimated as:

$$t_{DIS}^{TOTAL} = t_{S-REST}^{MAX} + t_{D-HV-DIS} + t_{VDD-DIS} + t_{XCAP-DIS} \quad (8)$$

where t_{S-REST}^{MAX} is maximum of t_{S-REST}; $t_{D-HV-DIS}$ is the debounce time for activating AX-CAP discharge, which is around 40ms; $t_{VDD-DIS}$ is the discharge time for C_{DD}; and $t_{XCAP-DIS}$ is the discharge time for the X-capacitor.

Since C_{DD} is discharged by internal 1mA current, the discharge time, $t_{VDD-DIS}$ can be estimated as:

$$t_{VDD-DIS} = \frac{C_{DD} \cdot (\frac{N_A}{N_S} \cdot V_O - V_{DD-OFF})}{1 \times 10^{-3}} \quad (9)$$

where V_{DD-OFF} is around 11V. When V_{DD} drops to V_{DD-OFF}, HV starts to charge C_{DD}. Since the power supply is unplugged, the residual energy of X-capacitor is discharged. The discharge time $t_{XCAP-DIS}$ can be estimated as:

$$t_{XCAP-DIS} \approx -R_{HV} \cdot C_X \cdot \ln(\frac{V_{IN} \times 37\%}{V_{IN} - V_{DD\_OFF}}) \quad (10)$$

By taking the parameters into Equations 9 and 10, to calculate $t_{VDD-DIS}$ and $t_{XCAP-DIS}$:

$$t_{VDD-DIS} = \frac{47 \times 10^{-6} \cdot (\frac{7}{8} \cdot 19 - 11)}{1 \times 10^{-3}} = 264 \times 10^{-3} \text{ (Sec.)}$$

$$t_{XCAP-DIS} \approx -200 \times 10^3 \cdot 0.33 \times 10^{-6} \cdot \ln(\frac{373 \times 37\%}{373 - 11})$$

$$= 64 \times 10^{-3} \text{ (Sec.)}$$

Therefore, t_{DIS}^{TOTAL} can be calculated as 528ms, considering the maximum input voltage and maximum t_{S-REST}. To have margin for discharging, the X-capacitor is recommended to be no more than 0.5μF.

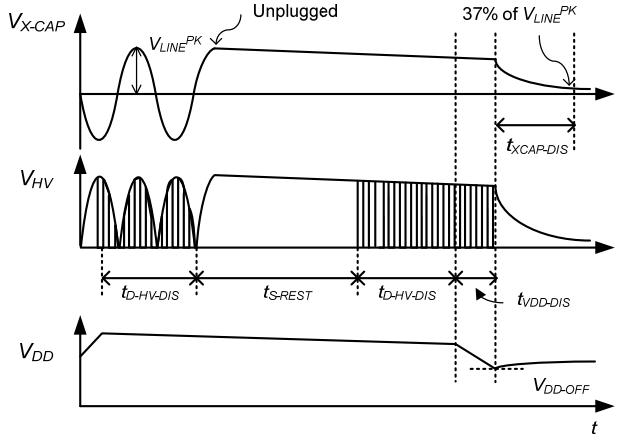

Figure 17. Timing Diagram for AX-CAP™ Discharge

Step 14 - Other Components

RT Pin Series Resistors (R_A and R_{NTC}) for Over-Temperature Protection (OTP)

The RT pin provides adjustable over-temperature protection (OTP) and an external latch-triggering function. For OTP application, an NTC thermistor, R_{NTC}, usually in series with a resistor R_A, is connected between the RT pin and ground, as shown in Figure 18. The internal current source, I_{RT} (100μA) introduces voltage drop across RT, calculated as:

$$V_{RT} = I_{RT} \cdot (R_{NTC} + R_A) \quad (11)$$

where V_{RT} is internally clamped at 5V. At high ambient temperature, R_{NTC} decreases, reducing V_{RT}. When V_{RT} is lower than V_{RTTH1} (1.035V) longer than t_{D-OTP1} (14.5ms), the OTP is triggered and FAN6756 enters Latch Mode protection. Note that OTP is disabled in Standby Mode.

The latch protection can be also trigged by pulling down the RT pin voltage using an opto-coupler or transistor. Once V_{RT} is less than V_{RTTH2} (0.7V) for longer than t_{D-OTP2} (185μs), the protection is triggered and FAN6756 enters Latch Mode.

When OTP is not used, a 100kΩ resistor is recommended between this pin and ground to prevent noise interference. If a filter capacitor C_{RT} is connected in parallel with the RT pin resistors; note that the rising time to 0.7V should not be larger than 185μs. Otherwise, the latch protection would be triggered before a successful startup.

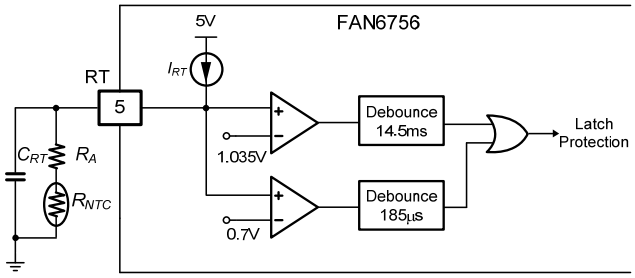

Figure 18. Thermal Protection Circuit

Design Example:

According to the 100kΩ NTC thermistor datasheet, the resistance at 100°C is around 4.3kΩ, by Equation 11:

$$R_A = \frac{V_{RT}}{I_{RT}} - R_{NTC} = \frac{1.035}{100 \times 10^{-6}} - 4.3 \times 10^3 = 6.1 \times 10^3 \ (\Omega)$$

The maximum value of C_{RT} can be evaluated by:

$$V_{RT}(t)\big|_{t=185\mu} = 5 \cdot (1 - e^{-\frac{185\mu}{C_{RT} \cdot 100k}}) > 0.7 .$$

Therefore,

$$C_{RT} < 12 \times 10^{-9} \ (F)$$

For filtering noise, C_{RT} is selected as 1nF.

RC Filter of SENSE Pin

Although the internal blanking circuit blanks the turn-on spike for t_{LEB} (280ns) when MOSFET switches on, as Figure 19 shows; a low-pass filter formed by R_{LPF} and C_{LPF} is recommended for noise filtering. The selection guide is to filter the turn-on and turn-off noise without distorting the current-sense waveform. R_{LPF} and C_{LPF} are selected as 100Ω and 470pF, respectively.

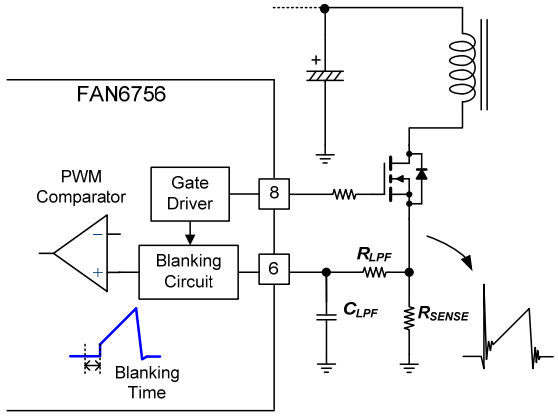

Figure 19. Current-Sensing Circuit and Waveform

Trouble Shooting

Prevent Error Triggering of Sense Pin Short-Circuit Protection (SSCP)

FAN6756 provides safety protection for Limited Power Source (LPS) test. To protect the power supply against a short circuit across the current-sense resistor, FAN6756 shuts down when current-sense voltage is very low — even with a relatively large duty cycle. As shown in Figure 20, the current-sense voltage is sampled at $t_{ON-SSCP}$ (4.55μs) after the gate turn-on. If the sampled voltage (V_{S-CS}) is lower than V_{SSCP} for 11 consecutive switching cycles (170μs), the FAN6756 shuts down immediately. V_{SSCP} varies linearly with line voltage. If V_{LINE}^{PK} is 122V, V_{SSCP} is typically 50mV (V_{SSCP-L}), while V_{LINE}^{PK} is 366V, V_{SSCP} is typically 100mV (V_{SSCP-H}).

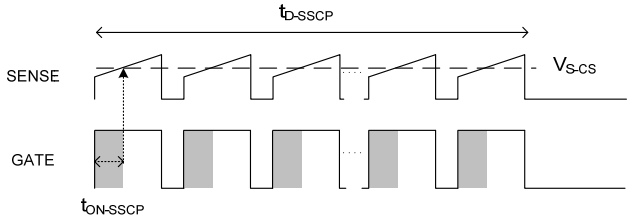

Figure 20. SSCP Detection Waveform

To prevent error triggering of SSCP, the SENSE pin voltage, V_{SENSE}, must not be lower than V_{S-CS} at $t_{ON-SSCP}$ except for SENSE pin short condition. Considering the minimum input voltage condition, the SENSE pin voltage when $t_{ON-SSCP}$ is derived as:

$$V_{SENSE}\big|_{t_{ON}=t_{ON-SSCP}} = I_{DS}^{PK} \cdot R_{CS} > V_{S-CS} \quad (12)$$

where $t_{ON\text{-}SSCP}$ is the minimum value for low-line condition, which is 4μs; I_{DS}^{PK} is derived from Equations 3 and 4 when the system operates in CCM and DCM, respectively; $V_{S\text{-}CS}$ is the maximum SSCP level for low-line condition, which is 70mV as defined in the datasheet. Assuming that the system operates in DCM, examine:

$$V_{SENSE} = \frac{88 \cdot 4 \times 10^{-6} \cdot 0.176}{513 \times 10^{-6}} = 120 \times 10^{-3} > 70 \times 10^{-3}$$

Users must take a close look of low input voltage conditions such as startup, power-off, brown-in/out, or AC cycle-drop test. If V_{SENSE} is lower than $V_{S\text{-}CS}$, then:

- Increase the input capacitor since larger input capacitance reduces DC bus voltage ripple and therefore, increases V_{IN}^{MIN}.
- Reduce primary inductance. However, it may be less effective since R_{SENSE} would also be decreased for OPP consideration.

Evaluate OPP Deviation for High/Low Line

Assuming that system operates in CCM under OPP condition, the output current can be evaluated by:

$$I_O^{OPP} = \frac{\eta}{V_O} \cdot \left(\frac{V_{LIMIT} \cdot V_{IN} \cdot D}{R_{SENSE}} - \frac{V_{IN}^2 \cdot D^2}{2 \cdot L_M \cdot f_S}\right) \quad (13)$$

where V_{LIMIT} is given by Equation 1 and D is the PWM duty cycle:

$$D = \frac{V_{RO}}{V_{IN} + V_{RO}} \quad (14)$$

By plotting OPP percentage versus line voltage with Equation 13, as shown in Figure 21; the power level for OPP then can be examined.

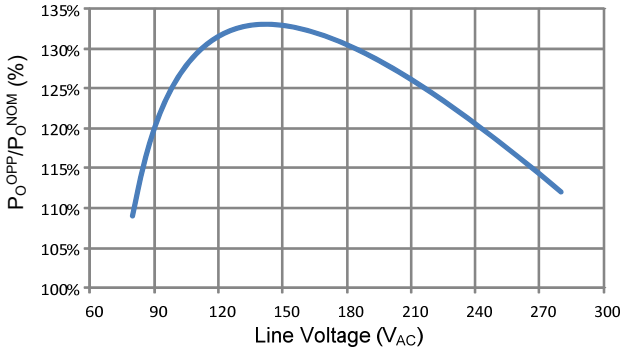

Figure 21. OPP Percentage vs. Line Voltage

3. Final Schematic of Design Example

This section summarizes the final design of design example. The key system specification is summarized in Table 1 and the key design parameters are summarized in Table 2. The final schematic is shown in Figure 22.

Table 1. System Specification

Input	
Input Voltage Range	90-264V_{AC}
Line Frequency Range	47-63Hz
Output	
Output Voltage (V_o)	19V
Output Power (P_o^{NOM})	65W

Table 2. Key Design Parameters for Transformer

Number of Turns for Primary-Side Winding (N_P)	38
Number of Turns for Secondary-Side Winding (N_S)	8
Number of Turns for Auxiliary Winding (N_A)	7
Primary Inductor (L_M)	513μH
Switching Frequency (f_S)	65kHz

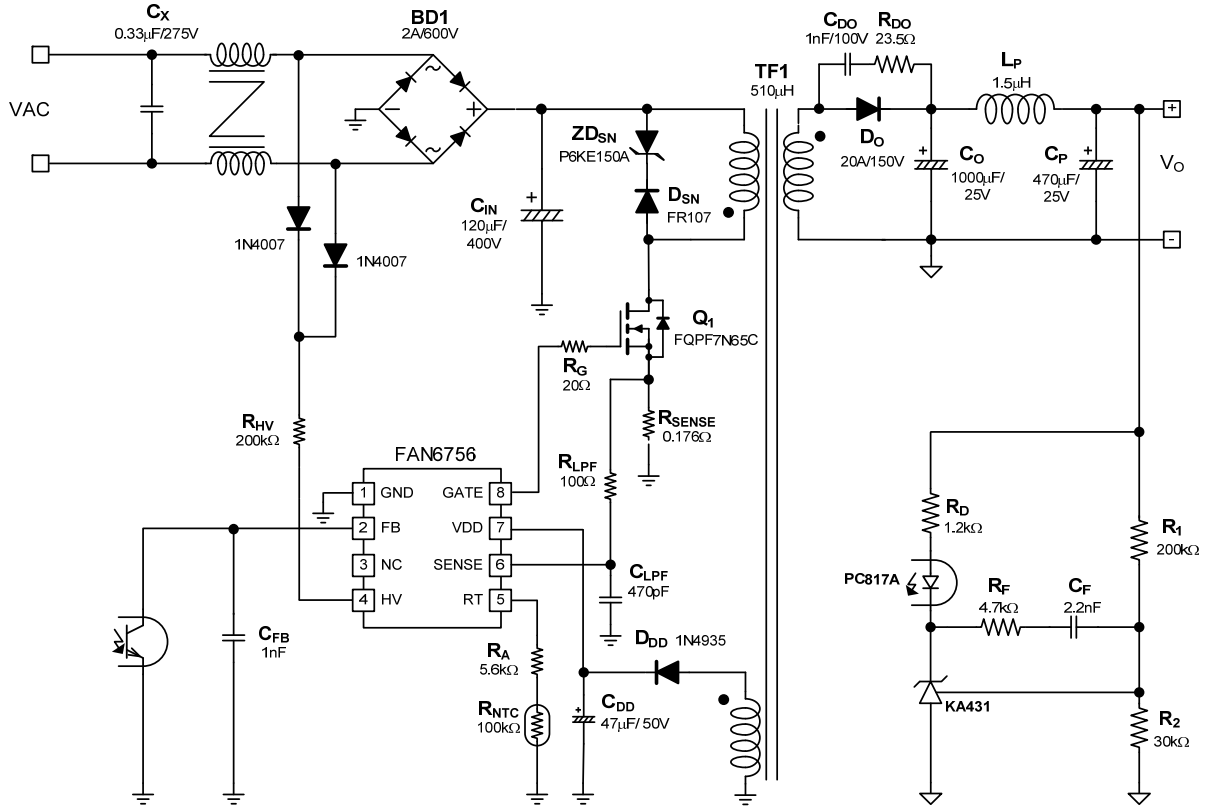

Figure 22. Final Schematic of Design Example

Lab Note

Before rework or solder/de-solder on the power supply, discharge the bulk capacitors in the primary side by an external resistor. Otherwise, the PWM IC may be damaged by external high voltage during soldering/de-soldering.

This device is sensitive to ESD discharge. To improve production yield, the production line should be ESD protected according to ANSI ESD S1.1, ESD S1.4, ESD S7.1, ESD STM 12.1, and EOS/ESD S6.1.

4. Printed Circuit Board (PCB) Layout

PCB layout is a critical design issue for SMPS where current or voltage changes with high dv/dt or di/dt. Good PCB layout minimizes excessive EMI and helps the power supply survive during surge or ESD tests. Figure 23 shows the grounding method for PCB layout.

Guidelines:

- To get better EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to capacitor C_{IN} directly, then to the switching circuits.
- The high-frequency power loop is **C_{IN} – TF1 – Q_1 – R_{SENSE} – C_{IN}**. The area enclosed by this current loop should be as small as possible. Keep the traces (especially GND4→1) short, direct, and wide. High-voltage traces related to the drain of Q_1 and snubber should be kept far from control circuits to prevent unnecessary interference. If a heat-sink is used for Q_1, connect its heat-sink to ground for better EMI.
- As indicated by GND3, the ground of control circuits should be connected together first, then to other circuitry.
- As indicated by GND2, the area enclosed by transformer auxiliary winding, D_{DD} and C_{DD} should also be kept small.
- Place C_{LPF} close to the FAN6756 for good decoupling.
- Control circuits should not be placed on the ESD discharge path.
- A Y-capacitor between primary side and secondary side is required. If the Y-capacitor is connected to the primary ground (GND5), connect the capacitor directly to the negative terminal of BD_1 or C_{IN} (GND1).
- Point discharge for common choke and Y-capacitor can decrease high-frequency impedance and increase ESD immunity. However, the creepage between these pointed ends should be large enough to meet the requirements of applicable standards.

Two suggestions with different pros and cons for ground connections are offered:

- Star-grounding (GND3→1, 4→1, and 2→1) or GND3→2→4→1. This could avoid common impedance interference for sense signal.
- GND3→2→1 and GND4→1: This could be better for ESD testing where the earth ground is not available for the power supply. Regarding the ESD discharge path, the charges from secondary through the transformer stray capacitance to GND2 first. The charges then go from GND2 to GND1 and back to the mains.

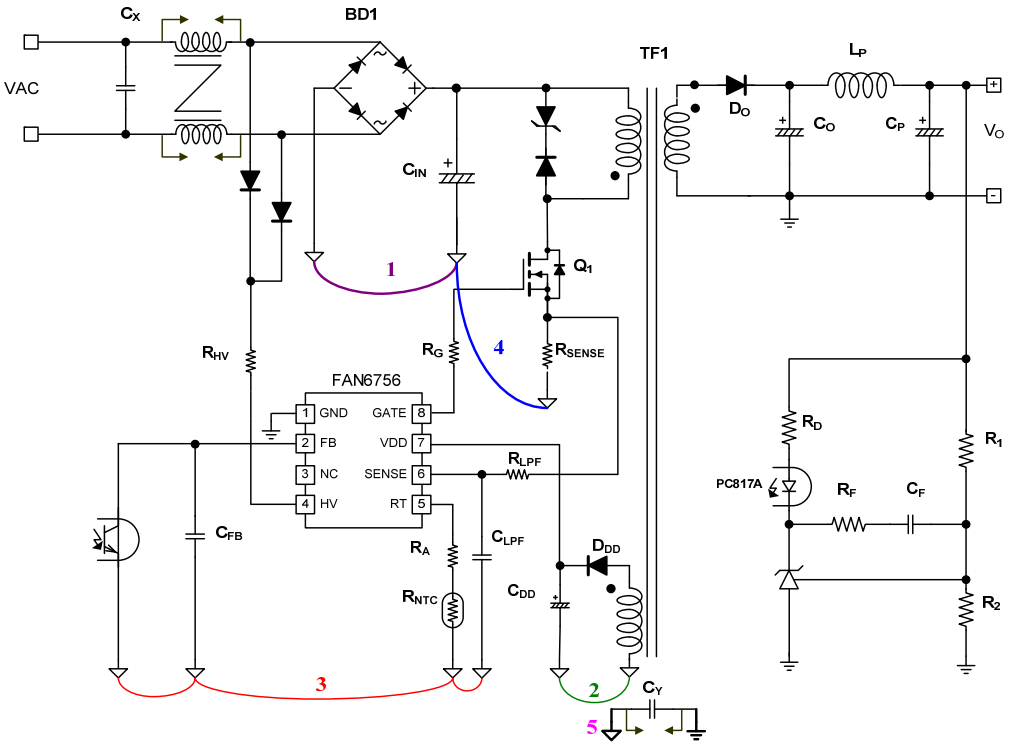

Figure 23. Grounding PCB Layout Diagram

5. Related Datasheets

FAN6756 — mWSaver™ PWM Controller