AN-5005

Fairchild Semiconductor
Application Note
March 1999
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FAIRCHILD SEMICONDUCTOR™

PC100 Memory Driver Competitive Comparisons

Introduction

The latest developments in chipset and motherboard design have taken memory performance requirements to new levels. The memory bus speed has been increased from 66MHz to 100MHz to keep pace with the needs of advanced operating systems and software. Feeding today's PC/workstation/server often requires large banks of dense SDRAM (Synchronous DRAM) ICs arranged on DIMMs (Dual in-line memory modules). Due to the inability of the system memory controller to drive the large amount of memory devices and maintain signal integrity or system timing requirements, many of today's DIMMs require buffering of the address and control signal paths. Intel has published a specification for 100MHz SDRAM memory modules called PC100. Proper selection of the logic devices to register and redrive heavily loaded address and control signal paths requires careful consideration of device parameters and can result in a SDRAM DIMM design that uses the fewest components and provides reliable circuit performance (Note 1). This application note compares Fairchild Semiconductor's logic solutions for buffered (or registered) DIMMs to other competitive solutions.

Note 1: See Fairchild Semiconductor AN-5003 PC100 SDRAM Memory Driver Solutions

Overview

Fairchild Semiconductor's *CROSSVOLT*™ VCX family offers a variety of logic solutions that meet or exceed the PC100 specification.

Device #	Function
74VCX16835	18 Bit Universal Buffer
74VCX162835	18 Bit Universal Buffer w/ 25 Ω Resistor
74VCX16838	16 Bit Selectable Register Buffer
74VCX162838	16 Bit Selectable Register Buffer w/ 25 Ω Resistor
74VCX16839	20 Bit Selectable Register Buffer
74VCX162839	20 Bit Selectable Register Buffer w/ 25 Ω Resistor

The information in this application note provides functional and specification comparisons to several ALVC devices that are also used in DIMM applications. There are several device number differences between the two families. The table below provides a cross reference between VCX and ALVC.

VCX and ALVC Cross Reference Table

Fairchild Device #	ALVC Device #	Function
74VCX16835	74ALVC16835	18 Bit Universal Buffer
74VCX162835	74ALVC162835	18 Bit Universal Buffer w/ 25 Ω Resistor
74VCX16838	74ALVC16334	16 Bit Selectable Register Buffer
74VCX162838	74ALVC162334	16 Bit Selectable Register Buffer w/ 25 Ω Resistor
74VCX16839	74ALVC16836	20 Bit Selectable Register Buffer
74VCX162839	74ALVC162836	20 Bit Selectable Register Buffer w/ 25 Ω Resistor

Comparison of 74VCX16835 vs. 74ALVC16835

Part Descriptions

74VCX16835	18 Bit Universal Buffer with 3-STATE Outputs
74ALVC16835	18 Bit Universal Buffer with 3-STATE Outputs

Functional Comparison

The 74VCX16835 and 74ALVC16835 are pin and functionally equivalent.

Function Table

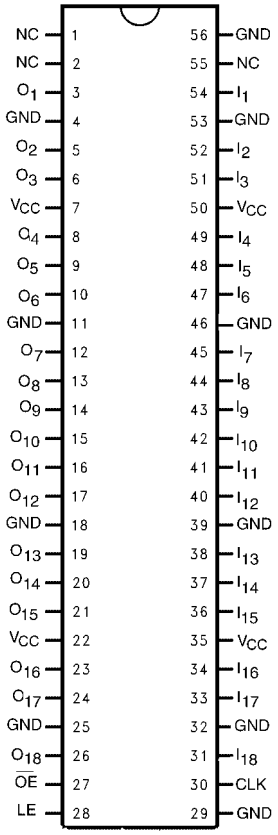
Inputs				Outputs
$\overline{OE}$	LE	CLK	I_n	O_n
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	H	X	I_0 (Note 2)
L	L	L	X	I_0 (Note 3)

H = Logic HIGH
L = Logic LOW
X = Don't Care, but not floating
Z = High Impedance
↑ = LOW-to-HIGH Transition

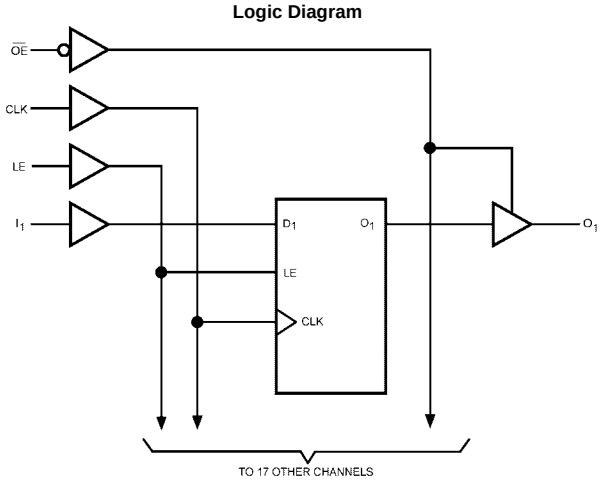
Note 2: Output level before the indicated steady-state input conditions were established provided that CLK was HIGH before LE went LOW.

Note 3: Output level before the indicated steady-state input conditions were established.

Connection Diagram



Logic Diagram



Comparison of 74VCX16835 vs. 74ALVC16835 (Continued)

AC Comparison

The following table shows a comparison of the 74VCX16835 device and the equivalent ALVC device. The table also compares performance vs. the Intel PC100 Rev 1.2 Registered DIMM specification.

AC Specifications Table

Parameter	Symbol	PC100 (1.2)		74VCX16835		74ALVC16835		Units	Test Conditions
		Min	Max	Min	Max	Min	Max		
CLK Input Capacitance	C_{IN}	3.30	6.00	3.5 (Typ)		3.5 (Typ)		pF	10 MHz
Maximum Clock Frequency	f_{MAX}	150		250		150		MHz	
Output Edge Rate	$t_{THL/LH}$	1.00	2.50					V/ns	C_L = 50pF V_{CC} = 3.3V +/- 0.15V Between 1.2V –1.8V
Propagation Delay – Register	$t_{PHL/LH}$ CLK to Y	1.7	4.5	1.7	4.5	1.7	4.5	ns	C_L = 50pF V_{CC} = 3.3V +/- 0.15V CLK to any Y
Propagation Delay – Register	$t_{PHL/LH}$ CLK to Y	1.5	3.0	1.5	3.0	1.5	2.9	ns	C_L = 0pF V_{CC} = 3.3V +/- 0.15V CLK to any Y
Propagation Delay – Buffer	$t_{PHL/LH}$ A to Y	1.0	4.5	1.0	3.6	1.0	4.0	ns	C_L = 50pF V_{CC} = 3.3V +/- 0.15V A to any Y
Propagation Delay – Buffer	$t_{PHL/LH}$ A to Y	0.9	2.0	0.7	2.1	0.9	2.0	ns	C_L = 0pF V_{CC} = 3.3V +/- 0.15V A to any Y
Maximum Allowable SSO Delay			300					ps	C_L = 50pF, Any output combination, V_{CC} = 3.3V +/- 0.15V
Setup Time	t_{SET}	1.7		1.5		1.7		ns	V_{CC} = 3.3V +/- 0.15V Any input
Hold Time	t_{HOLD}	0.7		0.7		0.7		ns	V_{CC} = 3.3V +/- 0.15V Any input
Input Current	I_{IN}		10.0		5.0		5.0	uA	V_{IN} = 0V to 3.45V V_{CC} = 3.3V +/- 0.15V

Note: AC Specifications Table for the VCX and ALVC products above are for $V_{CC} = \pm 10\%$, and $T_A = -40$ to $85^{\circ}C$

Comparison of 74VCX162835 vs. 74ALVC162835

Part Descriptions

74VCX162835	18 Bit Universal Buffer with 3-STATE Outputs and 25 Ω Resistors
74ALVC162835	18 Bit Universal Buffer with 3-STATE Outputs and 25 Ω Resistors

Functional Comparison

The 74VCX162835 and 74ALVC162835 are pin and functionally equivalent.

Function Table

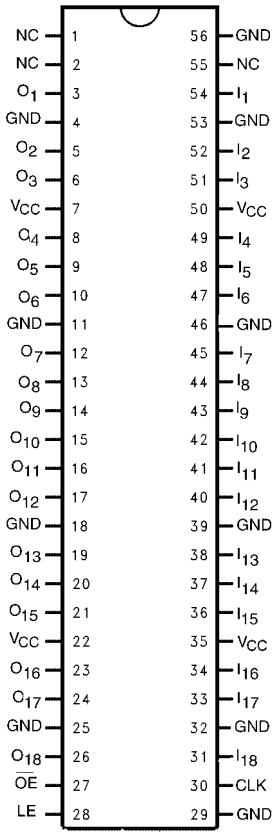
Inputs				Outputs
$\overline{OE}$	LE	CLK	I_n	O_n
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	H	X	I_o (Note 4)
L	L	L	X	I_o (Note 5)

H = Logic HIGH
L = Logic LOW
X = Don't Care, but not floating
Z = High Impedance
↑ = LOW-to-HIGH Transition

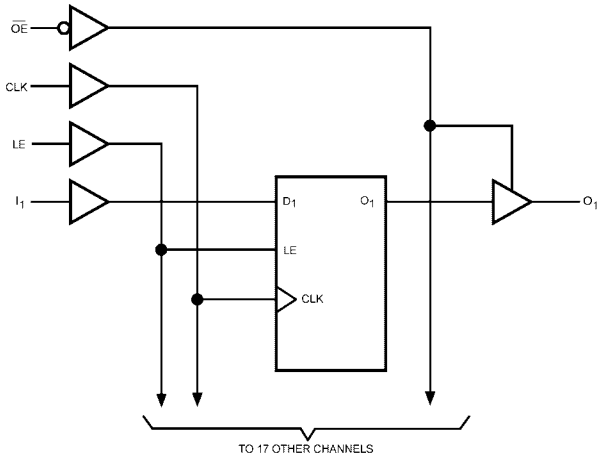
Note 4: Output level before the indicated steady-state input conditions were established provided that CLK was HIGH before LE went LOW.

Note 5: Output level before the indicated steady-state input conditions were established.

Connection Diagram



Logic Diagram



Comparison of 74VCX162835 vs. 74ALVC162835 (Continued)

AC Comparison

The following table shows a comparison of the 74VCX162835 device and the equivalent ALVC device. The table also compares performance vs. the Intel PC100 Rev 1.2 Registered DIMM specification.

AC Specifications Table

Parameter	Symbol	PC100 (1.2)		74VCX162835		74ALVC162835		Units	Test Conditions
		Min	Max	Min	Max	Min	Max		
CLK Input Capacitance	C_{IN}	3.30	6.00	3.5 (Typ)		3.5 (Typ)		pF	10 MHz
Maximum Clock Frequency	f_{MAX}	150		250		150		MHz	
Output Edge Rate	$t_{THL/LH}$	1.00	2.50					V/ns	C_L = 50pF V_{CC} = 3.3V +/- 0.15V Between 1.2V –1.8V
Propagation Delay – Register	$t_{PHL/LH}$ CLK to Y	1.9	4.5	1.9	4.5	1.9	5.0	ns	C_L = 50pF V_{CC} = 3.3V +/- 0.15V CLK to any Y
Propagation Delay – Register	$t_{PHL/LH}$ CLK to Y	1.4	2.9	1.4	2.9	1.4	2.9	ns	C_L = 0pF V_{CC} = 3.3V +/- 0.15V CLK to any Y
Propagation Delay – Buffer	$t_{PHL/LH}$ A to Y	1.0	4.5	1.0	4.2	1.0	4.0	ns	C_L = 50pF V_{CC} = 3.3V +/- 0.15V A to any Y
Propagation Delay – Buffer	$t_{PHL/LH}$ A to Y	0.9	2.0	0.7	2.6	0.9	2.0	ns	C_L = 0pF V_{CC} = 3.3V +/- 0.15V A to any Y
Maximum Allowable SSO Delay			300					ps	C_L = 50pF, Any output combination, V_{CC} = 3.3V +/- 0.15V
Setup Time	t_{SET}	1.7		1.5		1.7		ns	V_{CC} = 3.3V +/- 0.15V Any input
Hold Time	t_{HOLD}	0.7		0.7		0.7		ns	V_{CC} = 3.3V +/- 0.15V Any input
Input Current	I_{IN}	1.9	4.5	1.9	4.5	1.9	5.0	uA	V_{IN} = 0V to 3.45V V_{CC} = 3.3V +/- 0.15V

Note: AC Specifications Table for the VCX and ALVC products above are for $V_{CC} = \pm 10\%$, and $T_A = -40$ to $85^{\circ}C$

Comparison of 74VCX16838 vs. 74ALVC16334

Part Descriptions

74VCX16838	16 Bit Selectable Register Buffer with 3-STATE Outputs
74ALVC16334	16 Bit Universal Bus Driver with 3-STATE Outputs

Functional Comparison

The 74VCX16838 and 74ALVC16334 are pin and functionally equivalent for registered DIMM applications.

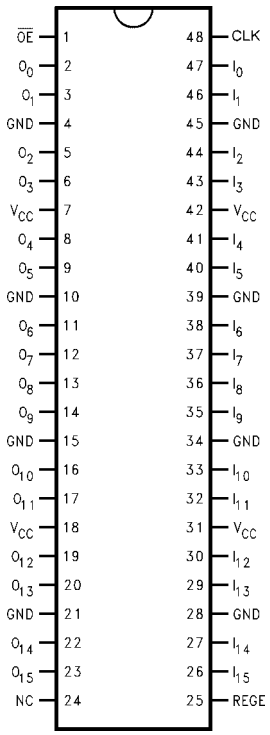
This means that one will see no functional difference when used in a registered DIMM application. There is however differences in the actual function of the devices. The 74VCX16838 was designed specifically for the Intel PC100 Rev 1.2 Registered DIMM specification and supports two modes of operation: a registered mode and a flow through mode. The 74ALVC16334 has additional functionality not required by the Intel PC100 Rev 1.2 Registered DIMM specification. While these devices support registered mode and flow through mode they have an additional latch mode.

Function Table for 74VCX16838

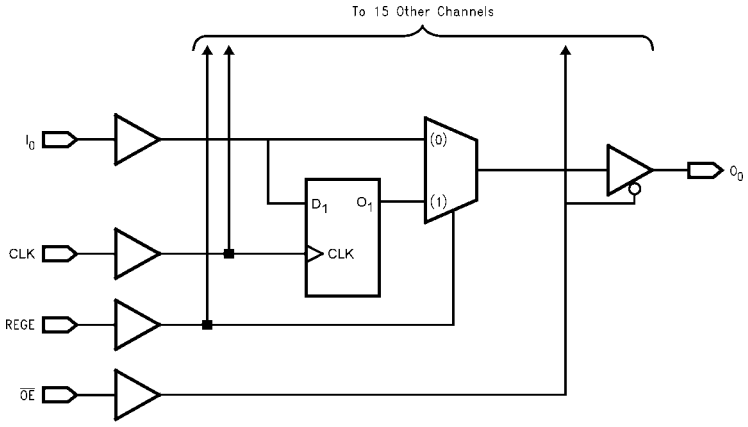
Inputs				Outputs
CLK	**REGE**	I_n	$\overline{OE}$	O_n
↑	H	H	L	H
↑	H	L	L	L
X	L	H	L	H
X	L	L	L	L
X	X	X	H	Z

H = Logic HIGH
L = Logic LOW
X = Don't Care, but not floating
Z = High Impedance
↑ = LOW-to-HIGH Transition

Connection Diagram for 74VCX16838



Logic Diagram for 74VCX16838



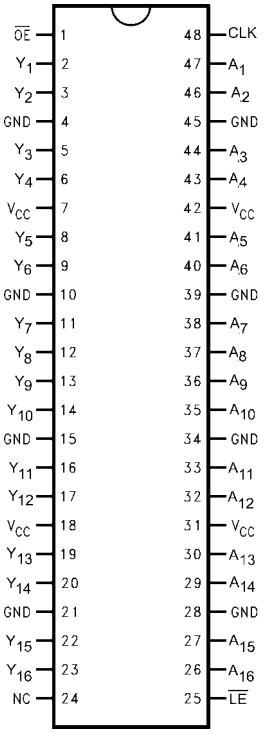
Comparison of 74VCX16838 vs. 74ALVC16334 (Continued)

Function Table for 74ALVC16334

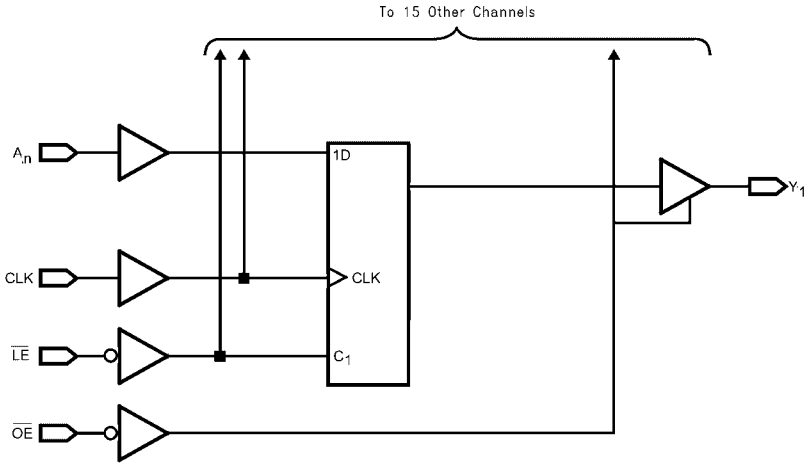
Inputs				Outputs
$\overline{OE}$	$\overline{LE}$	CLK	A_n	Y_n
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	L or H	X	Y_0(Note 6)

Note 6: Output level before the indicated steady-state input conditions were established.

Connection Diagram for 74ALVC16334



Logic Diagram for 74ALVC16334



Comparison of 74VCX16838 vs. 74ALVC16334 (Continued)

When the devices are in registered or flow through mode they will behave as functional equivalents. The waveforms shown in Figure 1 show how the devices respond in flow through and registered modes.

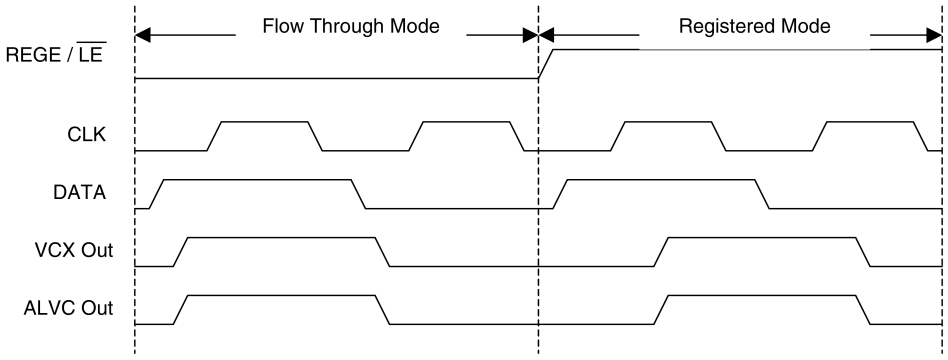


FIGURE 1. Flow Through Mode Waveforms

The actual functional differences can only be seen by transitioning the REGE($\overline{LE}$) pin when the data latched into the internal register is different from the data on the input port. The waveforms to generate this condition are shown in Figure 2. The 74VCX16838 is implemented such that the REGE pin selects between the flow through mode and the registered modes. The 74ALVC16334 is implemented such that the $\overline{LE}$ pin will force the internal latches enabled and pass data through these latches in flow-through mode.

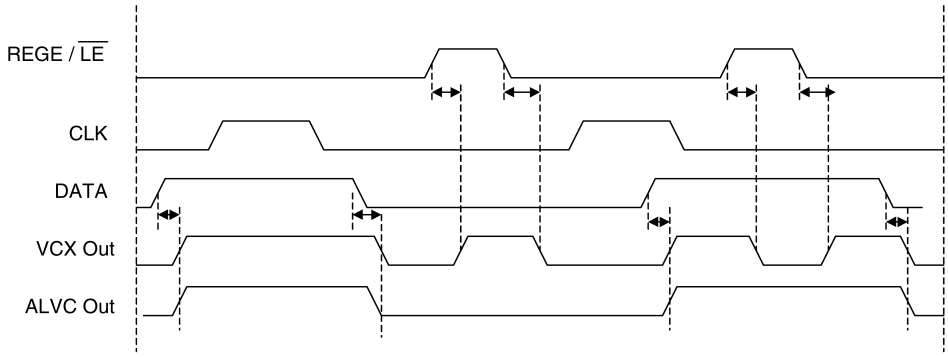


FIGURE 2. Transitioning Waveforms

The functional differences shown do not impact registered DIMM Module application because the REGE pin is typically fixed in one state or the other for a given application. The implementation chosen for the 74VCX16838 was done to provide improved AC performance in flow-through mode.

Comparison of 74VCX16838 vs. 74ALVC16334 (Continued)

AC Comparison

The following table shows a comparison of the 74VCX16838 device and the equivalent ALVC device. The table also compares performance vs. the Intel PC100 Rev 1.2 Registered DIMM specification.

AC Specifications Table

Parameter	Symbol	PC100 (1.2)		74VCX16838		74ALVC16334		Units	Test Conditions
		Min	Max	Min	Max	Min	Max		
CLK Input Capacitance	C_{IN}	3.30	6.00	3.5 (Typ)		3.5 (Typ)		pF	10 MHz
Maximum Clock Frequency	f_{MAX}	150		250		150		MHz	
Output Edge Rate	$t_{THL/LH}$	1.00	2.50					V/ns	C_L = 50pF V_{CC} = 3.3V +/- 0.15V Between 1.2V –1.8V
Propagation Delay – Register	$t_{PHL/LH}$ CLK to Y	1.7	4.5	1.1	3.3	1.0	4.1	ns	C_L = 50pF V_{CC} = 3.3V +/- 0.15V CLK to any Y
Propagation Delay – Register	$t_{PHL/LH}$ CLK to Y	1.5	3.0					ns	C_L = 0pF V_{CC} = 3.3V +/- 0.15V CLK to any Y
Propagation Delay – Buffer	$t_{PHL/LH}$ A to Y	1.0	4.5	1.1	2.8	1.1	3.3	ns	C_L = 50pF V_{CC} = 3.3V +/- 0.15V A to any Y
Propagation Delay – Buffer	$t_{PHL/LH}$ A to Y	0.9	2.0					ns	C_L = 0pF V_{CC} = 3.3V +/- 0.15V A to any Y
Maximum Allowable SSO Delay			300					ps	C_L = 50pF, Any output combination, V_{CC} = 3.3V +/- 0.15V
Setup Time	t_{SET}	1.7		1.5		1.5		ns	V_{CC} = 3.3V +/- 0.15V Any input
Hold Time	t_{HOLD}	0.7		1.0		0.9		ns	V_{CC} = 3.3V +/- 0.15V Any input
Input Current	I_{IN}		10.0		5.0		5.0	uA	V_{IN} = 0V to 3.45V V_{CC} = 3.3V +/- 0.15V

Note: AC Specifications Table for the VCX and ALVC products above are for $V_{CC} = \pm 10\%$, and $T_A = -40$ to $85^{\circ}C$

Comparison of 74VCX162838 vs. 74ALVC162334

Part Descriptions

74VCX162838	16 Bit Selectable Register Buffer with 3-STATE Outputs and 25Ω Resistors
74ALVC162334	16 Bit Universal Bus Driver with 3-STATE Outputs and 25Ω Resistors

Functional Comparison

The 74VCX162838 and 74ALVC162334 are pin and functionally equivalent for registered DIMM applications.

This means that one will see no functional difference when used in a registered DIMM application. There is however differences in the actual function of the devices. The 74VCX162838 was designed specifically for the Intel PC100 Rev 1.2 Registered DIMM specification and supports two modes of operation: a registered mode and a flow through mode. The 74ALVC162334 has additional functionality not required by the Intel PC100 Rev 1.2 Registered DIMM specification. While these devices support registered mode and flow through mode they have an additional latch mode.

When the devices are in registered or flow through mode they will behave as functional equivalents. The waveforms shown in Figure 1 show how the devices respond in flow through and registered modes.

The actual functional differences can only be seen by transitioning the REGE($\overline{LE}$) pin when the data latched into the internal register is different from the data on the input port. The waveforms to generate this condition are shown in Figure 2. The 74VCX162838 is implemented such that the REGE pin selects between the flow through mode and the registered modes. The 74ALVC162334 is implemented such that the $\overline{LE}$ pin will force the internal latches enabled and pass data through these latches in flow-through mode.

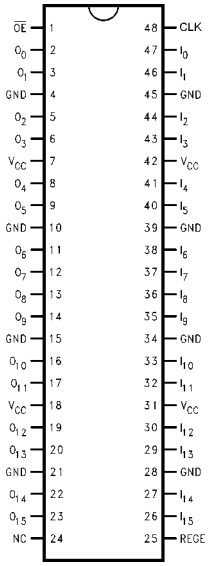
The functional differences shown do not impact registered DIMM Module application because the REGE pin is typically fixed in one state or the other for a given application. The implementation chosen for the 74VCX162838 was done to provide improved AC performance in flow-through mode.

Function Table for 74VCX162838

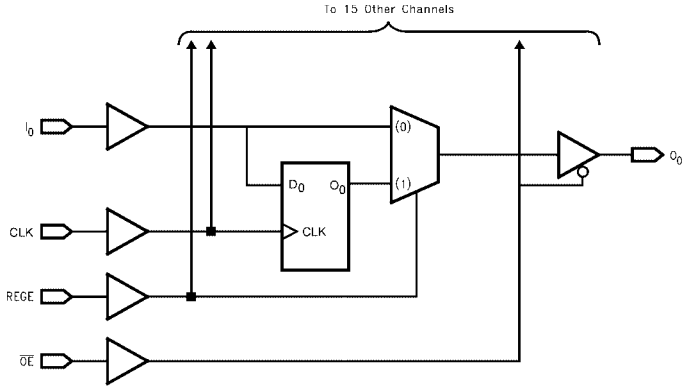
Inputs				Outputs
CLK	REGE	I_n	$\overline{OE}$	O_n
↑	H	H	L	H
↑	H	L	L	L
X	L	H	L	H
X	L	L	L	L
X	X	X	H	Z

H = Logic HIGH
L = Logic LOW
X = Don't Care, but not floating
Z = High Impedance
↑ = LOW-to-HIGH Transition

Connection Diagram for 74VCX162838



Logic Diagram for 74VCX162838



Comparison of 74VCX162838 vs. 74ALVC162334 (Continued)

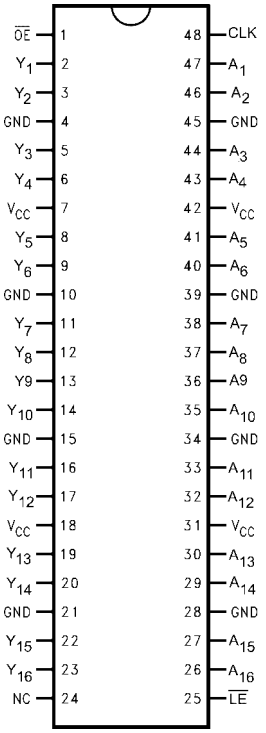
Function Table for 74ALVC162334

Inputs				Outputs
$\overline{OE}$	$\overline{LE}$	CLK	A_n	Y_n
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	L or H	X	Y_0(Note 7)

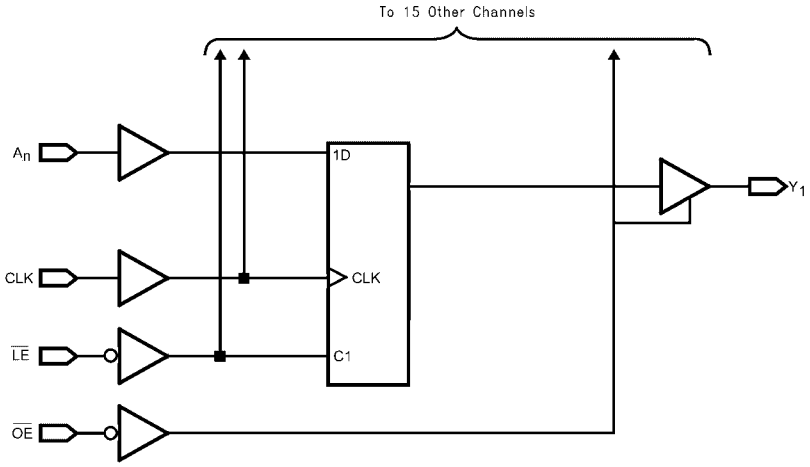
H = Logic HIGH
L = Logic LOW
X = Don't Care, but not floating
Z = High Impedance
↑ = LOW-to-HIGH Transition

Note 7: Output level before the indicated steady-state input conditions were established.

Connection Diagram for 74ALVC162334



Logic Diagram for 74ALVC162334



Comparison of 74VCX162838 vs. 74ALVC162334 (Continued)

AC Comparison

The following table shows a comparison of the 74VCX162838 device and the equivalent ALVC device. The table also compares performance vs. the Intel PC100 Rev 1.2 Registered DIMM specification.

AC Specifications Table

Parameter	Symbol	PC100 (1.2)		74VCX162838		74ALVC162334		Units	Test Conditions
		Min	Max	Min	Max	Min	Max		
CLK Input Capacitance	C_{IN}	3.30	6.00	6.0 (Typ)		5.0 (Typ)		pF	10 MHz
Maximum Clock Frequency	f_{MAX}	150		200		150		MHz	
Output Edge Rate	$t_{THL/LH}$	1.00	2.50					V/ns	C_L = 50pF V_{CC} = 3.3V +/- 0.15V Between 1.2V –1.8V
Propagation Delay – Register	$t_{PHL/LH}$ CLK to Y	1.9	4.5	1.1	4.2	1.0	4.9	ns	C_L = 50pF V_{CC} = 3.3V +/- 0.15V CLK to any Y
Propagation Delay – Register	$t_{PHL/LH}$ CLK to Y	1.4	2.9					ns	C_L = 0pF V_{CC} = 3.3V +/- 0.15V CLK to any Y
Propagation Delay – Buffer	$t_{PHL/LH}$ A to Y	1.0	4.5	1.1	3.8	1.1	3.9	ns	C_L = 50pF V_{CC} = 3.3V +/- 0.15V A to any Y
Propagation Delay – Buffer	$t_{PHL/LH}$ A to Y	0.9	2.0					ns	C_L = 0pF V_{CC} = 3.3V +/- 0.15V A to any Y
Maximum Allowable SSO Delay			300					ps	C_L = 50pF, Any output combination, V_{CC} = 3.3V +/- 0.15V
Setup Time	t_{SET}	1.7		1.5		1.5		ns	V_{CC} = 3.3V +/- 0.15V Any input
Hold Time	t_{HOLD}	0.7		1.0		0.9		ns	V_{CC} = 3.3V +/- 0.15V Any input
Input Current	I_{IN}		10.0		5.0		5.0	uA	V_{IN} = 0V to 3.45V V_{CC} = 3.3V +/- 0.15V

Note: AC Specifications Table for the VCX and ALVC products above are for V_{CC} = ± 10%, and T_A = –40 to 85°C

Comparison of 74VCX16839 vs. 74ALVC16836

Part Descriptions

74VCX16839	20 Bit Selectable Register Buffer with 3-STATE Outputs
74ALVC16836	20 Bit Universal Bus Driver with 3-STATE Outputs

Functional Comparison

The 74VCX16839 and 74ALVC16836 are pin and functionally equivalent for registered DIMM applications.

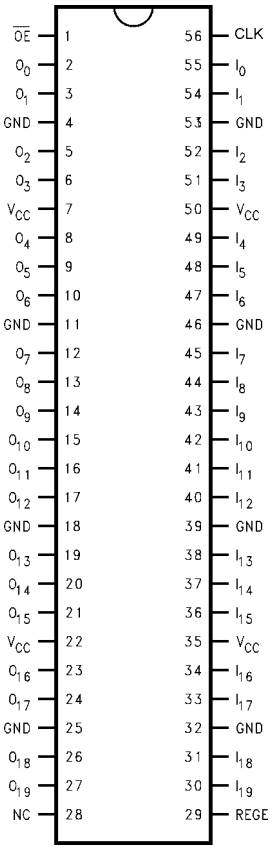
This means that one will see no functional difference when used in a registered DIMM application. There is however differences in the actual function of the devices. The 74VCX16839 was designed specifically for the Intel PC100 Rev 1.2 Registered DIMM specification and supports two modes of operation: a registered mode and a flow through mode. The 74ALVC16836 has additional functionality not required by the Intel PC100 Rev 1.2 Registered DIMM specification. While these devices support registered mode and flow through mode they have an additional latch mode.

Function Table for 74VCX16839

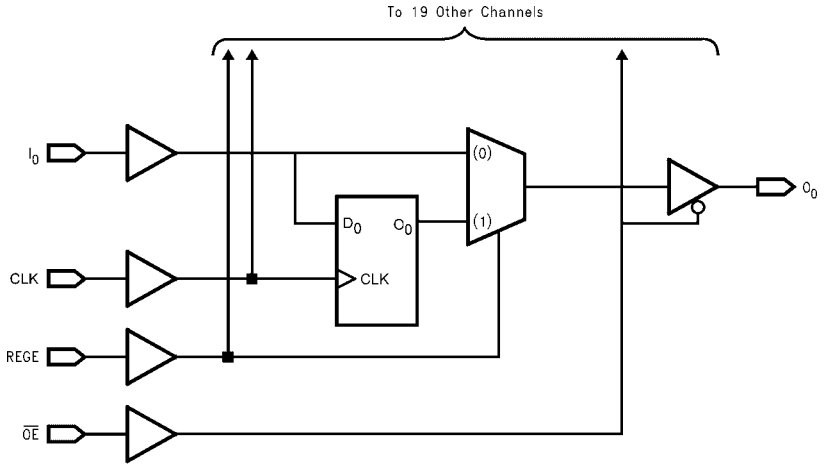
Inputs				Outputs
CLK	**REGE**	I_n	$\overline{OE}$	O_n
↑	H	H	L	H
↑	H	L	L	L
X	L	H	L	H
X	L	L	L	L
X	X	X	H	Z

H = Logic HIGH
L = Logic LOW
X = Don't Care, but not floating
Z = High Impedance
↑ = LOW-to-HIGH Transition

Connection Diagram for 74VCX16839



Logic Diagram for 74VCX16839



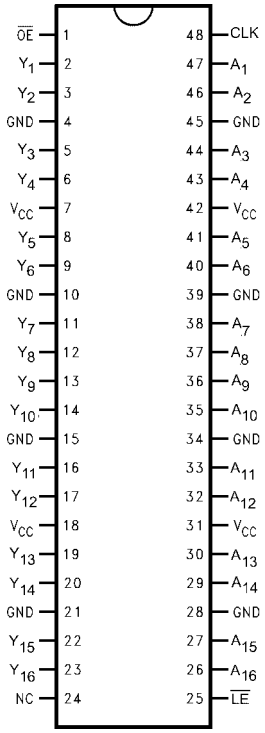
Comparison of 74VCX16839 vs. 74ALVC16836 (Continued)

Function Table for 74ALVC16836

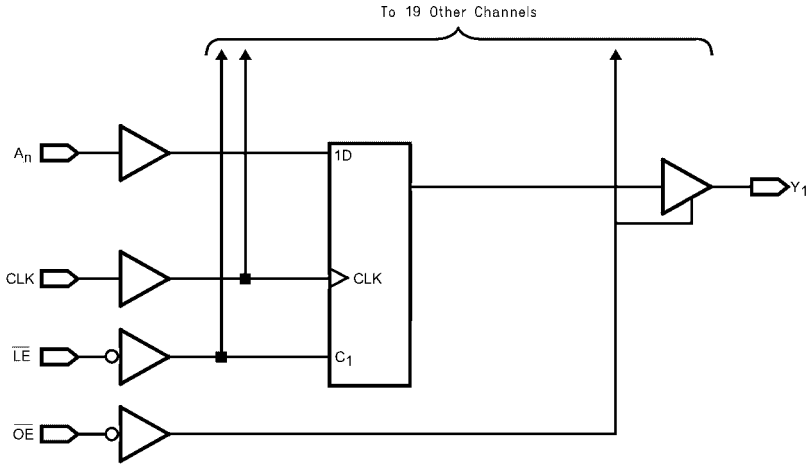
Inputs				Outputs
$\overline{OE}$	$\overline{LE}$	CLK	A_n	Y_n
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	H	X	Y_0
L	H	L	X	Y_0

H = Logic HIGH
L = Logic LOW
X = Don't Care, but not floating
Z = High Impedance
Y_0 = Indicates the previous state
↑ = LOW-to-HIGH Transition

Connection Diagram for 74ALVC16836



Logic Diagram for 74ALVC16836



Comparison of 74VCX16839 vs. 74ALVC16836 (Continued)

When the devices are in registered or flow through mode they will behave as functional equivalents. The waveforms shown in Figure 3 show how the devices respond in flow through and registered modes.

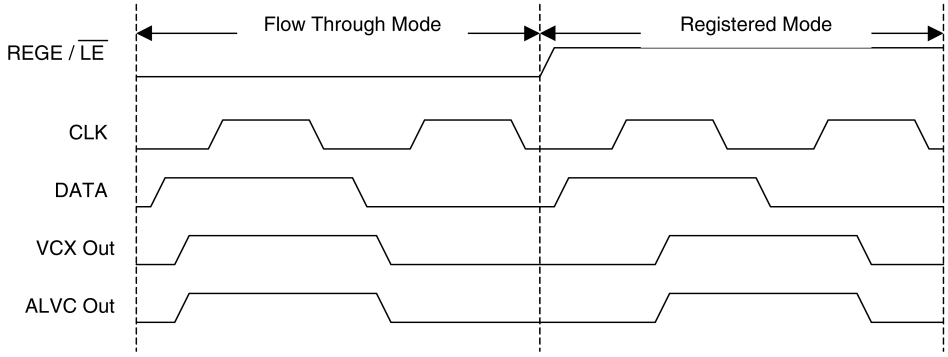


FIGURE 3. Flow Through Mode Waveforms

The actual functional differences can only be seen by transitioning the REGE($\overline{LE}$) pin when the data latched into the internal register is different from the data on the input port. The waveforms to generate this condition are shown in Figure 4. The 74VCX16839 is implemented such that the REGE pin selects between the flow through mode and the registered modes. The 74ALVC16836 is implemented such that the $\overline{LE}$ pin will force the internal latches enabled and pass data through these latches in flow-through mode.

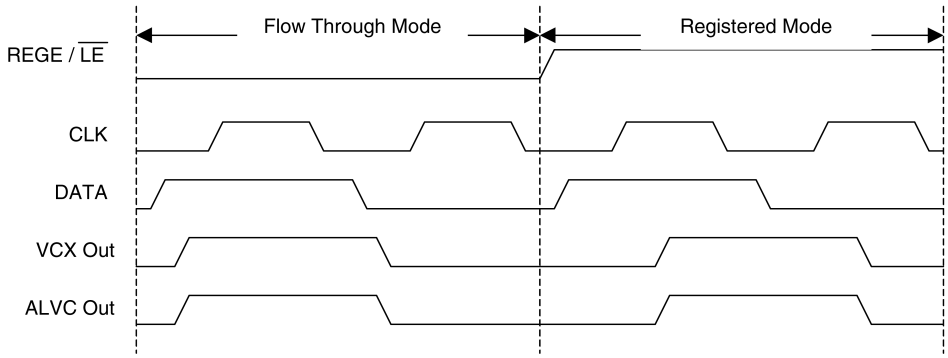


FIGURE 4. Flow Through Mode Waveforms

The functional differences shown do not impact registered DIMM Module application because the REGE pin is typically fixed in one state or the other for a given application. The implementation chosen for the 74VCX16839 was done to provide improved AC performance in flow-through mode.

Comparison of 74VCX16839 vs. 74ALVC16836 (Continued)

AC Comparison

The following table shows a comparison of the 74VCX16839 device and the equivalent ALVC device. The table also compares performance vs. the Intel PC100 Rev 1.2 Registered DIMM specification.

AC Specifications Table

Parameter	Symbol	PC100 (1.2)		74VCX16839		74ALVC16836		Units	Test Conditions
		Min	Max	Min	Max	Min	Max		
CLK Input Capacitance	C_{IN}	3.30	6.00	6.0 (Typ)		5.0 (Typ)		pF	10 MHz
Maximum Clock Frequency	f_{MAX}	150		250		150		MHz	
Output Edge Rate	$t_{THL/LH}$	1.00	2.50					V/ns	C_L = 50pF V_{CC} = 3.3V +/- 0.15V Between 1.2V –1.8V
Propagation Delay – Register	$t_{PHL/LH}$ CLK to Y	1.7	4.5	1.1	3.8	1.4	4.5	ns	C_L = 50pF V_{CC} = 3.3V +/- 0.15V CLK to any Y
Propagation Delay – Register	$t_{PHL/LH}$ CLK to Y	1.5	3.0					ns	C_L = 0pF V_{CC} = 3.3V +/- 0.15V CLK to any Y
Propagation Delay – Buffer	$t_{PHL/LH}$ A to Y	1.0	4.5	1.1	2.8	1.0	3.6	ns	C_L = 50pF V_{CC} = 3.3V +/- 0.15V A to any Y
Propagation Delay – Buffer	$t_{PHL/LH}$ A to Y	0.9	2.0					ns	C_L = 0pF V_{CC} = 3.3V +/- 0.15V A to any Y
Maximum Allowable SSO Delay			300					ps	C_L = 50pF, Any output combination, V_{CC} = 3.3V +/- 0.15V
Setup Time	t_{SET}	1.7		1.5		1.5		ns	V_{CC} = 3.3V +/- 0.15V Any input
Hold Time	t_{HOLD}	0.7		1.0		0.9		ns	V_{CC} = 3.3V +/- 0.15V Any input
Input Current	I_{IN}		10.0		5.0		5.0	uA	V_{IN} = 0V to 3.45V V_{CC} = 3.3V +/- 0.15V

Note: AC Specifications Table for the VCX and ALVC products above are for V_{CC} = ± 10%, and T_A = –40 to 85°C

Comparison of 74VCX162839 vs. 74ALVC162836

Part Descriptions

74VCX162839	20 Bit Selectable Register Buffer with 3-STATE Outputs and 25Ω Resistors
74ALVC162836	20 Bit Universal Bus Driver with 3-STATE Outputs and 25Ω Resistors

Functional Comparison

The 74VCX162839 and 74ALVC162836 are pin and functionally equivalent for registered DIMM applications.

This means that one will see no functional difference when used in a registered DIMM application. There is however differences in the actual function of the devices. The 74VCX162839 was designed specifically for the Intel PC100 Rev 1.2 Registered DIMM specification and supports two modes of operation: a registered mode and a flow through mode. The 74ALVC162836 has additional functionality not required by the Intel PC100 Rev 1.2 Registered DIMM specification. While these devices support registered mode and flow through mode they have an additional latch mode.

When the devices are in registered or flow through mode they will behave as functional equivalents. The waveforms shown in Figure 3 show how the devices respond in flow through and registered modes.

The actual functional differences can only be seen by transitioning the REGE($\overline{LE}$) pin when the data latched into the internal register is different from the data on the input port. The waveforms to generate this condition are shown in Figure 4 (see pg.15). The 74VCX162839 is implemented such that the REGE pin selects between the flow through mode and the registered modes. The 74ALVC162836 is implemented such that the $\overline{LE}$ pin will force the internal latches enabled and pass data through these latches in flow-through mode.

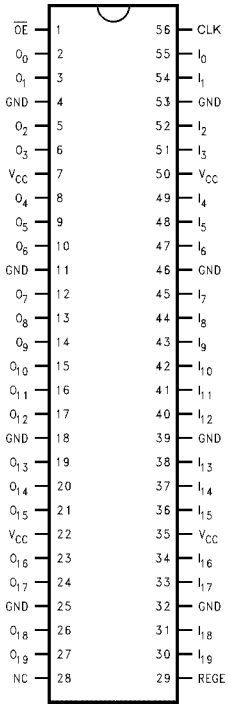
The functional differences shown do not impact registered DIMM Module application because the REGE pin is typically fixed in one state or the other for a given application. The implementation chosen for the 74VCX162839 was done to provide improved AC performance in flow-through mode.

Function Table for 74VCX162839

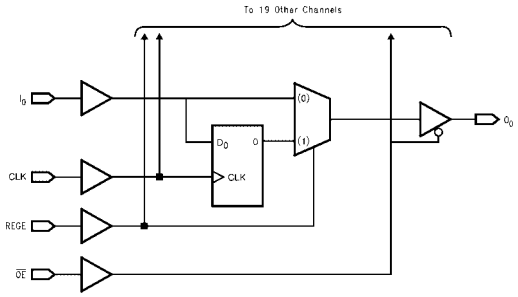
Inputs				Outputs
CLK	**REGE**	**I_n**	**$\overline{OE}$**	**O_n**
↑	H	H	L	H
↑	H	L	L	L
X	L	H	L	H
X	L	L	L	L
X	X	X	H	Z

H = Logic HIGH
L = Logic LOW
X = Don't Care, but not floating
Z = High Impedance
↑ = LOW-to-HIGH Transition

Connection Diagram for 74VCX162839



Logic Diagram for 74VCX162839



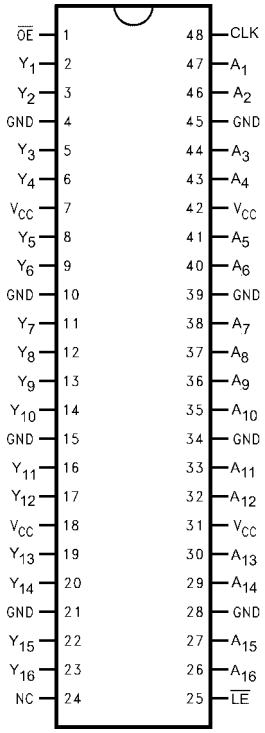
Comparison of 74VCX162839 vs. 74ALVC162836 (Continued)

Function Table for 74ALVC162836

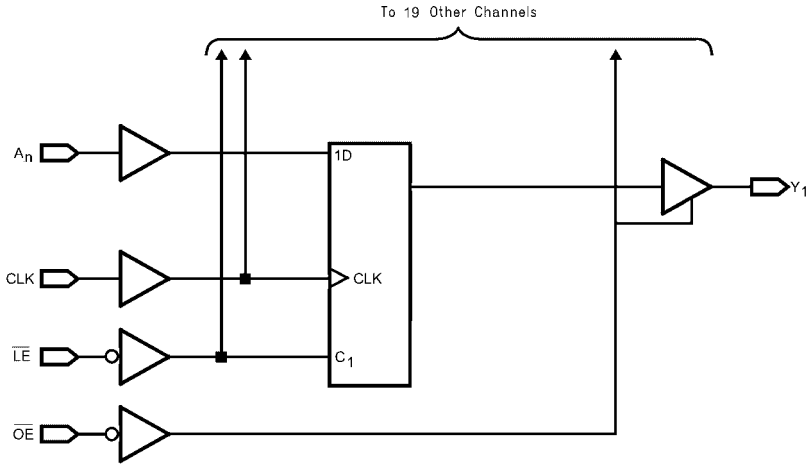
Inputs				Outputs
$\overline{OE}$	$\overline{LE}$	CLK	A_n	Y_n
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	L or H	X	Y_0(Note 8)

Note 8: Output level before the indicated steady-state input conditions were established.

Connection Diagram for 74ALVC162836



Logic Diagram for 74ALVC162836



Comparison of 74VCX162839 vs. 74ALVC162836 (Continued)

AC Comparison

The following table shows a comparison of the 74VCX162839 device and the equivalent ALVC device. The table also compares performance vs. the Intel PC100 Rev 1.2 Registered DIMM specification.

AC Specifications Table

Parameter	Symbol	PC100 (1.2)		74VCX162839		74ALVC162836		Units	Test Conditions
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Maximum Clock Frequency	f_{MAX}	150		250		150		MHz	
Output Edge Rate	$t_{THL/LH}$	1.00	2.50					V/ns	C_L = 50pF V_{CC} = 3.3V +/- 0.15V Between 1.2V –1.8V
Propagation Delay – Register	$t_{PHL/LH}$ CLK to Y	1.9	4.5	1.1	4.7	1.1	5.0	ns	C_L = 50pF V_{CC} = 3.3V +/- 0.15V CLK to any Y
Propagation Delay – Register	$t_{PHL/LH}$ CLK to Y	1.4	2.9					ns	C_L = 0pF V_{CC} = 3.3V +/- 0.15V CLK to any Y
Propagation Delay – Buffer	$t_{PHL/LH}$ A to Y	1.0	4.5	1.1	3.7	1.2	4.0	ns	C_L = 50pF V_{CC} = 3.3V +/- 0.15V A to any Y
Propagation Delay – Buffer	$t_{PHL/LH}$ A to Y	0.9	2.0					ns	C_L = 0pF V_{CC} = 3.3V +/- 0.15V A to any Y
Maximum Allowable SSO Delay			300					ps	C_L = 50pF, Any output combination, V_{CC} = 3.3V +/- 0.15V
Setup Time	t_{SET}	1.7		1.5		1.5		ns	V_{CC} = 3.3V +/- 0.15V Any input
Hold Time	t_{HOLD}	0.7		1.0		0.9		ns	V_{CC} = 3.3V +/- 0.15V Any input
Input Current	I_{IN}		10.0		5.0		5.0	uA	V_{IN} = 0V to 3.45V V_{CC} = 3.3V +/- 0.15V

Note: AC Specifications Table for the VCX and ALVC products above are for $V_{CC} = \pm 10\%$, and $T_A = -40$ to 85°C

Conclusion

As can be seen from the above comparisons, Fairchild Semiconductor's solutions for buffered or registered DIMMs have comparable or better performance than competitive solutions. Through careful consideration of device performance, functional requirement, and bit-width requirements, successful PC100 DIMM designs can be achieved with high signal integrity and system performance.