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A New PSPICE Electro-Thermal Subcircuit For Power MOSFETs

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Keywords

Device characterization, device modeling, high power discrete devices, modeling, MOS device, power semiconductor devices, semiconductor devices, simulation, thermal design.

Abstract

An empirical self-heating SPICE MOSFET model which accurately portrays the vertical DMOS power MOSFET electrical and thermal responses is presented. This macro-model implementation is the culmination of years of evolution in MOSFET modeling. This new version brings together the thermal and the electrical models of a VDMOS MOSFET. The existing electrical model [2,3] is highly accurate and is recognized in the industry. The sequence of the model calibration procedure using parametric data is described. Simulation response of the new self-heating MOSFET model track the dynamic thermal response and is independent of SPICE's global temperature definition.

1. Introduction

Many power MOSFET models available today are based on an ideal lateral MOSFET device. They offer poor correlation between simulated and actual circuit performance in several areas. They have low and high current inaccuracies that could mislead power circuit designers. This situation is further complicated by the dynamic performance of the models. The ideal low power SPICE level-1 NMOS MOSFET model does not account for the nonlinear capacitive characteristics Ciss, Coss, Crss of a power MOSFET. Higher level SPICE MOSFET models may be used to implement the non-linear capacitance with mixed results. The need for this higher level modeling accuracy becomes apparent in high frequency applications where gate charge losses as a proportion of overall losses become significant.

The inherent inaccuracies of modeling a power VDMOS with the SPICE MOSFET model dictated need for an alternative approach; a macro-model.

A macro-model such as the one defined by Wheatley and Hepp [1] can address the short comings of the ideal low power SPICE MOSFET model. Highly accurate results

are possible by surrounding a temperature independent gain block (implemented using three level-1 MOSFET models) with resistive, capacitive, inductive and other SPICE circuit elements.

It is possible to develop a model from parametric measurements in a single iteration. The model extraction procedure from parametric data must follow a given sequence. Many of the changes to the model affect different behaviour. Failure to follow this sequence will result in repeated model calibration iterations.

The MOSFET model reference on which this work is based has been explained in [1, 2, 3, 10]. The reader is encouraged to refer to these references for a full understanding of the MOSFET model parameters herein referenced. Use of the model, once extracted is not discussed here, but reference [10] addresses the use.

Recent works [8, 9] have demonstrated methods of circumventing the SPICE global temperature definition, providing a means of using the device's own junction temperature as a self-heating feedback mechanism.

The model developed in [8] has limitations involving proprietary algorithms, rendering the method of limited interest. Model implementation is convoluted, involving a MOSFET analog behavioral model (ABM) implementation whose operating characteristics are dependent on a SPICE level-3 NMOS MOSFET. As a result, both the switching circuit and the load must be duplicated for the model to function. The implementation in [9] does not model the drain-source avalanche property of a MOSFET. Neither [8] nor [9] attempt to model the temperature characteristics of the intrinsic body diode. Introduced self-heating modeling concepts are non-proprietary and may be adapted to other MOSFET models.

2. Self-Heating SPICE MOSFET Model

The self-heating macro-model from Figure 1 is the evolution of years of work and improvements from numerous authors [1-7]. A significant advantage of this model is that knowledge of device physics or process details are not necessary to implement the parametric data within the model.

Parametric data for several temperature points are used for model calibration resulting in a macromodel which provides representative simulation data for any rated operating junction temperature.

Temperature dependent model parameters respond in closed loop form to the junction temperature information provided by node *Tj*. Performance is independent of SPICE's global temperature definition listed as *.TEMP* and temperature option *TNOM*, circumventing the level-1 NMOS model primitive temperature limitation. All MOSFET operating losses are inclusive in the current source *G_Pdiss* representing instanta-

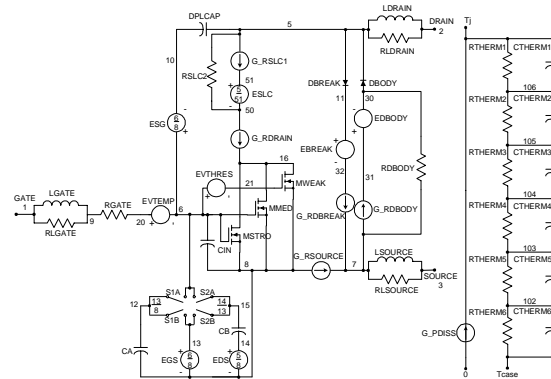neous power dissipation into the thermal model.

Figure 1 Self-heating MOSFET macro-model independent of global temperature definition

Figure 1. Self-heating MOSFET macro-model independent of global temperature definition

Multiple MOSFETs may be simulated at different and variable junction temperatures. Each MOSFET may be connected to a heat sink model via node *Tcase*. The heat sink model may be device specific, so heat sink optimization becomes possible. Current source *G_Pdiss* is referenced to the simulation ground reference, permitting use of the model in bridge topologies.

An example of a symbol representation of the self-heating MOSFET model is shown in Figure 2. Symbol files for OrCAD's two circuit entry tools "PSPICE Schematic" and "OrCAD Capture" may be downloaded from www.fairchildsemi.com. Recommended symbol implementation is to designate the pinout attribute for *Tj* as optional (*ERC = DON'T CARE, Float=UniqueNet*). *Tj* is the representation of the device junction temperature. It may be used as a monitoring point, or it may be connected to a defined voltage source to override the self-heating feature. *Tcase* must be connected to a heat sink model. Treatment of connections to the model's gate, drain, and source terminals are no different than those of the standard MOSFET model.
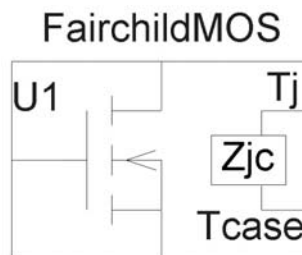

Figure 2. Self-heating MOSFET symbol

3. Self-Heating SPICE MOSFET Model

Ability to describe the value of a resistor and its temperature coefficients as a behavioral model referenced to a voltage node is necessary to express dependence on junction temperature. PSPICE resistor ABMs do not permit voltage node references.

Dynamic temperature dependence of the MOSFET's resistive element (expressed as separate lumped elements) and of the diode's resistive component cannot be implemented without a resistor ABM.

This limitation is overcome with a voltage-controlled current source ABM expression (Figure 3). By using the nodes of the current source for voltage control, resistor behaviour may be expressed as I = V/R(T_j). The resistance R(T_j) is replaced by a behavioral model expression dependent on the voltage node *Tj* representation of junction temperature. This voltage-controlled current source ABM model was used to implement voltage dependent expressions of *RDRAIN*, *RSOURCE*, and *RSLC1*.
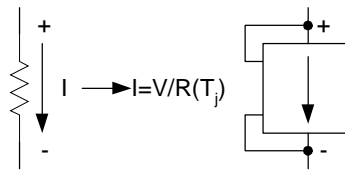

Figure 3. Implementing a voltage dependent ABM resistor model

Temperature dependent resistive elements of diodes *DBODY* and *DBREAK* were separated from the diode model, and expressed as voltage-controlled current source ABM models *G_RDBODY* and *G_RDBREAK*. A very large value resistor *RDBODY* was added to improve convergence.

EDBODY is added in series with *DBODY* to incorporate the temperature dependency of the intrinsic body diode forward conduction drop.

Junction temperature information is implemented by the inclusion of the MOSFET's thermal network $Z_{\theta JC}$ and current source *G_PDISS*. The thermal network parameters are supplied in Fairchild Semiconductor data sheets. *G_PDISS* calculates the MOSFET instantaneous operating loss, and expresses the result in the form of a current. This is a circuit form implementation of the junction temperature from expression (1)

$$T_j = P_{dissipation} \cdot Z_{\theta JC} + T_{case} \tag{1}$$

where T_j = junction temperature, $P_{dissipation}$ = instantaneous power loss, $Z_{\theta JC}$ = thermal impedance junction- to-case and T_{case} = case temperature. The unit conversion for the electrical analogy of the thermal system is listed in Table 1.

Electrical	$\Leftrightarrow$	Thermal
Ohm		^{o}C/Watt
Farad		Joules/^{o}C
Amp		Watt
Volt		^{o}C

Table 1 Electrical/thermal analogy

4. Parameter Extraction Methodology

The sequence of the parameter extraction procedure is very important since many of the changes to the library affect different behavior. For instance, changing parameters in the transfer curve affect the saturation curves.

The recommended methodology is shown below.
1. The transfer curve
2. The saturation curve
3. The body diode forward conduction
4. Breakdown voltage
5. T_{rr}
6. Capacitance (C_{rss}, C_{oss}, C_{iss})
7. Gate charge
8. Temperature coefficients
9. Thermal model

Extraction is achieved more rapidly if data is plotted log-log, semilog, $\sqrt{I}$ versus t, etc. First extraction may take days. It becomes a rapidly learned process with repeated usage.

4.1 Transfer Curve

Three level-1 MOSFET transistors are used to model the gain block for the full current range from the sub-threshold region through high current. The three transistor models are *MweakMOD*, *MmedMOD* and *MstroMOD*. The parameters *VTO* and *KP* of each transistor are used for alignment of the model with measured data.

*.MODEL MmedMOD NMOS (**VTO=3.3 KP=9** IS=1e-30 N=10 TOX=1 L=1u W=1u*
+RG=1.36 T_ABS=25)
*.MODEL MstroMOD NMOS (**VTO=4.0 KP=275** IS=1e-30 N=10 TOX=1 L=1u W=1u*
+T_ABS=25)
*.MODEL MweakMOD NMOS (**VTO=2.72 KP=0.03** IS=1e-30 N=10 TOX=1 L=1u*
+W=1u RG=13.6 RS=0.1 T_ABS=25)

Source resistance (*G_Rsource*) is added to lower the gain at high currents. It is also a contributing element to the device $r_{DS(ON)}$. Plotting the square root of I_{DS} versus V_{GS} results in a linear curve instead of a quadratic curve, thus improving the visual resolution of the data at the higher current range.

*G_Rsource 8 7 VALUE={V(8,7)/(**2.5e-3***(1+5e-3*(V(th+)-25)+1e-6*pwr((V(th+)-*
+25),2)))}

4.2 Saturation Curves

Several gate biases should be used to model the saturation curves. For instance, to model a standard gate device use V_{GS} = 10V, 5V and 3.5V. *G_Rdrain* is used to fit the model in the linear region. Increasing *G_Rdrain* will decrease the current of the saturation curves. Next, the space charge limiting effect is modeled using ESLC. The multiplier X in ESLC (1e-6*X, the exponent of the power statement) is adjusted. Lowering X will round off the curves at high currents. If two saturation curves (for instance at V_{gs}=10V and V_{gs}=5V) do not match in the linear region, it may be necessary to readjust KP of the strong transistor MstroMOD. Modeling between transfer and saturation curves will then need to be repeated until both curves fit the data.

G_Rdrain 50 16 VALUE={V(50,16)/(1e-4* (1+5.5e-2*(v(th+)-25)+3.2e-4*PWR((v(th+)-+25),2)))} ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51))) *(PWR(V(5,51)/(1e +6*300),10))}

4.3 Body Diode Forward Voltage

Match diode curve data at low currents by adjusting parameters *IS* and *N* in *DbodyMOD*. With the forward voltage plotted on a log scale, *N* will adjust the slope and *IS* will shift the curve left or right.

*.MODEL DbodyMOD D (**IS=2.4e-11 N=1.04** CJO=4.35e-9 M=0.54 TT=1.0e-9 +XTI=3.9 T_ABS=25)*

The high current region is modeled on the linear scale. *G_Rdbody* is used to match diode curve data at high currents by adding series resistance, thus lowering the curve.

*G_Rdbody 7 31 VALUE={V(7,31)/(**1.65e-3*** (1+2.7e-3*(V(TH+)-25)+2e-+7*PWR((V(TH+)-25),2)))}*

IKF can be used to smooth the transition region between low currents and high currents. After changing *IKF*, it is often necessary to readjust *G_Rdbody*.

*.MODEL DbodyMOD D (IS=2.4e-11 N=1.04 CJO=4.35e-9 M=0.54 TT=1.0e-9 +XTI=3.9 **IKF=100** T_ABS=25)*

4.4 Breakdown Voltage

Low current breakdown is modeled with *Ebreak*.

*Ebreak 11 32 VALUE={**69.3***(1+9.5e-4* (V(TH+)-25)+1e-7*PWR((V(TH+)-25),2))}*

High current breakdown is modeled with *G_Rdbreak*.

*G_Rdbreak 32 7 VALUE={v(32,7)/(**7.0e-2*** (1+5e-4*(V(TH+)-25)+1e-7**
+PWR((V(TH+)-25),2)))}

4.5 T$_{rr}$

Intrinsic body diode reverse recovery is modeled at 100A/µS and the maximum rated DC current. Parameter *TT* of the body diode *DbodyMOD* is used to match the modeled Ta to the measured Ta.

*.MODEL DbodyMOD D (IS=2.4e-11 N=1.04 CJO=4.35e-9 M=0.54 **TT=1.0e-9***
+XTI=3.9 T_ABS=25)

4.6 Capacitance

Capacitance is modeled for drain-to-source voltages of 0.1V to the breakdown voltage. Crss is modeled first, setting *CJO* and *M* of *DplcapMOD*. *CJO* will adjust the level of the capacitance curve while *M* will adjust the slope. Next, C$_{oss}$ is modeled with *CJO* and *M* of *DbodyMOD*. This is done in a similar manner to C$_{rss}$. Finally input capacitance C$_{iss}$ is adjusted by setting *Cin* of the model.

*.MODEL DplcapMOD D (**CJO=1.7e-9** IS=1e-30 N=10 **M=0.47**)*
*.MODEL DbodyMOD D (IS=2.4e-11 N=1.04 **CJO=4.35e-9 M=0.54** TT=1.0e-9*
+XTI=3.9 T_ABS=25) Cin 6 8 6.1e-9

4.7 Gate Charge

Modeling of the gate charge curve is a four step process (Figure 4). First, adjust the slope through the most negative gate voltages by adjusting *Ca*. Next, adjust the slope breakpoint by adjusting S1A and S1B switch voltages (VON and VOFF) to account for the discontinuity between the two slopes at negative voltages. *VON* and *VOFF* of *S1AMOD* and *S1BMOD* should be the reverse of the one another (*VON* of *S1AMOD* should be *VOFF* of *S1BMOD*, and vice versa).
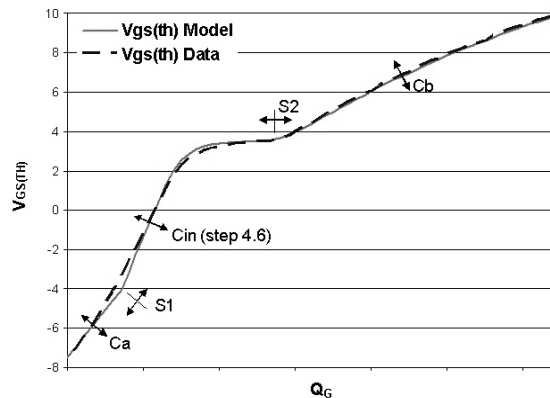

Figure 4 Modeling gate charge

*Ca 12 8 **1.5e-9***
*.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 **VON=-4 VOFF=-1.5**)*
*.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 **VON=-1.5 VOFF=-4**)*

Third, switch voltages of *S2A* and *S2B* are adjusted to set the length of the plateau region. The voltage level of the plateau will be setup by the modeling done for the transfer curve and can not be adjusted at this point. *S2AMOD* and *S2BMOD* should be reverse of each other as stated above for *S1AMOD* and *S1BMOD*. Fourth, adjust the slope of the curve above the plateau by adjusting *Cb. Ca* and *Cb* should be nearly identical in value.

*Cb 15 14 **1.5e-9***
*.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 **VON=-1 VOFF=0.5**)*
*.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 **VON=0.5 VOFF=-1**)*

VON values for the switches *S1A* through *S2B* should be increasing in a positive direction. There should be a minimum of 0.5V separating each *VON* value. Reduction of the separation below 0.5V can result in convergence errors.

4.8 Temperature Coefficients

Repeat steps 4.1 through 4.4 at a low and high temperature (ex. -25°C and 125°C). For step 4.2 saturation curves, only one gate bias will be used in temperature coefficient matching and should be the gate voltage that is used for rating r$_{DS(ON)}$. Temperature coefficients are not a factor for transient analyses (capacitance, T$_{rr}$ and gate charge).

Transfer Curve: At high currents adjust the temperature parameters of *Evtemp*. At low currents adjust the temperature parameters of *Evthres*. The temperature coefficients of *G_Rsource* may be used to fit the curve at high currents. The first parameter highlighted in each line below is a linear coefficient and the second is a square function coefficient.

*Evtemp 20 6 VALUE={**-2.5e-3***(V(TH+)-25) **+1e-6***PWR((V(TH+)-25),2)}*
*Evthres 6 21 VALUE={**-6.7e-3***(V(TH+)-25)**-1.5e-5***PWR((V(TH+)-25),2)}*
G_Rsource 8 7 VALUE={V(8,7)/(2.5e-3 (1**+5e-3***(V(th+)-25)**+1e-6***pwr((V(th+)-25) +,2)))}*

Saturation Curves: First adjust the temperature parameters of *G_Rdrain*. Then model the temperature parameters of *G_RSLC1*. This models the space charge limiting effect over temperature.

G_Rdrain 50 16 VALUE={V(50,16)/(1e-4 (1**+5.5e-2***(v(th+)-25)**+3.2e-4***pwr((v(th+)- +25),2)))} G_RSLC1 5 51 VALUE={v(5,51)/(1e-6* (1**+1e-3***(v(th+)-25)**+1e- +5***pwr((v(th+)-25),2)))}*

Body Diode Forward Voltage: At low currents the forward voltage is modeled with the temperature coefficients of *EDbody*. The last parameter in *EDbody* is used to limit V_f above 175°C. Thermal parameters of *G_Rdbody* are used to model the high current region.

*EDbody 31 30 VALUE={IF(V(TH+)<175, **-1.5e-3***V(TH+)**+.03**,**0.2325**)}*
G_Rdbody 7 31 VALUE={V(7,31)/(1.65e-3 (1**+2.7e-3***(V(TH+)-25)**+2e-7****
+PWR((V(TH+)-25),2)))}

Breakdown voltage: Low current breakdown is modeled with thermal parameters of *Ebreak*. Thermal parameters of *G_Rdbreak* are used to model high current.

G_Rdbreak 32 7 VALUE={v(32,7)/(7.0e-2 (1**+5e-4***(V(TH+)-25)**+1e-7***PWR((V(TH+)-*
+25),2)))}
Ebreak 11 32 VALUE={69.3(1**+9.5e-4*** (V(TH+)-25)**+1e-7***PWR((V(TH+)-25),2))}*

4.9 Thermal Model

The thermal model is modeled independently of the electrical model. Components *CTHERM1* through *CTHERM6* and *RTHERM1* through *RTHERM6* are used to fit the simulated thermal impedance curve to the measured data. To ensure a good thermal model, the thermal capacitors should be increasing in value from CTHERM1 through CTHERM6. Thermal resistors should also be increasing in value from RTHERM1 through RTHERM6.

*CTHERM1 Tj 106 **6.45E-3***
*CTHERM2 106 105 **3e-2***
*CTHERM3 105 104 **1.4e-2***
*CTHERM4 104 103 **1.65e-2***
*CTHERM5 103 102 **4.85e-2***
*CTHERM6 102 Tcase **1e-1***
*RTHERM1 Tj 106 **3.24e-3***
*RTHERM2 106 105 **8.08e-3***
*RTHERM3 105 104 **2.28e-2***
*RTHERM4 104 103 **1e-1***
*RTHERM5 103 102 **1.1e-1***
*RTHERM6 102 Tcase **1.4e-1***

5. Simulation Results

Simulation results and parametric data from MOSFET FDP038AN06A0 are plotted in Figures 4, 5, 6, 7 for gate charge, gate threshold, $r_{DS(ON)}$, and conduction saturation voltage. Excellent agreement exists.
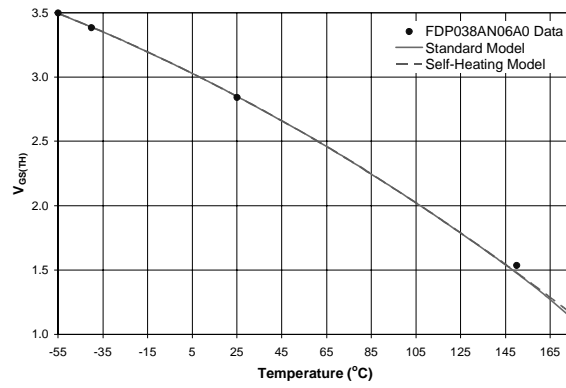
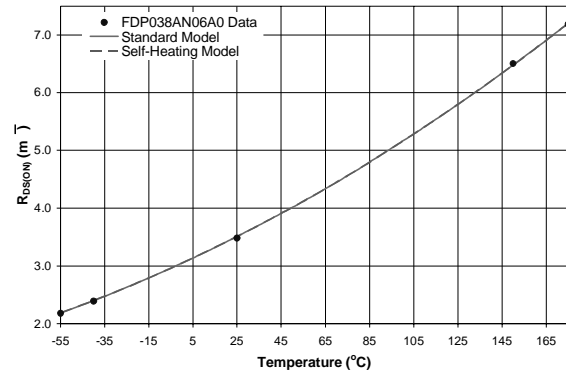Figure 5 FDP038AN06A0 threshold voltage
Conditions: I_D = 250µA

Figure 6 FDP038AN06A0 $r_{DS(ON)}$
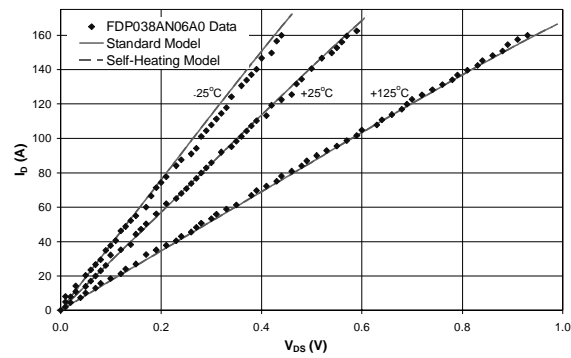Conditions: I_D = 80A, V_{GS} = 10V

Figure 7 FDP038AN06A0 saturation voltage
Conditions: V_{GS} = 10V

6. Simulation Convergence

The self-heating model was tested under numerous circuit configurations. It was found to be numerically stable. Failure to converge can occur under some large signal simulations if PSPICE's setup option *ABSTOL* setting is less than 1µA.
UIS simulations [10] were performed on a Dell Latitude CSx having a 500MHz Pentium III processor with 256MB of RAM. Windows 2000 was the operating system used with virus scan software enabled. PSPICE Schematics version 9.1 was used.

Simulation time results were:
   - standard model = 7.9s
   - self-heating model = 13.7s

Simulation time will be longer with the self-heating model when significant and rapid junction temperature variation occurs. This is a result of the dynamic interaction from the junction temperature feedback on the MOSFET temperature dependent parameters.

7. Future Model Developments

Minor inaccuracy is introduced if previously published Fairchild Semiconductor MOSFET models are modified to become self-heating models, but are well within device parametric tolerance (not demonstrated in this paper). The inaccuracy can be eliminated by including the variable *T_ABS=25* in the level-1 NMOS MOSFET during device specific model calibration, permitting full compatibility of the model with the new self-heating model. This term was included for the standard MOSFET model calibration of the FDP038AN06A0. Temperature dependency of the self-heating model intrinsic body diode leakage current could be introduced by adding a junction temperature dependent current source across the body diode.

8. Conclusion

The self heating PSPICE power MOSFET macro-model provides the next evolutionary step in circuit simulation accuracy. The inclusion of a thermal model coupled to the temperature sensitive MOSFET electrical parameters results in a self-heating PSPICE MOSFET macro-model which allows increased accuracy during time domain simulations. The effect of temperature change due to power dissipation during time domain simulations can now be modeled.

The modeling modification concepts introduced are non-proprietary and may be adapted to MOSFET SPICE models from any manufacturer. A methodology for calibrating a MOSFET model using parametric data was described. Adherence to the calibration sequence yields a highly accurate model.

References

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.SUBCKT FDP038AN06A0_5NODE 2 1 3 Tj Tcase
Ca 12 8 1.5e-9
Cb 15 14 1.5e-9
Cin 6 8 6.1e-9
EDbody 31 30 VALUE={IF(V(Tj,0)<175,-1.5E-3*V(Tj,0)+.03,-.2325)}
Dbody 30 5 DbodyMOD
Dbreak 5 11 DbreakMOD
Dplcap 10 5 DplcapMOD
RDBODY 30 7 1E15
G_Rdbody 7 31 VALUE={V(7,31)/(1.65e-3*(1+2.7E-3*(V(Tj,0)-25)+2E-
+7*PWR((V(Tj,0)-25),2)))}
G_Rdbreak 32 7 VALUE={v(32,7)/(7.0e-2*(1+5e-4*(V(Tj,0)-25)+1e-7*PWR((V(Tj,0)-
+25),2)))}
Ebreak 11 32 VALUE={69.3*(1+9.5E-4*(V(Tj,0)-25)+1e-7*PWR((V(Tj,0)-25),2))}
Eds 14 8 5 8 1
Egs 13 8 6 8 1
Esg 6 10 6 8 1
Evthres 6 21 VALUE={-6.7E-3*(V(Tj,0)-25)-1.5E-5*PWR((V(Tj,0)-25),2)}
Evtemp 20 6 VALUE={-2.5e-3*(V(Tj,0)-25)+1e-6*PWR((V(Tj,0)-25),2)}
Lgate 1 9 4.81e-9
Ldrain 2 5 1.0e-9
Lsource 3 7 4.63e-9
RLgate 1 9 48.1
RLdrain 2 5 10
RLsource 3 7 46.3
Mmed 16 6 8 8 MmedMOD
Mstro 16 6 8 8 MstroMOD
Mweak 16 21 8 8 MweakMOD
G_Rdrain 50 16 VALUE={V(50,16)/(1E-4*(1+5.5E-2*(v(Tj,0)-25)+3.2E-4*pwr((v(Tj,0)-
+25),2)))} Rgate 9 20 1.36
G_RSLC1 5 51 VALUE={v(5,51)/(1e-6*(1+1E-3*(v(Tj,0)-25)+1E-5*pwr((v(Tj,0)-
+25),2)))}
RSLC2 5 50 1e3
G_Rsource 8 7 VALUE={V(8,7)/(2.8E-3*(1+5e-3*(V(Tj,0)-25)+1e-6*pwr((V(Tj,0)-
+25),2)))}
S1a 6 12 13 8 S1AMOD
S1b 13 12 13 8 S1BMOD
S2a 6 15 14 13 S2AMOD
S2b 13 15 14 13 S2BMOD
ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*300),10))}
G_PDISS 0 TH+ VALUE={I(ESLC)*V(5,7) + I(EVTEMP)*V(9,7)+I(EBREAK)*V(5,7) +
+I(EDBODY)*V(7,5)}
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CTHERM1 Tj 106 6.45E-3
CTHERM2 106 105 3e-2
CTHERM3 105 104 1.4e-2
CTHERM4 104 103 1.65e-2
CTHERM5 103 102 4.85e-2
CTHERM6 102 Tcase 1e-1
RTHERM1 Tj 106 3.24e-3
RTHERM2 106 105 8.08e-3
RTHERM3 105 104 2.28e-2
RTHERM4 104 103 1e-1
RTHERM5 103 102 1.1e-1
RTHERM6 102 Tcase 1.4e-1
.MODEL DbodyMOD D (T_ABS=25 IS=2.4E-11 N=1.04 CJO=4.35e-9 M=0.54
+TT=1.0e-9 XTI=3.9)
.MODEL DbreakMOD D ()
.MODEL DplcapMOD D (CJO=1.7e-9 IS=1e-30 N=10 M=0.47)
.MODEL MmedMOD NMOS (T_ABS=25 VTO=3.3 KP=9 IS=1e-30 N=10 TOX=1
+L=1u W=1u RG=1.36)
.MODEL MstroMOD NMOS (T_ABS=25 VTO=4.0 KP=275 IS=1e-30 N=10 TOX=1
+L=1u W=1u)
.MODEL MweakMOD NMOS (T_ABS=25 VTO=2.72 KP=0.03 IS=1e-30 N=10 TOX=1
+L=1u W=1u
+RG=13.6 RS=.1)
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4 VOFF=-1.5)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-1.5 VOFF=-4)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-1 VOFF=.5)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=.5 VOFF=-1)
.END
```

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