SigmaDSP® Multichannel Audio Processor with Embedded 2ADC/8DAC Codec

ADAV400

FEATURES

- Fully programmable audio digital signal processing (DSP) for enhanced sound processing
- Features SigmaStudio™, a proprietary graphical programming tool for fast development of custom signal flows
- Easy implementation of third party audio algorithms
- Scalable digital audio delay line
  - Pool of 400 ms (for example, 200 ms for stereo channel)
- High performance integrated analog-to-digital converters (ADCs) and digital-to-analog converters (DACs)
  - 1 stereo analog input (ADC)
  - 4 stereo analog inputs with mux to stereo ADC
  - 4 stereo (8-channel) analog outputs (DACs)
- Dedicated headphone output with integrated amplifier
- Multichannel digital I/O
  - 8-channel I²S input and output modes
  - 8- and 16-channel TDM input and output modes
  - 2-channel (1 stereo) asynchronous I²S input with integrated sample rate converter (SRC), supporting sample rates from 5 kHz to 50 kHz
- I²C® control interface
- Operates from 3.3 V (analog), 1.8 V (digital core), 3.3 V (digital interface)
- Features on-chip regulator for single 3.3 V operation
- 80-lead LQFP package (14 mm x 14 mm)
- Temperature range: 0°C to +70°C

APPLICATIONS

- Advanced TV (ATV) audio processing
  - Custom Audio Flows
  - Sound Enhancement
  - 3rd Party Audio Algorithms
- DVD Receiver and HTiB
  - Virtualiser for 2.0 or 2.1 systems
  - Post Processing

FUNCTIONAL BLOCK DIAGRAM

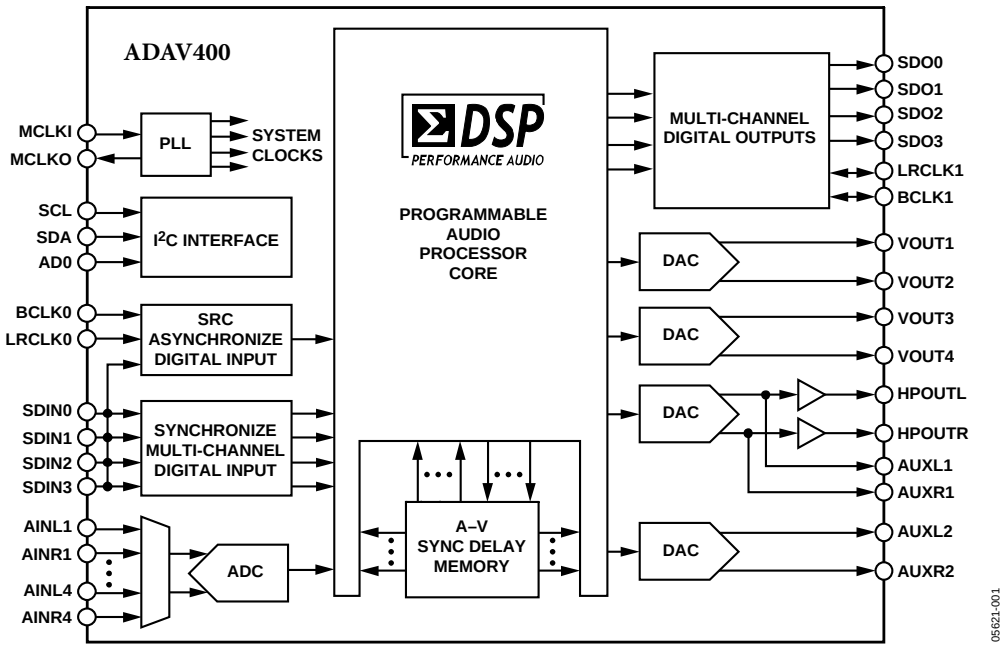

Figure 1.

Rev. PrG

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REVISION HISTORY

Preliminary Version Rev PrG

GENERAL DESCRIPTION

The ADAV400 is an enhanced audio processor. Integrating high performance analog and digital I/O with a powerful audio specific programmable core enables designers to differentiate their products through audio performance.

The audio processing core is based on Analog Devices SigmaDSP technology featuring full 28-bit processing (56-bit in double precision mode), a sophisticated, fully programmable, dynamics processor and delay memory.

This technology allows the system designer to compensate for real world limitations of speakers, amplifiers, and listening environments. This compensation results in a dramatic improvement of the perceived audio quality through speaker equalization, multiband compression and limiting, and third party branded algorithms.

The analog I/O integrates Analog Devices proprietary continuous time, multibit, sigma-delta (Σ-Δ) architecture. This integration brings a higher level of performance to systems that are required to meet system branding certification by third party algorithm providers. The analog inputs feature a 95 dB dynamic range ADC fed from a 4-stereo input mux. The main speaker outputs can be supplied as a voltage output from the integrated 95 dB dynamic range DAC channels. A dedicated headphone DAC with integrated amplifiers and additional auxiliary analog outputs is also available.

The ADAV400 supports multichannel digital inputs and outputs. An integrated SRC on one channel provides the capability to support any input sample rates in the range from 5 kHz to 50 kHz, synchronizing this input to the internal DSP engine.

The ADAV400 is supported by a powerful graphical programming tool that includes blocks such as general filters, EQ filters, dynamics processing, mixers, volume, and third party algorithms for fast development of custom signal flows.

SPECIFICATIONS

AVDDn[1] = 3.3 V, ODVDD = 3.3 V, DVDD = internal voltage regulator, temperature = 0°C to +70°C, master clock = 12.288 MHz, measurement bandwidth = 20 Hz to 20 kHz, ADC input signal = 1 kHz, DAC output signal = 1 kHz, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
REFERENCE SECTION					
Absolute Voltage V_{REF}		1.5		V	
V_{REF} Temperature Coefficient		130		ppm/°C	
AUX ANALOG INPUTS (SINGLE-ENDED)					
Number of Channels		8			4 stereo channels
Full-Scale Analog Input		100		µA rms	2 V rms input with 20 kΩ series resistor
DC Offset		±10		mV	Relative to V_{REF}
ADC SECTION					Stereo ADC
Resolution		24		Bits	
Dynamic Range					−60 dB with respect to full-scale analog input
A-Weighted	90	95		dB	
Total Harmonic Distortion + Noise		−93		dB	−3 dB with respect to full-scale analog input
Interchannel Gain Mismatch		0.1		dB	Left and right channel gain mismatch
Crosstalk		−78		dB	Analog channel crosstalk (AINYm[1] to AINYm[1])
					One channel = −3 dB, other channel = 0 V
Gain Error		−6		%	
Power Supply Rejection		−83		dB	1 kHz, 300 mV p-p signal at AVDDn[1]
ADC DIGITAL DECIMATOR FILTER CHARACTERISTICS @ 48 kHz					
Pass Band		22.5		kHz	
Pass-Band Ripple		±0.0002		dB	
Transition Band		24		kHz	
Stop Band		26.5		kHz	
Stop-Band Attenuation		100		dB	
Group Delay		1040		µs	
DAC OUTPUTS (SINGLE-ENDED)					DAC amplifier register contents = 0x0010
Number of Channels		8			4 stereo output channels
Resolution		24		Bits	
Full-Scale Analog Output		1		V rms	
Dynamic Range					−60 dB with respect to full-scale code input
A-Weighted	90	95		dB	
Total Harmonic Distortion + Noise[2]		−90		dB	−3 dB with respect to full-scale code input
Crosstalk		−100		dB	Analog channel crosstalk (VOUTm[1] to VOUTm[1])
					One channel = −3 dB, other channels = 0 V
Gain Error		5		%	
Interchannel Gain Mismatch		0.1		dB	Left and right channel gain mismatch
DC Offset		1		mV	Relative to V_{REF}
Power Supply Rejection		−87		dB	1 kHz, 300 mV p-p signal at AVDDn[1]
DAC DIGITAL INTERPOLATION FILTER CHARACTERISTICS @ 48 kHz					
Pass Band		21.769		kHz	
Pass-Band Ripple		±0.01		dB	
Transition Band		23.95		kHz	
Stop Band		26.122		kHz	
Stop-Band Attenuation		75		dB	
Group Delay		580		µs	

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
HEADPHONE OUTPUT (SINGLE-ENDED)					Measured at headphone output with 32 Ω load, headphone amplifier register contents = 0x0001
Number of Channels		2			1 stereo channel
Resolution		24		Bits	
Full-Scale Analog Output		1		V rms	
Dynamic Range					−60 dBFS with respect to full-scale code input
A-Weighted		92		dB	
Total Harmonic Distortion Plus Noise		−84		dB	−3 dBFS with respect to full-scale code input
Gain Error		4		%	
Interchannel Gain Mismatch		0.5		dB	
DC Offset		−200		mV	Relative to V_{REF}
Power Supply Rejection		−84		dB	1 kHz, 300 mV p-p signal at AVDDn[1]
PLL SECTION[3]					
Master Clock Input (MCLKI)	64 × f_S		512 × f_S	MHz	
SRC[3]					
Dynamic Range					−60 dBFS input (worst-case input f_S = 50 kHz)
A-Weighted		115		dB	
Total Harmonic Distortion + Noise		−113		dB	0 dBFS input (worst-case input f_S = 50 kHz)
Sample Rate	5		50	kHz	
DIGITAL INPUT/OUTPUT					
Input Voltage HI (V_{IH})	2.0		ODVDD	V	
Input Voltage LO (V_{IL})			0.8	V	
Input Leakage (I_{IH} @ V_{IH} = ODVDD)			10	µA	
Input Leakage (I_{IL} @ V_{IL} = 0 V)	−60			µA	
Output Voltage HI (V_{OH} @ I_{OH} = 0.4 mA)	2.4			V	
Output Voltage LO (V_{OL} @ I_{OL} = −3.2 mA)			0.4	V	
Input Capacitance		2		pF	
SUPPLIES					
Analog Supplies AVDDn[1]	3.15	3.30	3.45	V	
Digital Supplies DVDD	1.6	1.8	2.0	V	
Interface Supply ODVDD	3.15	3.30	3.45	V	
Supply Current, Normal Mode					MCLK = 12.288 MHz, ADC and DACs active, headphone outputs active and driving a 32 Ω load, Power control register = 0xFFFF
Analog Current (AVDD1)		90	110	mA	
Digital and Interface Current		120	135	mA	
PLL Current		5	6	mA	
Supply Current, Power-Down Mode					$\overline{\text{RESET}}$ low, MCLK = 3.074 MHz, AINx = AGND, DAC and headphone outputs floating
Analog Current		6	8.5	mA	
Digital and Interface Current		1.5	6	mA	
PLL Current		5	50	µA	

[1] In this table, n refers to supply number, m refers to channel number, and Y refers to stereo channel identifier: L for left channel or R for right channel.
[2] Measured on one DAC with other DACs and ADCs off.
[3] Guaranteed by design.

DIGITAL TIMING

Table 2.

Parameter	Min	Max	Unit	Comments
MASTER CLOCK AND RESET				
f_{MCLKI} (MCLKI Frequency)	3.024	24.576	MHz	
t_{MCH} (MCLKI High)	10		ns	
t_{MCL} (MCLKI Low)	10		ns	
t_{RLPW} ($\overline{\text{RESET}}$ Low Pulse Width)	20		ns	
I^2C PORT				
f_{SCL} (SCL Clock Frequency)		400	kHz	
t_{SCLH} (SCL High)	0.6		µs	
t_{SCLL} (SCL Low)	1.3		µs	
Start Condition				
t_{SCS} (Setup Time)	0.6		µs	Relevant for repeated start condition
t_{SCH} (Hold Time)	0.6		µs	The first clock is generated after this period
t_{DS} (Data Setup Time)	100		ns	
t_{SCR} (SCL Rise Time)		300	ns	
t_{SCF} (SCL Fall Time)		300	ns	
t_{SDR} (SDA Rise Time)		300	ns	
t_{SDF} (SDA Fall Time)		300	ns	
STOP CONDITION				
t_{SCSH} (Setup Time)	0.6		µs	
SERIAL PORTS				
Slave Mode				
t_{SBH} (BCLKx High)	40		ns	
t_{SBL} (BCLKx Low)	40		ns	
f_{SBF} (BCLKx Frequency)	$64 \times f_S$			
t_{SLS} (LRCLKx Setup)	10		ns	To BCLK rising edge
t_{SLH} (LRCLKx Hold)	10		ns	From BCLK rising edge
t_{SDS} (SDINx Setup)	10		ns	To BCLK rising edge
t_{SDH} (SDINx Hold)	10		ns	From BCLK rising edge
t_{SDD} (SDOx Delay)		40	ns	From BCLK falling edge
Master Mode				
t_{MLD} (LRCLKx Delay)		5	ns	From BCLK falling edge
t_{MDD} (SDOx Delay)		40	ns	From BCLK falling edge
t_{MDS} (SDINx Setup)	10		ns	From BCLK rising edge
t_{MDH} (SDINx Hold)	10		ns	From BCLK rising edge

Digital Timing Diagrams

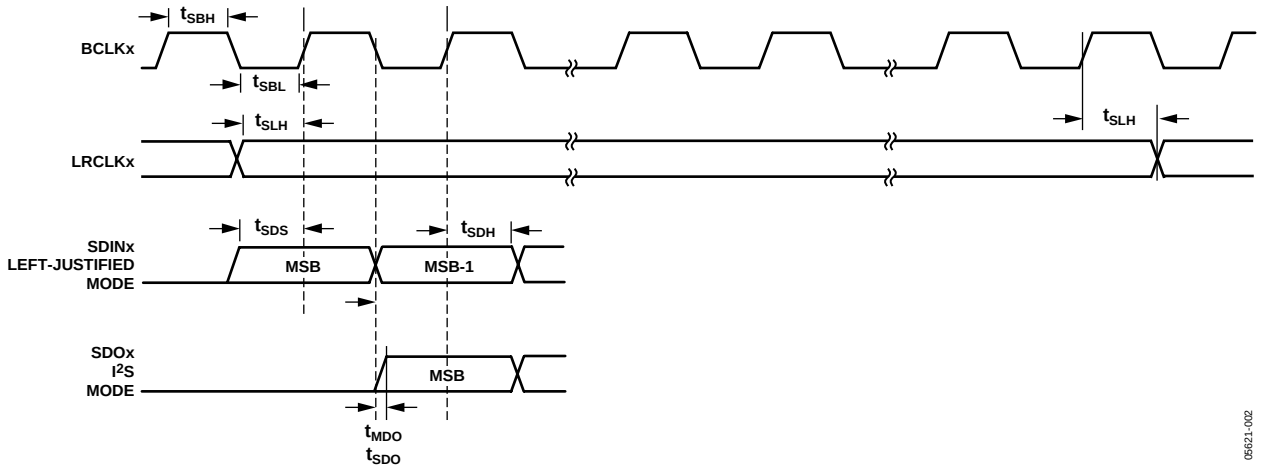


Figure 2. Serial Port Timing

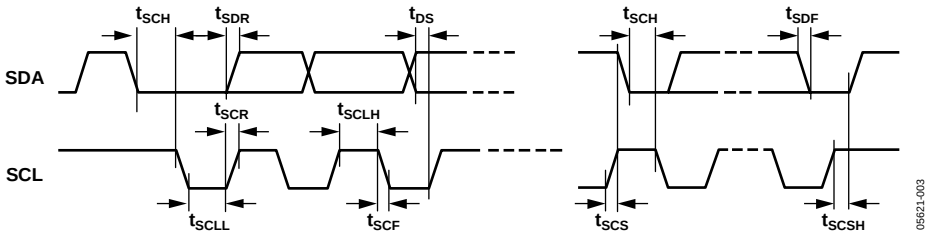


Figure 3. I²C Port Timing

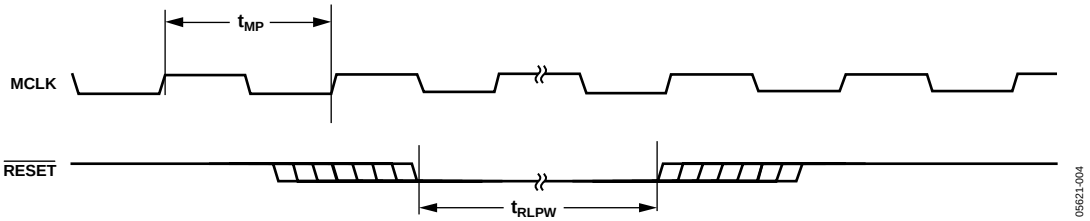


Figure 4. Master Clock and Reset Timing

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
DVDD to DGND	0 V to 2.2 V
ODVDD to DGND	0 V to 4.0 V
AVDD to AGND	0 V to 4.0 V
AGND to DGND	−0.3 V to +0.3 V
Digital Inputs	DGND − 0.3 V to ODVDD + 0.3 V
Analog Inputs	AGND − 0.3 V to ADVDD + 0.3 V
Reference Voltage	Indefinite short-circuit to ground
Soldering (10 sec)	+300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

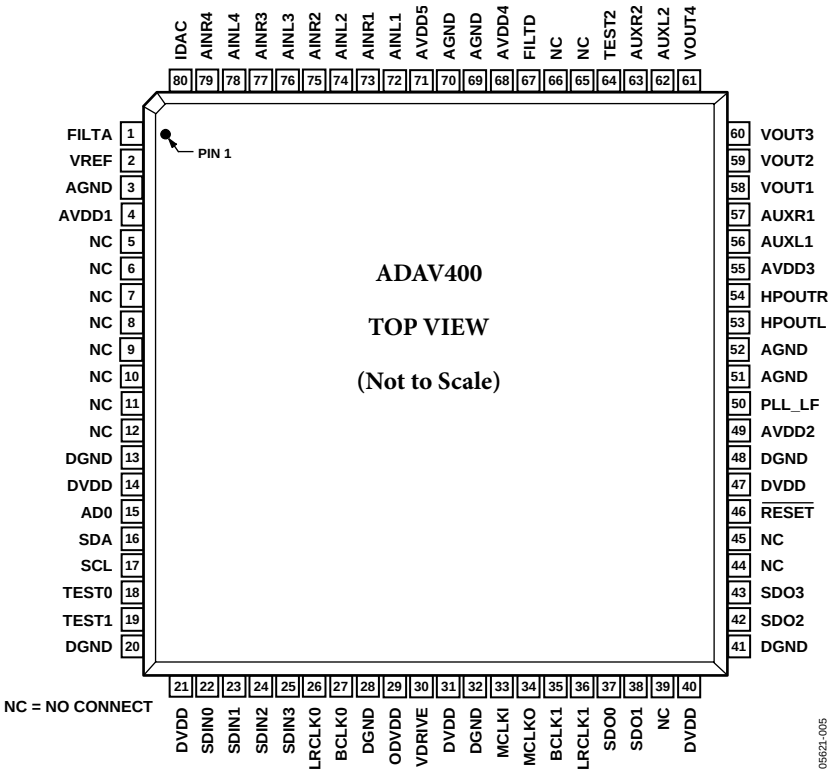


Figure 5. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	I/O	Description
1	FILTA	O	ADC Filter Decoupling Node for the ADC. Decouple this pin with a 47 µF capacitor and 0.1 µF capacitor to AGND.
2	VREF		Voltage Reference. This pin is driven by an internal 1.5 V reference voltage. Decouple this pin with a 47 µF capacitor and 0.1 µF capacitor to AGND.
3	AGND		ADC Ground. Connect this pin to the analog ground plane.
4	AVDD1		Analog Power Supply Pin. Connect this pin to +3.3 V and decouple it with a 47 µF capacitor and 0.1 µF capacitor to AGND as close as possible to the pin.
5 to 12, 39, 44, 45, 65, 66	NC		Not Connected Internally.
13, 20, 28, 32, 41, 48	DGND		Digital Ground. Connect this pin to the digital ground plane.
14, 21, 31, 40, 47	DVDD		Digital Power Supply Pins. Connect these pins to +1.8 V, either directly or by using the on-chip regulator. Decouple each pin with a 47 µF capacitor and 0.1 µF capacitor to DGND as close as possible to the pin.
15	AD0	I	I^2C Address Select. Tie to ODVDD or DGND. This pin selects the address for the communication of the ADAV400 with the control port. This allows two ADAV400s to be used with a single I^2C port.
16	SDA	I/0	Serial Data Input/Output for the I^2C Control Port.
17	SCL	I	Serial Clock for the I^2C Control Port.
18	TEST0		Test Pin. Connect to ODVDD.
19	TEST1		Test Pin. Connect to ODVDD.
22 to 25	SDIN[0:3]	I	Serial Data Inputs. These input pins provide the digital audio data to the signal processing core. Any one of the four inputs can be routed to the SRC for sample rate conversion; however, this input is not available to the core directly, but only as the output of the SRC. The serial format is selected by writing to Bits[2:0] of the input sport control register. The input serial port is always a synchronous slave device. The serial port uses BCLK1 and LRCLK1 from the output serial port as timing signals for SDIN0 to SDIN3.

Pin No.	Mnemonic	I/O	Description
26	LRCLK0	I	Left-Right Clock for SRC. This input frame synchronization signal is associated with the SDIN0 to SDIN3 signals when one of these channels is connected to the SRC.
27	BCLK0	I	Bit Clock for SRC. This input clock is associated with the SDIN0 to SDIN3 signals when one of these channels is connected to the SRC.
29	ODVDD		Digital Interface Supply (3.3 V) Pin. Connect this pin to a +3.3 V digital supply. Decouple the pin with a 47 µF capacitor and 0.1 µF capacitor to AGND as close as possible to the pin.
30	VDRIVE		Drive for External PNP Transistor. The base of the voltage regulator's external PNP transistor is driven from this pin.
33	MCLKI	I	Master Clock Input. The ADAV400 uses a phase-locked loop (PLL) to generate the appropriate internal clock for the DSP core.
34	MCLKO	O	Audio Clock Output. The MCLKO pin can be programmed to output the internal audio clock. This clock can be used elsewhere in the system if it is required to synchronize additional components with the ADAV400. Use Bit 5 to Bit 3 in User Control Register 1 to select the clock on this pin.
35	BCLK1	I/O	Bit Clock for Serial Data Input/Output. This clock and the LRCLK1 are used as clock and frame sync signals for the SDINx and SDOx pins. These clocks are inputs to the ADAV400 when the port is configured as a slave and outputs when the port is configured as a master. On power up, these pins are set to slave mode to avoid conflicts with external master mode devices.
36	LRCLK1	I/O	Left-Right Clock for Serial Data Input/Output. This clock and the BCLK1 are used as clock and frame sync signals for the SDINx and SDOx pins. These clocks are inputs to the ADAV400 when the port is configured as a slave and outputs when the port is configured as a master. On power up, these pins are set to slave mode to avoid conflicts with external master mode devices.
37, 38, 42, 43	SDO[0:3]	0	Serial Data/TDM/Data Outputs. Use these pins for serial digital outputs. For non-TDM systems, these pins can output four channels of digital audio using a variety of standard two-channel formats. The configuration of the output port is set by the output sport control register.
46	$\overline{\text{RESET}}$	I	Active Low Reset Signal. After $\overline{\text{RESET}}$ goes high, all the circuit blocks of the ADAV400 are powered down. Individually power up the blocks by programming the appropriate bits in the power control register. When the audio processor core is powered up, it takes 3,072 MCLK cycles to initialize the internal circuitry. Do not attempt to load a new program during this period. When the core is powered up, it takes approximately 32,768 MCLK periods to initialize the data RAM. The data RAM is not available during this time.
49	AVDD2		Analog Power Supply Pin for the PLL. Connect this pin to +3.3 V and decouple it with a 47 µF capacitor and 0.1 µF capacitor to AGND as close as possible to the pin.
50	PLL_LF		PLL Loop Filter. External components are required to allow the PLL to function correctly. See the PLL Block section for details of these components.
51	AGND		PLL Ground. Connect this pin to the analog ground plane.
52	AGND		Headphone Driver Ground. Connect this pin to the analog ground plane.
53	HPOUTL	O	Left Headphone Output. Analog output from the headphone amplifiers.
54	HPOUTR	O	Right Headphone Output. Analog output from the headphone amplifiers.
55	AVDD3		Analog Power Supply Pin for the Headphone Driver. Connect this pin to +3.3 V and decouple it with a 47 µF capacitor and 0.1 µF capacitor to AGND as close as possible to the pin.
56	AUXL1	O	Auxiliary DAC Output Left 1. Analog output from the on-chip auxiliary DACs.
57	AUXR1	O	Auxiliary DAC Output Right 1. Analog output from the on-chip auxiliary DACs.
58 to 61	VOUT[1:4]	O	Main DAC Output 1 to Output 4. Analog outputs from the on-chip DACs.
62	AUXL2	O	Auxiliary DAC Output Left 2. Analog output from the on-chip auxiliary DACs.
63	AUXR2	O	Auxiliary DAC Output Right 2. Analog output from the on-chip auxiliary DACs.
64	TEST2		Test Pin. This pin should be left unconnected.
67	FILTD		DAC Filter Decoupling Node. Decouple this pin with a 47 µF capacitor and 0.1 µF capacitor to AGND.
68	AVDD4		Analog Power Supply Pin for the DAC. Connect this pin to +3.3 V and decouple it with a 47 µF capacitor and 0.1 µF capacitor to AGND as close as possible to the pin.
69, 70	AGND		DAC Ground. Connect this pin to the analog ground plane.
71	AVDD5		Analog Power Supply Pin for the DAC. Connect this pin to +3.3 V and decouple it with a 47 µF capacitor and 0.1 µF capacitor to AGND as close as possible to the pin.
72, 74, 76, 78	AINL[1:4]	I	Left Analog Input 1 to Input 4. The analog inputs are current inputs driven via a 20 kΩ resistor as shown in Figure 17.
73, 75, 77, 79	AINR[1:4]	I	Right Analog Input 1 to Input 4. The analog inputs are current inputs driven via a 20 kΩ resistor as shown in Figure 17.
80	IDAC		DAC External Bias Resistor. This is an external bias pin for the DAC circuitry. Connect a 20 kΩ resistor between this pin and AGND.

TYPICAL PERFORMANCE CHARACTERISTICS

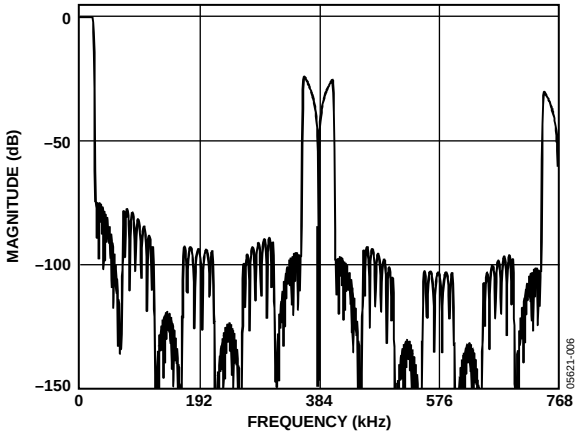


Figure 6. DAC Composite Filter Response (48 kHz)

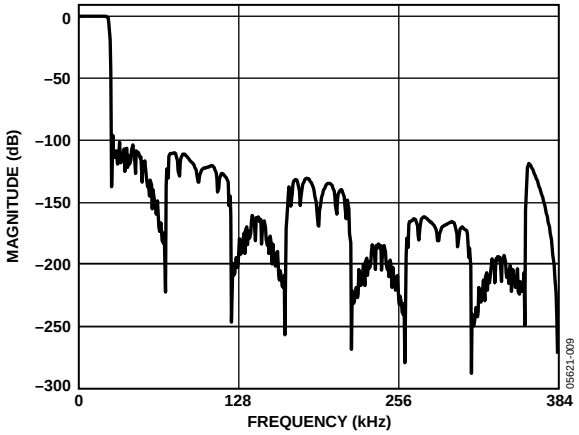


Figure 9. ADC Composite Filter Response (48 kHz)

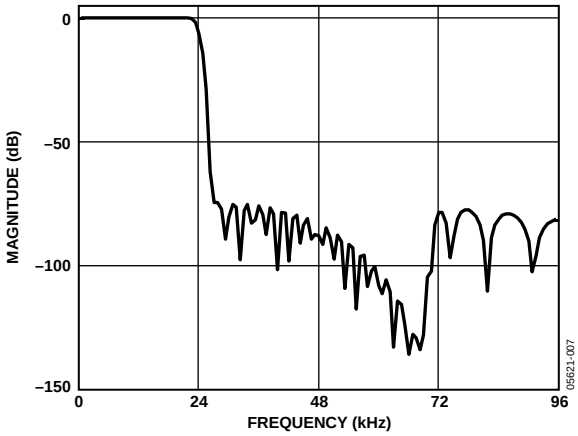


Figure 7. DAC Pass-Band Filter Response (48 kHz)

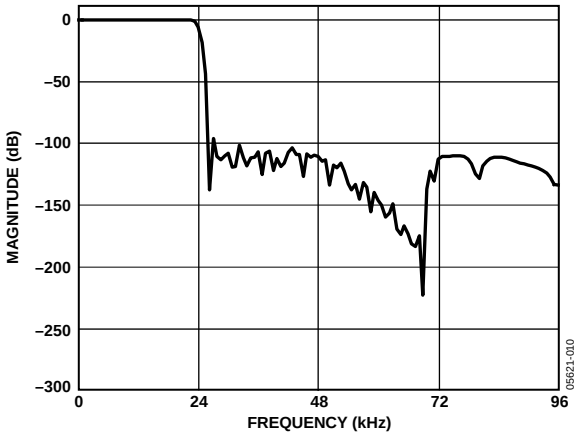


Figure 10. ADC Pass-Band Filter Response (48 kHz)

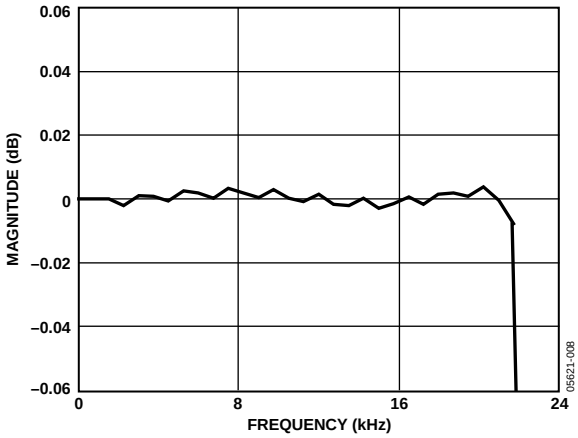


Figure 8. DAC Pass-Band Ripple (48 kHz)

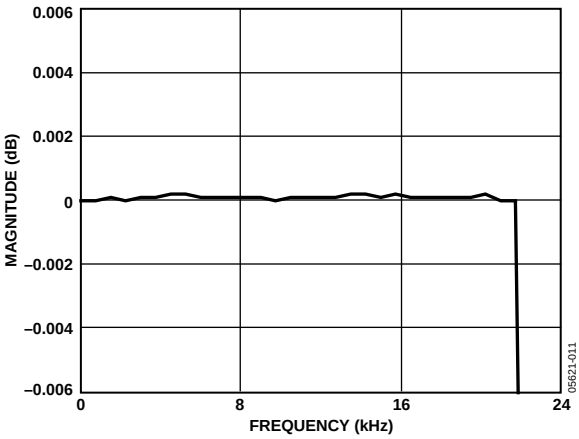


Figure 11. ADC Pass-Band Ripple (48 kHz)

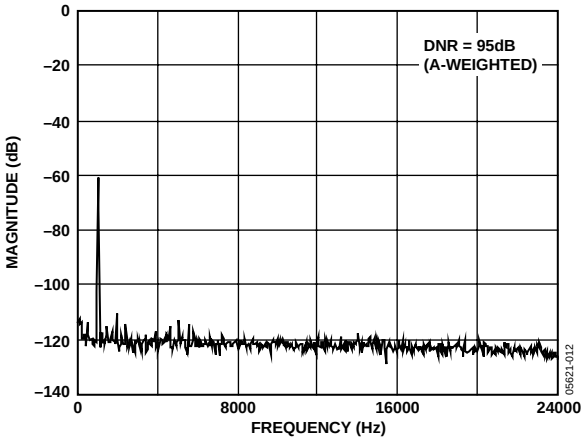


Figure 12. DAC Dynamic Range

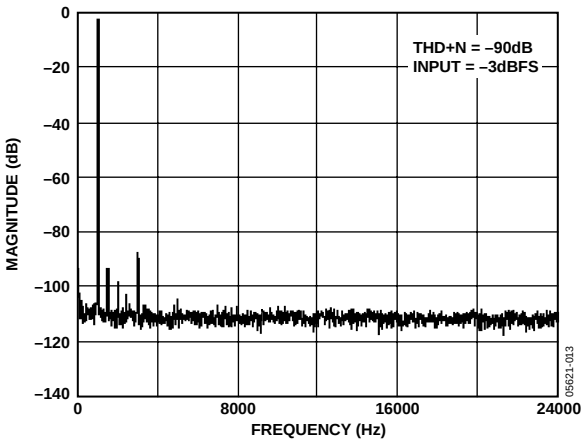


Figure 13. DAC Total Harmonic Distortion+ Noise

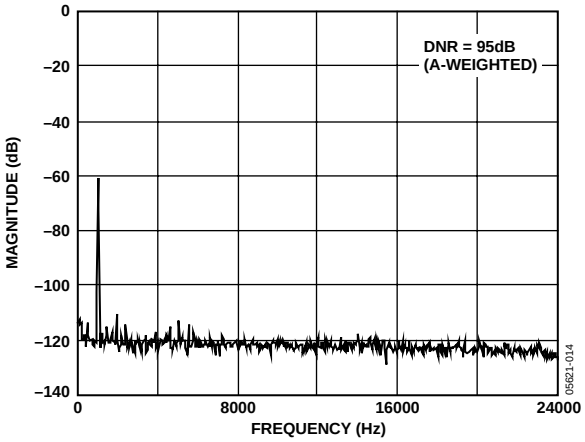


Figure 14. ADC Dynamic Range

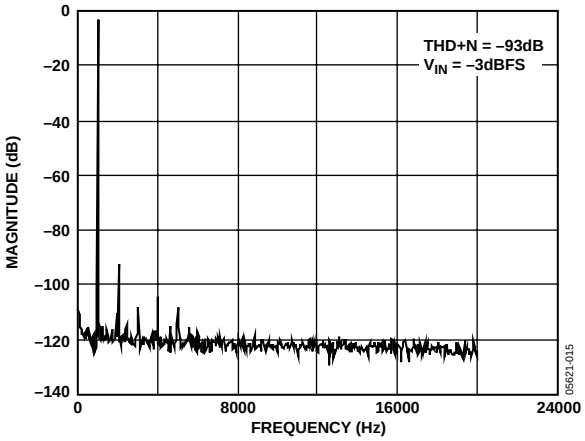


Figure 15. ADC Total Harmonic Distortion + Noise

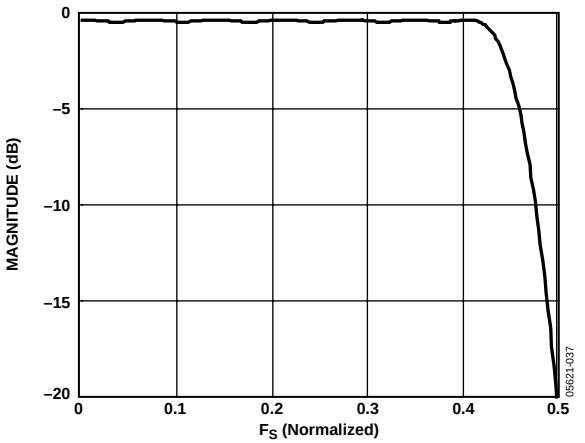


Figure 16. Sample Rate Converter Transfer Function

THEORY OF OPERATION

The ADAV400 is an enhanced audio processor containing an Analog Devices SigmaDSP digital processing core. The digital processor accepts digital inputs from up to four stereo channels, typically operating at 48 kHz. A sample rate converter (SRC) is included, allowing a single stereo channel that is not sampled at 48 kHz to be converted to 48 kHz before being processed. In addition, any of the four stereo analog sources can be processed by converting them to digital data via the high performance on-chip ADC. Processed data is available in digital form as a standard audio stream such as I^2S or left/right justified. The processed audio data can also be converted to analog form by using the four high performance on-chip stereo DACs.

The core of the ADAV400 is a 28-bit DSP (56-bit with double precision), optimized for audio processing. Signal processing parameters are stored in a 1024-location parameter RAM. The program RAM can be loaded with a custom program after power-up. New values are written to the program and parameter RAM using the control port. The values stored in the parameter RAM control individual signal processing blocks, such as IIR equalization filters, dynamics processors, audio delays, and mixer levels. A safeload feature allows transparent updating of the parameters without causing clicks on the output signals.

The target/slew RAM contains 64 locations that can be used as channel volume controls or for other parameter updates. These RAM locations take a target value for a given parameter and ramp the current parameter value to the new value using a specified time constant and one of a selection of linear or logarithmic curves.

The ADAV400 has a sophisticated control port that supports complete read/write capability of all memory locations except the target/slew RAM.

The ADAV400 has very flexible serial data input/output ports that allow for glueless interconnection to a variety of ADCs, DACs, general-purpose DSPs, S/PDIF receivers, and sample rate converters. The digital inputs and outputs of the ADAV400 can be configured in I^2S, left-justified or right-justified, or TDM serial port-compatible modes. It can support 16, 20, and 24 bits in all modes. The ADAV400 accepts serial audio data in MSB first and twos complement formats.

The digital core of ADAV400 operates at 1.8 V and the other circuit blocks operate from a 3.3 V power supply. An on-board regulator allows a single 3.3 V supply for both digital supplies using the configuration shown in Figure 20.

The ADAV400 is fabricated on a single monolithic integrated circuit and is housed in an 80-lead LQFP package for operation over the −40°C to +105°C automotive temperature range.

ANALOG INPUT MULTIPLEXER

The ADAV400 has eight analog input channels arranged as four stereo pairs. Any one of these stereo channels can be connected to a high performance ADC. The digital output of the ADC is then used by the audio processor core. The ADC multiplexer is controlled by Bit 3 to Bit 0 of the ADC input mux register. Set only one of these bits at a time. The ADC, ADC digital engine, and reference buffer must be powered up to use the ADC. This is achieved by setting Bit 14 and Bit 13 to 1 in the power control register. The analog input is a current input by default, but can be converted to a voltage input by using series resistors, as shown in Figure 17.

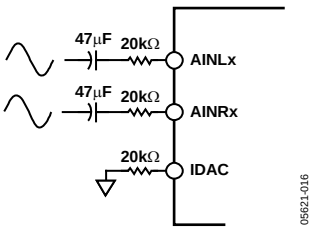


Figure 17. Analog Input Configuration

SAMPLE RATE CONVERTER BLOCK

The ADAV400 contains an SRC, allowing input sample rates other than 48 kHz to be used as digital inputs. The SRC is powered up by setting the SRC bit in the power control register (see Table 36). To use the SRC, the user programs Bit 6 and Bit 5 in the SRC serial port control register (see Table 34) to select which one of the four SDIN channels is connected to the input of the SRC. Using the SRC implies that one of the SDIN inputs is at a sample rate other than the default 48 kHz, therefore, it should not be used by the audio processor core. To prevent this input from being available to the core, set the SRC mux enable bit in the User Control Register 1. This bit enables the SRC input multiplexer and masks the selected input so that it is not available to the audio processor core. When the SRC mux enable bit is 0, SDIN3 appears at the output of the SRC. Figure 18 shows how the SRC block is configured. Note that the SRC has a filter cutoff frequency of 20 kHz for a 48 kHz sample rate. If a different sample rate is used, the cutoff frequency scales accordingly.

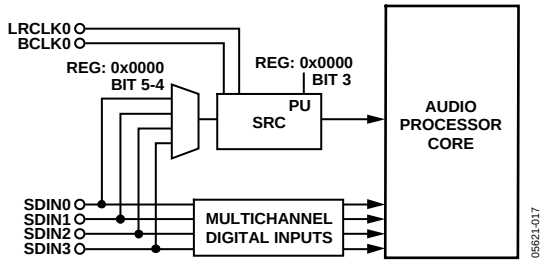


Figure 18. SRC Input Configuration

PLL BLOCK

The ADAV400 contains a phase-locked loop (PLL) that generates all the clocks required by the system from a single input source. An input clock source is required. The clock frequency can be 64 × f_S, 128 × f_S, 256 × f_S, or 512 × f_S. Program Bit 2 and Bit 1 in User Control Register 1 for the appropriate clock frequency to ensure that the correct clock frequencies are generated. The PLL is powered down by default; Bit 15 in the power control register must be set to use the PLL (see Table 36). Bit 0 of User Control Register 1 determines whether the PLL is used (see Table 38). This bit is cleared after a reset, indicating that the PLL is not used and the clock on the MCLKI pin is used by the audio processing core. This allows the user to write to the part while the PLL is off. Power-up the PLL and set Bit 0 of User Control Register 1 to enable the PLL to generate all the clocks required for normal operation.

The PLL requires some external components to operate correctly. These components, shown in Figure 19, form a loop filter that integrates the current pulses from a charge pump and produces a voltage to tune the VCO. A good quality capacitor, such as polyphenylene sulfide (PPS) film, is recommended.

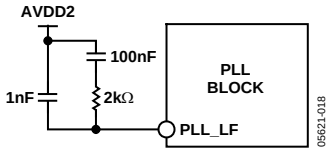


Figure 19. PLL Loop Filter Components

A 3.3 V analog supply, connected to AVDD2, is required to operate the PLL. Where the supply for AVDD1 is also used for the PLL, additional filtering is recommended to prevent digital noise created by the PLL block being coupled to the analog circuitry powered by the AVDD1 supply.

ANALOG OUTPUTS

The ADAV400 contains eight high performance DACs arranged as four stereo pairs. The DACs are the main outputs from the audio processor core. One pair of DACs are connected to integrated headphone amplifiers, although the outputs are also available on the AUXL1 and AUXR1 pins. Each stereo DAC has independent power control and is powered down by default. Power up the DACs by setting the appropriate bit in the power control register. Note that the output of the DAC section forms an inverting amplifier; thus, for a positive full-scale digital code, the DAC generates a negative full-scale signal. If required, this can be inverted in the audio flow. The headphone amplifiers are also inverting amplifiers thereby correcting the inversion for the headphone outputs.

HEADPHONE AMPLIFIER

The ADAV400 has an integrated stereo headphone amplifier that is capable of driving a 32 Ω load. The headphone amplifier is internally connected to the output of Auxiliary DAC 1. The amplifiers are powered down by default and powered up by setting Bit 4 and Bit 3 in the power control register. Auxiliary DAC 1 also needs to be powered up when the headphone amplifier is required. The outputs of the headphone amplifiers use the same RC filters as the VOUT pins (see Figure 37).

VOLTAGE REGULATOR

The ADAV400 includes an on-chip voltage regulator that allows the chip to be used in systems where a 1.8 V supply is not available, but a 3.3 V supply is. The only external components needed are a PNP transistor (such as an FZT953), a single capacitor, and a single resistor. The recommended design for the voltage regulator is shown in Figure 20. The 10 µF capacitor shown in this schematic is recommended for decoupling, but is not necessary for operation. Here, VDD is the main system voltage (3.3 V). A voltage of 1.8 V is generated at the transistor's collector that is connected to the DVDD pins. The reference voltage on VDRIVE is 2.6 V and is generated by the regulator. VDRIVE is connected to the base of the PNP transistor. Connect a 1 kΩ resistor between VDRIVE and VDD.

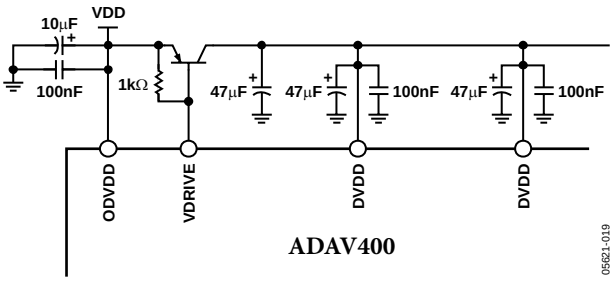


Figure 20. Voltage Regulator Design

There are two specifications to take into consideration when choosing a regulator transistor. First, the transistor's current amplification factor (h_{FE} or beta) should be at least 100. Second, the transistor's collector needs to be able to dissipate the heat generated when regulating from 3.3 V to 1.8 V. The maximum digital current draw of the ADAV400 is 135 mA. The equation for the minimum power dissipation is as follows:

(3.3 V – 1.8 V) × 135 mA = 202.5 mW

If the regulator is not used in the design, tie VDRIVE to ground.

SIGNAL PROCESSING

The ADAV400 is designed to provide all signal processing functions commonly used in stereo or multichannel playback systems. The signal processing flow is set by the software supplied by Analog Devices, which allows graphical entry and real-time control of all signal processing functions.

Many of the signal processing functions are coded using full, 56-bit double-precision arithmetic. The input and output word lengths are 24 bits. Four extra headroom bits are used in the processor to allow internal gains of up to 24 dB without clipping. Additional gains are achieved by initially scaling down the input signal in the signal flow.

The signal processing blocks can be arranged in a custom program that is loaded to the RAM of the ADAV400. The available signal processing blocks are explained in the Numeric Formats and Programming sections.

NUMERIC FORMATS

It is common in DSP systems to use a standardized method of specifying numeric formats. Fractional number systems are specified by an A.B format, where A is the number of bits to the left of the decimal point and B is the number of bits to the right of the decimal point.

The ADAV400 uses the same numeric format for both the coefficient values (stored in the parameter RAM) and the signal data values.

Numeric Format: 5.23

Range: −16.0 to (+16.0 − 1 LSB)

Examples:
1000 0000 0000 0000 0000 0000 0000 = −16.0
1110 0000 0000 0000 0000 0000 0000 = −4.0
1111 1000 0000 0000 0000 0000 0000 = −1.0
1111 1110 0000 0000 0000 0000 0000 = −0.25
1111 1111 1111 1111 1111 1111 1111 = (1 LSB below 0.0)
0000 0000 0000 0000 0000 0000 0000 = 0.0
0000 0010 0000 0000 0000 0000 0000 = +0.25
0000 1000 0000 0000 0000 0000 0000 = +1.0
0010 0000 0000 0000 0000 0000 0000 = +4.0
0111 1111 1111 1111 1111 1111 1111 = (+16.0 − 1 LSB)

The serial port accepts up to 24 bits on the input and is sign-extended to the full 28 bits of the core. This allows internal gains of up to 24 dB without encountering internal clipping.

A digital clipper circuit is used between the output of the DSP core and the serial output ports (see Figure 21). This clips the top four bits of the signal to produce a 24-bit output with a range of +1.0 (− 1 LSB) to −1.0.

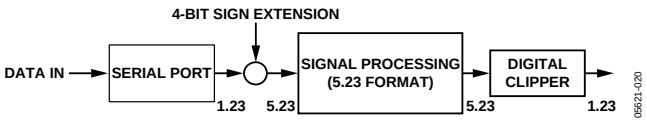


Figure 21. Numeric Precision and Clipping Structure

PROGRAMMING

On power-up, the default program of the ADAV400 passes the unprocessed input signals to the outputs, but the outputs are muted by default. There are 2,560 instruction cycles per audio sample. This DSP runs in a stream-oriented manner, meaning all 2,560 instructions are executed each sample period. The ADAV400 can also be set up to accept double- or quad-speed inputs by reducing the number of instructions per sample. This reduction is set in the audio core control register.

The part is easily programmed using graphical tools provided by Analog Devices. No knowledge of writing DSP code is needed to program the ADAV400. Simply connect graphical blocks such as biquad filters, dynamics processors, mixers, and delays in a signal flow schematic. The schematic is then compiled, and the program and parameter files are loaded into the program RAM of the ADAV400 through the control port. Signal processing blocks available in the provided libraries include:

- Single and double precision bi-quad filters
- Mono- and multi-channel dynamics processors
- Mixers and splitters
- Tone and noise generators
- First-order filters
- Fixed and variable gain
- RMS look-up tables
- Loudness
- Delay
- Stereo enhancement (Phat Stereo™)
- Dynamic bass boost
- Interpolators and decimators

Additional blocks are always in development. Analog Devices also provides proprietary and third-party algorithms for applications such as matrix decoding, bass enhancement, and surround virtualizers. Contact Analog Devices for information about licensing these algorithms.

CONTROL PORT

The ADAV400 has many different control options that can be set through an I²C interface. The ADAV400 uses a 2-wire I²C bus control port. Most signal processing parameters are controlled by writing new values to the parameter RAM using the control port. Other functions, such as mute and input/output mode control, are programmed by writing to the control registers.

The control port is capable of full read/write operation for all memories and registers. All addresses can be accessed in either single-address or burst mode. A control word consists of the chip address, the register/RAM subaddress, and the data to be written. The number of bytes per word depends on the type of data that is written.

The first byte of a control word (Byte 0) contains the 7-bit chip address plus the R/$\overline{W}$ bit. The next two bytes (Byte 1 and Byte 2) together form the subaddress of the memory or register location within the ADAV400. This subaddress must be two bytes because the memories within the ADAV400 are directly addressable and their sizes exceed the range of single-byte addressing. All subsequent bytes (Byte 3, Byte 4, and so on) contain data such as control port, program, or parameter data. The exact formats for specific types of writes are listed in Table 17 to Table 26.

The ADAV400 has several mechanisms for updating signal processing parameters in real time without causing pops or clicks. In cases where large blocks of data need to be downloaded, halt the output of the DSP core using Bit 9 of the audio core control register, load the new data, and then restart the core. This is typically done during the booting sequence at start-up, or when loading a new program into RAM. In cases where only a few parameters need to be changed, they can be loaded without halting the program. To avoid unwanted side effects while loading parameters on the fly, the SigmaDSP provides safeload registers. The safeload registers buffer a full set of parameters (such as the five coefficients of a biquad), and then transfer these parameters into the active program within one audio frame. The safeload mode uses internal logic to prevent contention between the DSP core and the control port.

I²C PORT

The ADAV400 supports a 2-wire serial (I²C-compatible) microprocessor bus driving multiple peripherals. Two pins, serial data (SDA) and serial clock (SCL), carry information between the ADAV400 and the system I²C master controller. The ADAV400 is always a slave on the I²C bus, which means that it never initiates a data transfer. Each slave device is recognized by a unique address.

The ADAV400 has four possible slave addresses, two for writing operations and two for reading. These are unique addresses for the device and are illustrated in Table 5. The LSB of the byte sets either a read or a write operation; Logic Level 1 corresponds to a read operation and Logic Level 0 corresponds to a write operation. The seventh bit of the address is set by tying the AD0 pin of the ADAV400 to Logic Level 0 or Logic Level 1.

Table 5. I²C Addresses

AD0	R/$\overline{W}$	Slave Address
0	0	0x28
0	1	0x29
1	0	0x2A
1	1	0x2B

Addressing

Initially, all devices on the I²C bus are in an idle state wherein the devices monitor the SDA and SCL lines for a start condition and the proper address. The I²C master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA while SCL remains high. This indicates that an address/data stream follows. All devices on the bus respond to the start condition and read the next byte (7-bit address + R/$\overline{W}$ bit) MSB-first. The device that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This ninth bit is known as an acknowledge bit. All other devices withdraw from the bus at this point and return to the idle condition. The R/$\overline{W}$ bit determines the direction of the data. A Logic Level 0 on the LSB of the first byte means the master writes information to the peripheral. A Logic Level 1 on the LSB of the first byte means the master reads information from the peripheral. A data transfer takes place until a stop condition is encountered. A stop condition occurs when SDA transitions from low to high while SCL is held high. Figure 22 shows the timing of an I²C write.

Burst mode addressing, where the subaddresses are automatically incremented at word boundaries, can be used for writing large amounts of data to contiguous memory locations. This increment happens automatically if a stop condition is not encountered after a single word write. The registers and memories in the ADAV400 range in width from one to six bytes, so the auto-increment feature knows the mapping between subaddresses and the word length of the destination register (or memory location). A data transfer is always terminated by a stop condition.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, these cause an immediate jump to the idle condition. During a given SCL high period, the user should only issue one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the ADAV400 does not issue an acknowledge and returns to the idle condition. If the user exceeds the highest subaddress while in auto-increment mode, one of two actions is taken. In read mode, the ADAV400 outputs the highest subaddress register contents until the master device issues a no acknowledge,

indicating the end of a read. A no acknowledge condition is where the SDA line is not pulled low on the ninth clock pulse on SCL. If the highest subaddress location is reached while in write mode, the data for the invalid byte is not loaded into any subaddress register, a no acknowledge is issued by the ADAV400, and the part returns to the idle condition.

I²C Read and Write Operations

Table 6 shows the timing of a single word write operation. Every ninth clock, the ADAV400 issues an acknowledge by pulling SDA low.

Table 7 shows the timing of a burst mode write sequence. This table shows an example where the target destination registers are two bytes. The ADAV400 knows to increment its subaddress register every two bytes because the requested subaddress corresponds to a register or memory area with a 2-byte word length.

The timing of a single word read operation is shown in Table 8. Note that the first R/$\overline{W}$ bit is still a 0, indicating a write operation. This is because the subaddress still must be written in order to set up the internal address. After the ADAV400 acknowledges the receipt of the subaddress, the master must issue a repeated start command followed by the chip address byte with the R/$\overline{W}$ set to 1 (read). This causes the SDA of the ADAV400 to turn around and begin driving data back to the master. The master then responds every ninth clock with an acknowledge pulse to the ADAV400.

Table 9 shows the timing of a burst mode read sequence. This table shows an example where the target read registers are two bytes. The ADAV400 knows to increment its subaddress register every two bytes because the requested subaddress corresponds to a register or memory area with word lengths of two bytes. Other address ranges may have a variety of word lengths ranging from one to six bytes; the ADAV400 always decodes the sub-address and sets the auto-increment circuit so that the address increments after the appropriate number of bytes.

Key for Table 6 to Table 9:

S = start bit
P = stop bit
AM = acknowledge by master
AS = acknowledge by slave

Table 6. Single Word I²C Write

S	Chip Address, R/$\overline{W}$ = 0	AS	Subaddress High	AS	Subaddress Low	AS	Data Byte 1	AS	Data Byte 2	…	AS	Data Byte N	**P**

Table 7. Burst Mode I²C Write

S	Chip Address, R/$\overline{W}$ = 0	AS	Subaddress High	AS	Subaddress Low	AS	Data-Word 1 Byte 1	AS	Data-Word 1 Byte 2	AS	Data-Word 2 Byte 1	AS	Data-Word 2 Byte 2	AS	…	**P**

Table 8. Single Word I²C Read

S	Chip Address, R/$\overline{W}$ = 0	AS	Subaddress High	AS	Subaddress Low	AS	S	Chip Address R/$\overline{W}$ = 1	AS	Data Byte 1	AM	Data Byte 2	…	AM	Data Byte N	**P**

Table 9. Burst Mode I²C Read

S	Chip Address, R/$\overline{W}$ = 0	AS	Subaddress High	AS	Subaddress Low	AS	S	Chip Address R/$\overline{W}$ = 1	AS	Data-Word 1 Byte 1	AM	Data-Word 1 Byte 2	AM	…	**P**

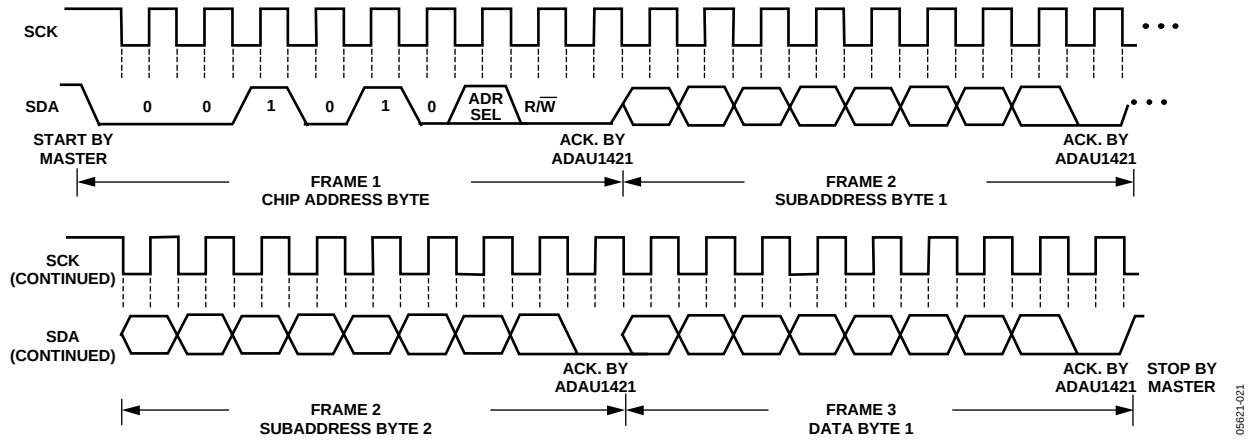


Figure 22. I²C Write Format

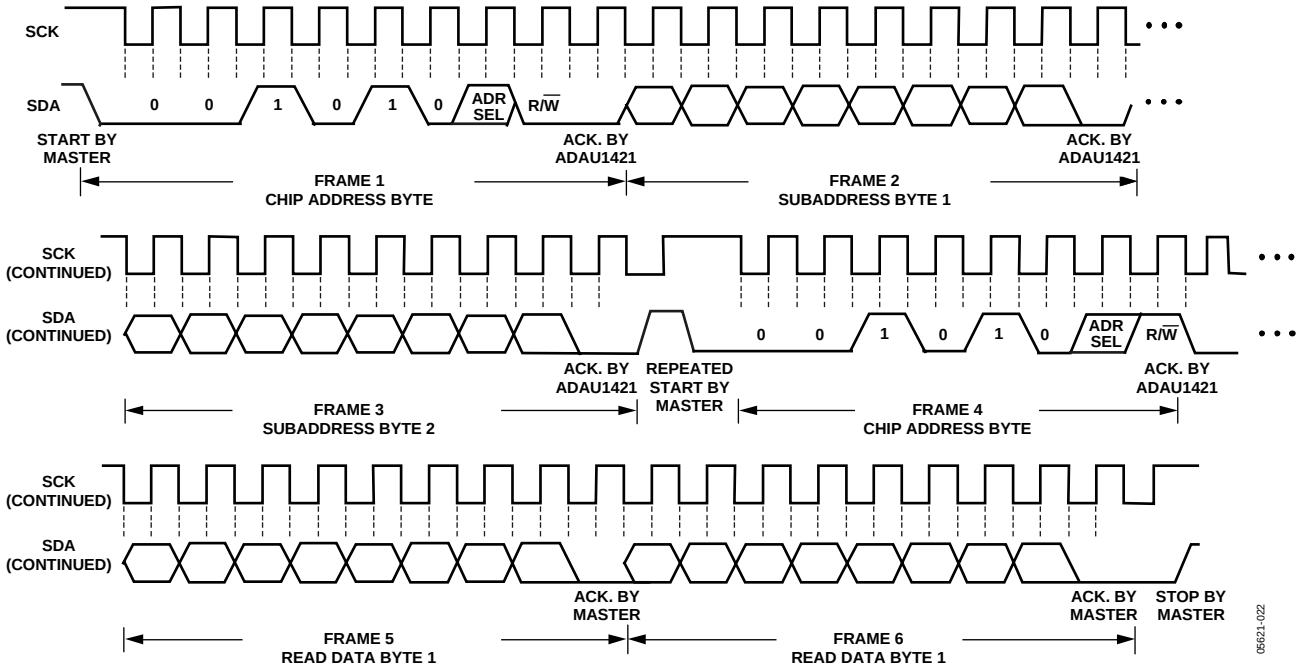


Figure 23. I²C Read Format

RAMS AND REGISTERS

Table 10. Control Port Addresses

I²C Subaddress	Register Name	Read/Write Word Length
0 to 1023 (0x0000 to 0x03FF)	Parameter RAM	Write: 4 Bytes, Read: 4 Bytes
1024 to 4095 (0x0400 to 0x0FFF)	Program RAM	Write: 6 Bytes, Read: 6 Bytes
4096 to 4159 (0x1000 to 0x103F)	Target/Slew RAM	Write: 5 Bytes, Read: N/A
4160 to 4164 (0x1040 to 0x1044)	Parameter RAM Data Safeload Register[0: 4]	Write: 5 Bytes, Read: N/A
4165 to 4169 (0x1045 to 0x1049)	Parameter RAM Indirect Address Safeload Register[0:4]	Write: 2 Bytes, Read: N/A
4170 to 4175 (0x104A to 0x104F)	Data Capture Register[0:5] (Control Port Readback)	Write: 2 Bytes, Read: 3 Bytes
4176 to 4177 (0x1050 to 0x1051)	Data Capture Registers (Digital Output)	Write: 2 Bytes, Read: N/A
4178 (0x1052)	Audio Core Control Register	Write: 2 Bytes, Read: 2 Bytes
4179 (0x1053)	RAM Modulo Control Register	Write: 1 Byte, Read: 1 Byte
4180 (0x1054)	Serial Output Control Register	Write: 2 Bytes, Read: 2 Bytes
4181 (0x1055)	Serial Input Control Register	Write: 1 Byte, Read: 1 Byte
4182 (0x1056)	SRC Serial Port Control Register	Write: 1 Byte, Read: 1 Byte
4183 (0x1057)	ADC Input Mux Control Register	Write: 2 Bytes, Read: 2 Bytes
4184 (0x1058)	Power Control Register	Write: 2 Bytes, Read: 2 Bytes
4185 (0x1059)	User Control 1 Register	Write: 2 Bytes, Read: 2 Bytes
4186 (0x105A)	User Control 2 Register	Write: 2 Bytes, Read: 2 Bytes
4365 (0x110D)	DAC Amplifier Register	Write: 2 Bytes, Read: 2 Bytes

Table 11. RAM Read/Write Modes

Memory	Size	Subaddress Range	Read	Write	Burst Mode Available	Write Modes
Parameter RAM	1024 × 28	0 to 1023 (0x0000 to 0x03FF)	Yes	Yes	Yes	Direct Write[1], Safeload Write
Program RAM	2560 × 42	1024 to 3584 (0x0400 to 0x0E00)	Yes	Yes	Yes	Direct Write[1]
Target/Slew RAM	64 × 34	4096 to 4159 (0x1000 to 0x1044)	No	Yes	No	Safeload Write

[1] To avoid clicks or pops, shut down the DSP core first.

CONTROL PORT ADDRESSING

Table 10 shows the addressing of the RAM and register spaces of the ADAV400. The address space encompasses a set of registers and three RAMs; one each for holding signal processing parameters, holding the program instructions, and ramping parameter values. The program and parameter RAMs initialize on power-up. Table 11 lists the sizes and available writing modes of the parameter, program, and target/slew RAMs.

PARAMETER RAM CONTENTS

The parameter RAM is 28 bits wide and occupies Address 0 to Address 1023. The parameter RAM is initialized to all 0s on power-up. The data format of the parameter RAM is twos complement 5.23. This means that the coefficients can range from +16.0 (− 1 LSB) to −16.0, with 1.0 represented by the binary word 0000 1000 0000 0000 0000 0000 0000.

Options for Parameter Updates

The parameter RAM can be written and read using one of the two following methods:

1. **Direct Read/Write**. This method allows direct access to the program and parameter RAMs. This mode of operation is normally used during a complete new load of the RAMs using burst mode addressing. To avoid clicks or pops in the outputs, set the clear registers bit in the audio core control register to 0. It is also possible to use this mode during live program execution. However, because there is no hand-shaking between the core and the control port, the parameter RAM is unavailable to the DSP core during control writes, resulting in clicks and pops in the audio stream.

2. **Safeload Write.** Up to five safeload registers can be loaded with parameter RAM address data. The data is transferred to the requested address when the RAM is not busy. Use this method for dynamic updates while live program material is playing through the ADAV400.

For example, a complete update of one biquad section can occur in one audio frame while the RAM is not busy. This method is not available for writing to the program RAM or control registers. The following sections discuss these two options in more detail.

RECOMMENDED PROGRAM/PARAMETER LOADING PROCEDURES

When writing large amounts of data to the program or parameter RAM in direct write mode, disable the processor core to prevent unpleasant noises from appearing at the audio output. The ADAV400 contains several mechanisms for disabling the core.

If the loaded program does not use the target/slew RAM as the main system volume control (for example, the default power-up program):

1. Assert Bit 9 (low to assert—default setting) and Bit 6 (high to assert) of the audio control register. This zeroes the accumulators, the serial output registers, and the serial input registers.
2. Fill the program RAM using burst mode writes.
3. Fill the parameter RAM using burst mode writes.
4. Assert Bit 7 of the audio control register to initiate a data memory clear sequence. Wait at least 100 µs for this sequence to complete. This bit is automatically cleared after the operation is complete.
5. Deassert Bit 9 and Bit 6 of the audio control register to allow the core to begin normal operation

If the loaded program does use the target/slew RAM as the main system volume control:

1. Assert Bit 12 of the audio control register. This begins a volume ramp down, with a time constant determined by the upper bits of the target RAM. Wait for this ramp-down to complete (the user can poll Bit 13 of the audio control register, or simply wait for a given amount of time).
2. Assert Bit 9 (low to assert) and Bit 6 (high to assert) of the audio control register. This zeroes the accumulators, the serial output registers, and the serial input registers.
3. Fill the program RAM using burst mode writes.
4. Fill the parameter RAM using burst mode writes.
5. Assert Bit 7 of the audio control register to initiate a data memory clear sequence. Wait at least 100 µs for this sequence to complete. This bit is automatically cleared after the operation is complete.
6. Deassert Bit 9 and Bit 6 of the audio control register.
7. If the newly loaded program also uses the target/slew RAM, deassert Bit 12 of the audio control register to begin a volume ramp-up procedure.

TARGET/SLEW RAM

The target/slew RAM is a bank of 64 RAM locations, each of which can each be set to autoramp from one value to a desired final value in one of four modes.

Summary

When a program is loaded into the program RAM using one or more locations in the slew RAM to access internal coefficient data, the target/slew RAM is used by the DSP. Typically, these coefficients are used for volume controls or smooth cross-fading effects, but can be used to update any value in the parameter RAM. Each of the 64 locations in the slew RAM are linked to corresponding locations in the target RAM. When a new value is written to the target RAM using the control port, the corresponding slew RAM location begins to ramp toward the target. The value is updated once per audio frame (LRCLK period).

The target RAM is 34 bits wide. The lower 28 bits contain the target data in 5.23 format for the linear and exponential (constant dB and RC type) ramp types. For constant time ramping, the lower 28 bits contain 16 bits in 2.14 format and 12 bits to set the current step. The upper six bits are used to determine the type and speed of the ramp envelope in all modes. The format of the data write for linear and exponential formats is shown in Table 12. Table 13 shows the data write format for the constant time ramping.

In normal operation, write data to the target/slew RAM using the safeload registers as described in the Safeload Registers section. A mute slew RAM bit is included in the audio control register to simultaneously set all the slew RAM target values to 0. This is useful for implementing a global multichannel mute. When this bit is deasserted, all slew RAM values return to their original premuted states.

Table 12. Linear, Constant dB, and RC Type Ramp Data Write

Byte 0	Byte 1	Bytes[2:4]
000000, curve_type[1:0]	time_const[3:0], data[27:24]	data[23:0]

Table 13. Constant Time Ramp Data Write

Byte 0	Byte 1	Bytes[2:4]
000000, curve_type[1:0]	update_step[0], #_of_steps[2:0], data[15:12]	data[11:0], reserved[11:0]

The four ramping curve types are:

Linear
The value slews to target using a fixed step size.

Constant dB
The value slews to target using the current value to calculate the step size. The resulting curve has a constant rise and decay when measured in dB.

RC Type
The value slews to target using the difference between target and current values to calculate the step size, producing a simple RC-type curve for rising and falling.

Constant Time
The value slews to the target in a fixed number of steps in a linear fashion. The control port mute has no affect on this type.

Table 14. Target/Slew RAM Ramp Type Settings

Settings	Ramp Type
00	Linear
01	Constant dB
10	RC Type
11	Constant Time

The following sections detail how the control port writes to the target/slew RAM to control the time constant and ramp type parameters.

Ramp Types[1:3]—Linear, Constant dB, RC Type (34-Bit Write)

The target word for the first three ramp types is broken into three parts. The 34-bit command is written with six leading 0s to extend the data write to five bytes. The parts of the target RAM write are:

Ramp Type (2 bits).
Time Constant (4 bits).
0000 = fastest
1111 = slowest
Data (28 bits): 5.23 format.

Ramp Type 4—Constant Time (34-Bit Write)

The target word for the constant time ramp type is written in five parts, with the 34-bit command written with six leading 0s to extend the data write to five bytes. The parts of the constant time target RAM write are:

Ramp Type (2 bits).
Update Step (1 bit). Set to 1 when new target is loaded to trigger step value update. Value is automatically reset after the step value is updated.
Number of Steps (3 bits). The number of steps that it takes to slew to the target value is set by these three bits, with the number of steps equal to $2^{3\text{-bit setting} + 6}$.
000 = 64
001 = 128
010 = 256
011 = 512
100 = 1024
101 = 2048
110 = 4096
111 = 8196
Data (16 bits). 2.14 format.
Reserved (12 bits). When writing to the RAM, set all of these bits to 0.

Target and Slew RAM Initialization

On reset, the target/slew RAM initializes to preset values. The target RAM initializes to a linear ramp type with a time constant of 5 and the data set to 1.0. The slew RAM initializes to a value of 1.0. These defaults give a full-scale (1.0 to 0.0) ramp time of 21.3 ms.

Linear Update Math

Linear math is the addition or subtraction of a constant value, referred to as a step. The equation to describe this step size is

$$step = \frac{2^{13}}{\frac{10^{2\times(tconst-5)}}{20}}$$

The result of the equation is normalized to a 5.23 data format. This gives a time constant range from 6.75 ms to 213.4 ms. (–60 dB relative to 0 dB full-scale). An example of this kind of update is shown in Figure 24 and Figure 25. All slew RAM figure examples, except the half-scale constant time ramp plot, show an increasing or decreasing ramp between –80 dB and 0 dB (full-scale). All figures except the constant time plots (Figure 29 and Figure 30) use a time constant of 0x7 (0x0 being the fastest and 0xF being the slowest).

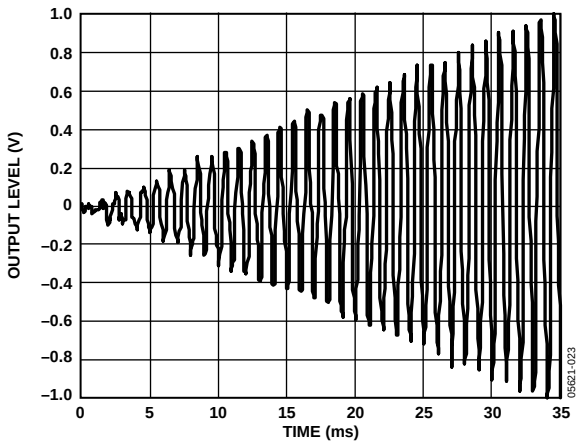


Figure 24. Slew RAM—Linear Update Increasing Ramp

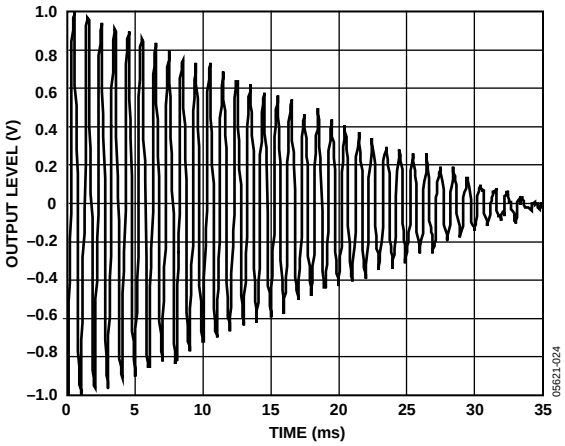


Figure 25. Slew RAM—Linear Update Decreasing Ramp

Constant dB and RC Type (Exponential) Update Math

Exponential math is accomplished by shifts and adds with a range from 6.1 ms to 1.27 s (−60 dB relative to 0 dB full-scale). When the ramp type is set to 01 (constant dB), each step size is set to the current value in the slew data. When the ramp type bits are set to 10 (RC type), the step sizes are equal to the difference between the values in the target RAM and slew RAM. Figure 26 and Figure 27 show examples of this type of target/slew RAM ramping. A decreasing ramp of both the constant dB and RC type ramps is a mirror image of the constant dB increasing ramp, and is shown in Figure 28.

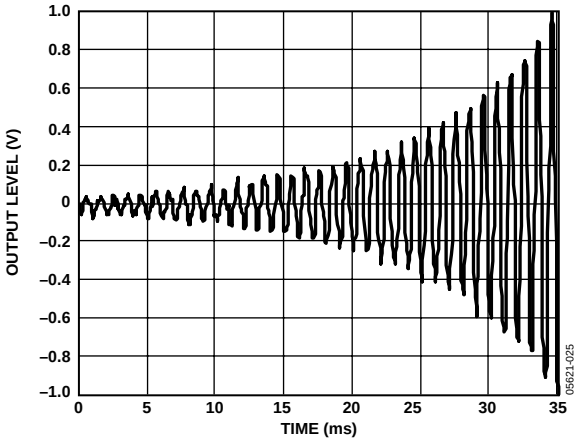


Figure 26. Slew RAM—Constant dB Update Increasing Ramp

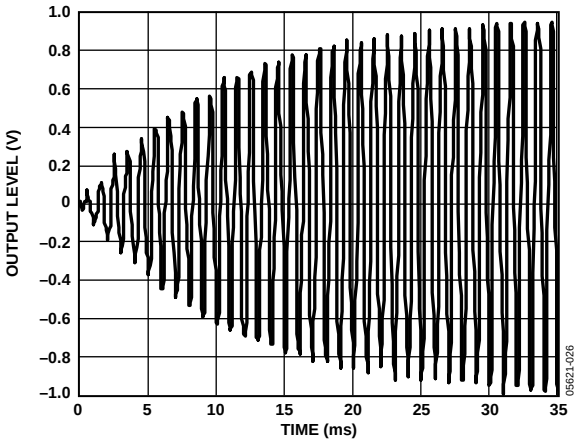


Figure 27. Slew RAM—RC Type Update Increasing Ramp

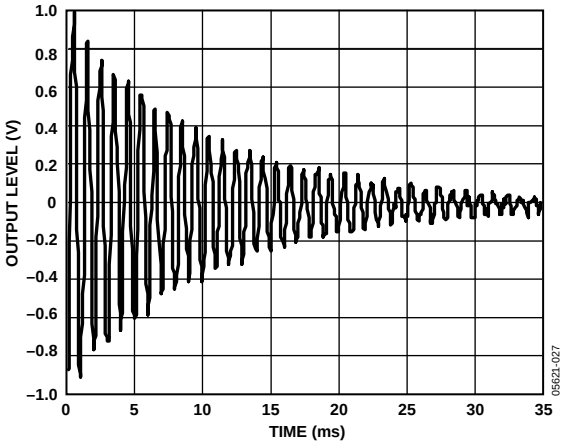


Figure 28. Slew RAM—Constant dB and RC Type Update Decreasing Ramp, Full Scale

Constant Time Update Math

Constant time math is accomplished by adding a step value that is calculated after each new target is loaded. The equation for this step size is

$$Step = (Target\ Data - Slew\ Data)/(Number\ of\ Steps)$$

Figure 29 shows a plot of the target/slew RAM operating in constant time mode. For this example, 128 steps are used to reach the target value. This type of ramping takes a fixed amount of time for a given number of steps, regardless of the difference in the initial state and the target value. Figure 30 shows a plot of a constant time ramp from –80 dB to –6 dB (half scale) using 128 steps; thus, the ramp takes the same amount of time as the previous ramp from –80 dB to 0 dB. A constant time decreasing ramp plot is shown in Figure 30.

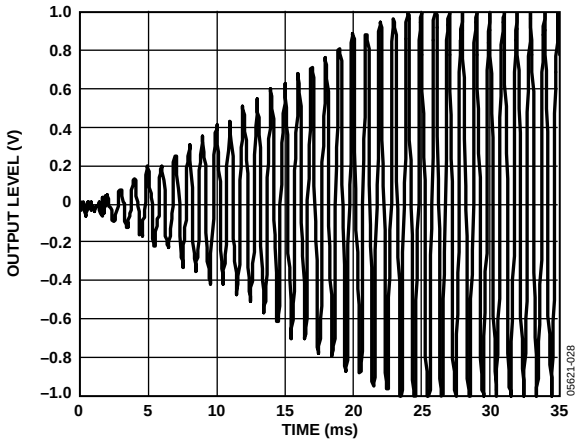


Figure 29. Slew RAM—Constant Time Update Increasing Ramp, Full Scale

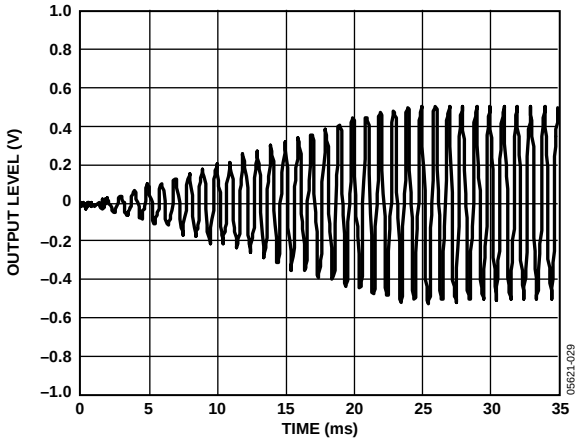


Figure 30. Slew RAM—Constant Time Update Increasing Ramp, Half Scale

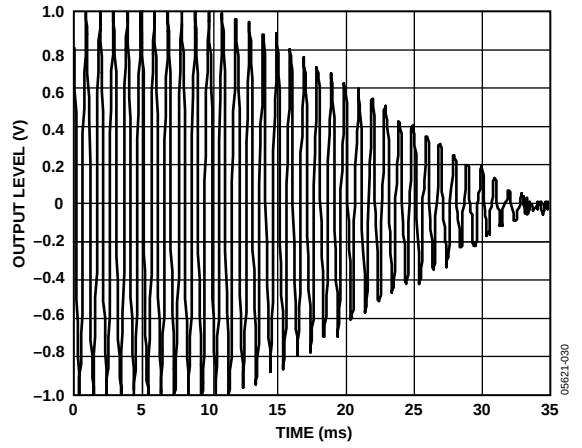


Figure 31. Slew RAM—Constant Time Update Decreasing Ramp, Full Scale

SAFELOAD REGISTERS

Many applications require real-time control of signal processing parameters, such as filter coefficients, mixer gains, multichannel virtualizing parameters, or dynamics processing curves. To prevent instability from occurring, all of the parameters of a biquad filter must be updated at the same time. Otherwise, the filter can execute for one or two audio frames with a mix of old and new coefficients. This mix causes temporary instability leading to transients that take a long time to decay. To eliminate this problem, the ADAV400 loads a set of 10 registers in the control port (five for 28-bit parameters, and another five for indirectly addressing the target/slew RAMs) with the desired parameter or target/slew RAM address and data. Five registers are used because a biquad filter uses five coefficients, and it is desirable to be able to do a complete biquad update in one transaction. The safeload registers can be used to update either the parameter RAM or target/slew RAM values. Once these registers are loaded, the appropriate initiate safe transfer bit (there are separate bits for parameter and target/slew loads) in the audio control register should be set to initiate the loading into RAM.

Program lengths should be limited to 2,555 cycles (2,560 − 5) to ensure that the ADAV400 is able to perform the safeloads. It is guaranteed that the safeload occurs within one LRCLK period (21 μs at f_S = 48 kHz) of the initiate safe transfer bit being set. The safeload logic automatically sends only those safeload registers that have been written to since the last safeload operation. For example, if only two parameters are to be sent, only two of the five safeload registers must be written to. When the initiate safe transfer bit (in the audio control register) is asserted, only those two registers are sent; the other three registers are not sent to the RAM and can still hold old or invalid data.

Table 15. Data Capture Control Registers

Register Bits	Function
13:2	12-Bit Program Counter Address
1:0	Register Select
	00 = Mult_X_input
	01 = Mult_Y_input
	10 = MAC_output
	11 = Accum_fback

DATA CAPTURE REGISTERS

The ADAV400 data capture feature allows the data at any node in the signal processing flow to be sent to one of six control port-readable registers or to a serial output pin. Use this feature to monitor and display information about internal signal levels or compressor/limiter activity.

The ADAV400 contains six independent control port-readable data capture registers, and two digital output capture registers. Use these registers when debugging the signal processing flow.

For each of the data capture registers, a capture count and a register select must be set. The capture count is a number between 0 and 2,559 that corresponds to the program step number where the capture will occur. The register select field programs one of four registers in the DSP core that transfers to the data capture register when the program counter equals the capture count. The register select field selections are shown in Table 16.

Table 16. Data Capture Output Register Select

Settings	Register
00	Multiplier X Input (Mult_X_input)
01	Multiplier Y Input (Mult_Y_input)
10	Multiplier-Accumulator Output (MAC_out)
11	Accumulator Feedback (Accum_fback)

The capture count and register select bits are set by writing to one of the eight data capture registers at register addresses.

4170: Control Port Data Capture Setup Register 0
4171: Control Port Data Capture Setup Register 1
4172: Control Port Data Capture Setup Register 2
4173: Control Port Data Capture Setup Register 3
4174: Control Port Data Capture Setup Register 4
4175: Control Port Data Capture Setup Register 5
4176: Digital Out Data Capture Setup Register 0
4177: Digital Out Data Capture Setup Register 1

The captured data is in 5.19 twos complement data format for all eight register select fields. The four LSBs are truncated from the internal 5.23 data-word.

The data that must be written to set up the data capture is a concatenation of the 12-bit program count index with the 2-bit register select field. The capture count and register select values that correspond to the desired point to be monitored in the signal processing flow are found in a file output from the program compiler. The capture registers are accessed by reading from locations 4170 to 4175 (0x104A to 0x104F) for control port capture registers. The formats for reading and writing to the data capture registers are listed in Table 23 and Table 24.

AUDIO CORE CONTROL REGISTER

The controls in this register set the operation of the DSP core of the ADAV400. Bit 6 to Bit 9 are used to initiate a shutdown of the core. The output is muted when this is performed; therefore, if slew RAM locations are used as volume controls in the program, assert Bit 12 of the audio core control register (Table 30) to avoid a click or pop when shutdown is asserted. Bit 13 indicates when this operation is complete.

Slew RAM Muted (Bit 13)

This bit is set to 1 when the slew RAM mute operation has been completed. This bit is read-only and is automatically cleared by reading.

Write Zero to Target RAM (Bit 12)

Setting this bit to 1 is equivalent to writing zeros to all locations in the target RAM. The RAM then slews to zero, muting the volume. To enable normal operation, clear this bit to zero.

Use Serial Out LRCLK for Output Latch (Bit 10)

Normally, data is transferred from the DSP core to the serial output registers at the end of each program cycle. In some cases, such as when output sample rate is set to some multiple of input sampling rate, it is desirable to transfer the internal core data multiple times during a single input audio sample period. Setting this bit to 1 allows the output LRCLK signal to control this data transfer rather than the internal end-of-sequence signal. Operation in this mode can require custom assembly language coding in the Analog Devices graphical tools.

Clear Registers to All Zeros (Bit 9)

Setting this bit to 0 sets the contents of the accumulators and serial output registers to 0. Like the other register bits, this one defaults to 0. This means the ADAV400 powers up in clear mode and does not pass signals until a 1 is written to this bit. This is intended to prevent noises from inadvertently occurring during the power-up sequence.

Force Multiplier to Zero (Bit 8)

When this bit is set to 1, the input to the DSP multiplier is set to 0, which results in the multiplier output being 0. This control bit is included for maximum flexibility, and is normally not used.

Initialize Data Memory with Zeros (Bit 7)

Setting this bit to 1 initializes all data memory locations to 0. This bit is cleared to 0 after the operation is complete. Assert this bit after a complete program/parameter download has occurred to ensure click-free operation.

Zero Serial Input Port (Bit 6)

When this bit is set to 1, the serial input channels are forced to all zeros and effectively muted.

Initiate Safe Transfer to Target RAM (Bit 5)

Setting this bit to 1 initiates a safeload transfer to the target/slew RAM. This bit clears when the operation is completed. Of five safeload register pairs (address/data), only those registers that have been written since the last safeload event are transferred. Address 0 corresponds to the first target RAM location.

Initiate Safe Transfer to Parameter RAM (Bit 4)

Setting this bit to 1 initiates a safeload transfer to the parameter RAM. This bit clears when the operation is completed. Of five safeload registers pairs (address/data), only those registers that have been written since the last safeload event are transferred. Address 0 corresponds to the first parameter RAM location.

Input Serial Port to Sequencer Sync (Bits[3:2])

Normally, the internal sequencer is synchronized to the incoming audio frame rate by comparing the internal program counter with the edge of the LRCLK input signal. In some cases the ADAV400 is used to decimate an incoming signal by some integer factor. In this case, it is desirable to synchronize the sequencer to a submultiple of the incoming LRCLK rate to make more than one audio input sample available to the program during a single audio output frame. For example, if these bits are set to 01 (LRCLK/2), a 96 kHz input can be used with a 48 kHz output, allowing two consecutive input samples to be processed during a single audio output frame. Operation

in this mode may require custom assembly language coding in the Analog Devices graphical tools.

Program Length (Bits[1:0])

96 kHz and 192 kHz Modes

These bits set the length of the internal program. The default program length is 2,560 instructions for f_S = 48 kHz, but the program length can be shortened by factors of 2 to accommodate sample rates higher than 48 kHz. For f_S = 96 kHz, set the program length to 1,280 (01), and for f_S = 192 kHz, set the length at 640 steps (10).

Low Power Modes

All the blocks in the ADAV400 are individually controlled by power-up bits. Following a reset, all the bits are zero indicating that all the blocks are powered down. Blocks are powered up individually by setting the appropriate bit in the power control register (see Table 36).

RAM CONFIGURATION REGISTER

The ADAV400 uses a modulo RAM addressing scheme to allow filters and other blocks to be coded easily without requiring filter data to be explicitly moved during the filtering operation. This is accomplished by adding the contents of an address offset counter to the actual base address supplied in the core of the ADAV400. This address offset counter is automatically incremented at the audio frame rate.

This method works well for most audio applications that involve filtering. In some cases, however, it is desirable to have direct access to the RAM, bypassing the auto-incrementing address offset counter. For this reason, the data memories in the ADAV400 can be divided into modulo and nonmodulo portions by programming the RAM modulo control register (see Table 31). The address range from 0 to 512 × (RAM configuration register contents) is treated as modulo memory with auto-incrementing address offset registers. The maximum setting of this register is the full size of the RAM, or 6,144 (6k) data-words. Note that addresses in this range automatically wrap around the modulo boundary as set by the register. This feature is not normally used with blocks supplied by Analog Devices. For normal operation, this register remains in its default state to set up the entire RAM to use the auto-increment feature. This feature is included for maximum programming flexibility and can be used for special software development.

CONTROL PORT READ/WRITE DATA FORMATS

The read/write formats of the control port are designed to be byte-oriented. This allows for easy programming of common microcontroller chips. In order to fit into a byte-oriented format, 0s are appended to the data fields before the MSB to extend the data-word to the next multiple of eight bits. For example, 28-bit words written to the parameter RAM are appended with four leading 0s to reach 32 bits (4 bytes); 40-bit words written to the program RAM are not appended with any 0s because it is already a full 5 bytes. These zero-extended data fields are appended to a 3-byte field consisting of a 7-bit chip address, a read/write bit, and an 11-bit RAM/register address. The control port knows how many data bytes to expect based on the address that is received in the first three bytes.

The total number of bytes for a single location write command can vary from four bytes (for a control register write), to eight bytes (for a program RAM write). Burst mode is used to fill contiguous register or RAM locations. A burst mode write is done by writing the address and data of the first RAM/register location to be written. Rather than ending the control port transaction, the next data word can be written immediately without first writing its specific address. The ADAV400 control ports auto-increment the address of each write, even across the boundaries of the different RAMs and registers.

Table 17. Parameter RAM Read/Write Format (Single Address)

Byte 0	Byte 1	Byte 2	Byte 3	Bytes[4:6]
chip_adr [6:0], R/$\overline{W}$	000, param_adr [12:8]	param_adr [7:0]	0000, param [27:24]	param [23:0]

Table 18. Parameter RAM Block Read/Write Format (Burst Mode)

Byte 0	Byte 1	Byte 2	Byte 3	Bytes[4:6]	Byte 7	Byte 11
chip_adr [6:0], R/$\overline{W}$	000, param_adr [12:8]	param_adr [7:0]	0000, param [27:24]	param [23:0]	Byte 8	Byte 12
					Byte 9	Byte 13
					Byte 10	Byte 14
			<—param_adr—>		param_adr + 1	param_adr + 2

Table 19. Program RAM Read/Write Format (Single Address)

Byte 0	Byte 1	Byte 2	Bytes[3:7]
chip_adr [6:0], R/$\overline{W}$	000, prog_adr [12:8]	prog_adr [7:0]	prog [39:0]

Table 20. Program RAM Block Read/Write Format (Burst Mode)

Byte 0	Byte 1	Byte 2	Bytes[3:7]	Byte 8	Byte 13
chip_adr [6:0], R/$\overline{W}$	000, prog_adr [12:8]	prog_adr [7:0]	prog [39:0]	Byte 9	Byte 14
				Byte 10	Byte 15
				Byte 11	Byte 16
				Byte 12	Byte 17
		<—prog_adr—>		prog_adr +1	prog_adr +2

Table 21. Control Register Read/Write Format (Core, Serial Out 0, Serial Out 1)

Byte 0	Byte1	Byte 2	Byte 3	Byte 4
chip_adr [6:0], R/$\overline{W}$	000, reg_adr [12:8]	reg_adr [7:0]	data [15:8]	data [7:0]

Table 22. Control Register Read/Write Format (RAM Configuration, Serial Input)

Byte 0	Byte1	Byte 2	Byte 3
chip_adr [6:0], R/$\overline{W}$	000, reg_adr [12:8]	reg_adr [7:0]	data [7:0]

Table 23. Data Capture Register Write Format

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
chip_adr [6:0], R/$\overline{W}$	000, data_capture_adr [12:8]	data_capture_adr [7:0]	000, progCount [10:6]	progCount [5:0], regSel [1:0]

Table 24. Data Capture (Control Port Readback) Register Read Format

Byte 0	Byte 1	Byte 2	Bytes[3:5]
chip_adr [6:0], R/$\overline{W}$	000, data_capture_adr [12:8]	data_capture_adr [7:0]	data [23:0]

Table 25. Safeload Register Data Write Format

Byte 0	Byte 1	Byte 2	Byte 3	Bytes[4:7]
chip_adr [6:0], R/$\overline{W}$	000, safeload_adr [12:8]	safeload_adr [7:0]	000000, data [33:32]	data [31:0]

Table 26. Safeload Register Address Write Format

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
chip_adr [6:0], R/$\overline{W}$	000, safeload_adr [12:8]	safeload_adr [7:0]	000000, param_adr [9:8]	param_adr [7:0]

SERIAL DATA INPUT/OUTPUT PORTS

The flexible serial data input and output ports of the ADAV400 can be set to accept or transmit data in 2-channel formats or in an 8- or 16-channel TDM stream. Data is processed in twos complement, MSB-first format. The left channel data field always precedes the right channel data field in the 2-channel streams. In the TDM modes, Slot 0 to Slot 3 (8-channel TDM) or Slot 0 to Slot 7 (16-channel TDM) fall in the first half of the audio frame, and Slot 4 to Slot 7 (or Slot 8 to Slot 15 in 16-channel TDM) are in the second half of the frame. The serial modes are set in the serial output and serial input control registers.

The input serial port is synchronized with the output serial port; in other words, BCLK1 and LRCLK1 are used for both. The output serial port can be programmed to be a master or slave port.

The input control register allows control of clock polarity and data input modes. The valid data formats are I^2S , left-justified, right-justified (24-/20-/18- or 16-bit), 8-channel and 16-channel TDM. In all modes, except for the right-justified modes, the serial port accepts an arbitrary number of bits up to a limit of 24. Extra bits do not cause an error, but they do truncate internally. Proper operation of the right-justified modes requires exactly 64 BCLKs per audio frame.

The LRCLK in TDM mode can be input to the ADAV400 as either a 50/50 duty cycle clock or as a bit-wide pulse.

In TDM mode, the ADAV400 is a master for 48 kHz and 96 kHz data, but not for 192 kHz data. LRCLK1 and BCLK1 are used as the left/right clock and bit clock, respectively, for the TDM stream. Apply input data for the TDM stream to SDIN0; TDM output data is available on SDO0. In 16-channel TDM mode, the ADCs and DACs cannot be used.

Table 27 displays the modes in which the serial output port function.

The output control registers give the user control of clock polarities, clock frequencies, clock types, and data format. In all modes, except for the right-justified modes (MSB delayed by 8, 12, or 16), the serial port accepts an arbitrary number of bits up to a limit of 24. Extra bits do not cause an error, but truncate internally. Proper operation of the right-justified modes requires the LSB to align with the edge of the LRCLK. The default settings of all serial port control registers correspond to 2-channel I^2S mode. LRCLK1 and BCLK1 are clocks for the serial output port.

All registers default to all 0s. All register settings apply to both master and slave modes, unless otherwise noted.

Table 28 shows the proper configurations for standard audio data formats.

Table 27. Serial Output Port Master/Slave Mode Capabilities

f_S	2-Channel Modes (I^2S, Left-Justified, Right-Justified)	8-Channel TDM	16-Channel TDM
48 kHz	Master and slave	Master and slave	Slave only
96 kHz	Master and slave	Master and slave	Slave only
192 kHz	Master and slave	Slave only	Slave only

Table 28. Data Format Configurations

Format	LRCLK Polarity	LRCLK Type	BCLK Polarity	MSB Position
I^2S (Figure 32)	Frame begins on falling edge	Clock	Data changes on falling edge	Delayed from LRCLK edge by one BCLK
Left-Justified (Figure 33)	Frame begins on rising edge	Clock	Data changes on falling edge	Aligned with LRCLK edge
Right-Justified (Figure 34)	Frame begins on rising edge	Clock	Data changes on falling edge	Delayed from LRCLK edge by 8, 12, or 16 BCLKs
TDM with Clock (Figure 35)	Frame begins on falling edge	Clock	Data changes on falling edge	Delayed from start of word clock by one BCLK
TDM with Pulse (Figure 36)	Frame begins on rising edge	Pulse	Data changes on falling edge	Delayed from start of word clock by one BCLK

Figure 35 shows just one of the formats in which the ADAV400 can operate in TDM mode. Refer to the Serial Data Input/Output Ports section for a more complete description of the modes of operation.

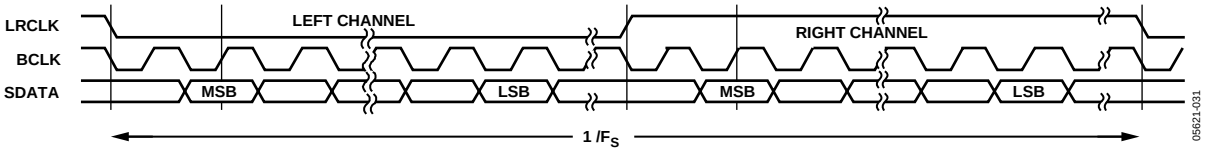


Figure 32. I²S Mode—16 to 24 Bits per Channel

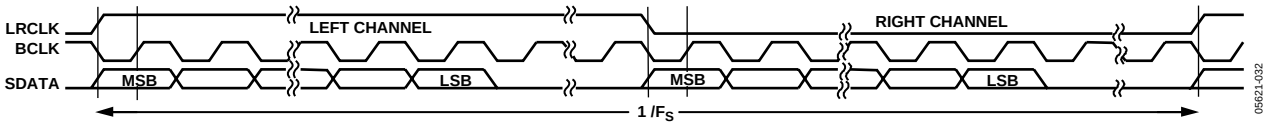


Figure 33. Left-Justified Mode—16 to 24 Bits per Channel

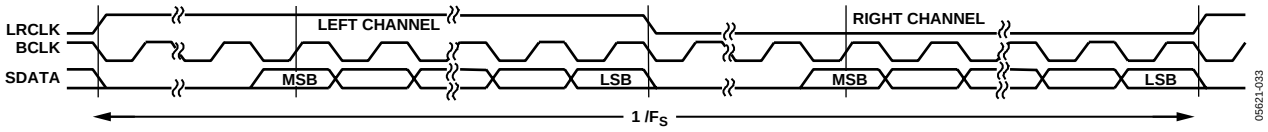


Figure 34. Right-Justified Mode—16 to 24 Bits per Channel

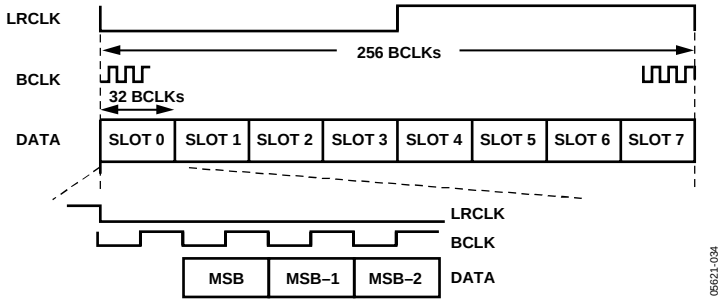


Figure 35. 8-Channel TDM Mode

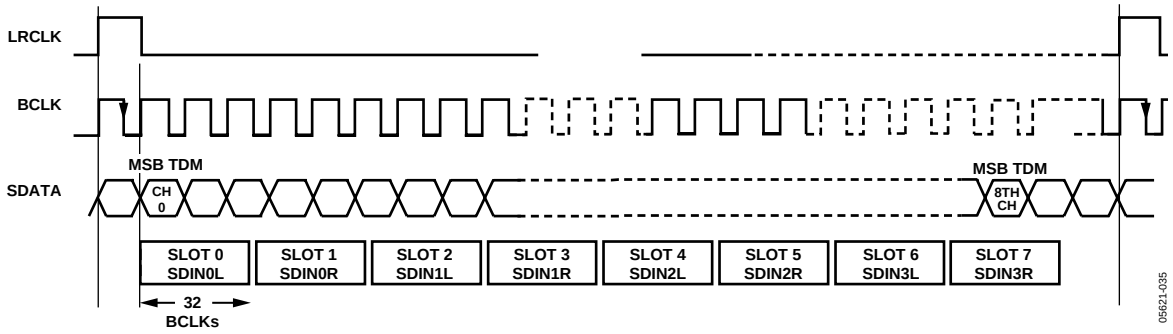


Figure 36. TDM Mode with Pulse Word Clock

CONTROL REGISTERS

Table 29. Audio Register Map

Register Address (Hex)	Register Name	Register Width (Bits)
0x1052	Audio Core Control Register	16
0x1053	RAM Modulo Control Register	8
0x1054	Serial Output Control Register	16
0x1055	Serial Input Control Register	8
0x1056	SRC Serial Port Control Register	8
0x1057	ADC Input MUX Control Register	16
0x1058	Power Control Register	16
0x1059	User Control Register 1	16
0x105A	User Control Register 2	16
0x110D	DAC Amplifier Register	16
0x1113	Headphone Amplifier Register	16

Table 30. Audio Core Control Register

Register Address 0x1052 Default = 0x000

Register Bits	Function
15	Reserved (Set to 0)
14[1]	Enable SDO2 and SDO3 0 = enabled 1 = disabled
13	Indicates when Slew RAM is Muted (Read Only)
12	Equivalent to Writing 0s to the Target RAM 0 = normal operation 1 = RAM zeroed
11	Reserved (Set to 0)
10	LRCLK Used for Output Serial Data Transfer 0 = disabled 1 = enabled
9	Clears Internal Processor Registers (Active Low) 0 = registers cleared 1 = normal operation
8	Forces Multiplier Input to Zero 0 = normal operation 1 = force zero
7	Initializes Data RAM to Zero 0 = normal operation 1 = enabled
6	Mute Serial Input Ports 0 = normal operation 1 = muted
5	Initiate Safeload-to-Target/Slew RAM 0 = off 1 = on
4	Initiate Safeload-to-Parameter RAM 0 = off 1 = on
3:2	Determines the Input SPORT-to-Program Sequencer Ratio 00 = LRCLK 01 = LRCLK/2 10 = LRCLK/4 11= LRCLK/8
1:0	Program Length 00 = 2560 (48 kHz) 01 = 1280 (96 kHz digital IO only) 10 = 640 (192 kHz digital IO only) 11 = reserved

[1] The polarity of this bit is inverted when read.

Table 31. RAM Modulo Control Register (8 Bits)
Register Address 0x1053 Default = 0x28

Register Bits	Function
7:6	Reserved (Set to 0)
5:0	Ram Modulo Size (1 LSB = 512 locations)

Table 32. Serial Output Control Register
Register Address 0x1054 Default = 0x0000

Register Bits	Function
15	Dither Enable 0 = disabled 1 = enabled
14	TDM Mode Function 0 = 8-channel TDM 1 = 16-channel TDM
13	LRCLK Polarity 0 = left low, right high 1 = left high, right low
12	BCLK Polarity 0 = data changes on falling edge 1 = data changes on rising edge
11	Master/Slave Mode Select 0 = slave 1 = master
10:9	BCLK Frequency (Master Mode) 00 = 3.072 MHz (48 kHz) 01 = 6.144 MHz (96 kHz digital IO only) 10 = 12.288 MHz (192 kHz digital IO only) 11 = reserved
8:7	LRCLK Frequency (Master Mode) 00 = 48 kHz 01 = 96 kHz 10 = 192 kHz 11 = reserved
6	Frame Sync Type 0 = LRCLK 1 = pulse
5	TDM Enable 0 = serial data out 1 = TDM out
4:2	MSB Position 000 = delay by 1 001 = delay by 0 010 = delay by 8 011 = delay by 12 100 = delay by 16 All others are reserved
1:0	Word Length 00 = 24 bits 01 = 20 bits 10 = 16 bits 11 = 16 bits

Table 33. Serial Input Control Register (8 Bits)
Register Address 0x1055 Default = 0x00

Register Bits	Function
7:6	Reserved (Set to 0)
5	TDM Mode Function 0 = 8-channel TDM 1 = 16-channel TDM
4	LRCLK Polarity 0 = left low, right high 1 = left high, right low
3	BCLK Polarity 0 = data changes on falling edge 1 = data changes on rising edge
2:0	Serial Input Mode 000 = I²S 001 = left justified 010 = 8-channel TDM 011 = right justified, 24 bits 100 = right justified, 20 bits 101 = right justified, 18 bits 110 = right justified, 16 bits All others are reserved

Table 34. SRC Serial Port Control Register (8 Bits)
Register Address 0x1056 Default = 0x00

Register Bits	Function
7	Reserved (Set to 0)
6:5	SRC Serial Input Port Select 00 = SDIN3 01 = SDIN2 10 = SDIN1 11 = SDIN0
4	LRCLK Polarity 0 = left low, right high 1 = left high, right low
3	BCLK Polarity 0 = data changes on falling edge 1 = data changes on rising edge
2:0	Serial Input mode 000 = I²S 001 = left justified 010 = 8-channel TDM 011 = right justified, 24 bits 100 = right justified, 20 bits 101 = right justified, 18 bits 110 = right justified, 16 bits All others are reserved

SERIAL OUTPUT CONTROL REGISTERS

Dither Enable (Bit 15)

Setting this bit to 1 enables dither on the appropriate channels.

LRCLK Polarity (Bit 13)

When set to 0, the left channel data is clocked when LRCLK is low, and the right data is clocked when LRCLK is high. When set to 1, this sequence is reversed.

BCLK Polarity (Bit 12)

This bit controls on which edge of the bit clock the output data is clocked. Data changes on the falling edge of BCLK1 when this bit is set to 0, and on the rising edge when this bit is set to 1.

Master/Slave (Bit 11)

This bit determines whether the output port is a clock master or slave. The default setting is slave; on power-up, Pin BCLK1 and Pin LRCLK1 are set as inputs until this bit is set to 1, at which time they become clock outputs.

BCLK Frequency (Bits[10:9])

When the output port is used as a clock master, these bits set the frequency of the output bit clock, which is divided down from the PLL.

Frame Sync Frequency (Bits[8:7])

When the output port is used as a clock master, these bits set the frequency of the output word clock on the LRCLK1 pin, which is divided down from the PLL.

Frame Sync Type (Bit 6)

This bit sets the type of signal on the LRCLK1 pin. When set to 0, the signal is a word clock with a 50% duty cycle; when set to 1, the signal is a pulse with a duration of one bit clock at the beginning of the data frame.

TDM Enable (Bit 5)

Setting this bit to 1 changes the output port from multiple serial outputs to a single TDM output stream on the SDO0 pin. This bit must be set in both serial output control registers to enable 16-channel TDM on SDO0.

MSB Position (Bits[4:2])

These three bits set the position of the MSB of the data with respect to the LRCLK edge. The data outputs of the ADAV400 are always MSB first.

Output Word Length (Bits[1:0])

These bits set the word length of the output data-word. All bits following the LSB are set to 0.

SERIAL INPUT CONTROL REGISTER

8-/16-Channel TDM Input (Bit 5)

Setting this bit to 0 puts the ADAV400 into 8-channel TDM input mode, with the input stream coming in on SDIN0. Setting this bit to 1 puts the part in 16-channel TDM input mode, input on SDIN0.

LRCLK Polarity (Bit 4)

When set to 0, the left channel data on the SDINx pins is clocked when LRCLK1 is low; and the right input data is clocked when LRCLK1 is high. When set to 1, this sequence is reversed.

In TDM mode, when this bit is set to 0, data is clocked in starting with the next appropriate BCLK edge (set in Bit 3 of this register) following a falling edge on the LRCLK1 pin. When set to 1 and running in TDM mode, the input data is valid on the BCLK edge following a rising edge on the word clock (LRCLK1). The serial input port can also operate with a pulse input signal, rather than a clock. In this case, the first edge of the pulse is used by the ADAV400 to start the data frame. When this polarity bit is set to 0, use a low pulse; use a high pulse when the bit is set to 1.

BCLK Polarity (Bit 3)

This bit controls on which edge of the bit clock the input data changes, and on which edge it is clocked. Data changes on the falling edge of BCLK1 when this bit is set to 0, and on the rising edge when this bit is set at 1.

Serial Input Mode (Bits[2:0])

These two bits control the data format that the input port expects to receive. Bit 3 and Bit 4 of this control register override the settings in Bit 2 to Bit 0; therefore, all four bits must be changed together for proper operation in some modes. The clock diagrams for these modes are shown in Figure 32, Figure 33, and Figure 34. Note that for left-justified and right-justified modes, the LRCLK polarity is high, then low, which is opposite from the default setting of Bit 4.

When these bits are set to accept a TDM input, the ADAV400 data starts after the edge defined by Bit 4. Figure 35 shows an 8-channel TDM stream with a high-to-low triggered LRCLK and data changing on the falling edge of the BCLK. The ADAV400 expects the MSB of each data slot delayed by one BCLK from the beginning of the slot, just like in the stereo I^2S format. In 8-channel TDM mode, the channels alternate with left and right channels starting with SDIN0 as shown in Figure 35. When in 16-channel TDM mode, the first half-frame holds Channel 0 to Channel 7, and the second half-frame has Channel 8 to Channel 15. Figure 36 shows an example of a TDM stream running with a pulse word clock used to interface to ADI codecs in their auxiliary mode. To work in this mode on either the input or output serial ports, the ADAV400 should be set to frame beginning on the rising edge of LRCLK, data changing on the falling edge of BCLK, and MSB position delayed from the start of the word clock by one BCLK. Table 28 explains the clock settings for each of these formats.

Table 35. ADC Input MUX Control Register
Register Address 0x1057 Default = 0x0001

Register Bits	Function
15:4	Reserved (Set to 0)
3	AIN4 to ADC
2	AIN3 to ADC
1	AIN2 to ADC
0	AIN1 to ADC

Table 36. Power Control Register
Register Address 0x1058 Default = 0x0000

Register Bits	Function
	0 = Powered Down, 1 = Powered Up
15	PLL
14	Reference Buffer
13	ADC
12	VOUT4 DAC
11	VOUT3 DAC
10	VOUT2 DAC
9	VOUT1 DAC
8	AUX2 Right DAC
7	AUX2 Left DAC
6	AUX1/HP Right DAC
5	AUX1/HP Left DAC
4	Headphone Amplifier Right
3	Headphone Amplifier Left
2	SRC
1	Digital ADC and DAC Engine
0	Audio Processor

Table 37. User Control Register 2
Register Address 0x105A Default = 0x0000

Register Bits	Function
15:8	Reserved (Set to 0)
7	Headphone Amplifier Mute 0 = Normal Operation 1 = Mute
6:5	Reserved (Set to 0)
4:0	Headphone Amplifier Attenuation 00000 = 0 dB 00001 = −1.5 dB 00010 = −3.0 dB 11110 = −45.0 dB 11111 = −46.5 dB

Table 38. User Control Register 1
Register Address 0x1059 Default = 0x0000

Register Bits	Function
15:13	Reserved (Set to 0)
12:9	Reserved (Set to 0) These bits read back as 0b1111
8	SRC Mux Enable 0 = disabled 1 = enabled
7	(Read Only) Indicates SRC is Locked 0 = SRC not locked 1 = SRC locked
6	Enables MCLK Out Pin 0 = MCLKO pin disabled 1 = MCLKO pin enabled
5:3	MCLKO Select 000 = reserved 001 = ADC and DAC digital engine clock 010 = reserved 011 = reserved 1xx = ADC and DAC clock
2:1	PLL Clock Select 00 = 64 x f_S (3.072 MHz) 01 = 128 x f_S (6.144 MHz) 10 = 256 x f_S (12.288 MHz) 11 = 512 x f_S (24.576 MHz)
0	Enable PLL 0 = PLL bypassed 1 = PLL in use

Table 39. DAC Amplifier Register
Register Address 0x110D Default = 0x0000

Register Bits	Function
15:5	Reserved (set to 0)
4	DAC Amplifier Chopping[1] 0 = enabled 1 = disabled
3:0	Reserved (set to 0)

[1] Set this bit to 1 to obtain maximum performance from the DAC amplifier.

Table 40. Headphone Amplifier Register
Register Address 0x1113 Default = 0x0000

Register Bits	Function
15:1	Reserved (set to 0)
0	Headphone Amplifier Chopping[1] 0 = enabled 1 = disabled

[1] Set this bit to 1 to obtain maximum performance from the DAC amplifier.

TYPICAL APPLICATION DIAGRAM

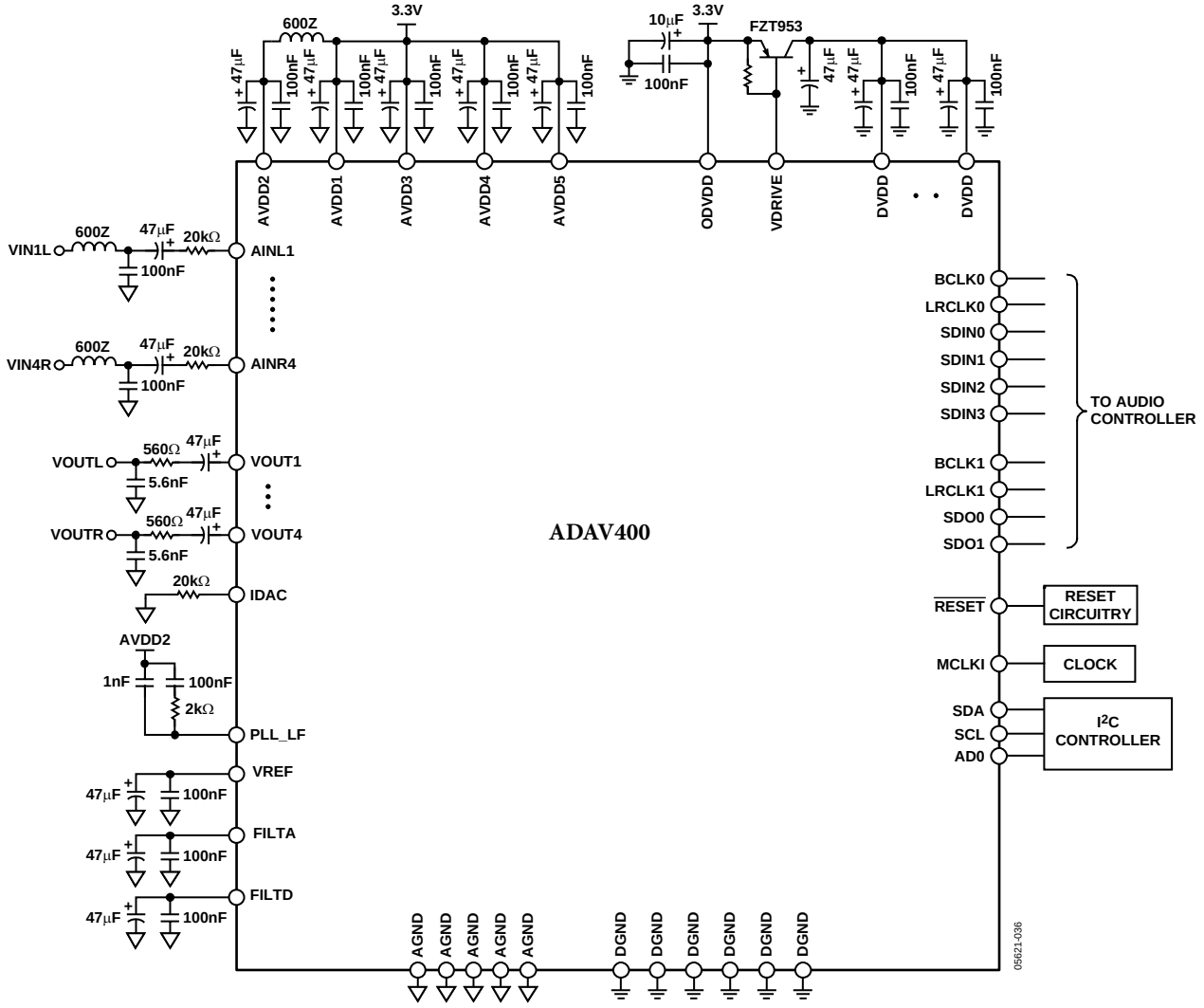
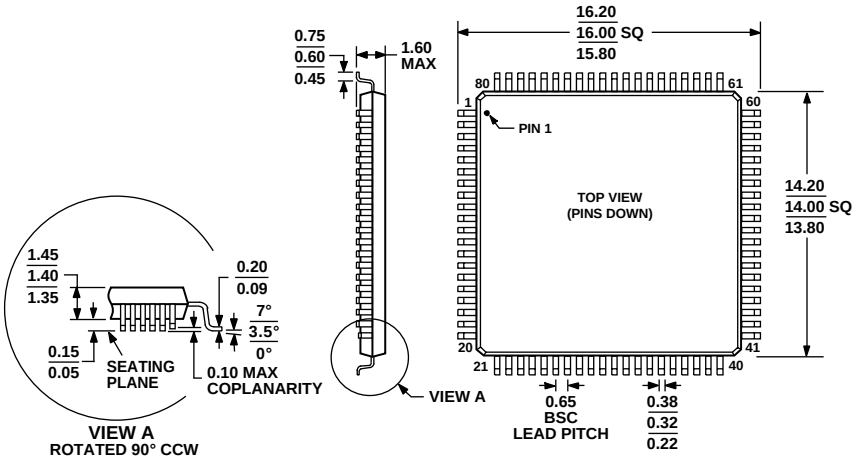


Figure 37. Typical Application Circuit

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BEC

Figure 38. 80-Lead Low Profile Quad Flat Package [LQFP]
(ST-80-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADAV400KSTZ[2]	0°C to +70°C	Low Profile Quad Flat Package [LQFP]	ST-80-2
ADAV400KSTZ-REEL[2]	0°C to +70°C	Low Profile Quad Flat Package [LQFP]	ST-80-2

[1] The ADAV400 is a Pb-free environmentally friendly product. It is manufactured using the most up-to-date materials and processes. The coating on the leads of each device is 100% pure Sn electroplate. The device is suitable for Pb-free applications, and can withstand surface-mount soldering at up to 255°C (±5°C). In addition, it is backward-compatible with conventional Sn/Pb soldering processes. This means the electroplated Sn coating can be soldered with Sn/Pb solder pastes at conventional reflow temperatures of 220°C to 235°C.
[2] Z = Pb-free part.

NOTES

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