

# Single-Supply, Differential 18-Bit ADC Driver

# ADA4941-1

#### **FEATURES**

Single-ended-to-differential converter Excellent linearity Distortion -110 dBc @100 KHz for V<sub>o</sub>, dm = 2 V p-p Low noise: 10.2 nV/ $\sqrt{Hz}$ , output-referred, G = 2 Extremely low power: 2.2 mA (3 V supply) High input impedance: 24 M $\Omega$ User-adjustable gain High speed: 31 MHz, -3 dB bandwidth (G = +2) Fast settling time: 300 ns to 0.005% for a 2 V step Low offset: 0.8 mV max, output-referred, G = 2 Rail-to-rail output Disable feature Wide supply voltage range: 2.7 V to 12 V Available in space-saving, 3 mm × 3 mm LFCSP

#### APPLICATIONS

Single-supply data acquisition systems Instrumentation Process control Battery-power systems Medical instrumentation

### FUNCTIONAL BLOCK DIAGRAM





Figure 2. Distortion vs. Frequency at Various Output Amplitudes

#### **GENERAL DESCRIPTION**

The ADA4941-1 is a low power, low noise differential driver for ADCs up to 18 bits in systems that are sensitive to power. The ADA4941-1 is configured in an easy-to-use, single-ended-to-differential configuration and requires no external components for a gain of 2 configuration. A resistive feedback network can be added to achieve gains greater than 2. The ADA4941-1 provides essential benefits, such as low distortion and high SNR, that are required for driving high resolution ADCs.

With a wide input voltage range (0 V to 3.9 V on a single 5 V supply), rail-to-rail output, high input impedance, and a useradjustable gain, the ADA4941-1 is designed to drive singlesupply ADCs with differential inputs found in a variety of low power applications, including battery-operated devices and single-supply data acquisition systems. The ADA4941-1 is ideal for driving the 16-bit and 18-bit PulSAR<sup>®</sup> ADCs such as the AD7687, AD7690, and AD7691.

The ADA4941-1 is manufactured on ADI's proprietary secondgeneration XFCB process, which enables the amplifier to achieve 18-bit performance on low supply currents.

The ADA4941-1 is available in a small 8-lead LFCSP as well as a standard 8-lead SOIC and is rated to work over the extended industrial temperature range,  $-40^{\circ}$ C to  $+125^{\circ}$ C.

Rev. 0

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### **REVISION HISTORY**

4/06—Revision 0: Initial Version

## **SPECIFICATIONS**

 $T_A = 25^{\circ}$ C,  $V_S = 3$  V, OUT+ connected to FB (G = 2),  $R_{L_s dm} = 1 \text{ k}\Omega$ , REF = 1.5 V, unless otherwise noted.

### Table 1.

Parameter	Conditions	Min	Тур	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	$V_0 = 0.1 V p - p$	21	30		MHz
	$V_0 = 2.0 V p - p$	4.6	6.5		MHz
Overdrive Recovery Time	+Recover/–Recovery		320/650		ns
Slew Rate	$V_0 = 2 V$ step		22		V/µs
Settling Time 0.005%	$V_0 = 2 V p - p step$		300		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion	$f_c = 40 \text{ kHz}, V_0 = 2 \text{ V p-p}, \text{HD2/HD3}$		-116/-112		dBc
	$f_c = 100 \text{ kHz}, V_0 = 2 \text{ V p-p}, \text{HD2/HD3}$		-101/-98		dBc
	$f_c = 1 \text{ MHz}, V_0 = 2 \text{ V p-p}, \text{HD2/HD3}$		-75/-71		dBc
RTO Voltage Noise	f = 100 kHz		10.2		nV/√Hz
Input Current Noise	f = 100 kHz		1.6		pA/√Hz
DC PERFORMANCE					
Differential Output Offset Voltage			0.2	0.8	mV
Differential Input Offset Voltage Drift			1.0		μV/°C
Single-Ended Input Offset Voltage	Amp A1 or Amp A2		0.1	0.4	, mV
Single-Ended Input Offset Voltage Drift			0.3		μV/°C
Input Bias Current	IN and REF		3	4.5	μA
Input Offset Current	IN and REF		0.1		μA
Gain	(+OUT – –OUT)/(IN – REF)	1.98	2.00	2.01	V/V
Gain Error		-1		+1	%
Gain Error Drift			0.005		%/°C
INPUT CHARACTERISTICS					
Input Resistance	IN and REF		24		MΩ
Input Capacitance	IN and REF		1.4		рF
Input Common-Mode Voltage Range		0.2		1.9	V
Common-Mode Rejection Ratio (CMRR)	$CMRR = V_{OS, dm}/V_{CM}$ , $VREF = VIN$ , $V_{CM} = 0.2 V$ to 1.9 V, $G = 4$	81	105		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Each single-ended output, $G = 4$	±2.90	±2.95		V
Output Current			25		mA
Capacitive Load Drive	20% overshoot, $V_0$ , dm = 200 mV p-p		20		pF
POWER SUPPLY					
Operating Range		2.7		12	V
Quiescent Current			2.2	2.4	mA
Quiescent Current—Disable			10	16	μA
Power Supply Rejection Ratio (PSRR)					
+PSRR	$PSRR = V_{OS, dm}/\Delta V_S, G = 4$	86	100		dB
–PSRR		86	110		dB
DISABLE					
DIS Input Voltage	Disabled, DIS = High		≥1.5		V
	Enabled, DIS = Low		≤1.0		V
DIS Input Current	Disabled, DIS = High		5.5	8	μA
-	Enabled, DIS = Low		4	6	μA
Turn-On Time			0.7		μs
Turn-Off Time			30		μs

 $T_A = 25^{\circ}$ C,  $V_S = 5$  V, OUT+ connected to FB (G = 2),  $R_{L, dm} = 1 \text{ k}\Omega$ , REF = 2.5 V, unless otherwise noted.

### Table 2.

Parameter	Conditions	Min	Тур	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	$V_0 = 0.1 V p - p$	22	31		MHz
	$V_0 = 2.0 \text{ V p-p}$	4.9	7		MHz
Overdrive Recovery Time	+Recover/-Recoverv		200/600		ns
Slew Rate	$V_0 = 2V$ step		24.5		V/us
Settling Time 0.005%	$V_0 = 6 V p p step$		610		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion	fc = 40 kHz, Vo = 2 V р-р, HD2/HD3		-118/-119		dBc
	$f_c = 100 \text{ kHz}, V_0 = 2 \text{ V p-p}, \text{HD2/HD3}$		-110/-112		dBc
	$f_c = 1 \text{ MHz}, V_0 = 2 \text{ V p-p}, \text{HD2/HD3}$		-83/-73		dBc
RTO Voltage Noise	f = 100 kHz		10.2		nV/√Hz
Input Current Noise	f = 100 kHz		1.6		pA/√Hz
DC PERFORMANCE					
Differential Output Offset Voltage			0.2	0.8	mV
Differential Input Offset Voltage Drift			1.0		µV/°C
Single-Ended Input Offset Voltage	Amp A1 or Amp A2		0.1	0.4	mV
Single-Ended Input Offset Voltage Drift			0.3		µV/°C
Input Bias Current	IN and REF		3	4.5	μA
Input Offset Current	IN and REF		0.1		μA
Gain	(+OUT – –OUT)/(IN – REF)	1.98	2	2.01	V/V
Gain Error		-1		+1	%
Gain Error Drift			0.005		%/°C
INPUT CHARACTERISTICS					
Input Resistance	IN-and-REF		24		MΩ
Input Capacitance	IN and REF		1.4		pF
Input Common-Mode Voltage Range		0.2		3.9	V
Common-Mode Rejection Ratio (CMRR)	$CMRR = V_{OS, dm}/V_{CM}, VREF = VIN, V_{CM} = 0.2 V to 3.9 V, G = 4$	84	106		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Each single-ended output, G = 4	±4.85	±4.93		V
Output Current			25		mA
Capacitive Load Drive	20% overshoot, V <sub>0</sub> , dm = 200 mV p-p		20		pF
POWER SUPPLY					
Operating Range		2.7		12	V
Quiescent Current			2.3	2.6	mA
Quiescent Current—Disable			12	20	μΑ
Power Supply Rejection Ratio (PSRR)					
+PSRR	$PSRR = V_{OS, dm}/\Delta V_S, G = 4$	87	100		dB
–PSRR		87	110		dB
DISABLE					
DIS Input Voltage	Disabled, DIS = High		≥1.5		V
	Enabled, DIS = Low		≤1.0		V
DIS Input Current	Disabled, DIS = High		5.5	8	μΑ
	Enabled, DIS = Low		4	6	μΑ
Turn-On Time			0.7		μs
Turn-Off Time			30		μs

 $T_A = 25^{\circ}$ C,  $V_S = \pm 5$  V, OUT+ connected to FB (G = 2),  $R_{L,dm} = 1$  k $\Omega$ , REF = 0 V, unless otherwise noted.

#### Table 3.

$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Parameter	Conditions	Min	Тур	Max	Unit
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	DYNAMIC PERFORMANCE					
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	–3 dB Bandwidth	V <sub>o</sub> = 0.1 V p-p	23	32		MHz
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		V <sub>0</sub> = 2.0 V p-p	5.2	7.5		MHz
Silew Rate Settling Time 0.005% NOISE/DISTORTION PERFORMANCE Harmonic DistortionV_0 = 12 V p.p step $26$ Vijs 980Vijs nsNOISE/DISTORTION PERFORMANCE Harmonic Distortionfr = 400 kHz, Vo = 2 V p. ph.D2/HD3 fr = 100 kHz-109/-112dBcRTO Voltage Noise Input Current Noisefr = 100 kHz10.2nV/VHzDIFferential Output Offset Voltage Differential Input Offset Voltage Drift Input Current Noiseadv0.20.8mVDIFferential Output Offset Voltage Differential Output Offset Voltage Drift Input Griset Voltage Drift Input Griset Voltage Drift Input Griset Voltage Drift Input Offset Voltage Drift Input Offset Voltage Drift Input Offset Voltage Drift Input Griset Current Input Griset CurrentAmp A1 or Amp A20.10.4mVGain Error Gain Error DriftIN and REF Input Common-Mode Voltage Range Common-Mode Voltage RangeIN and REF IN and REF1.822.01VVInput Capacitance Output Current Quiescent Current DISIngle-Ended DiveEach single-ended output, G = 4VVOperating Range Quiescent Current Disabled, DIS = Low2.71.2VVDisabled, DIS = Low2.71.0dB2.7mADisabled, DIS = LowS7100JAJAJADisabled, DIS = LowGain Grino Quiescent CurrentS710JADisabled, DIS	Overdrive Recovery Time	+Recover/-Recovery		200/650		ns
Setting Time 0.005%         Vo = 12 V p-p step         980         ns           NOISE/DISTORTION PERFORMANCE $f_c = 40  \text{kHz}, V_0 = 2  V p-p, HD2/HD3$ $-118/-119$ dBc           Harmonic Distortion $f_c = 100  \text{kHz}, V_0 = 2  V p-p, HD2/HD3$ $-109/-112$ dBc           RTO Voltage Noise $f_c = 100  \text{kHz}, V_0 = 2  V p-p, HD2/HD3$ $-009/-112$ dBc           Input Current Noise $f = 100  \text{kHz}, V_0 = 2  V p-p, HD2/HD3$ $-002/-000$ $NV/VHz$ Differential Output Offset Voltage Drift $10.6$ $0.2$ $0.8$ mV           Single-Ended Input Offset Voltage Drift         IN and REF $0.1$ $0.4$ $M/VC$ Input Offset Current         IN and REF $1.98$ $2$ $2.01$ $VV$ Gain         (+OUTOUT)/(IN - REF) $1.98$ $2$ $2.01$ $VV$ Input Offset Current         IN and REF $-1$ $+1$ $\%$ Input Capacitance         IN and REF $-4.8$ $+3.9$ $V$ Common-Mode Rejection Ratio (CMRR)         CMRR = V_{0xim}/V_{0xi}, VRE = VIN, V_{0x} = 0.25 $V_{5} \pm 0.14$ $V$ Output Contanda t	Slew Rate	$V_0 = 2 V step$		26		V/µs
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Settling Time 0.005%	$V_0 = 12 V p - p step$		980		ns
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	NOISE/DISTORTION PERFORMANCE					
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Harmonic Distortion	$f_{c} = 40 \text{ kHz}, V_{0} = 2 \text{ V p-p}, \text{HD2/HD3}$		-118/-119		dBc
RTO Voltage Noise $f_c = 1 MHz$ , $V_0 = 2 V p-p$ , HD2/HD3 $-84/-75$ dBcInput Current Noise $f = 100 \text{ kHz}$ $10.2$ $nV/VHz$ DC PERFORMANCE $1.6$ $pA/VHz$ Differential Output Offset Voltage $nV$ $1.6$ $pA/VHz$ Differential Input Offset Voltage Drift $nV$ $1.0$ $uV''C$ Single-Ended Input Offset Voltage Drift $nM$ A1 or Amp A2 $0.1$ $0.4$ $mV''C$ Input Bias CurrentIN and REF $0.1$ $\mu$ $\mu$ Input Offset CurrentIN and REF $0.1$ $\mu$ $\mu$ Gain Error $0.1$ $\mu$ $\mu$ $\mu$ Gain Error DriftIN and REF $0.05$ $\theta$ $\theta$ Input CapacitanceIN and REF $0.05$ $\theta$ $\theta$ Input CapacitanceIN and REF $1.4$ $pF$ $\theta$ Input CapacitanceIN and REF $1.4$ $pF$ $\theta$ Input CapacitanceIN and REF $-4.8$ $-4.8$ $+3.9$ $V$ Common-Mode Rejection Ratio (CMRR) $V_{cut}=4.8V to +3.9V, G = 4$ $V_5 - 0.25$ $V_5 \pm 0.14$ $V$ Output Voltage Swing $0$ $CMR = V_{0.4m}/\Delta_{V_3} G = 4$ $RT$ $TT$ $V$ Quiescent Current $20\%$ overshoot, $V_0$ , $dm = 200 mV p-p$ $20$ $pF$ $P$ POWER SUPPLY $2.5$ $2.7$ $T$ $12$ $V$ Quiescent Current $2.6\%$ overshoot, $V_0$ , $dm = 200 mV p-p$ $2.7$ $12$ $V$ Disabled, DIS = High $2 - 3$ $V$ $V$ <t< td=""><td></td><td>f<sub>c</sub> = 100 kHz, V<sub>o</sub> = 2 V p-p, HD2/HD3</td><td></td><td>-109/-112</td><td></td><td>dBc</td></t<>		f <sub>c</sub> = 100 kHz, V <sub>o</sub> = 2 V p-p, HD2/HD3		-109/-112		dBc
RTO Voltage Noise Input Current Noise $f = 100 \text{ kHz}$ $10.2$ $nV/hz$ Input Current Noise $f = 100 \text{ kHz}$ $1.6$ $pA//Hz$ D/FREPORMANCE Differential loput Offset Voltage Drift Single-Ended Input Offset Voltage Drift $n0$ $0.2$ $0.8$ $mV$ Single-Ended Input Offset Voltage Drift Input Diffset Voltage DriftAmp A1 or Amp A2 $0.11$ $0.4$ $mV$ Gain Error Gain Error DriftIN and REF $0.11$ $\mu A$ $\mu A$ Gain Error Drift $0.005$ $\theta/C$ $\theta/C$ INPUT CHARACTERISTICSIN and REF $0.005$ $\theta/C$ Input Offset Voltage Range Common-Mode Voltage RangeIN and REF $1.4$ $\rho F$ Output Current Output Voltage Swing Output Voltage SwingEach single-ended output, G = 4 $V_5 - 0.25$ $V_5 \pm 0.14$ $V$ Output Voltage Swing Output Voltage Swing Output Voltage SwingEach single-ended output, G = 4 $2.7$ $12$ $V$ Operating Range Operating Range Operating Range $2.7$ $12$ $V$ $V$ Output Voltage Swing Output Voltage SwingEach single-ended output, G = 4 $87$ $100$ $dB$ Disabled, DIS = High PSR = Vos, $dm/AV_{S_2}$ G = 4 $87$ $100$ $dB$ $dB$ DIS Input Current Operating Range DIS Input CurrentDisabled, DIS = High Enabled, DIS = Low $2-3$ $V$ $V$ DIS Input Current DISabled, DIS = High Enabled, DIS = Low $2-3$ $V$ $V$ DIS Input Current DISabled, DIS = Low $3.0$ $4.5$		f <sub>c</sub> = 1 MHz, V <sub>o</sub> = 2 V p-p, HD2/HD3		-84/-75		dBc
$\begin{array}{ c c c c c } \mbox{Input Current Noise} & f = 100 \mbox{ Hz} & 1.6 & pA//Hz \\ \hline DC PERFORMANCE & 0.2 & 0.8 & mV \\ \hline Differential louptol Offset Voltage Drift & 1.0 & 1.0 & \muV/^C \\ Single-Ended Input Offset Voltage Drift & 1.0 & mV \\ \mbox{Single-Ended Input Offset Voltage Drift & 1.0 & 1.0 & \muV/^C \\ \mbox{Input Bias Current & IN and REF & 3.3 & 4.5 & \muA \\ \mbox{Input Offset Current & IN and REF & 0.1 & \muA \\ \mbox{Gain Error Drift & 0.005 & 96/^C \\ \mbox{Gain Error Drift & 0.005 & 96/^C \\ \mbox{Input Capacitance & IN and REF & 1.4 & pF \\ \mbox{Input Capacitance & IN and REF & 1.4 & pF \\ \mbox{Input Capacitance & IN and REF & 1.4 & pF \\ \mbox{Input Capacitance & IN and REF & 2.4 & 4.3.9 & V \\ \mbox{Output Corrent & 0.005 & 96/^C \\ \mbox{Input Gapacitance & IN and REF & & - & - & 24 & M\Omega \\ \mbox{Input Gapacitance & IN and REF & - & -4.8 & 4.3.9 & V \\ \mbox{Output Corrent & 0.005 & 0.6 & 0.0 & 0.0 & 0 \\ \mbox{Input Gapacitance & IN and REF & - & -4.8 & 4.3.9 & V \\ \mbox{Output Voltage Swing & 0.0 & 0.0 & 0.0 & 0 & 0 & 0 \\ \mbox{Output Voltage Swing & 0.0 & 0.0 & 0.0 & 0 & 0 & 0 & 0 \\ \mbox{Output Voltage Swing & 0.0 & 0.0 & 0.0 & 0 & 0 & 0 & 0 & 0 &$	RTO Voltage Noise	f = 100 kHz		10.2		nV/√Hz
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Input Current Noise	f = 100 kHz		1.6		pA/√Hz
Differential Output Offset Voltage Differential Input Offset Voltage Drift0.20.8mVDifferential Input Offset Voltage Drift1.0 $\mu$ V/°CSingle-Ended Input Offset Voltage DriftMmp A1 or Amp A20.3 $\mu$ V/°CInput Bias CurrentIN and REF34.5 $\mu$ AGain(+OUT - OUT)/(IN - REF)1.9822.01V/VGain Error1.1+1%%%/°CINPUT CHARACTERISTICSIN and REF0.005%/°CInput CapacitanceIN and REF1.4pFInput CapacitanceIN and REF-4.84.5VOUTPUT CHARACTERISTICSIN and REF-4.8+3.9VInput CapacitanceIN and REF-4.8+3.9VOUTPUT CHARACTERISTICSCMRR = V <sub>05.60</sub> /V <sub>OW</sub> VREF = VIN, V <sub>CM</sub> = -4.8 V to +3.9 V, G = 4V-4.8+3.9OUTPUT CHARACTERISTICSEach single-ended output, G = 4V_S ± 0.14VVOutput Voltage SwingEach single-ended output, G = 4V_S ± 0.25V_S ± 0.14VOutput Current20% overshoot, Vo, dm = 200 mV p-p20pFPPOWER SUPPLY2.52.7mAdBOutput Voltage Ing Range2.712VQuiescent CurrentdBOutput VoltageDisabled, DIS = High2.712VPOWER Supply Rejection Ratio (PSRN)+PSR87110dBPSRBLDisabled, DIS = High2-3VVDIS Input Voltage </td <td>DC PERFORMANCE</td> <td></td> <td></td> <td></td> <td></td> <td></td>	DC PERFORMANCE					
Differential Input Offset Voltage Drift Single-Ended Input Offset Voltage Drift $\mu M$ An or Amp A2 $1.0$ $\mu M^{V/C}$ Input Bias CurrentIN and REF $3.3$ $4.5$ $\mu M^{V/C}$ Input Offset CurrentIN and REF $0.1$ $\mu M^{V/C}$ Gain(+OUTOUT)/(IN - REF) $1.98$ $2$ $2.01$ $V/V$ Gain Error $-1$ $+1$ $\%$ $\%^{V/C}$ INPUT CHARACTERISTICSInput ResistanceIN and REF $$ $$ $\%^{V/C}$ Input CapacitanceIN and REF $$ $4.8$ $+3.9$ $V$ Input Common-Mode Voltage Range $$ $-4.8$ $+3.9$ $V$ Output Voltage SwingEach single-ended output, G = 4 $V_s - 0.25$ $V_s \pm 0.14$ $V$ Output Voltage Swing $V_{con} = -4.8$ $V_s - 0.25$ $V_s \pm 0.14$ $V$ Output Voltage Swing20% overshoot, $V_0$ , $dm = 200 \text{ mV } p$ -p $20$ $pF$ POWER SUPPLY $20\%$ overshoot, $V_0$ , $dm = 200 \text{ mV } p$ -p $2.7$ $12$ $V$ Quiescent Current $2.5$ $2.7$ $A$ $A$ Quiescent Current $2.5$ $2.7$ $A$ $A$ Quiescent Current $2.5$ $A$ $A$ $A$ PSRPSR $PSR = V_{0s, dm}/\Delta V_{s}, G = 4$ $87$ $100$ $A$ DIS Input Voltage $A$ $A$ $A$ $A$ $A$ Disabled, DIS = Low $$ $A$ $A$ $A$ $A$ DIS Input Voltage $A$ $A$ $A$ $A$ <td< td=""><td>Differential Output Offset Voltage</td><td></td><td></td><td>0.2</td><td>0.8</td><td>mV</td></td<>	Differential Output Offset Voltage			0.2	0.8	mV
Single-Ended Input Offset Voltage Single-Ended Input Offset Voltage Drift Input Bias CurrentAmp A1 or Amp A20.10.4mVSingle-Ended Input Offset Voltage Drift Input Bias CurrentIN and REF34.5 $\mu$ AGain Gain Error Gain Error DriftI.9822.01V/VGain Error Drift0UT)/(IN - REF)1.9822.01V/VInput Basistance1+11%%/C%/CInput CapacitanceIN and REF24MQ%/CInput CapacitanceIN and REF24MQ%/CInput Common-Mode Voltage Range Common-Mode Voltage Range4.81.4yFyOUTPUT CHARACTERISTICSVCM = -4.8V to +3.9V, G=4wwwwOUTPUT CHARACTERISTICSVCM = -4.8V to +3.9V, G=4wywwOutput Voltage Swing Output Voltage SwingEach single-ended output, G = 4Vs = 0.25Vs ± 0.14VVOutput Voltage SupPly Operating Range POwer SupPly Rejection Ratio (PSRR)PSR = Vcs, dm/ΔVs, G = 487100KKPSRRPSRR = Vcs, dm/ΔVs, G = 487100KKKKKDIS Input Voltage DIS Input VoltageDisabled, DIS = Low $< -3$ VVKDIS Input Voltage Turn-On Time Turn-On TimeDisabled, DIS = Low $< -3$ VKKKKKKKKKKKKKKK <td< td=""><td>Differential Input Offset Voltage Drift</td><td></td><td></td><td>1.0</td><td></td><td>μV/°C</td></td<>	Differential Input Offset Voltage Drift			1.0		μV/°C
Single-Ended Input Offset Voltage DriftIN and REF0.3 $\mu/'^{C}$ Input Bias CurrentIN and REF0.1 $\mu$ AGain(+OUTOUT)/(IN - REF)1.9822.01V/VGain Error Drift-1+1%Gain Error Drift0.005%/'C%/'CINPUT CHARACTERISTICSIN and REF24MQInput CapacitanceIN and REF1.4pFInput Common-Mode Voltage RangeCMRR = Vor, dm/VCM, VREF = VIN, Vom = -4.8 V to +3.9V, G = 443.9VOUTPUT CHARACTERISTICSCMRR = Vor, dm/VCM, VREF = VIN, Vom = -4.8 V to +3.9V, G = 4V5105OUTPUT CHARACTERISTICSEach single-ended output, G = 4Vs - 0.25Vs ± 0.14VOutput Voltage Swing20% overshoot, Vo, dm = 200 mV p-p20pFPOWER SUPPLY2.712VVQuiescent Current2.52.7mAQuiescent Current2.712VQuiescent Current87100dBPower Supply Rejection Ratio (PSRR)PSRR = Vos, dm/ΔVs, G = 487100dBPostRDisabled, DIS = Low $\leq -3$ VVDIS Input VoltageDisabled, DIS = Low $\leq -4$ VDIS Input VoltageDisabled, DIS = Low $\leq -4$ VTurn-On Time0.05 $\leq -4$ V $\leq -4$ VTurn-Off Time0.05 $\leq -4$ V $\leq -4$ VDIS Input CurrentDisabled, DIS = Low $\leq -4$ <	Single-Ended Input Offset Voltage	Amp A1 or Amp A2		0.1	0.4	mV
Input Bias CurrentIN and REF34.5 $\mu A$ Input Offset CurrentIN and REF0.1 $\mu A$ Gain(+OUTOUT)/(IN - REF)1.9822.01V/VGain Error Drift-1-1+11%Gain Error DriftIN and REF0.005%/°CINPUT CHARACTERISTICSIN and REF24MQInput ResistanceIN and REF1.4pFInput CapacitanceIN and REF24MQInput Common-Mode Voltage RangeCMRR = V <sub>0S, dm</sub> /V <sub>OM</sub> , VREF = VIN, V <sub>OM</sub> = -4.8V to +3.9V, G = 443.9VOUTPUT CHARACTERISTICSEach single-ended output, G = 4Vs - 0.25Vs ± 0.14VOutput Voltage SwingEach single-ended output, G = 4Vs - 0.25Vs ± 0.14VOutput Current20% overshoot, Vo, dm = 200 mV p-p20pFPOWER SUPPLY2.712VVQuiescent Current_DisablePSR = V <sub>OS, dm</sub> /ΔV <sub>Sx</sub> , G = 487100LQuiescent Current_DisableDisabled, DIS = Low $4 = 6$ µADIS Input VoltageDisabled, DIS = Low $5 = -3$ VDIS Input VoltageDisabled, DIS = Low $4 = 6$ µATurn-On TimeInsabled, DIS = Low $4 = 6$ µATurn-On TimeInsabled, DIS = Low $4 = 6$ µATurn-Off TimeInsabled, DIS = Low $4 = 6$ µA	Single-Ended Input Offset Voltage Drift			0.3		μV/°C
$\begin{array}{ c c c c } \mbox{Input Offset Current} &  N and REF & 0.1 & \muA \\ \hline Gain Error & (+OUT - OUT)/(IN - REF) & 1.98 & 2 & 2.01 & V/V \\ \hline Gain Error Drift & -0.005 & 9//°C \\ \hline INPUT CHARACTERISTICS & IN and REF & -0.1 & 24 & M\Omega \\ \mbox{Input Capacitance} & IN and REF & -0.1 & 1.4 & pF \\ \hline Input Common-Mode Voltage Range & -4.8 & +3.9 & V \\ \hline Common-Mode Voltage Range & -4.8 & +3.9 & V \\ \hline Common-Mode Voltage Range & -4.8 & +3.9 & V \\ \hline OUTPUT CHARACTERISTICS & IN and REF & -0.1 & 0.05 & dB \\ \hline OUTPUT CHARACTERISTICS & CMRR = V_{05, dm}/V_{CM}, VREF = VIN, & 85 & 105 & dB \\ \hline OUTPUT CHARACTERISTICS & CMRR = V_{05, dm}/V_{CM}, VREF = VIN, & 25 & V_{5} \pm 0.14 & V \\ \hline Output Voltage Swing & Each single-ended output, G = 4 & V_{5} - 0.25 & V_{5} \pm 0.14 & V \\ \hline Output Current & 20\% overshoot, V_{0}, dm = 200 mV p-p & 20 & pF \\ \hline POWER SUPPLY & 21 & V \\ \hline Outescent Current & 20\% overshoot, V_{0}, dm = 200 mV p-p & 25 & 2.7 & mA \\ \hline Quiescent Current & 15 & 2.6 & \muA \\ \hline Power Supply Rejection Ratio (PSRR) & PSR = V_{05, dm}/\Delta V_{5}, G = 4 & 87 & 100 & dB \\ \hline PSR & DIS Input Voltage & Disabled, DIS = High & 2 -3 & V \\ \hline DIS Input Voltage & Disabled, DIS = Low & 5 -4 & V \\ \hline DIS Input Current & Disabled, DIS = Low & 0.7 & 10 & \muA \\ \hline Turn-On Time & 30 & \muS \\ \hline Turn-OffTime & 30 & \muS \\ \hline \ \equivable and the product a$	Input Bias Current	IN and REF		3	4.5	μΑ
Gain $(+OUT - OUT)/(IN - REF)$ 1.98         2         2.01         V/V           Gain Error Drift         -1         +1         %           INPUT CHARACTERISTICS         IN and REF         0.005         %/°C           Input Capacitance         IN and REF         1.4         pF           Input Common-Mode Voltage Range         -4.8         +3.9         V           Common-Mode Rejection Ratio (CMRR)         CMRR = V <sub>OS, dm</sub> /V <sub>OW</sub> , VREF = VIN, V <sub>OM</sub> = -4.8 V to +3.9 V, G = 4         Vs - 0.25         Vs ± 0.14         V           OUTPUT CHARACTERISTICS         Each single-ended output, G = 4         Vs - 0.25         Vs ± 0.14         V           Output Current         20% overshoot, Vo, dm = 200 mV p-p         20         pF           POWER SUPPLY         20% overshoot, Vo, dm = 200 mV p-p         2.7         12         V           Quiescent Current         2.7         12         V         Quiescent Current         µA           Quiescent Current         2.5         2.7         mA         dB           Power Supply Rejection Ratio (PSRN)         PSR         PSR         87         100         W           PIS Input Voltage         Disabled, DIS = High         2-3         V         V           DIS Input Vol	Input Offset Current	IN and REF		0.1		μΑ
Gain Error Gain Error Drift-1+1% % 0.005%/°CINPUT CHARACTERISTICS Input Resistance Input CapacitanceIN and REF24MΩInput Common-Mode Voltage Range Common-Mode Rejection Ratio (CMRR)IN and REF-4.8+3.9VOUTPUT CHARACTERISTICS Output Voltage Swing Output Voltage SwingCMRR = $V_{05, dm}/V_{CM}$ VREF = VIN, $V_{CM} = -4.8$ V to +3.9 V, G = 4-4.8Vs - 0.25Vs $\pm 0.14$ VOUTPUT CHARACTERISTICS Output Voltage Swing Output Current Capacitive Load DriveEach single-ended output, G = 4Vs - 0.25Vs $\pm 0.14$ VOutput Voltage Range Output Current Quiescent Current Quiescent Current—Disable POwer Supply Rejection Ratio (PSRR) + PSRRPSRR = $V_{05, dm}/\Delta V_{5r}$ G = 487100dBDISABLE DIS Input VoltageDisabled, DIS = High Enabled, DIS = Low $2 - 3$ VVTurn-On Time Turn-On Time Turn-Of TimeDisabled, DIS = Low46 $\mu A$	Gain	(+OUT – –OUT)/(IN – REF)	1.98	2	2.01	V/V
Gain Error Drift0.005%/°CINPUT CHARACTERISTICSIN and REF4MΩInput CapacitanceIN and REF1.4pFInput Common-Mode Voltage Range-4.8+3.9VCommon-Mode Rejection Ratio (CMRR)CMRR = $V_{05, dm}/V_{OM}$ , VREF = VIN, $V_{CM} = -4.8 V$ to +3.9 V, G = 485105dBOUTPUT CHARACTERISTICSEach single-ended output, G = 4 $V_5 - 0.25$ $V_5 \pm 0.14$ VOutput Voltage Swing Output CurrentEach single-ended output, G = 4 $V_5 - 0.25$ $V_5 \pm 0.14$ VQuiescent Current Quiescent Current + PSRR20% overshoot, $V_0$ , dm = 200 mV p-p20pFPOWER SUPPLY Operating Range Power Supply Rejection Ratio (PSRR) + PSRRPSR = $V_{05, dm}/\Delta V_5$ , G = 487100dBDISABLE DIS Input VoltageDisabled, DIS = High Enabled, DIS = Low $\geq -3$ VDIS Input Current Input CurrentDisabled, DIS = Low $4 = 6$ $\mu A$ DIS Input Current Input CurrentDisabled, DIS = Low $4 = 6$ $\mu A$ DIS Input Current Input CurrentDisabled, DIS = Low $4 = 6$ $\mu A$ DIS Input Current Input CurrentDisabled, DIS = Low $4 = 6$ $\mu A$ DIS Input Current Input CurrentDIS = Low $4 = 6$ $\mu A$ DIS Input CurrentDisabled, DIS = Low $4 = 6$ $\mu A$ DIS Input CurrentDisabled, DIS = Low $4 = 6$ $\mu A$ DIS Input CurrentDisabled, DIS = Low $4 = 6$ $\mu A$ <t< td=""><td>Gain Error</td><td></td><td>-1</td><td></td><td>+1</td><td>%</td></t<>	Gain Error		-1		+1	%
$\begin{array}{  l l l l l l l l l l l l l l l l l l $	Gain Error Drift			0.005		%/°C
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	INPUT CHARACTERISTICS					
Input CapacitanceIN and REF1.4 $\rho F$ Input Common-Mode Voltage Range Common-Mode Rejection Ratio (CMRR)CMRR = V <sub>05,dm</sub> /V <sub>04</sub> , VREF = VIN, V <sub>0M</sub> = -4.8 V to +3.9 V, G = 485105dBOUTPUT CHARACTERISTICS Output Voltage Swing Output Current Capacitive Load DriveEach single-ended output, G = 4 $V_s - 0.25$ $V_s \pm 0.14$ VPOWER SUPPLY Operating Range Quiescent Current uisscent Current Power Supply Rejection Ratio (PSRR) + PSRR20% overshoot, Vo, dm = 200 mV p-p20pFPSR - PSRRPSR = Vo <sub>5,dm</sub> /ΔVs, G = 487100dBDIS Input Voltage DIS Input Current DIS Input Current DIS Input CurrentDisabled, DIS = High Enabled, DIS = Low $\geq -3$ VVTurn-On Time Turn-On TimeDisabled, DIS = Low46 $\mu$ ATurn-Off TimeInput Current Input Current300 $\mu$	Input Resistance	IN-and REF		24		MΩ
Input Common-Mode Voltage Range Common-Mode Rejection Ratio (CMRR)-4.8+3.9V $V_{CMR} = V_{OS,dm}/V_{CMr}$ VREF = VIN, $V_{CM} = -4.8$ V to +3.9 V, G = 485105dBOUTPUT CHARACTERISTICS Output Voltage Swing Output Current Capacitive Load DriveEach single-ended output, G = 4Vs - 0.25Vs ± 0.14VOUTPUT CHARACTERISTICS Output Current Capacitive Load Drive20% overshoot, Vo, dm = 200 mV p-p20pFPOWER SUPPLY Operating Range Quiescent Current Quiescent Current—Disable +PSRR -PSRR2.712VPSR = Vos, dm/ΔVs, G = 487100dBDIS Input VoltageDisabled, DIS = High Enabled, DIS = Low2-3VDIS Input Current Disabled, DIS = Low710µATurn-On Time Turn-Off Time300µsµs	Input Capacitance	IN and REF		1.4		pF
Common-Mode Rejection Ratio (CMRR)CMRR = $V_{OS, dm}/V_{OM}$ , VREF = VIN, $V_{CM} = -4.8 V \text{ to } +3.9 V$ , G = 485105dBOUTPUT CHARACTERISTICSEach single-ended output, G = 4 $V_5 - 0.25$ $V_5 \pm 0.14$ VOutput Voltage SwingEach single-ended output, G = 4 $V_5 - 0.25$ $V_5 \pm 0.14$ VOutput Current20% overshoot, Vo, dm = 200 mV p-p20pFPOWER SUPPLY20% overshoot, Vo, dm = 200 mV p-p20VOperating Range2.712VQuiescent Current2.52.7mAQuiescent Current1526 $\mu A$ Power Supply Rejection Ratio (PSRR)PSRR = $V_{OS, dm}/\Delta V_S$ , G = 487100dB+PSRRPSRR = $V_{OS, dm}/\Delta V_S$ , G = 487100dBDIS Input VoltageDisabled, DIS = High $2 - 3$ VVDIS Input CurrentDisabled, DIS = High710 $\mu A$ Turn-On TimeTurn-Off Time30 $\mu S$ $\mu S$	Input Common-Mode Voltage Range		-4.8		+3.9	V
VCM = -4.8 V t0 +3.9 V, G = 4Vs = 0.25Vs $\pm$ 0.14VOUTPUT CHARACTERISTICSEach single-ended output, G = 4Vs = 0.25Vs $\pm$ 0.14VOutput Current20% overshoot, Vo, dm = 200 mV p-p20pFCapacitive Load Drive20% overshoot, Vo, dm = 200 mV p-p20pFPOWER SUPPLY2.712VQuiescent Current2.52.7mAQuiescent Current2.52.7mAQuiescent CurrentPSR = Vos, dm/ΔVs, G = 487100dB-PSRRPSRR = Vos, dm/ΔVs, G = 487100dBDIS Input VoltageDisabled, DIS = High $\leq$ -4VVDIS Input CurrentDisabled, DIS = High710 $\mu$ ATurn-On TimeTurn-Off Time0.7 $\mu$ s $\mu$ s	Common-Mode Rejection Ratio (CMRR)	$CMRR = V_{OS, dm}/V_{CM}, VREF = VIN,$	85	105		dB
OUTPOT CHARGETERISTICSEach single-ended output, G = 4 $V_S - 0.25$ $V_S \pm 0.14$ VOutput Voltage SwingEach single-ended output, G = 4 $V_S - 0.25$ $V_S \pm 0.14$ VOutput Current20% overshoot, Vo, dm = 200 mV p-p20pFPOWER SUPPLY2.712VOperating Range2.712VQuiescent Current2.52.7mAQuiescent Current—Disable152.6 $\mu$ APower Supply Rejection Ratio (PSRR)PSRPSR87100dB+PSRRPSRDisabled, DIS = High $\geq -3$ VVDIS Input VoltageDisabled, DIS = High $\geq -4$ VVDIS Input CurrentDisabled, DIS = High $7$ 10 $\mu$ ATurn-On TimeTurn-Of Time30 $\mu$ S $\mu$ S		$v_{CM} = -4.8 v (0 + 3.9 v, G = 4$				
Output Vorage swing Output CurrentEach single-ended Output, G = 4 $V_S = 0.23$ $V_S \pm 0.14$ $V$ Output Current Capacitive Load Drive20% overshoot, Vo, dm = 200 mV p-p $20$ pFPOWER SUPPLY2.712VOperating Range Quiescent Current Quiescent Current—Disable +PSRR2.712VPower Supply Rejection Ratio (PSRR) +PSRRPSRR = Vos, dm/ $\Delta$ Vs, G = 487100dBDISABLE DIS Input VoltageDisabled, DIS = High Enabled, DIS = Low $\geq -3$ VDIS Input CurrentDisabled, DIS = High Enabled, DIS = Low710 $\mu$ ATurn-On Time Turn-Off Time-30V	Output Voltage Swing	Each single ended output $C = 4$	V- 0.25	$V_{2} \pm 0.14$		V
Capacitive Load Drive20% overshoot, Vo, dm = 200 mV p-p20pFPOWER SUPPLY2.712VOperating Range2.712VQuiescent Current2.52.7mAQuiescent Current—Disable1526 $\mu$ APower Supply Rejection Ratio (PSRR)PSRR = Vos, dm/ $\Delta$ Vs, G = 487100dB-PSRRDISABLEDisabled, DIS = High $\geq -3$ VDIS Input VoltageDisabled, DIS = High $\geq -3$ VDIS Input CurrentDisabled, DIS = Low46Turn-On Time0.7 $\mu$ S $\mu$ STurn-Off Time30 $\mu$ S	Output Current	Lach single-ended output, G = 4	VS - 0.25	VS ± 0.14		mΔ
Capacitive20% overshood, vo, dm = 200 mV p p20prPOWER SUPPLY $2.7$ 12VOperating Range $2.7$ 12VQuiescent Current $2.5$ $2.7$ mAQuiescent Current—Disable $15$ 26 $\mu$ APower Supply Rejection Ratio (PSRR) $PSRR = V_{OS, dm}/\Delta V_{S, G} = 4$ 87100dB-PSRRPSRR = $V_{OS, dm}/\Delta V_{S, G} = 4$ 87110dBDISABLEDisabled, DIS = High $\geq -3$ VDIS Input VoltageDisabled, DIS = High $\leq -4$ VDIS Input CurrentDisabled, DIS = High710Turn-On Time0.7 $\mu$ STurn-Off Time30 $\mu$ S	Capacitive Load Drive	$20\%$ overshoot $V_{0}$ dm = $200$ mV n-n		20		nE
Operating Range Quiescent Current Quiescent Current —Disable Power Supply Rejection Ratio (PSRR) +PSRR —PSRR2.712V $PSRR = V_{OS, dm}/\Delta V_S, G = 4$ 2.52.7mA $PSRR$ PSRR = $V_{OS, dm}/\Delta V_S, G = 4$ 87100dBDISABLE DIS Input VoltageDisabled, DIS = High Enabled, DIS = Low $\geq -3$ VDIS Input CurrentDisabled, DIS = High Enabled, DIS = Low710 $\mu A$ Turn-On Time Turn-Of Time0.7 $\mu s$ $\mu s$	POWER SUPPLY	2070 Overshoot, vo, am = 200 mv p p		20		
Operating rangeInternationInternationInternationQuiescent Current Quiescent Current—Disable Power Supply Rejection Ratio (PSRR) +PSRRPSRR = Vos, dm/ $\Delta$ Vs, G = 487100dB-PSRRPSRR = Vos, dm/ $\Delta$ Vs, G = 487100dBDISABLE DIS Input VoltageDisabled, DIS = High Enabled, DIS = Low $\geq -3$ VDIS Input CurrentDisabled, DIS = High Enabled, DIS = Low $< -4$ VDIS Input CurrentDisabled, DIS = High Enabled, DIS = Low710 $\mu$ ATurn-On Time Turn-Off Time0.77 $\mu$ s	Operating Bange		27		12	v
Quiescent Current Power Supply Rejection Ratio (PSRR) +PSRR -PSRRPSRR = $V_{OS, dm}/\Delta V_{S}, G = 4$ 1526 $\mu A$ PSRR -PSRRPSRR = $V_{OS, dm}/\Delta V_{S}, G = 4$ 87100dBDISABLE DIS Input VoltageDisabled, DIS = High Enabled, DIS = Low $\geq -3$ VDIS Input CurrentDisabled, DIS = High Enabled, DIS = High Enabled, DIS = Low $< -4$ VDIS Input CurrentDisabled, DIS = High Enabled, DIS = Low $< -4$ VDIS Input CurrentDisabled, DIS = Low $< -4$ VDIS Input CurrentDisabled, DIS = Low $< 0.7$ $< \mu A$ Turn-On Time Turn-Off Time $0.7$ $\mu S$	Quiescent Current			2.5	2.7	mA
Power Supply Rejection Ratio (PSRR) +PSRRPSRR = V_{OS, dm}/\Delta V_S, G = 487100dB-PSRRPSRR = V_{OS, dm}/\Delta V_S, G = 487110dBDISABLE DIS Input VoltageDisabled, DIS = High Enabled, DIS = Low $\geq -3$ VDIS Input CurrentDisabled, DIS = High Enabled, DIS = High Enabled, DIS = Low $2 - 4$ VDIS Input CurrentDisabled, DIS = High Enabled, DIS = Low710 $\mu A$ Turn-On Time Turn-Off Time0.7 $\mu S$ $30$ $\mu S$	Oujescent Current—Disable			15	26	uА
+PSRRPSRR = $V_{OS, dm}/\Delta V_S$ , G = 487100dB-PSRR87110dBDISABLEDisabled, DIS = High $\geq -3$ VDIS Input VoltageDisabled, DIS = Low $\leq -4$ VDIS Input CurrentDisabled, DIS = High $7$ 10LowLow46 $\mu A$ Turn-On Time0.7 $\mu S$ Turn-Off Time30 $\mu S$	Power Supply Rejection Ratio (PSRR)					P
-PSRR87110dBDISABLEDisabled, DIS = High $\geq -3$ VDIS Input VoltageDisabled, DIS = Low $\leq -4$ VDIS Input CurrentDisabled, DIS = High710DIS Input CurrentDisabled, DIS = Low46Turn-On Time0.7 $\mu$ STurn-Off Time30 $\mu$ S	+PSRR	$PSRR = V_{OS, dm} / \Delta V_{S}, G = 4$	87	100		dB
DISABLE DIS Input VoltageDisabled, DIS = High Enabled, DIS = Low $\geq -3$ VDIS Input CurrentDisabled, DIS = Low $\leq -4$ VDIS Input CurrentDisabled, DIS = High Enabled, DIS = Low710 $\mu A$ Turn-On Time Turn-Off Time0.7 $\mu S$ $\mu S$	–PSRR		87	110		dB
DIS Input VoltageDisabled, DIS = High Enabled, DIS = Low $\geq -3$ VDIS Input CurrentDisabled, DIS = Low $\leq -4$ VDIS Input CurrentDisabled, DIS = High Enabled, DIS = Low710 $\mu$ ATurn-On Time Turn-Off Time0.7 $\mu$ s $\mu$ s	DISABLE					
Enabled, DIS = Low $\leq -4$ VDIS Input CurrentDisabled, DIS = High710 $\mu A$ Enabled, DIS = Low46 $\mu A$ Turn-On Time0.7 $\mu S$ Turn-Off Time30 $\mu S$	DIS Input Voltage	Disabled, DIS = High		≥ –3		V
DIS Input Current         Disabled, DIS = High         7         10         μA           Enabled, DIS = Low         4         6         μA           Turn-On Time         0.7         μs           Turn-Off Time         30         μs		Enabled, DIS = Low		≤ -4		V
Enabled, DIS = Low         4         6         μA           Turn-On Time         0.7         μs           Turn-Off Time         30         μs	DIS Input Current	Disabled, DIS = High		7	10	μA
Turn-On Time0.7μsTurn-Off Time30μs		Enabled, DIS = Low		4	6	μA
Turn-Off Time 30 µs	Turn-On Time			0.7		μs
	Turn-Off Time			30		μs

### **ABSOLUTE MAXIMUM RATINGS**

#### Table 4.

Rating
12 V
See Figure 3
–65°C to +125°C
–40°C to +85°C
300°C
150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### THERMAL RESISTANCE

 $\theta_{JA}$  is specified for the worst-case conditions, that is,  $\theta_{JA}$  is specified for a device soldered in the circuit board with its exposed paddle soldered to a pad (if applicable) on the PCB surface that is thermally connected to a copper plane, with zero airflow.

#### Table 5. Thermal Resistance

Package Type	θ」Α	οıc	Unit
8-Lead SOIC on 4-layer board	126	28	°C/W
8-Lead LFCSP with EP on 4-layer board	83	19	°C/W

#### **Maximum Power Dissipation**

The maximum safe power dissipation in the ADA4941-1 package is limited by the associated rise in junction temperature  $(T_I)$  on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4941-1. Exceeding a junction temperature of 150°C for an extended period can result in changes in the silicon devices potentially causing failure. The power dissipated in the package ( $P_D$ ) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins ( $V_s$ ) times the quiescent current ( $I_s$ ). The power dissipated due to the load drive depends upon the particular application. For each output, the power due to load drive is calculated by multiplying the load current by the associated voltage drop across the device. The power dissipated due to all of the loads is equal to the sum of the power dissipation due to each individual load. RMS voltages and currents must be used in these calculations.

Airflow increases heat dissipation, effectively reducing  $\theta_{IA}$ . In addition, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduces the  $\theta_{IA}$ . The exposed paddle on the underside of the package must be soldered to a pad on the PCB surface that is thermally connected to a copper plane to achieve the specified  $\theta_{IA}$ .

Figure 3 shows the maximum safe power dissipation in the packages vs. the ambient temperature for the 8-lead SOIC (126°C/W) and for the 8-lead LFCSP (83°C/W) on a JEDEC standard 4-layer board. The LFCSP must have its underside paddle soldered to a pad that is thermally connected to a PCB plane.  $\theta_{JA}$  values are approximations.



Figure 3. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

### **ESD CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



## **PIN CONFIGURATION AND FUNCTION DESCRIPTIONS**



### Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	FB	Feedback Input
2	REF	Reference Input
3	V+	Positive Power Supply
4	OUT+	Noninverting Output
5	OUT-	Inverting Output
6	V-	Negative Power Supply
7	DIS	Disable
8	IN	Input

### **TYPICAL PERFORMANCE CHARACTERISTICS**

Unless otherwise noted,  $V_S = 5 V$ ,  $R_{L,dm} = 1 k\Omega$ , REF = 2.5 V, DIS = LOW, OUT+ directly connected to FB (G = 2),  $T_A = 25^{\circ}C$ .



Figure 5. Small Signal Frequency Response for Various Power Supplies



Figure 6. Small Signal Frequency Response at Various Temperatures



Figure 7. Small Signal Frequency Response for Various Resistive Loads



Figure 8. Large Signal Frequency Response for Various Power Supplies



Figure 9. Large Signal Frequency Response at Various Temperatures



Figure 10. Large Signal Frequency Response for Various Resistive Loads



Figure 14. Large Signal Frequency Response for Various Gains





2

Figure 11. Small Signal Frequency Response for Various Gains



Figure 12. Small Signal Frequency Response for Various Capacitive Loads



Figure 13. REF Input Small Signal Frequency Response for Various Supplies

Figure 15. Frequency Response for Various Output Amplitudes



Figure 16. Distortion vs. Frequency for Various Loads



Figure 17. Distortion vs. Output Amplitude for Various Supplies (G = +2)



Figure 18. Distortion vs. Frequency for Various Supplies



Figure 19. Distortion vs. Frequency at Various Output Amplitudes



Figure 20. Distortion vs. Output Amplitude for Various Supplies (G = -2)



Figure 21. Distortion vs. Frequency for Various Gains



Figure 22. Small Signal Transient Response for Various Capacitive Loads



Figure 23. Small Signal Transient Response for Various Supplies







Figure 25. Input Overdrive Recovery,  $V_{\rm S} = \pm 5 V$ 



Figure 26. Large Signal Transient Response for Various Supplies







Figure 28. Input Overdrive Recovery,  $V_{\rm S} = +5 V$ 



Figure 29. Power Supply Rejection Ratio vs. Frequency



Figure 30. Power Supply Current vs. Temperature



Figure 31. Differential Output Offset Voltage vs. Temperature



Figure 32. Output Saturation Voltage vs. Temperature







Figure 34. Differential Output Offset Distribution



Figure 35. Differential Output Voltage Noise vs. Frequency



Figure 36. Input Bias Current vs. Temperature for Various Supplies



Figure 37. REF Input Bias Current vs. Temperature







Figure 39. Input Bias Current vs. Input Voltage



Figure 40. REF Input Bias Current vs. REF Input Voltage



Figure 41. Disable Supply Current vs. Temperature for Various Supplies





Figure 43. Disabled Input-to-Output Isolation vs. Frequency











### **THEORY OF OPERATION**

The ADA4941-1 is a low power, single-ended input, differential output amplifier optimized for driving high resolution ADCs. Figure 47 illustrates how the ADA4941-1 is typically connected. The amplifier is composed of an uncommitted amplifier, A1, driving a precision inverter, A2. The negative input of A1 is brought out to Pin 1 (FB), allowing for user-programmable gain. The inverting op amp, A2, provides accurate inversion of the output of A1, VOP, producing the output signal VON.



Figure 47. Basic Connections (Power Supplies Not Shown)

The voltage applied to the REF pin appears as the output common-mode voltage. Note that the voltage applied to the REF pin does not affect the voltage at the OUT+ pin. Because of this, a differential offset can exist between the outputs, while the desired output common-mode voltage is present. For example, when VOP = 3.5 V and VON = 1.5 V, the output common-mode voltage is equal to 2.5 V, just as it is when both outputs are at 2.5 V. In the first case, the differential voltage (or offset) is 2.0 V, and in the latter case, the differential voltage is 0 V. When calculating output voltages, both differential and common-mode voltages must be considered at the same time to avoid undesired differential offsets.

### **BASIC OPERATION**

In Figure 47,  $R_G$  and  $R_F$  form the external gain-setting network. VG and VREF are externally applied voltages.  $V_O$ , cm is defined as the output common-mode voltage and  $V_O$ , dm is defined as the differential-mode output voltage. The following equations can be derived from Figure 47:

$$VOP = VIN\left(1 + \frac{R_F}{R_G}\right) - VG\left(\frac{R_F}{R_G}\right)$$
(1)

$$VON = -VIN\left(1 + \frac{R_F}{R_G}\right) + VG\left(\frac{R_F}{R_G}\right) + 2(VREF)$$
(2)

$$V_{O}, dm =$$

$$VOP - VON = 2(VIN) \left( 1 + \frac{R_{F}}{R_{G}} \right) - 2VG \left( \frac{R_{F}}{R_{G}} \right) - 2(VREF)$$
<sup>(3)</sup>

$$V_{o}, cm = \left(\frac{VOP + VON}{2}\right) = VREF$$
(4)

When  $R_F = 0$  and  $R_G$  is removed, Equation 3 simplifies to the following:

$$V_{0}, dm = 2(VIN) - 2(VREF)$$
(5)



Figure 48. Dual Supply, G = 2.4, Single-Ended-to-Differential Amplifier

Figure 48 shows an example of a dual-supply connection. In this example, VG and VREF are set to 0 V, and the external  $R_F$  and  $R_G$ -network provides a noninverting gain of 1.2 in A1. This example takes full advantage of the rail-to-rail output stage. The gain equation is

$$VOP - VON = 2.4(VIN) \tag{6}$$

The in-series, 825  $\Omega$  resistor combined with Pin 8 compensates for the voltage error generated by the input offset current of A1. The linear output range of both A1 and A2 extends to within 200 mV of each supply rail, which allows a peak-to-peak differential output voltage of 19.2 V on ±5 V supplies.



Figure 49. Single +5V Supply, G=2 Single-Ended-to-Differential Amplifier

Figure 49 shows a single 5 V supply connection with A1 used as a unity gain follower. The 2.5 V at the REF pin sets the output common-mode voltage to 2.5 V. The transfer function is then

$$VOP - VON = 2(VIN) - 5 V$$
<sup>(7)</sup>

In this case, the linear output voltage is limited by A1. On the low end, the output of A1 starts to saturate and show degraded linearity when VOP approaches 200 mV. On the high end, the input of A1 becomes saturated and exhibits degraded linearity when VIN moves beyond 4 V (within 1 V of VCC). This limits the linear differential output voltage in the circuit shown in Figure 49 to about 7.6 V p-p.



Figure 50. 5 V Supply, G = 5, Single-Ended-to-Differential Amplifier

Figure 50 shows a single 5 V supply connection for G = 5. The  $R_F$  and  $R_G$  network sets the gain of A1 to 2.5, and the 2.5 V at the REF input provides a centered 2.5 V output common-mode voltage. The transfer function is then

$$VOP - VON = 5(VIN) - 5 V$$
(8)

The output range limits of A1 and A2 limit the differential output voltage of the circuit shown in Figure 50 to approximately 8.4 V p-p.

**DC ERROR CALCULATIONS** 



Figure 51 shows the major contributions to the dc output voltage error. For each output, the total error voltage can be calculated using familiar op amp concepts. Equation 9 expresses the dc voltage error present at the VOP output.

$$VOP\_error = \left(1 + \frac{R_F}{R_G}\right) \left[V_{OS}\_A1 - (I_{BP}\_A1)(R_S\_IN)\right] + (I_{BP}\_A1)R_F$$
(9)

When using data from the Specifications tables, it is often more expedient to use input offset current in place of the individual input bias currents when calculating errors. Input offset current is defined as the magnitude of the difference between the two input bias currents. Using this definition, each input bias current can be expressed in terms of the average of the two input bias currents, I<sub>B</sub>, and the input offset current, I<sub>OS</sub>, as  $I_{BP,N} = I_B \pm I_{OS}/2$ . DC errors are minimized when  $R_S = R_F || R_G$ . In this case, Equation 9 is reduced to

$$VOP\_error = \left(1 + \frac{R_F}{R_G}\right) \left[V_{OS}\_A1\right] + (I_{OS})R_F \quad (R_S = R_F || R_G)$$

Equation 10 expresses the dc voltage error present at the VON output.

$$VON\_error = -(VOP\_error) + 2[V_{OS}\_A2 - (I_{BP}\_A2)(R_{S}\_REF + 500)] + 1000(I_{BN}\_A2)$$
(10)

The internal 500  $\Omega$  resistor is provided on-chip to minimize dc errors due to the input offset current in A2. The minimum error is achieved when R<sub>s</sub>\_REF = 0  $\Omega$ . In this case, Equation 10 is reduced to

$$VON\_error = -(VOP\_error) + 2[V_{OS}\_A2] + (I_{OS})1000 \qquad (R_s\_REF = 0 \ \Omega)$$

The differential output voltage error  $V_0$ \_error, dm, is the difference between VOP\_error and VON\_error:

$$V_{0}$$
\_error,  $dm = VOP$ \_error -  $VON$ \_error (11)

The output offset voltage of each amplifier in the ADA4941-1 also includes the effects of finite common-mode rejection ratio (CMRR), power supply rejection ratio (PSRR), and dc openloop gain (A<sub>VOL</sub>).

$$V_{\rm OS} = V_{\rm OS} - nom + \frac{\Delta V_{\rm CM}}{CMRR} + \frac{\Delta V_{\rm S}}{PSRR} + \frac{\Delta VOUT}{A_{\rm VOL}}$$
(12)

where:

 $V_{OS}$ \_nom is the nominal output offset voltage without including the effects of CMRR, PSRR, and  $A_{VOL}$ .

 $\Delta$  indicates the change in conditions from nominal.

 $V_{CM}$  is the input common-mode voltage (for A1, the voltage at IN, and for A2, the voltage at REF).

 $V_s$  is the power supply voltage.

VOUT is either op amp output.

Table 7, Table 8, and Table 9 show typical error budgets for the circuits shown in Figure 48, Figure 49, and Figure 50.

 $R_F = 1.0 \text{ k}\Omega$ ,  $R_G = 4.99 \text{ k}\Omega$ ,  $R_S\_IN = 825 \Omega$ ,  $R_S\_REF = 0 \Omega$ 

Table 7. Output Voltage Error Budget for G = 2.4 AmplifierShown in Figure 48

Error Source	Typical Value	VOP_error	VON_error	Vo_dm_error
Vos_A1	0.1 mV	+0.12 mV	–0.12 mV	+0.24 mV
$I_{BP}A1$	3 μΑ	+2.48 mV	–2.48 mV	–4.96 mV
I <sub>BN</sub> _A1	3 μΑ	–2.48 mV	+2.48 mV	+4.96 mV
$V_{OS}A2$	0.1 mV	0 mV	+0.2 mV	+0.2 mV

Total  $V_0$ \_error, dm = 0.44 mV

 $R_F = 0 \Omega$ ,  $R_G = \infty$ ,  $R_S_IN = 0 \Omega$ ,  $R_S_REF = 0 \Omega$ 

Table 8. Output Voltage Error Budget for Amplifier Shownin Figure 49

Error Source	Typical Value	VOP_error	VON_error	Vo_dm_error
Vos_A1	0.1 mV	+0.1 mV	–0.1 mV	+0.2 mV
I <sub>BP</sub> _A1	3 μΑ	+2.48 mV	–2.48 mV	–4.96 mV
I <sub>BN</sub> _A1	3 μΑ	–2.48 mV	+2.48 mV	+4.96 mV
Vos_A2	0.1 mV	0 mV	+0.2 mV	+0.2 mV

Total Vo\_error, dm = 0.4 mV

 $R_F = 1.02 \text{ k}\Omega$ ,  $R_G = 665 \Omega$ ,  $R_S\_IN = 402 \Omega$ ,  $R_S\_REF = 0 \Omega$ 

Table 9. Output Voltage Error Budget for G = 5 AmplifierShown in Figure 50

Error Source	Typical Value	VOP_error	VON_error	Vo_dm_error
Vos_A1	0.1 mV	+0.25 mV	–0.25 mV	+0.5 mV
I <sub>BP</sub> _A1	3 μΑ	+1.21 mV	–1.21 mV	–2.4 mV
$I_{BN}A1$	3 μΑ	–1.21 mV	+1.21 mV	+2.4 mV
Vos_A2	0.1 mV	0 mV	+0.2 mV	+0.2 mV

Total V<sub>0</sub>\_error, dm = 0.7mV

### **OUTPUT VOLTAGE NOISE**



Figure 52. Noise Sources

Figure 52 shows the major contributors to the ADA4941-1 differential output voltage noise. The differential output noise mean-square voltage equals the sum of twice the noise meansquare voltage contributions from the noninverting channel (A1), plus the noise mean-square voltage terms associated with the inverting channel (A2).

$$\overline{V_{O}, dm_n^2} = 2\left[\left(1 + \frac{R_F}{R_G}\right) \times (\overline{vn_A I})\right]^2 + 2 \times \left[\left(1 + \frac{R_F}{R_G}\right) \times (\overline{ip_A I} \times R_S)\right]^2 + 2\left[\overline{in_A I} \times R_F\right]^2 + (13)$$

$$2\left[\sqrt{4 kTR_F}\right]^2 + 2\left[\sqrt{4 kTR_G} \times \frac{R_F}{R_G}\right]^2 + 2 \times \left[\left(1 + \frac{R_F}{R_G}\right) \times \sqrt{4 kTR_S}\right]^2 + \overline{VON_n^2}$$

where  $\overline{\text{VON}_n}^2$  is calculated as

$$\overline{VON_n}^2 = 4 \left( \overline{vn_A 2^2} \right) + 4 \left[ (\overline{ip_A 2})(500 + R_s REF) \right]^2 + \left[ 1000(\overline{in_A 2}) \right]^2 + (14) \\ 8 kT(1000) + 16 kT(500) + 16 kT(R_s REF)$$

where:

 $\overline{vn}_A 1$  and  $\overline{vn}_A 2$  are the input voltage noises of A1 and A2, each equal to 2.1 nV/ $\sqrt{\text{Hz}}$ .

 $\overline{in\_A1}$ ,  $\overline{in\_A2}$ ,  $\overline{ip\_A1}$ , and  $\overline{ip\_A2}$  are amplifier input current noise terms, each equal to 1 pA/ $\sqrt{Hz}$ .

 $R_S$ ,  $R_F$ , and  $R_G$  are the external source, feedback, and gain resistors, respectively.

kT is Boltzmann's constant times absolute temperature, equal to 4.2 x 10<sup>-21</sup> W-s at room temperature.

*Rs\_REF* is any source resistance at the REF pin.

When A1 is used as a unity gain follower, the output voltage noise spectral density is at its minimum,  $10 \text{ nV}/\sqrt{\text{Hz}}$ . Higher voltage gains have higher output voltage noise.

Table 10, Table 11, and Table 12 show the noise contributions and output voltage noise for the circuits in Figure 48, Figure 49, and Figure 50.

Noise Source	Typical Value	VOP Contribution (nV√Hz)	VON Contribution (nV $\sqrt{Hz}$ )	$V_0$ , dm Contribution (nV $\sqrt{Hz}$ )
vn_A1	2.1 nV/√Hz	2.5	2.5	5
ip_A1	1 pA/√Hz	1	1	2
in_A1	1 pA/√Hz	1	1	2
$\sqrt{4 \ kTR_F}$	4 nV/√Hz	4	4	8
$\sqrt{4 \ kTR_G}$	9 nV/√Hz	1.8	1.8	3.6
$\sqrt{4 \ kTR_s}$	3.6 nV/√Hz	4.4	4.4	8.8
vn_inverter	9.2 nV/√Hz	0	9.2	9.2
$\sqrt{R_{s}REF}$	0	0	0	0
$ip\_A2 \times R_s\_REF$	0	0	0	0
	Totals	6.8	11.4	16.5

 $R_F = 1.0 \text{ k}\Omega$ ,  $R_G = 4.99 \text{ k}\Omega$ ,  $R_S = 825 \Omega$ ,  $R_S\_REF = 0 \Omega$ .

 $\overline{vn\_inverter}$  = noise contributions from A2 and its associated internal 1 k $\Omega$  feedback resistors and 500  $\Omega$  offset current balancing resistor.

Noise Source	Typical Value	VOP Contribution (nV√Hz)	VON Contribution (nV√Hz)	V₀, dm Contribution (nV√Hz)
vn_A1	2.1 nV/√Hz	2.1	2.1	4.2
ip_A1	0	0	0	0
in_A1	0	0	0	0
$\sqrt{4 \ kTR_F}$	0	0	0	0
$\sqrt{4 \ kTR_G}$	0	0	0	0
$\sqrt{4 \ kTR_s}$	0	0	0	0
vn_inverter	9.2 nV/√Hz	0	9.2	9.2
$\sqrt{R_s\_REF}$	0	0	0	0
$\overline{ip}A2 \times R_sREF$	0	0	0	0
	Totals	2.1	9.4	10

Table 11. Output Voltage Noise, G = 2 Differential Amplifier Shown in Figure 49

 $R_F = 0 \ \Omega, R_G = \infty, R_S = 0 \ \Omega, R_S\_REF = 0 \ \Omega.$ 

Table 12. Output Voltage Noise,	G = 5 Differential Am	plifier Shown in Figure 50
1 0 2		1 0

Noise Source	Typical Value	VOP Contribution (nV√Hz)	VON Contribution (nV√Hz)	$V_o$ , dm Contribution (nV $\sqrt{Hz}$ )
vn_A1	2.1 nV/√Hz	5.25	5.25	10.5
ip_A1	1 pA/√Hz	1	1	2
in_A1	1 pA/√Hz	1	1	2
$\sqrt{4 \ kTR_F}$	4 nV/√Hz	4	4	8
$\sqrt{4 \ kTR_G}$	3.26 nV/√Hz	4.9	4.9	9.8
$\sqrt{4 \ kTR_s}$	2.54 nV/√Hz	6.54	6.54	13.1
vn_inverter	9.2 nV/√Hz	0	9.2	9.2
$\sqrt{R_s\_REF}$	0	0	0	0
$ip\_A2 \times R_s\_REF$	0	0	0	0
	Totals	10.7	14.1	23.1

 $R_F = 1.02 \text{ k}\Omega$ ,  $R_G = 665 \Omega$ ,  $R_S = 402 \Omega$ ,  $R_S\_REF = 0 \Omega$ .

1

#### FREQUENCY RESPONSE VS. CLOSED-LOOP GAIN

The operational amplifiers used in the ADA4941-1 are voltage feedback with an open-loop frequency response that can be approximated with the integrator response, as shown in Figure 53.



Figure 53. ADA4941-1 Op Amp Open-Loop Gain vs. Frequency

For each amplifier, the frequency response can be approximated by the following equations:

$$V_{O}\_AI = VIN \times \left(1 + \frac{R_F}{R_G}\right) \times \left(\frac{1}{1 + \left[\frac{R_F + R_G}{1 - R_G^-}\right] \times \frac{f}{fcr}}\right)$$
(15)

(Noninverting Response)

$$V_{O}\_A2 = VIN \times \left(\frac{-R_{F}}{R_{G}}\right) \times \left(\frac{1}{1 + \left[\frac{R_{F} + R_{G}}{R_{G}}\right] \times \frac{f}{fcr}}\right)$$
(16)

(Inverting Response)

 $f_{\rm CR}$  is the gain-bandwidth frequency of the amplifier (where the open-loop gain shown in Figure 53 equals 1).  $f_{\rm CR}$  for both amplifiers is about 50 MHz.

The inverting amplifier A2 has a fixed feedback network. The transfer function is approximately

$$V_{O-A2} = -VIN \times \left(\frac{1}{1 + \frac{2 \times f}{50 \text{ MHz}}}\right) = -VOP \times \left(\frac{1}{1 + \frac{f}{25 \text{ MHz}}}\right) (17)$$

A1's frequency response depends on the external feedback network as indicated by Equation 15. The overall differential output voltage is therefore

$$V_{0}, dm = VOP - VON = VOP + VOP \times \left(\frac{1}{1 + \frac{f}{25 \text{ MHz}}}\right)$$
(18)

1

$$V_{O}, dm = VIN \times \left(1 + \frac{R_F}{R_G}\right) \times \left(\frac{1}{1 + \left[\frac{R_F + R_G}{R_G}\right] \times \frac{f}{50 \text{ MHz}}}\right) \times (19)$$

$$\left(1 + \frac{1}{1 + \frac{f}{25 \text{ MHz}}}\right)$$

 Multiplying the terms and neglecting negligible terms leads to the following approximation:

$$V_{O}, dm = VIN \left( 1 + \frac{R_{F}}{R_{G}} \right) \times \left[ \frac{2}{\left( 1 + \left[ \frac{R_{F} + R_{G}}{R_{G}} \right] \times \frac{f}{50 \text{ MHz}} \right) \times \left( 1 + \frac{f}{25 \text{ MHz}} \right)} \right]$$
(20)

There are two poles in this transfer function, and the lower frequency pole limits the bandwidth of the differential amplifier. If VOP is shorted to IN– (A1 is a unity gain follower), the 25 MHz closed-loop bandwidth of the inverting channel limits the overall bandwidth. When A1 is operating with higher noise gains, the bandwidth is limited by A1's closed-loop bandwidth, which is inversely proportional to the noise gain  $(1 + R_F/R_G)$ . For instance, if the external feedback network provides a noise gain of 10, the bandwidth drops to 5 MHz.

## APPLICATIONS overview

The ADA4941-1 is an adjustable-gain, single-ended-to-differential voltage amplifier, optimized for driving high resolution ADCs. Single-ended-to-differential gain is controlled by one feedback network, comprised of two external resistors:  $R_F$  and  $R_G$ .

### **USING THE REF PIN**

The REF pin sets the output base line in the inverting path and is used as a reference for the input signal. In most applications, the REF pin is set to the input signal midswing level, which in many cases is also midsupply. For bipolar signals and dual power supplies, REF is generally set to ground. In single-supply applications, setting REF to the input signal midswing level provides optimal output dynamic range performance with minimum differential offset. Note that the REF input only affects the inverting signal path or VON.

Most applications require a differential output signal with the same dc common-mode level on each output. It is possible for the signal measured across VOP and VON to have a commonmode voltage that is of the desired level but not common to both outputs. This type of signal is generally avoided because it does not allow for optimal use of the amplifier's output dynamic range.

Defining VIN as the voltage applied to the input pin, the equations that govern the two signal paths are given in Equation 21 and Equation 22.

VOP = VIN (21)

$$VON = -VIN + 2 (REF)$$
(22)

When the REF voltage is set to the midswing level of the input signal, the two output signals fall directly on top of each other with minimal offset. Setting the REF voltage elsewhere results in an offset between the two outputs. The best use of the REF pin can be further illustrated by considering a single-supply case with a 10 V power supply and an input signal that varies between 2 V and 7 V. This is a case where the midswing level of the input signal is not at midsupply but is at 4.5 V. Setting the REF input at 4.5 V and neglecting offsets, Equation 21 and Equation 22 are used to calculate the results. When the input signal is at its midpoint of 4.5 V, OUT+ is at 4.5 V, as is VON. This can be considered as a base line state where the differential output voltage is 0. When the input increases to 7 V, VOP tracks the input to 7 V, and VON decreases to 2 V. This can be viewed as a positive peak signal where the differential output voltage equals 5 V. When the input signal decreases to 2 V, VOP again tracks to 2 V, and VON increases to 7 V. This can be viewed as a negative peak signal where the differential output voltage equals -5 V. The resulting differential output voltage is 10 V p-p.

The previous discussion reveals how the single-ended-todifferential gain of 2 is achieved.

# INTERNAL FEEDBACK NETWORK POWER DISSIPATION

While traditional op amps do not have on-chip feedback elements, the ADA4941-1 contains two on-chip, 1 k $\Omega$  resistors that comprise an internal feedback loop. The power dissipated in these resistors must be included in the overall power dissipation calculations for the device. Under certain circumstances, the power dissipated in these resistors could be comparable to the device's quiescent dissipation. For example, on ±5 V supplies with the REF pin tied to ground and OUT– at +4 VDC, each 1 k $\Omega$  resistor carries 4 mA and dissipates 16 mW for a total of 32 mW. This is comparable to the quiescent power and must therefore be included in the overall device power dissipation calculations. For ac signals, rms analysis is required.

### **DISABLE FEATURE**

The ADA4941-1 includes a disable feature that can be asserted to minimize power consumption in a device that is not needed at a particular time. When asserted, the disable feature does not place the device output in a high impedance or tristate condition. The disable feature is active high. See the Specifications tables for the high and low level voltage specifications.

### **ADDING A 3-POLE, SALLEN-KEY FILTER**

The noninverting amplifier in the ADA4941-1 can be used as the buffer amplifier of a Sallen-Key filter. A 3-pole, low-pass filter can be designed to limit the signal bandwidth in front of an ADC. The input signal first passes through the noninverting stage where it is filtered. The filtered signal is then passed through the inverting stage to obtain the complementary output. Figure 54 illustrates a 3-pole, Sallen-Key, low-pass filter with a -3 dB cutoff frequency of 100 kHz. The 1.69 k $\Omega$  resistor is included to minimize dc errors due to the input offset current in A1. The passive RC filters on the outputs are generally required by the ADC converter that is being driven. The frequency response of the filter is shown in Figure 55.



Figure 54. Sallen-Key, Low-Pass Filter with 100 kHz Cutoff Frequency



Figure 55. Frequency Response of the Circuit Shown in Figure 54

### **DRIVING THE AD7687 ADC**

The ADA4941-1 is an excellent driver for high resolution ADCs, such as the AD7687, as shown in Figure 56. The Sallen-Key, low-pass filter shown in Figure 54 is included in this example but is not required. The circuit shown in Figure 56 accepts single-ended input signals that swing between 0 V and 3 V.

The ADR443 provides a stable, low noise, 3 V reference that is buffered by one of the AD8032 amplifiers and applied to the AD7687 REF input, providing a differential input full-scale level of 6 V. The reference voltage is also divided by two and buffered to supply the midsupply REF level of 1.5 V for the ADA4941-1.

### **GAIN OF -2 CONFIGURATION**

The ADA4941-1 can be operated in a configuration referred to as gain of -2. Clearly, a gain of -2 can be achieved by simply swapping the outputs of a gain of +2 circuit, but the configuration described here is different. The configuration is referred to as having negative gain to emphasize that the input amplifier, A1, is operated as an inverting amplifier instead of in its usual noninverting mode. As implied in its name, the voltage gain from VIN to V<sub>o</sub>, dm is -2 V/V. See Figure 57 for the gain of -2 configuration on  $\pm 5$  V supplies.

The gain of -2 configuration is most useful in applications that have wide input swings because the input common-mode voltages are held at constant levels. The signal size is therefore constrained by the output swing limits. The gain of -2 has a low input resistance that is equal to R<sub>G</sub>.



Figure 56. ADA4941-1 Driving the AD7687 ADC



Figure 57. Gain of -2 Configuration

### **OUTLINE DIMENSIONS**





#### **ORDERING GUIDE**

Model	Temperature Range	Package Description	Package Option	Ordering Quantity	Branding
ADA4941-1YRZ <sup>1</sup>	-40°C to +125°C	8-Lead SOIC_N	R-8	98	
ADA4941-1YRZ-RL <sup>1</sup>	-40°C to +125°C	8-Lead SOIC_N	R-8	2,500	
ADA4941-1YRZ-R7 <sup>1</sup>	-40°C to +125°C	8-Lead SOIC_N	R-8	1,000	
ADA4941-1YCPZ-R21	-40°C to +125°C	8-Lead LFCSP_VD	CP-8-2	250	H0C
ADA4941-1YCPZ-RL <sup>1</sup>	-40°C to +125°C	8-Lead LFCSP_VD	CP-8-2	5,000	H0C
ADA4941-1YCPZ-R7 <sup>1</sup>	-40°C to +125°C	8-Lead LFCSP_VD	CP-8-2	1,500	H0C

 $^{1}$  Z = Pb-free part.

## NOTES

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