Broadband Modem Mixed-Signal Front End

AD9869

FEATURES

Low cost 3.3 V CMOS MxFE for broadband modems
12-bit DAC converter
- **2×/4× interpolation filter**
- **200 MSPS DAC update rate**

Integrated 17 dBm line driver with 19.5 dB gain control
12-bit, 80 MSPS, ADC converter
−12 dB to +48 dB low noise RxPGA (<3 nV/√Hz)
Third-order, programmable low-pass filter
Flexible digital data path interface
- **Half- and full-duplex operation**
- **Pin compatible with the AD9866**
- **Various power-down/reduction modes**

Internal clock multiplier (PLL)
2 auxiliary programmable clock outputs
Available in a 64-lead LFCSP_VQ

APPLICATIONS

Broadband wireline networking

FUNCTIONAL BLOCK DIAGRAM

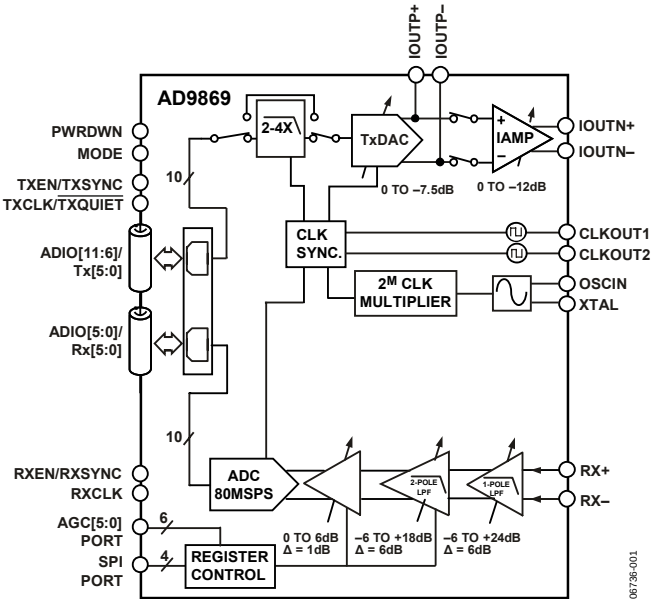

Figure 1.

GENERAL DESCRIPTION

The AD9869 is a mixed-signal front-end (MxFE®) IC for transceiver applications requiring Tx path and Rx path functionality with data rates up to 80 MSPS. A lower cost, pin-compatible version of the AD9866, the AD9869 removes the current amplifier (IAMP) IOUTP functionality and limits the PLL VCO operating range of 80 MHz to 200 MHz.

The part is well suited for half- and full-duplex applications. The digital interface is extremely flexible, allowing simple interfacing to digital back ends that support half- or full-duplex data transfers, often allowing the AD9869 to replace discrete ADC and DAC solutions. Power-saving modes include the ability to reduce power consumption of individual functional blocks or power down unused blocks in half-duplex applications. A serial port interface (SPI) allows software programming of the various functional blocks. An on-chip PLL clock multiplier and synthesizer provide all the required internal clocks, as well as two external clocks, from a single crystal or clock source.

The Tx signal path consists of a 2×/4× low-pass interpolation filter, a 12-bit TxDAC, and a line driver. The transmit path signal bandwidth can be as high as 34 MHz at an input data rate of 80 MSPS. The TxDAC provides differential current outputs that can be steered directly to an external load or to an internal low distortion current amplifier (IAMP) capable of delivering 17 dBm peak signal power. Tx power can be digitally controlled over a 19.5 dB range in 0.5 dB steps.

The receive path consists of a programmable amplifier (RxPGA), a tunable low-pass filter (LPF), and a 12-bit ADC. The low noise RxPGA has a programmable gain range of −12 dB to +48 dB in 1 dB steps. Its input referred noise is less than 3 nV/√Hz for gain settings beyond 36 dB. The receive path LPF cutoff frequency can be set over a 15 MHz to 35 MHz range or it can be simply bypassed. The 12-bit ADC achieves excellent dynamic performance up to an 80 MSPS span. Both the RxPGA and the ADC offer scalable power consumption allowing power/performance optimization.

The AD9869 provides a highly integrated solution for many broadband modems. It is available in a space-saving package, a 16-lead LFCSP, and is specified over the commercial temperature range (−40°C to +85°C).

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

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REVISION HISTORY

5/07—Revision 0: Initial Version

SPECIFICATIONS

Tx PATH SPECIFICATIONS

AVDD = 3.3 V ± 5%, DVDD = CLKVDD = DRVDD = 3.3 V ± 10%, f_{OSCIN} = 50 MHz, f_{DAC} = 200 MHz, R_{SET} = 2.0 kΩ, unless otherwise noted.

Table 1.

Parameter	Temp	Test Level[1]	Min	Typ	Max	Unit
TxDAC DC CHARACTERISTICS						
Resolution	Full			12		Bits
Update Rate	Full	II			200	MSPS
Full-Scale Output Current (IOUTP_FS)	Full	IV	2		25	mA
Gain Error[2]	25°C	I		±2		% FS
Offset Error	25°C	V		2		µA
Voltage Compliance Range	Full		−1		+1.5	V
TxDAC GAIN CONTROL CHARACTERISTICS						
Minimum Gain	25°C	V		−7.5		dB
Maximum Gain	25°C	V		0		dB
Gain Step Size	25°C	V		0.5		dB
Gain Step Accuracy	25°C	IV		Monotonic		dB
Gain Range Error	25°C	V		±2		dB
TxDAC AC CHARACTERISTICS[3]						
Fundamental				0.5		dBm
Signal-to-Noise and Distortion (SINAD)	Full	IV	66.6	69.2		dBc
Signal-to-Noise Ratio (SNR)	Full	IV	68.4	69.8		dBc
Total Harmonic Distortion (THD)	Full	IV		−79	−68.7	dBc
Spurious-Free Dynamic Range (SFDR)	Full	IV	68.5	81		dBc
IAMP DC CHARACTERISTICS						
IOUTN Full-Scale Current = IOUTN+ + IOUTN−	Full	IV	2		105	mA
AC Voltage Compliance Range	Full	IV	1		3.9	V
IAMPN AC CHARACTERISTICS[4]						
Fundamental	25°C			13		dBm
IOUTN SFDR (Third Harmonic)	Full	IV	43.3	45.2		dBc
REFERENCE						
Internal Reference Voltage[5]	25°C	I		1.23		V
Reference Error	Full	V		0.7	3.4	%
Reference Drift	Full	V		30		ppm/°C
Tx DIGITAL FILTER CHARACTERISTICS (2× Interpolation)						
Latency (Relative to $1/f_{DAC}$)	Full	V		43		Cycles
−0.2 dB Bandwidth	Full	V		0.2187		f_{OUT}/f_{DAC}
−3 dB Bandwidth	Full	V		0.2405		f_{OUT}/f_{DAC}
Stop-Band Rejection (0.289 f_{DAC} to 0.711 f_{DAC})	Full	V		50		dB
Tx DIGITAL FILTER CHARACTERISTICS (4× Interpolation)						
Latency (Relative to $1/f_{DAC}$)	Full	V		96		Cycles
−0.2 dB Bandwidth	Full	V		0.1095		f_{OUT}/f_{DAC}
−3 dB Bandwidth	Full	V		0.1202		f_{OUT}/f_{DAC}
Stop Band Rejection (0.289 f_{OSCIN} to 0.711 f_{OSCIN})	Full	V		50		dB
PLL CLK MULTIPLIER						
OSCIN Frequency Range						
PLL M Factor Set to 2	Full	IV	40		80	MHz
PLL M Factor Set to 4	Full	IV	20		50	MHz
PLL M Factor Set to 8	Full	IV	10		25	MHz
Internal VCO Frequency Range	Full	IV	80		200	MHz
Duty Cycle	Full	II	40		60	%

Parameter	Temp	Test Level[1]	Min	Typ	Max	Unit
OSCIN Impedance	25°C	V		10‖03		MΩ‖pF
CLKOUT1 Jitter[6]	25°C	III		12		ps rms
CLKOUT2 Jitter[7]	25°C	III		6		ps rms
CLKOUT1 and CLKOUT2 Duty Cycle[8]	Full	III	45		55	%

[1] See the Explanation of Test Levels section.
[2] Gain error and gain temperature coefficients are based on the ADC only (with a fixed 1.23 V external reference and a 1 V p-p differential analog input).
[3] TxDAC IOUTP_FS = 20 mA, differential output with 1:1 transformer with source and load termination of 50 Ω, f_{OUT} = 5 MHz, 4x interpolation.
[4] IOUTN full-scale current = 80 mA, f_{OSCIN} = 80 MHz, f_{DAC} =160 MHz, 2x interpolation.
[5] Use external amplifier to drive additional load.
[6] Internal VCO operates at 200 MHz; set to divide-by-1.
[7] Because CLKOUT2 is a divided-down version of OSCIN, its jitter is typically equal to OSCIN.
[8] CLKOUT2 is an inverted replica of OSCIN, if set to divide-by-1.

Rx PATH SPECIFICATIONS

AVDD = 3.3 V ± 5%, DVDD = CLKVDD = DRVDD = 3.3 V ± 10%, half- or full-duplex operation with CONFIG = 0 default power bias settings, unless otherwise noted.

Table 2.

Parameter	Temp	Test Level[1]	Min	Typ	Max	Unit
Rx INPUT CHARACTERISTICS						
Input Voltage Span						
RxPGA Gain = −10 dB	Full	III		6.33		V p-p
RxPGA Gain = +48 dB	Full	III		8		mV p-p
Input Common-Mode Voltage	25°C	III		1.3		V
Differential Input Impedance	25°C	III		400‖4.0		Ω‖pF
Input Bandwidth with RxLPF Disabled, RxPGA = 0 dB	25°C	III		53		MHz
Input Voltage Noise Density						
RxPGA Gain = 36 dB, $f_{-3\ dBF}$ = 26 MHz	25°C	III		2.7		nV/√Hz
RxPGA Gain = 48 dB, $f_{-3\ dBF}$ = 26 MHz	25°C	III		2.4		nV/√Hz
RxPGA CHARACTERISTICS						
Minimum Gain	25°C	III		−12		dB
Maximum Gain	25°C	III		48		dB
Gain Step Size	25°C	III		1		dB
Gain Step Accuracy	25°C	III		Monotonic		dB
Gain Range Error	25°C	III		0.5		dB
RxLPF CHARACTERISTICS						
Cutoff Frequency ($f_{-3\ dBF}$) Range	Full	III	15		35	MHz
Attenuation at 55.2 MHz with $f_{-3\ dBF}$ = 21 MHz	25°C	III		20		dB
Pass-Band Ripple	25°C	III		±1		dB
Settling Time						
5 dB RxPGA Gain Step @ f_{ADC} = 50 MSPS	25°C	III		20		ns
60 dB RxPGA Gain Step @ f_{ADC} = 50 MSPS	25°C	III		100		ns
ADC DC CHARACTERISTICS						
Resolution	N/A	N/A		12		Bits
Conversion Rate	Full	II	20		80	MSPS
Rx PATH LATENCY[2]						
Full-Duplex Interface	Full	V		10.5		Cycles
Half-Duplex Interface	Full	V		10.0		Cycles
Rx PATH COMPOSITE AC PERFORMANCE @ f_{ADC} = 50 MSPS[3]						
RxPGA Gain = 48 dB (Full-Scale = 8.0 mV p-p)						
Signal-to-Noise and Distortion (SINAD)	25°C	III		43.7		dBc
Total Harmonic Distortion (THD)	25°C	III		−71		dBc

Parameter	Temp	Test Level[1]	Min	Typ	Max	Unit
RxPGA Gain = 24 dB (Full-Scale = 126 mV p-p)						
Signal-to-Noise Ratio (SNR)	25°C	III		63.1		dBc
Total Harmonic Distortion (THD)	25°C	III		−67.2		dBc
RxPGA Gain = 0 dB (Full-Scale = 2.0 V p-p)						
Signal-to-Noise and Distortion (SINAD)	Full	IV		64.3		dBc
Total Harmonic Distortion (THD)	Full	IV		−67.3		dBc
Rx PATH COMPOSITE AC PERFORMANCE @ f_{ADC} = 80 MSPS[4]						
RxPGA Gain = 48 dB (Full-Scale = 8.0 mV p-p)						
Signal-to-Noise Ratio (SNR)	25°C	III		41.8		dBc
Total Harmonic Distortion (THD)	25°C	III		−67		dBc
RxPGA Gain = 24 dB (Full-Scale = 126 mV p-p)						
Signal-to-Noise Ratio (SNR)	25°C	III		58.6		dBc
Total Harmonic Distortion (THD)	25°C	III		−62.9		dBc
RxPGA Gain = 0 dB (Full-Scale = 2.0 V p-p)						
Signal-to-Noise Ratio (SNR)	25°C	II	61.1	62.9		dBc
Total Harmonic Distortion (THD)	25°C	II		−70.8	−60.8	dBc
Rx-to-Tx PATH FULL-DUPLEX ISOLATION (1 V p-p, 10 MHz Sine Wave Tx Output)						
RxPGA Gain = 40 dB						
IOUTP± Pins to RX± Pins	25°C	III		83		dBc
RxPGA Gain = 0 dB						
IOUTP± Pins to RX± Pins	25°C	III		123		dBc

[1] See the Explanation of Test Levels section.
[2] Includes RxPGA, ADC pipeline, and ADIO bus delay relative to f_{ADC}.
[3] f_{IN} = 5 MHz, AIN = −1.0 dBFS, LPF cutoff frequency set to 15.5 MHz with Register 0x08 = 0x80.
[4] f_{IN} = 5 MHz, AIN = −1.0 dBFS, LPF cutoff frequency set to 26 MHz with Register 0x08 = 0x80.

POWER SUPPLY SPECIFICATIONS

AVDD = 3.3 V, DVDD = CLKVDD = DRVDD = 3.3 V, R_{SET} = 2 kΩ, full-duplex operation with f_{DATA} = 80 MSPS[1], unless otherwise noted.

Table 3.

Parameter	Temp	Test Level[2]	Min	Typ	Max	Unit
SUPPLY VOLTAGES						
AVDD	Full	V	3.135	3.3	3.465	V
CLKVDD	Full	V	3.0	3.3	3.6	V
DVDD	Full	V	3.0	3.3	3.6	V
DRVDD	Full	V	3.0	3.3	3.6	V
IS_TOTAL (Total Supply Current)	Full	II		406	475	mA
POWER CONSUMPTION						
I_{AVDD} + I_{CLKVDD} (Analog Supply Current)	Full	IV		311	342	mA
I_{DVDD} + I_{DRVDD} (Digital Supply Current)	Full	IV		95	133	mA
POWER CONSUMPTION (Half-Duplex Operation with f_{DATA} = 50 MSPS)[3]						
Tx Mode						
I_{AVDD} + I_{CLKVDD}	25°C	IV		112	130	mA
I_{DVDD} + I_{DRVDD}	25°C	IV		46	49.5	mA
Rx Mode						
I_{AVDD} + I_{CLKVDD}	25°C	IV		225	253	mA
I_{DVDD} + I_{DRVDD}	25°C	IV		36.5	39	mA
POWER CONSUMPTION OF FUNCTIONAL BLOCKS[1] (I_{AVDD} + I_{CLKVDD})						
RxPGA and LPF	25°C	III		87		mA
ADC	25°C	III		108		mA
TxDAC	25°C	III		38		mA
IAMP (Programmable)	25°C	III	10		100	mA
Reference	25°C	III		170		mA
CLK PLL and Synthesizer	25°C	III		107		mA
MAXIMUM ALLOWABLE POWER DISSIPATION	Full	IV			1.66	W
STANDBY POWER CONSUMPTION						
IS_TOTAL (Total Supply Current)	Full			13		mA
POWER-DOWN DELAY (Using PWRDWN Pin)						
RxPGA and LPF	25°C	III		440		ns
ADC	25°C	III		12		ns
TxDAC	25°C	III		20		ns
IAMP	25°C	III		20		ns
CLK PLL and Synthesizer	25°C	III		27		ns
POWER-UP DELAY (Using PWRDWN Pin)						
RxPGA and LPF	25°C	III		7.8		µs
ADC	25°C	III		88		ns
TxDAC	25°C	III		13		µs
IAMP	25°C	III		20		ns
CLK PLL and Synthesizer	25°C	III		20		µs

[1] Default power-up settings for MODE = high and CONFIG = low, IOUTP_FS = 20 mA, does not include IAMP current consumption, which is application dependent.
[2] See the Explanation of Test Levels section.
[3] Default power-up settings for MODE = low and CONFIG = low.

DIGITAL SPECIFICATIONS

AVDD = 3.3 V ± 5%, DVDD = CLKVDD = DRVDD = 3.3 V ± 10%, R_{SET} = 2 kΩ, unless otherwise noted.

Table 4.

Parameter	Temp	Test Level[1]	Min	Typ	Max	Unit
CMOS LOGIC INPUTS						
High Level Input Voltage	Full	VI	DRVDD − 0.7			V
Low Level Input Voltage	Full	VI			0.4	V
Input Leakage Current					12	µA
Input Capacitance	Full	VI		3		pF
CMOS LOGIC OUTPUTS (C_{LOAD} = 5 pF)						
High Level Output Voltage (I_{OH} = 1 mA)	Full	VI	DRVDD − 0.7			V
Low Level Output Voltage (I_{OH} = 1 mA)	Full	VI			0.4	V
Output Rise/Fall Time						
High Strength Mode and C_{LOAD} = 15 pF	Full	VI		1.5/2.3		ns
Low Strength Mode and C_{LOAD} = 15 pF	Full	VI		1.9/2.7		ns
High Strength Mode and C_{LOAD} = 5 pF	Full	VI		0.7/0.7		ns
Low Strength Mode and C_{LOAD} = 5 pF	Full	VI		1.0/1.0		ns
RESET						
Minimum Low Pulse Width (Relative to f_{ADC})			1			Clock cycles

[1] See the Explanation of Test Levels section.

SERIAL PORT TIMING SPECIFICATIONS

AVDD = 3.3 V ± 5%, DVDD = CLKVDD = DRVDD = 3.3 V ± 10%, unless otherwise noted.

Table 5.

Parameter	Temp	Test Level[1]	Min	Typ	Max	Unit
WRITE OPERATION (See Figure 5)						
SCLK Clock Rate (f_{SCLK})	Full	IV			32	MHz
SCLK Clock High (t_{HI})	Full	IV	14			ns
SCLK Clock Low (t_{LOW})	Full	IV	14			ns
SDIO to SCLK Setup Time (t_{DS})	Full	IV	14			ns
SCLK to SDIO Hold Time (t_{DH})	Full	IV	0			ns
$\overline{SEN}$ to SCLK Setup Time (t_S)	Full	IV	14			ns
SCLK to $\overline{SEN}$ Hold Time (t_H)	Full	IV	0			ns
READ OPERATION (See Figure 6 and Figure 7)						
SCLK Clock Rate (f_{SCLK})	Full	IV			32	MHz
SCLK Clock High (t_{HI})	Full	IV	14			ns
SCLK Clock Low (t_{LOW})	Full	IV	14			ns
SDIO to SCLK Setup Time (t_{DS})	Full	IV	14			ns
SCLK to SDIO Hold Time (t_{DH})	Full	IV	0			ns
SCLK to SDIO (or SDO) Data Valid Time (t_{DV})	Full	IV			14	ns
$\overline{SEN}$ to SDIO Output Valid to High-Z (t_{EZ})	Full	IV		2		ns

[1] See the Explanation of Test Levels section.

HALF-DUPLEX DATA INTERFACE (ADIO PORT) TIMING SPECIFICATIONS

AVDD = 3.3 V ± 5%, DVDD = CLKVDD = DRVDD = 3.3 V ± 10%, unless otherwise noted.

Table 6.

Parameter	Temp	Test Level[1]	Min	Typ	Max	Unit
READ OPERATION[2] (See Figure 9)						
Output Data Rate	Full	II	20		80	MSPS
Three-State Output Enable Time (t_{PZL})	Full	II			3	ns
Three-State Output Disable Time (t_{PLZ})	Full	II			3	ns
Rx Data Valid Time (t_{VT})	Full	II	1.5			ns
Rx Data Output Delay (t_{OD})	Full	II			4	ns
WRITE OPERATION (See Figure 8)						
Input Data Rate (2× Interpolation)	Full	II	40		80	MSPS
Input Data Rate (4× Interpolation)	Full	II	20		50	MSPS
Tx Data Setup Time (t_{DS})	Full	II	1			ns
Tx Data Hold Time (t_{DH})	Full	II	2.5			ns
Latch Enable Time (t_{EN})	Full	II			3	ns
Latch Disable Time (t_{DIS})	Full	II			3	ns

[1] See the Explanation of Test Levels section.
[2] C_{LOAD} = 5 pF for digital data outputs.

FULL-DUPLEX DATA INTERFACE (Tx AND Rx PORT) TIMING SPECIFICATIONS

AVDD = 3.3 V ± 5%, DVDD = CLKVDD = DRVDD = 3.3 V ± 10%, unless otherwise noted.

Table 7.

Parameter	Temp	Test Level[1]	Min	Typ	Max	Unit
Tx PATH INTERFACE (See Figure 12)						
Input Nibble Rate (2× Interpolation)	Full	II	80		160	MSPS
Input Nibble Rate (4× Interpolation)	Full	II	40		100	MSPS
Tx Data Setup Time (t_{DS})	Full	II	2.5			ns
Tx Data Hold Time (t_{DH})	Full	II	1.5			ns
Rx PATH INTERFACE[2] (See Figure 13)						
Output Nibble Rate	Full	II	40		160	MSPS
Rx Data Valid Time (t_{DV})	Full	II	3			ns
Rx Data Hold Time (t_{DH})	Full	II	0			ns

[1] See the Explanation of Test Levels section.
[2] C_{LOAD} = 5 pF for digital data outputs.

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
ELECTRICAL	
AVDD, CLKVDD Voltage	3.9 V maximum
DVDD, DRVDD Voltage	3.9 V maximum
RX+, RX−, REFT, REFB	−0.3 V to AVDD + 0.3 V
IOUTP+, IOUTP−	−1.5 V to AVDD + 0.3 V
IOUTN+, IOUTN−	−0.3 V to +3.9 V
OSCIN, XTAL	−0.3 V to CLVDD + 0.3 V
REFIO, REFADJ	−0.3 V to AVDD + 0.3 V
Digital Input and Output Voltage	−0.3 V to DRVDD + 0.3 V
Digital Output Current	5 mA maximum
ENVIRONMENTAL	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature	125°C
Lead Temperature (Soldering, 10 sec)	150°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Thermal Resistance: 64-lead LFCSP (4-layer board).

θ_{JA} = 24°C/W (paddle soldered to ground plane, 0 LPM air).

θ_{JA} = 30.8°C/W (paddle not soldered to ground plane, 0 LPM air).

EXPLANATION OF TEST LEVELS

I. 100% production tested.

II. 100% production tested at 25°C and guaranteed by design and characterization at specified temperatures.

III. Sample tested only.

IV. Parameter is guaranteed by design and characterization testing.

V. Parameter is a typical value only.

VI. 100% production tested at 25°C and guaranteed by design and characterization for industrial temperature range.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

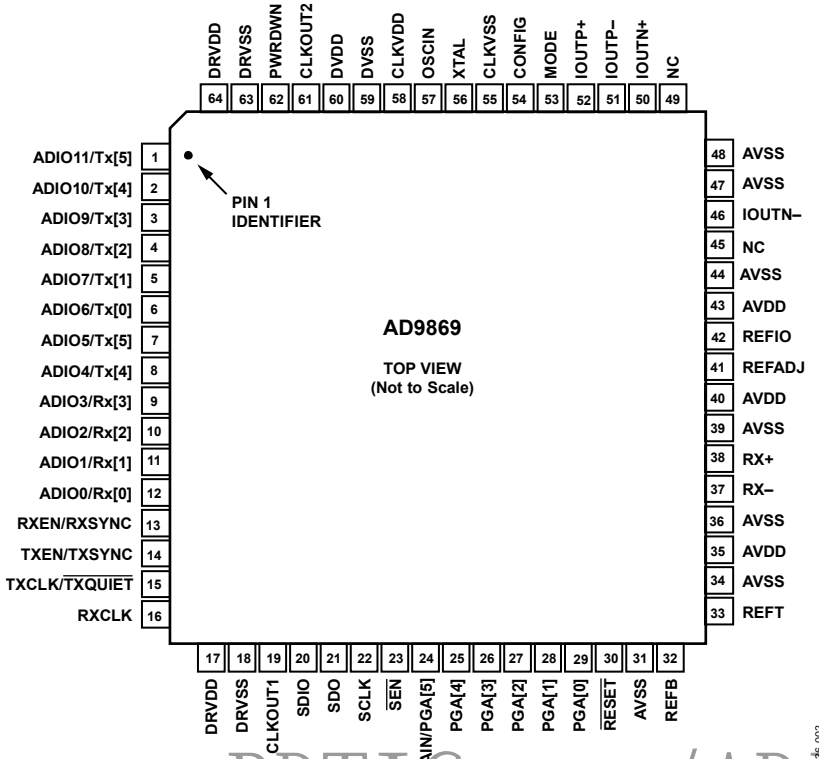

Figure 2. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Mode[1]	Description
1	ADIO11	HD	MSB of ADIO Buffer.
	Tx[5]	FD	MSB of Tx Nibble Input.
2 to 5	ADIO10 to ADIO7	HD	Bit 10 to Bit 7 of ADIO Buffer.
	Tx[4:1]	FD	Bit 4 to Bit 1 of Tx Nibble Input.
6	ADIO6	HD	Bit 6 of ADIO Buffer.
	Tx[0]	FD	LSB of Tx Nibble Input.
7	ADIO5	HD	Bit 5 of ADIO Buffer.
	Rx[5]	FD	MSB of Rx Nibble Output.
8, 9	ADIO4, ADIO3	HD	Bit 4 to Bit 3 of ADIO Buffer.
	Rx[4:3]	FD	Bit 4 to Bit 3 of Rx Nibble Output.
10	ADIO2	HD	Bit 2 of ADIO Buffer.
	Rx[2]	FD	Bit 2 of Rx Nibble Output.
11	ADIO1	HD	Bit 1 of ADIO Buffer.
	Rx[1]	FD	Bit 1 of Rx Nibble Output.
12	ADIO0	HD	LSB of ADIO Buffer.
	Rx[0]	FD	LSB of Rx Nibble Output.
13	RXEN	HD	ADIO Buffer Control Input.
	RXSYNC	FD	Rx Data Synchronization Output.
14	TXEN	HD	Tx Path Enable Input.
	TXSYNC	FD	Tx Data Synchronization Input.
15	TXCLK	HD	ADIO Sample Clock Input.
	$\overline{\text{TXQUIET}}$	FD	Fast TxDAC/IAMP Power-Down.
16	RXCLK	HD	ADIO Request Clock Input.
		FD	Rx and Tx Clock Output at 2 x f_{ADC}.

Pin No.	Mnemonic	Mode[1]	Description
17, 64	DRVDD		Digital Output Driver Supply Input.
18, 63	DRVSS		Digital Output Driver Supply Return.
19	CLKOUT1		f_{ADC}/N Clock Output (R = 1, 2, or 3).
20	SDIO		Serial Port Data Input/Output.
21	SDO		Serial Port Data Output.
22	SCLK		Serial Port Clock Input.
23	$\overline{SEN}$		Serial Port Enable Input.
24	GAIN	FD	Tx Data Port (Tx[5:0]) Mode Select.
	PGA[5]	HD or FD	MSB of PGA Input Data Port.
25 to 29	PGA[4:0]	HD or FD	Bit 4 to Bit 0 of PGA Input Data Port.
30	$\overline{RESET}$		Reset Input (Active Low).
31, 34, 36, 39, 44, 47, 48	AVSS		Analog Supply Return.
32, 33	REFB, REFT		ADC Reference Decoupling Nodes.
35, 40, 43	AVDD		Analog Power Supply Input.
37, 38	RX−, RX+		Receive Path − and + Analog Inputs.
41	REFADJ		TxDAC Full-Scale Current Adjust.
42	REFIO		TxDAC Reference Input/Output.
45, 49	NC		Do Not Connect; Leave Open.
46	IOUTN−		−Tx Mirror Current Output Sink.
50	IOUTN+		+Tx Mirror Current Output Sink.
51	IOUTP−		−TxDAC Current Output Source.
52	IOUTP+		+TxDAC Current Output Source.
53	MODE		Digital Interface Mode Select Input, Low = HD, High = FD.
54	CONFIG		Power-Up SPI Register Default Setting Input.
55	CLKVSS		Clock Oscillator/Synthesizer Supply Return.
56	XTAL		Crystal Oscillator Inverter Output.
57	OSCIN		Crystal Oscillator Inverter Input.
58	CLKVDD		Clock Oscillator/Synthesizer Supply.
59	DVSS		Digital Supply Return.
60	DVDD		Digital Supply Input.
61	CLKOUT2		f_{OSCIN}/L Clock Output (L = 1, 2, or 4).
62	PWRDWN		Power-Down Input.

[1] HD = half-duplex mode; FD = full-duplex mode.

SERIAL PORT

Table 10. SPI Register Mapping

Address (Hex)	Bit[1]	Description	Width	Power-Up Default Value			Comments
				MODE = 0 (Half-Duplex)		MODE = 1 (Full-Duplex)	
				CONFIG = 0	CONFIG = 1	CONFIG = 0	
SPI PORT CONFIGURATION AND SOFTWARE RESET							
0x00	7	4-Wire SPI	1	0	0	0	Default SPI configuration is 3-wire, MSB first.
	6	SPI LSB First	1	0	0	0	
	5	Software Reset	1	0	0	0	
POWER CONTROL REGISTERS (Via PWRDWN Pin)							
0x01	7	CLK Synthesizer	1	0	0	0	PWRDWN = 0. Default setting is for all blocks powered on.
	6	TxDAC/IAMP	1	0	0	0	
	5	Tx Digital	1	0	0	0	
	4	REF	1	0	0	0	
	3	ADC CML	1	0	0	0	
	2	ADC	1	0	0	0	
	1	PGA Bias	1	0	0	0	
	0	RxPGA	1	0	0	0	
0x02	7	CLK Synthesizer	1	0	0	0	PWRDWN = 1. Default setting is for all functional blocks powered down except PLL.
	6	TxDAC/IAMP	1	1	1	1	
	5	Tx Digital	1	1	1	1	
	4	REF	1	1	1	1	
	3	ADC CML	1	1	1	1	
	2	ADC	1	1	1	1	
	1	PGA Bias	1	1	1	1	
	0	RxPGA	1	1	1	1	
HALF-DUPLEX POWER CONTROL							
0x03	7:3	Tx OFF Delay	5	0xFF	0xFF	N/A	Default setting is for TXEN input to control power-on/power-off of Tx/Rx path. Tx driver delayed by 31 $1/f_{DATA}$ clock cycles.
	2	Rx_TXEN	1	0xFF	0xFF	N/A	
	1	Tx PWRDN	1	0xFF	0xFF	N/A	
	0	Rx PWRDN	1	0xFF	0xFF	N/A	
PLL CLOCK MULTIPLIER/SYNTHESIZER CONTROL							
0x04	4	f_{ADC} from PLL	1	0	0	0	
	3:2	PLL Divide-N	2	00	00	00	
	1:0	PLL Multiplier-M	2	01	10	01	
0x05	2	OSCIN to RXCLK	1	0	0	0	Full-duplex RXCLK normally at nibble rate.
	1	Invert RXCLK	1	0	0	0	
	0	Disable RXCLK	1	0	0	0	
0x06	7:6	CLKOUT2 Divide	2	01	01	01	Default setting is CLKOUT2 and CLKOUT1 enabled with divide-by-2.
	5	CLKOUT2 Invert	1	0	0	0	
	4	CLKOUT2 Disable	1	0	0	0	
	3:2	CLKOUT1 Divide	2	01	01	01	
	1	CLKOUT1 Invert	1	0	0	0	
	0	CLKOUT1 Disable	1	0	0	0	
Rx PATH CONTROL							
0x07	5	Initiate Offset Cal.	1	0	0	0	Default setting has LPF on. Rx path at nominal power bias setting for CONFIG = 0 and low power for CONFIG = 1.
	4	Rx Low Power	1	0	1	0	
	0	Enable Rx LPF	1	1	1	1	
0x08	7:0	Rx Filter Target Cutoff Frequency	8	0x80	0x61	0x80	Refer to the Low-Pass Filter section.

Address (Hex)	Bit[1]	Description	Width	Power-Up Default Value			Comments
				MODE = 0 (Half-Duplex)		MODE = 1 (Full-Duplex)	
				CONFIG = 0	CONFIG = 1	CONFIG = 0	
Tx/Rx PATH GAIN CONTROL							
0x09	6	Enable SPI Rx Gain	1	0x00	0x00	0x00	Default setting is for hardware Rx gain code via PGA or Tx data port.
	5:0	Rx Gain Code	6	0x00	0x00	0x00	
0x0A	6	Enable SPI Tx Gain	1	0x7F	0x7F	0x7F	Default setting is for Tx gain code via SPI control.
	5:0	Tx Gain Code	6	0x7F	0x7F	0x7F	
TxPGA AND RxPGA CONTROL							
0x0B	6	PGA Code for Tx	1	0	0	0	Default setting is RxPGA control active via PGA port.
	5	PGA Code for Rx	1	1	1	1	
	3	Force Gain Strobe	1	0	0	0	
	2	Rx Gain on Tx Port	1	0	0	1	
	1	3-Bit RxPGA Port	1	0	1	0	
Tx DIGITAL FILTER AND INTERFACE							
0x0C	7:6	Interpolation Factor	2	01	00	01	Default setting is 2× interpolation with LPF response. Data format is straight binary for half-duplex and twos complement for full-duplex interface.
	4	Invert TXEN/TXSYNC	1	0	0	0	
	3	Tx 5/5 Nibble[2]	1	N/A	N/A	0	
	2	LS Nibble First[2]	1	N/A	N/A	0	
	1	TXCLK Neg. Edge	1	0	0	0	
	0	Twos Complement	1	0	0	1	
Rx INTERFACE AND ANALOG/DIGITAL LOOPBACK							
0x0D	7	Analog Loopback	1	0	0	0	Data format is straight binary for half-duplex and twos complement for full-duplex interface. Analog loopback: ADC Rx data fed back to TxDAC. Digital loopback: Tx input data to Rx output port.
	6	Digital Loopback[2]	1	0	0	0	
	5	Rx Port Three-State	1	N/A	N/A	0	
	4	Invert RXEN/RXSYNC	1	0	0	0	
	3	Rx 5/5 Nibble	1	N/A	N/A	0	
	2	LS Nibble First	1	N/A	N/A	0	
	1	RXCLK Neg. Edge	1	0	0	0	
	0	Twos Complement	1	0	0	1	
DIGITAL OUTPUT DRIVE STRENGTH, TxDAC OUTPUT, AND REV ID							
0x0E	7	Low Digital Drive Strength	1	0	0	0	Default setting is for high drive strength and IAMP enabled.
	0	TxDAC Output	1	0	0	0	
0x0F	3:0	REV ID Number	4	0x00	0x00	0x00	
Tx IAMP GAIN AND BIAS CONTROL							
0x10	7	Select Tx Gain	1	0x04	0x04	0x04	N = 0, 1, 2, 3, 4.
	2:0	N	3	0x04	0x04	0x04	
0x12	6:4	Standing Current	3	0x01	0x01	0x01	Standing current.
	2:0	I_{OFF1} Standing Current	3	0x01	0x01	0x01	
0x13	7:5	CPGA Bias Adjust	3	0x00	0x00	0x00	Current bias setting for Rx path's functional blocks. Refer to the Power Reduction Options section.
	4:3	SPGA Bias Adjust	2				
	2:0	ADC Bias Adjust	4				

[1] Bits that are undefined should always be assigned a 0.
[2] Full-duplex only.

REGISTER MAP DESCRIPTION

The AD9869 contains a set of programmable registers (see Table 10) that are used to optimize its numerous features, interface options, and performance parameters from its default register settings. Registers pertaining to similar functions have been grouped together and assigned adjacent addresses to minimize the update time when using the multibyte serial port interface (SPI) read/write feature. Bits that are undefined within a register should be assigned a 0 when writing to that register.

The default register settings are intended to allow some applications to operate without using an SPI. The AD9869 can be configured to support a half- or full-duplex digital interface via the MODE pin, with each interface having two possible default register settings determined by the setting of the CONFIG pin.

For instance, applications that need to use only the Tx or Rx path functionality can configure the AD9869 for a half-duplex interface (MODE = 0), and use the TXEN pin to select between the Tx or Rx signal path with the unused path remaining in a reduced power state. The CONFIG pin can be used to select the default interpolation ratio of the Tx path and RxPGA gain mapping.

SERIAL PORT INTERFACE (SPI)

The serial port of the AD9869 has 3-wire or 4-wire SPI capability allowing read/write access to all registers that configure the device's internal parameters. Registers pertaining to the SPI are listed in Table 11. The default 3-wire serial communication port consists of a clock (SCLK), serial port enable ($\overline{SEN}$), and a bidirectional data (SDIO) signal. $\overline{SEN}$ is an active low, control gating, read and write cycle. When $\overline{SEN}$ is high, SDO and SDIO are three-stated. The inputs to SCLK, $\overline{SEN}$, and SDIO contain a Schmitt trigger with a nominal hysteresis of 0.4 V centered about DRVDD/2. The SDO pin remains three-stated in a 3-wire SPI interface.

Table 11. SPI Registers Pertaining to SPI Options

Address (Hex)	Bit	Description
0x00	7	Enable 4-wire SPI.
	6	Enable SPI LSB first.

A 4-wire SPI can be enabled by setting the 4-wire SPI bit high, causing the output data to appear on the SDO pin instead of on the SDIO pin. The SDIO pin serves as an input-only throughout the read operation. Note that the SDO pin is active only during the transmission of data and remains three-stated at any other time.

An 8-bit instruction header must accompany each read and write operation. The instruction header is shown in Table 12. The MSB is an R/$\overline{W}$ indicator bit with logic high indicating a read operation. The next two bits, N1 and N0, specify the number of bytes (one to four bytes) to be transferred during the data transfer cycle. The remaining five bits specify the address bits to be accessed during the data transfer portion. The data bits immediately follow the instruction header for both read and write operations.

Table 12. Instruction Header Information

MSB							LSB
17	16	15	14	13	12	11	10
R/$\overline{W}$	N1	N0	A4	A3	A2	A1	A0

The AD9869 serial port can support both MSB (most significant bit) first and LSB (least significant bit) first data formats. Figure 3 illustrates how the serial port words are built for the MSB first and Figure 4 illustrates LSB first modes. The bit order is controlled by the SPI LSB first bit (Register 0x00, Bit 6). The default value is 0, MSB first. Multibyte data transfers in MSB format can be completed by writing an instruction byte that includes the register address of the last address to be accessed. The AD9869 automatically decrements the address for each successive byte required for the multibyte communication cycle.

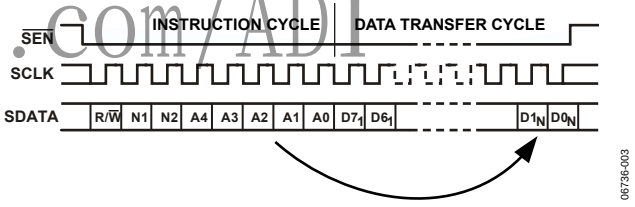

Figure 3. SPI Timing, MSB First

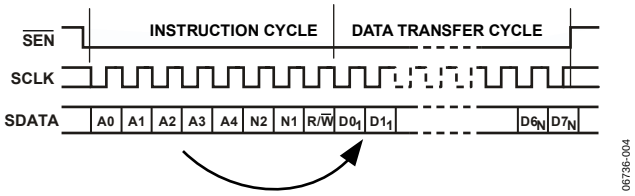

Figure 4. SPI Timing, LSB First

When the SPI LSB first bit is set high, the serial port interprets both instruction and data bytes LSB first. Multibyte data transfers in LSB format can be completed by writing an instruction byte that includes the register address of the first address to be accessed. The AD9869 automatically increments the address for each successive byte required for the multibyte communication cycle.

Figure 5 illustrates the timing requirements for a write operation to the SPI port. After the serial port enable ($\overline{SEN}$) signal goes low, data (SDIO) pertaining to the instruction header is read on the rising edges of the clock (SCLK). To initiate a write operation, the read/not-write bit is set low. After the instruction header is read, the eight data bits pertaining to the specified register are shifted into the SDIO pin on the rising edge of the next eight clock cycles. If a multibyte communication cycle is specified, the destination address is decremented (MSB first) and shifts in another eight bits of data. This process repeats until all the bytes specified in the instruction header (N1 bit, N0 bit) are shifted into the SDIO pin. $\overline{SEN}$ must remain low during the data transfer operation, only going high after the last bit is shifted into the SDIO pin.

Figure 6 illustrates the timing for a 3-wire read operation to the SPI port. After $\overline{SEN}$ goes low, data (SDIO) pertaining to the instruction header is read on the rising edges of SCLK. A read operation occurs if the read/not-write indicator is set high. After the address bits of the instruction header are read, the eight data bits pertaining to the specified register are shifted out of the SDIO pin on the falling edges of the next eight clock cycles. If a multibyte communication cycle is specified in the instruction header, a similar process as previously described for a multibyte SPI write operation applies. The SDO pin remains three-stated in a 3-wire read operation.

Figure 7 illustrates the timing for a 4-wire read operation to the SPI port. The timing is similar to the 3-wire read operation with the exception of the data appearing at the SDO pin, while the SDIO pin remains at high impedance throughout the operation. The SDO pin is an active output only during the data transfer phase and remains three-stated at all other times.

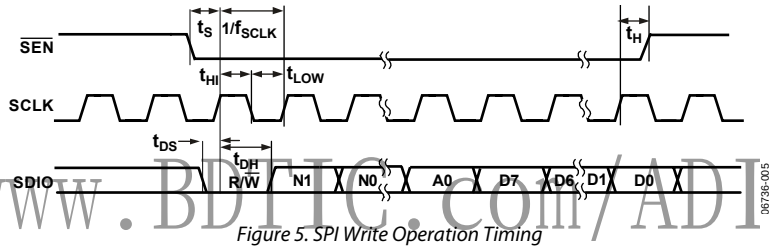

Figure 5. SPI Write Operation Timing

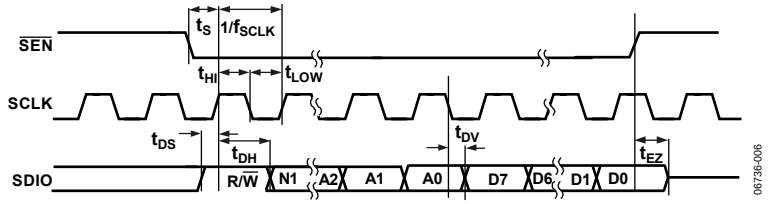

Figure 6. SPI 3-Wire Read Operation Timing

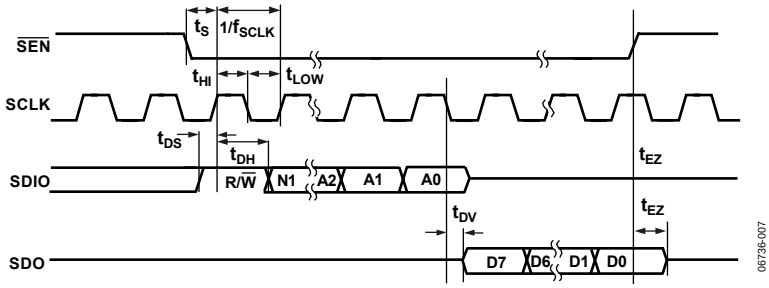

Figure 7. SPI 4-Wire Read Operation Timing

DIGITAL INTERFACE

The digital interface port is configurable for half-duplex or full-duplex operation by pin strapping the MODE pin low or high, respectively. In half-duplex mode, the digital interface port becomes a 12-bit bidirectional bus called the ADIO port. In full-duplex mode, the digital interface port is divided into two 6-bit ports called Tx[5:0] and Rx[5:0] for simultaneous Tx and Rx operations. In this mode, data is transferred between the ASIC and AD9869 in 6-bit (or 5-bit) nibbles. The AD9869 also features a flexible digital interface for updating the RxPGA and TxPGA gain registers via a 6-bit PGA port or Tx[5:0] port for fast updates, or via the SPI port for slower updates. See the RxPGA Control section for more information.

HALF-DUPLEX MODE

The half-duplex mode is selected when the MODE pin is tied low. In this mode, the bidirectional ADIO port is typically shared in burst fashion between the transmit path and receive path. Two control signals, TXEN and RXEN, from a DSP (or digital ASIC) control the bus direction by enabling the ADIO port's input latch and output driver, respectively. Two clock signals are also used, TXCLK to latch the Tx input data, and RXCLK to clock the Rx output data. The ADIO port can be disabled by setting TXEN and RXEN low (default setting), thus allowing it to be connected to a shared bus.

Internally, the ADIO port consists of an input latch for the Tx path in parallel with an output latch with three-state outputs for the Rx path. TXEN is used to enable the input latch; RXEN is used to three-state the output latch. A five-sample-deep FIFO is used on the Tx and Rx paths to absorb any phase difference between the AD9869 internal clocks and the externally supplied clocks (TXCLK, RXCLK). The ADIO bus accepts input data-words into the transmit path when the TXEN pin is high, the RXEN pin is low, and a clock is present on the TXCLK pin, as shown in Figure 8.

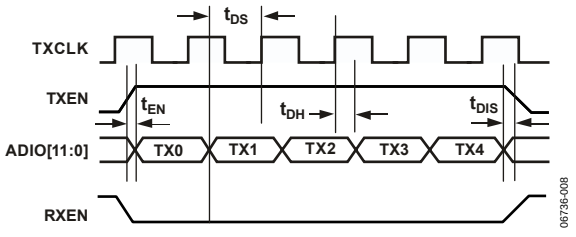

Figure 8. Transmit Data Input Timing Diagram

The Tx interpolation filter(s) following the ADIO port can be flushed with zeros if the clock signal into the TXCLK pin is present for 33 clock cycles after TXEN goes low. Note that the data on the ADIO bus is irrelevant over this interval.

The output from the receive path is driven onto the ADIO bus when the RXEN pin is high and when a clock is present on the RXCLK pin. While the output latch is enabled by RXEN, valid data appears on the bus after a 6-clock-cycle delay due to the internal FIFO delay. Note that Rx data is not latched back into the Tx path if TXEN is high during this interval with TXCLK present. The ADIO bus becomes three-stated once the RXEN pin returns low. Figure 9 shows the receive path output timing.

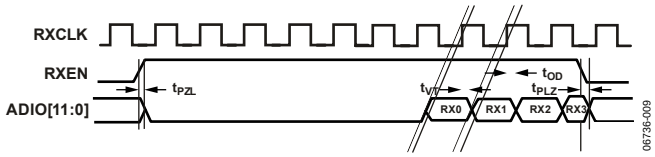

Figure 9. Receive Data Output Timing Diagram

To add flexibility to the digital interface port, several programming options are available in the SPI registers. These options are listed in Table 13. The default Tx and Rx data input formats are straight binary, but can be changed to twos complement. The default TXEN and RXEN settings are active high, but can be set to opposite polarities, thus allowing them to share the same control. In this case, the ADIO port can still be placed onto a shared bus by disabling its input latch via the control signal, and disabling the output driver via the SPI register. The clock timing can be independently changed on the transmit and receive paths by selecting either the rising or falling clock edge as the validating/sampling edge of the clock. Lastly, the output driver strength can be reduced for lower data rate applications.

Table 13. SPI Registers for Half-Duplex Interface

Address (Hex)	Bit	Description
0x0C	4	Invert TXEN.
	1	TXCLK negative edge.
	0	Twos complement.
0x0D	5	Rx port three-state.
	4	Invert RXEN.
	1	RXCLK negative edge.
	0	Twos complement.
0x0E	7	Low digital drive strength.

The half-duplex interface can be configured to act as a slave or a master to the digital ASIC. An example of a slave configuration is shown in Figure 10. In this example, the AD9869 accepts all the clock and control signals from the digital ASIC. Because the sampling clocks for the DAC and ADC are derived internally from the OSCIN signal, the TXCLK and RXCLK signals must be at exactly the same frequency as the OSCIN signal. The phase relationships among the TXCLK, RXCLK, and OSCIN signals can be arbitrary. If the digital ASIC cannot provide a low jitter clock source to OSCIN, use the AD9869 to generate the clock for its DAC and ADC and to pass the desired clock signal to the digital ASIC via CLKOUT1 or CLKOUT2.

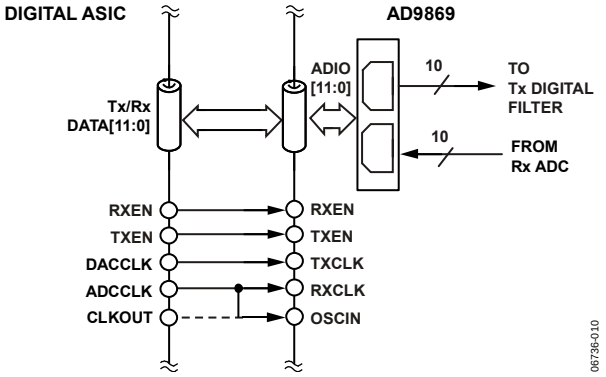

Figure 10. Example of a Half-Duplex Digital Interface with AD9869 Serving as the Slave

Figure 11 shows a half-duplex interface with the AD9869 acting as the master, generating all the required clocks. CLKOUT1 provides a clock equal to the bus data rate that is fed to the ASIC as well as back to the TXCLK and RXCLK inputs. This interface has the advantage of reducing the digital ASIC pin count by three. The ASIC needs only to generate a bus control signal that controls the data flow on the bidirectional bus.

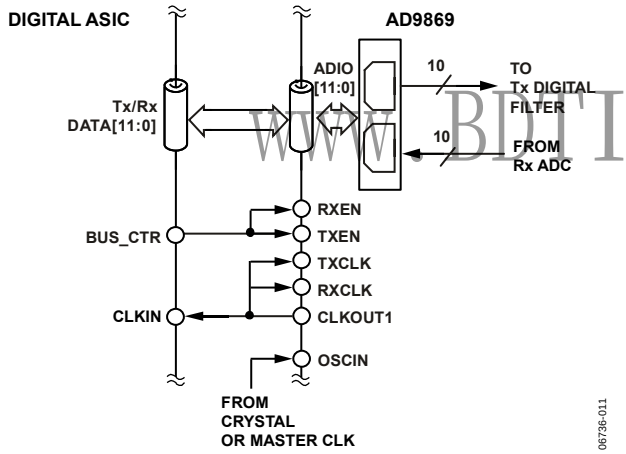

Figure 11. Example of a Half-Duplex Digital Interface with AD9869 Serving as the Master

FULL-DUPLEX MODE

The full-duplex mode interface is selected when the MODE pin is tied high. It can be used for full- or half-duplex applications. The digital interface port is divided into two 6-bit ports called Tx[5:0] and Rx[5:0], allowing simultaneous Tx and Rx operations for full-duplex applications. In half-duplex applications, the Tx[5:0] port can also be used to provide a fast update of the RxPGA during an Rx operation. This feature is enabled by default and can be used to reduce the required pin count of the ASIC (refer to RxPGA Control section for details).

In either application, Tx data and Rx data are transferred between the ASIC and AD9869 in 6-bit (or 5-bit) nibbles at twice the internal input/output word rates of the Tx interpolation filter and ADC. Note that the TxDAC update rate must not be less than the nibble rate. Therefore, the 2× or 4× interpolation filter must be used with a full-duplex interface.

The AD9869 acts as the master, providing RXCLK as an output clock that is used for the timing of both the Tx[5:0] and Rx[5:0] ports. RXCLK always runs at the nibble rate and can be inverted or disabled via an SPI register. Because RXCLK is derived from the clock synthesizer, it remains active provided that this functional block remains powered on. A buffered version of the signal appearing at OSCIN can also be directed to RXCLK by setting Bit 2 of Register 0x05. This feature allows the AD9869 to be completely powered down (including the clock synthesizer) while serving as the master.

The Tx[5:0] port operates in the following manner with the SPI register default settings:

1. Two consecutive nibbles of the Tx data are multiplexed together to form a 12-bit data-word in twos complement format.
2. The clock appearing on the RXCLK pin is a buffered version of the internal clock used by the Tx[5:0] port's input latch with a frequency that is always twice the ADC sample rate ($2 \times f_{ADC}$).
3. Data from the Tx[5:0] port is read on the rising edge of this sampling clock, as illustrated in the timing diagram shown in Figure 12. Note that $\overline{\text{TXQUIET}}$ must remain high for the reconstructed Tx data to appear as an analog signal at the output of the TxDAC or IAMP.
4. The TXSYNC signal is used to indicate which word belongs to which nibble. While TXSYNC is low, the first nibble of every word is read as the most significant nibble. The second nibble of that same word is read on the following TXSYNC high level as the least significant nibble. If TXSYNC is low for more than one clock cycle, the last transmit data is read continuously until TXSYNC is brought high for the second nibble of a new transmit word. This feature can be used to flush the interpolator filters with zeros. Note that the GAIN signal must be kept low during a Tx operation.

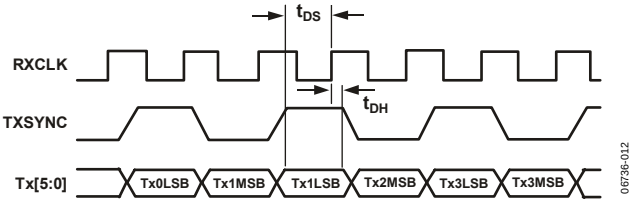

Figure 12. Tx[5:0] Port Full-Duplex Timing Diagram

The Rx[5:0] port operates in the following manner with the SPI register default settings:

1. Two consecutive nibbles of the Rx data are multiplexed together to form a 12-bit data-word in twos complement format.
2. The Rx data is valid on the rising edge of RXCLK, as illustrated in the timing diagram shown in Figure 13.
3. The RXSYNC signal is used to indicate which word belongs to which nibble. While RXSYNC is low, the first nibble of every word is transmitted as the most significant nibble. The second nibble of that same word is transmitted on the following RXSYNC high level as the least significant nibble.

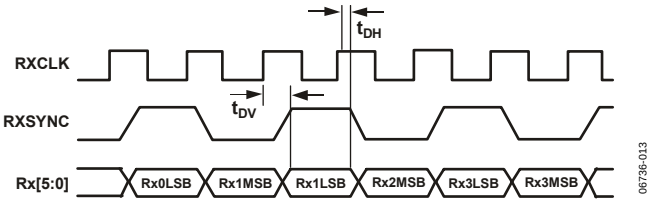

Figure 13. Full-Duplex Rx Port Timing

To add flexibility to the full-duplex digital interface port, several programming options are available in the SPI registers. These options are listed in Table 14. The timing for the Tx[5:0] and/or Rx[5:0] ports can be independently changed by selecting either the rising or falling clock edge as the sampling/validating edge of the clock. Inverting RXCLK (via Bit 1 of Register 0x05) affects both the Rx and Tx interface because they both use RXCLK.

Table 14. SPI Registers for Full-Duplex Interface

Address (Hex)	Bit	Description
0x05	2	OSCIN to RXCLK.
	1	Invert RXCLK.
	0	Disable RXCLK.
0x0B	2	Rx gain on Tx port.
0x0C	4	Invert TXSYNC.
	3	Tx 5/5 nibble.
	2	LS nibble first.
	1	TXCLK negative edge.
	0	Twos complement.
0x0D	5	Rx port three-state.
	4	Invert RXSYNC.
	3	Rx 5/5 nibble.
	2	LS nibble first.
	1	RXCLK negative edge.
	0	Twos complement.
0x0E	7	Low digital drive strength.

The default Tx and Rx data input formats are twos complement, but can be changed to straight binary. The default TXSYNC and RXSYNC settings can be changed such that the first nibble of the word appears while either TXSYNC, RXSYNC, or both are high. In addition, the least significant nibble can be selected as the first nibble of the word (least significant nibble first). The output driver strength can also be reduced for lower data rate applications.

For the AD9869, the most significant nibble defaults to 6 bits, and the least significant nibble defaults to 4 bits. This can be changed so that the least significant nibble and most significant nibble have 5 bits each. To accomplish this, set the 5/5 nibble bit (Bit 3 in Register 0x0C and Bit 3 in Register 0x0D), and use the Tx[5:1] and Rx[5:1] data pins.

Figure 14 shows a possible digital interface between an ASIC and the AD9869. The AD9869 serves as the master generating the required clocks for the ASIC. This interface requires that the ASIC reserve 16 pins for the interface, assuming a 6-bit nibble width and the use of the Tx port for RxPGA gain control. Note that the ASIC pin allocation can be reduced by 3 if a 5-bit nibble width is used and the gain (or gain strobe) of the RxPGA is controlled via the SPI port.

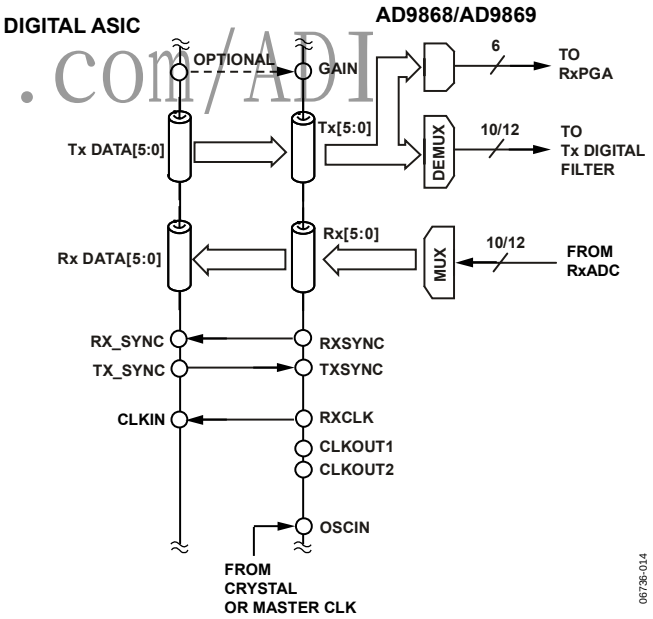

Figure 14. Example of a Full-Duplex Digital Interface with Optional RxPGA Gain Control via Tx[5:0]

RxPGA CONTROL

The AD9869 contains a digital PGA in the Rx path that is used to extend the dynamic range. The RxPGA can be programmed over −12 dB to +48 dB with 1 dB resolution using a 6-bit word, and with a 0 dB setting corresponding to a 2 V p-p input signal. The 6-bit word is fed into a look-up table (LUT) that is used to distribute the desired gain over three amplification stages within the Rx path. Upon power-up, the RxPGA gain register is set to its minimum gain of −12 dB. The RxPGA gain mapping is shown in Figure 15.

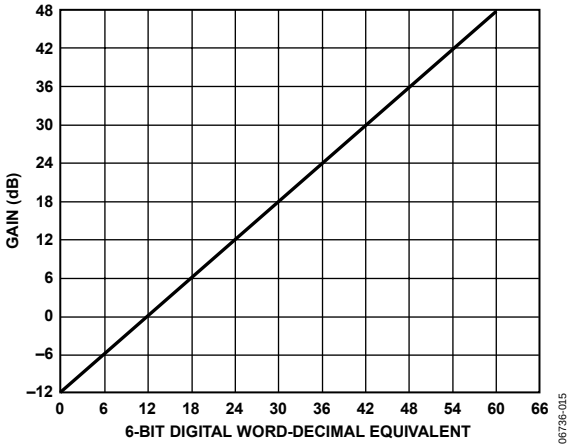

Figure 15. Digital Gain Mapping of RxPGA

Table 15 lists the SPI registers pertaining to the RxPGA.

Table 15. SPI Registers for RxPGA Control

Address (Hex)	Bit	Description
0x09	6	Enable RxPGA update via SPI.
	5:0	RxPGA gain code.
0x0B	6	Select TxPGA via PGA[5:0].
	5	Select RxPGA via PGA[5:0].
	3	Enable software gain strobe, full-duplex.
	2	Enable RxPGA update via Tx[5:0], full-duplex.
	1	3-Bit RxPGA gain mapping, half-duplex.

The RxPGA gain register can be updated via the Tx[5:0] port, the PGA[5:0] port, or the SPI port. The first two methods allow fast updates of the RxPGA gain register and should be considered for digital AGC functions requiring a fast closed-loop response. The SPI port allows direct update and readback of the RxPGA gain register via Register 0x09 with an update rate limited to 1.6 MSPS (with SCLK = 32 MHz). Note that Bit 6 of Register 0x09 must be set for a read or write operation.

Updating the RxPGA via the Tx[5:0] port is an option only in full-duplex mode[1]. In this case, a high level on the GAIN pin[2] with TXSYNC low programs the PGA setting on either the rising edge or falling edge of RXCLK, as shown in Figure 16. The GAIN pin must be held high, TXSYNC must be held low, and gain data must be stable for one or more clock cycles to update the RxPGA gain setting.

A low level on the GAIN pin enables data to be fed to the digital interpolation filter. This interface should be considered when upgrading existing designs from the AD9875/AD9876 MxFE products or from half-duplex applications trying to minimize an ASIC pin count.

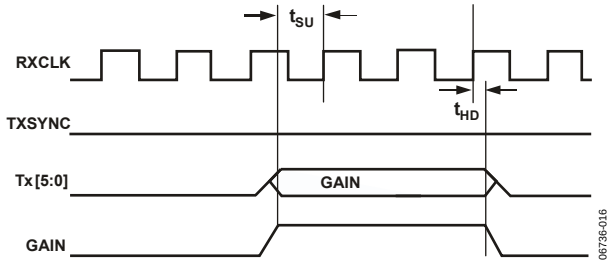

Figure 16. Updating RxPGA via Tx[5:0] in Full-Duplex Mode

Updating the RxPGA (or TxPGA) via the PGA[5:0] port is an option for both the half-duplex[3] and full-duplex interface. The PGA port consists of an input buffer that passes the 6-bit data appearing at its input directly to the RxPGA (or TxPGA) gain register with no gating signal required. Bit 5 or Bit 6 of Register 0x0B is used to select whether the data updates the RxPGA or TxPGA gain register. In applications that switch between RxPGA and TxPGA gain control via PGA[5:0], be sure that the RxPGA (or TxPGA) is not inadvertently loaded with the wrong data during a transition. In the case of an RxPGA-to-TxPGA transition, first deselect the RxPGA gain register, update the PGA[5:0] port with the desired TxPGA gain setting, and then select the TxPGA gain register.

Note that a silicon bug exists with the full-duplex interface (MODE = 1), which requires that the GAIN/PGA[5] pin remains low for the digital Tx path to remain enabled. Full-duplex protocol applications must use the SPI port to control the Tx and Rx gain. Half-duplex protocol applications using the function can use an AND gate with $\overline{\text{TXQUIET}}$ and the PGA5 bit serving as inputs to ensure that the GAIN/PGA[5] pin remains low during a Tx operation.

[1] Default setting for full-duplex mode (MODE = 1).
[2] The gain strobe can also be set in software via Register 0x0B, Bit 3 for continuous updating. This eliminates the requirement for the external gain signal, reducing the ASIC pin count by 1.
[3] Default setting for half-duplex mode (MODE = 0).

TxPGA CONTROL

The AD9869 also contains a digital PGA in the Tx path distributed between the TxDAC and IAMP. The TxPGA is used to control the peak current from the TxDAC and IAMP over a 7.5 dB and 19.5 dB span, respectively, with 0.5 dB resolution. A 6-bit word is used to set the TxPGA attenuation according to the mapping shown in Figure 17. The TxDAC gain mapping is applicable only when Bit 0 of Register 0x0E is set, and only when the 4 LSBs of the 6-bit gain word are relevant.

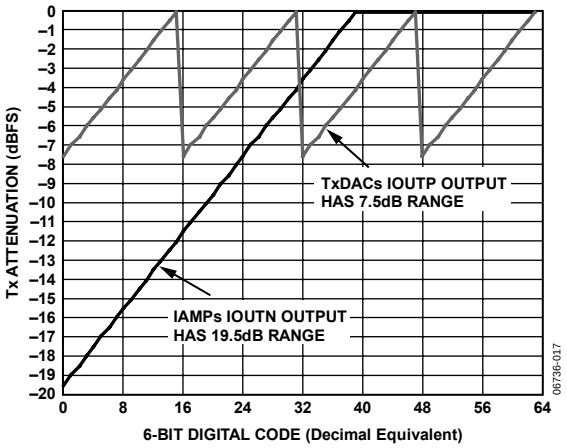

Figure 17. Digital Gain Mapping of TxPGA

The TxPGA register can be updated via the PGA[5:0] port or SPI port. The first method should be considered for fast updates of the TxPGA register. Its operation is similar to the description in the RxPGA Control section. The SPI port allows direct update and readback of the TxPGA register via Register 0x0A with an update rate limited to 1.6 MSPS (SCLK = 32 MHz). Bit 6 of Register 0x0A must be set for a read or write operation.

Table 16 lists the SPI registers pertaining to the TxPGA. The TxPGA control register default setting is for minimum attenuation (0 dBFS) with the PGA[5:0] port disabled for Tx gain control.

Table 16. SPI Registers TxPGA Control

Address (Hex)	Bit	Description
0x0A	6	Enable TxPGA update via SPI.
	5:0	TxPGA gain code.
0x0B	6	Select TxPGA via PGA[5:0].
	5	Select RxPGA via PGA[5:0].
0x0E	0	TxDAC output (IAMP disabled).

TRANSMIT PATH

The transmit path of the AD9869 (or its related part, the AD9868) consists of a selectable digital 2×/4× interpolation filter, a 12-bit (or 10-bit) TxDAC, and a current-output amplifier, IAMP (see Figure 18). Note that the additional two bits of resolution offered by the AD9869 result in a 10 dB to 12 dB reduction in the pass-band noise floor. The digital interpolation filter relaxes the Tx analog filtering requirements by simultaneously reducing the images from the DAC reconstruction process while increasing the analog filter's transition band. The digital interpolation filter can also be bypassed, resulting in lower digital current consumption.

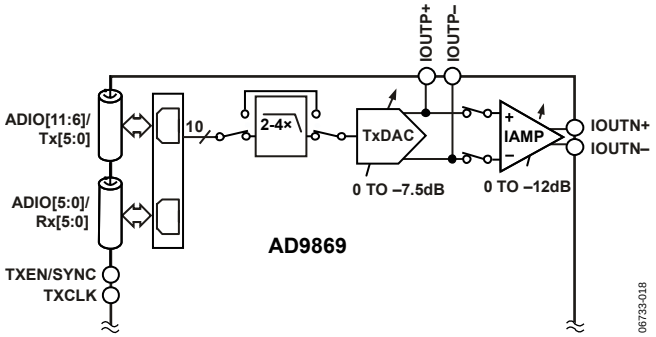

Figure 18. Functional Block Diagram of Tx Path

DIGITAL INTERPOLATION FILTERS

The input data from the Tx port can be fed into a selectable 2×/4× interpolation filter. The interpolation factor for the digital filter is set via SPI Register 0x0C with the settings shown in Table 17. The maximum input word rate, f_{DATA}, into the interpolation filter is 80 MSPS; the maximum DAC update rate is 200 MSPS. Therefore, applications with input word rates at or below 50 MSPS can benefit from 4× interpolation, whereas applications with input word rates between 50 MSPS and 80 MSPS can benefit from 2× interpolation.

Table 17. Interpolation Factor Set via SPI Register 0x0C

Bits[7:6]	Interpolation Factor
00	4
01	2
10	Do not use
11	Do not use

The interpolation filter consists of two cascaded half-band filter stages with each stage providing 2× interpolation. The first stage filter consists of 43 taps. The second stage filter, operating at the higher data rate, consists of 11 taps. The normalized wideband and pass-band filter responses (relative f_{DATA}) for the 2× low-pass interpolation filter and 4× low-pass interpolation filter are shown in Figure 19 and Figure 20, respectively.

These responses also include the inherent sinc(x) from the TxDAC reconstruction process and can be used to estimate any post analog filtering requirements.

The pipeline delays of the 2× and 4× filter responses are 21.5 clock cycles and 24 clock cycles, respectively, relative to f_{DATA}. The filter delay is also taken into consideration for applications configured for a half-duplex interface with the half-duplex power-down mode enabled. This feature allows the user to set a programmable delay that powers down the TxDAC and IAMP only after the last Tx input sample has propagated through the digital filter. See the Power Control and Dissipation section for more details.

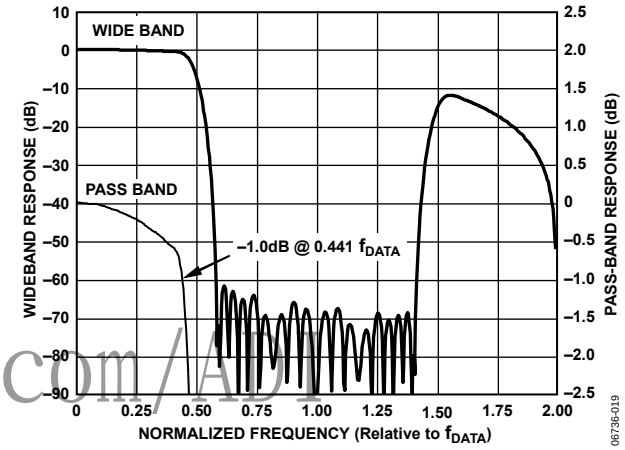

Figure 19. Frequency Response of 2× Interpolation Filter (Normalized to f_{DATA})

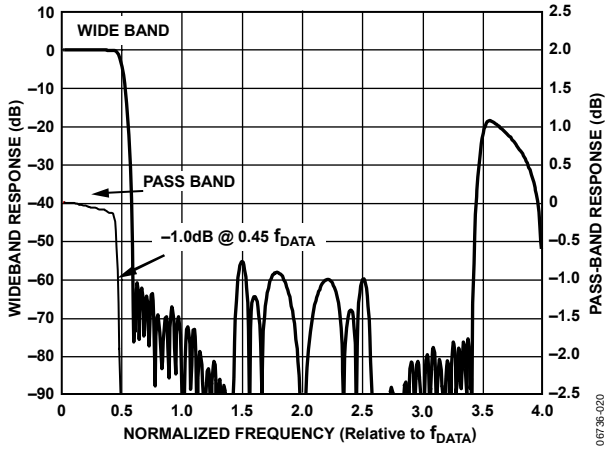

Figure 20. Frequency Response of 4× Interpolation Filter (Normalized to f_{DATA})

TxDAC AND IAMP ARCHITECTURE

The Tx path contains a TxDAC with a current amplifier, IAMP. The TxDAC reconstructs the output of the interpolation filter and sources a differential current output that can be directed to an external load or fed into the IAMP for further amplification. The TxDAC and IAMP peak current outputs are digitally programmable over a 0 dB to −7.5 dB and 0 dB to −19.5 dB range, respectively, in 0.5 dB increments. Note that this assumes default register settings for Register 0x10 and Register 0x11.

Applications demanding the highest spectral performance and/or lowest power consumption can use the TxDAC output directly. The TxDAC is capable of delivering a peak signal power-up to 10 dBm while maintaining respectable linearity performance. For power-sensitive applications requiring the highest Tx power efficiency, the TxDAC full-scale current output can be reduced to as low as 2 mA, and its load resistors sized to provide a suitable voltage swing that can be amplified by a low power, op amp-based driver.

Most applications requiring higher peak signal powers (up to 17 dBm) should use the IAMP. The IAMP can be configured as a current source for loads having a well-defined impedance (50 Ω or 75 Ω systems).

Figure 21 shows the equivalent schematic of the TxDAC and IAMP. The TxDAC provides a differential current output appearing at IOUTP+ and IOUTP−. The TxDAC can also be modeled as a differential current source generating a signal-dependent ac current, when ΔI_S has a peak current of I along with two dc current sources, sourcing a standing current equal to I. The full-scale output current, IOUTP_FS, is equal to the sum of these standing current sources (IOUTP_FS = 2 × I).

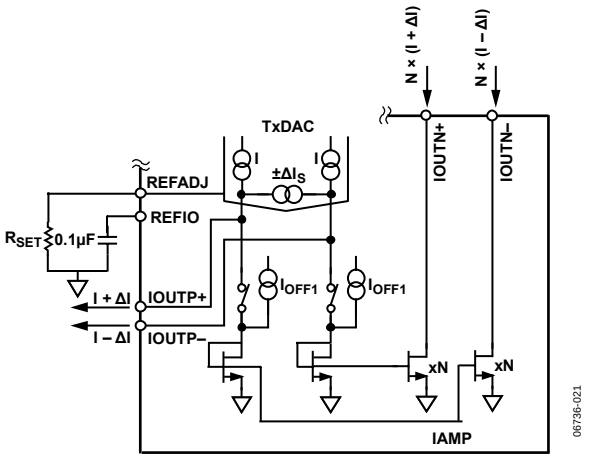

Figure 21. Equivalent Schematic of TxDAC and IAMP

The value of I is determined by the R_{SET} value at the REFADJ pin along with the Tx path's digital attenuation setting. With 0 dB attenuation, the value of I is

$$I = 16 \times (1.23/R_{SET}) \quad (1)$$

For example, an R_{SET} value of 1.96 kΩ results in I equal to 10.0 mA with IOUTP_FS equal to 20.0 mA. Note that the REFIO pin provides a nominal band gap reference voltage of 1.23 V and should be decoupled to analog ground via a 0.1 µF capacitor.

The differential current output of the TxDAC is always connected to the IOUTP pins, but it can be directed to the IAMP by clearing Bit 0 of Register 0x0E. As a result, the IOUTP pins must remain completely open if the IAMP is to be used. The IAMP consists of programmable current mirrors providing a gain factor of N that is programmable from 0 to 4 in steps of 1 (via Bits[2:0] of Register 0x10 with a default setting of N = 4). Bit 7 of this register must be set to overwrite the default settings of this register. The maximum peak current per output is 100 mA and occurs when the TxDAC standing current, I, is set for 12.5 mA (IOUTP_FS = 25 mA).

Because the current mirrors consist of NMOS devices, they sink current. Therefore, each output pin requires a dc current path to a positive supply. The voltage output of each output pin is allowed to swing between 0.5 V and 3.9 V. Lastly, both the standing current, I, and the ac current, ΔI_S, from the TxDAC are amplified by the gain factor (N) with the total standing current drawn from the positive supply being equal to

$$2 \times (N) \times I \quad (2)$$

Programmable current sources, I_{OFF1} via Register 0x12, can be used to improve the linearity performance under certain conditions by increasing their signal-to-standing current ratios. This feature provides a marginal improvement in distortion performance under large signal conditions when the peak ac current of the reconstructed waveform frequently approaches the dc standing current within the TxDAC (0 dBFS to −1 dBFS sine wave) causing the internal mirrors to turn off. However, the improvement in distortion performance diminishes as the crest factor (peak-to-rms ratio) of the ac signal increases. Most applications can disable these current sources (set to 0 mA via Register 0x12) to reduce the IAMP current consumption.

Table 18. SPI Registers for TxDAC and IAMP

Address (Hex)	Bit	Description
0x0E	0	TxDAC output.
0x10	7	Enable current mirror gain settings.
	2:0	Primary path NMOS gain of 0 to 4 with Δ = 1.
0x12	2:0	I_{OFF1} standing current.

Tx PROGRAMMABLE GAIN CONTROL

TxPGA functionality is also available to set the peak output current from the TxDAC or IAMP. The TxDAC and IAMP are digitally programmable via the PGA[5:0] port or SPI over a 0 dB to −7.5 dB range and 0 dB to −19.5 dB range, respectively, in 0.5 dB increments.

The TxPGA can be considered as two cascaded attenuators with the TxDAC providing a 7.5 dB range in 0.5 dB increments, and the IAMP providing a 12 dB range in 6 dB increments. As a result, the IAMP composite 19.5 dB span is valid only if Register 0x10 remains at its default setting of 0x04. Modifying this register setting corrupts the LUT and results in an invalid gain mapping.

TxDAC OUTPUT OPERATION

The differential current output of the TxDAC is available at the IOUTP+ and IOUTP− pins, and the IAMP should be disabled by setting Bit 0 of Register 0x0E. Any load connected to these pins must be ground referenced to provide a dc path for the current sources. Figure 22 shows the outputs of the TxDAC driving a doubly terminated 1:1 transformer with its center tap tied to ground. The peak-to-peak voltage, V p-p, across R_L (and IOUTP+ to IOUTP−) is equal to $2 \times I \times (R_L||R_S)$. With I = 10 mA and $R_L = R_S = 50\ \Omega$, V p-p is equal to 0.5 V with 1 dBm of peak power being delivered to R_L and 1 dBm being dissipated in R_S.

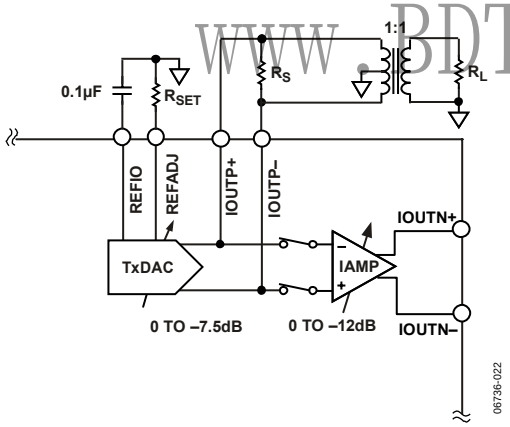

Figure 22. TxDAC Output Directly via Center-Tap Transformer

The TxDAC is capable of delivering up to 10 dBm peak power to a load, R_L. To increase the peak power for a fixed standing current, users must increase V p-p across IOUTP+ and IOUTP− by increasing one or more of the following parameters: R_S, R_L (if possible), and/or the turns ratio, N, of the transformer. For example, removing the R_S from Figure 22 and applying a 2:1 impedance ratio transformer results in 10 dBm of peak power capabilities to the load. Note that increasing the power output capabilities of the TxDAC reduces the distortion performance due to the higher voltage swings seen at IOUTP+ and IOUTP−.

Optimum distortion performance can typically be achieved by performing both of the following:

- Limiting the peak positive V_{IOUTP+} and V_{IOUTP-} to 0.8 V to avoid onset of TxDAC output compression (TxDAC voltage compliance is around 1.2 V).
- Limiting V p-p seen at IOUTP+ and IOUTP− to less than 1.6 V.

Applications demanding higher output voltage swings and power drive capabilities can benefit from using the IAMP.

IAMP CURRENT-MODE OPERATION

The IAMP can be configured for the current-mode operation (see Figure 23) for loads remaining relatively constant. In this mode, the IAMP delivers the signal-dependent current to the load via a center-tap transformer. Because the mirrors exhibit a high output impedance, they can be easily back-terminated (if required).

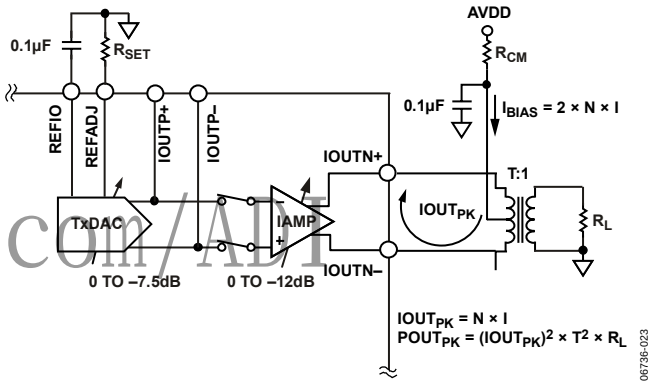

Figure 23. Current-Mode Operation

The IAMP gain, N, can be set between 0 and 4, while the TxDAC standing current, I, can be set between 2 mA and 12.5 mA (with the IOUTP outputs left open). The IOUTN outputs should be connected to the transformer, which needs to be specified to handle the dc standing current, I_{BIAS}, that is drawn by the IAMP. In addition, because I_{BIAS} remains signal independent, a series resistor should be inserted between AVDD and the center-tap transformer to provide provisions such that the IAMP common-mode voltage, V_{CM}, can be reduced since its optimum linearity performance is sensitive to both the Tx signal's peak-to-rms characteristics as well as the IAMP V_{CM}. Note that the V_{CM} bias should not exceed 3.3 V. The power dissipated in the IAMP alone is as follows:

$$P_{IAMP} = 2 \times N \times I \times V_{CM} \quad (3)$$

RECEIVE PATH

The receive signal path for the AD9869 (or its related part, the AD9868) consists of a 3-stage RxPGA, a 3-pole programmable LPF, and a 12-bit (or 10-bit) ADC (see Figure 24). Note that the additional two bits of resolution offered by the AD9869 result in a 3 dB to 5 dB lower noise floor, depending on the RxPGA gain setting and LPF cutoff frequency. Also working in conjunction with the receive path is an offset correction circuit. These blocks are discussed in detail in the following sections. Note that the power consumption of the RxPGA can be modified via Register 0x13 as discussed in the Power Control and Dissipation section.

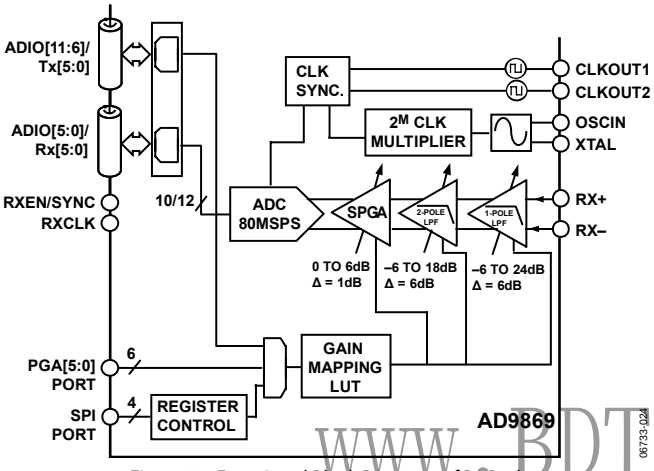

Figure 24. Functional Block Diagram of Rx Path

Rx PROGRAMMABLE GAIN AMPLIFIER

The RxPGA has a digitally programmable gain range from −12 dB to +48 dB with 1 dB resolution via a 6-bit word. Its purpose is to extend the dynamic range of the Rx path such that the input of the ADC is presented with a signal that scales within its fixed 2 V input span. There are multiple ways of setting the RxPGA gain as discussed in the RxPGA Control section, as well as an alternative 3-bit gain mapping having a range of −12 dB to +36 dB with a +8 dB resolution.

The RxPGA is comprised of two sections: a continuous time PGA (CPGA) for course gain and a switched capacitor PGA (SPGA) for fine gain resolution. The CPGA consists of two cascaded gain stages providing a gain range of −12 dB to +42 dB with a 6 dB resolution. The first stage features a low noise preamplifier (<3.0 nV/√Hz), thereby eliminating the need for an external preamplifier. The SPGA provides a gain range of 0 dB to 6 dB with a 1 dB resolution. A look-up table (LUT) is used to select the appropriate gain setting for each stage.

The nominal differential input impedance of the RxPGA input appearing at the device RX+ and RX– input pins is 400 Ω||4 pF (±20%) and remains relatively independent of gain setting.

The PGA input is self-biased at a 1.3 V common-mode level, allowing maximum input voltage swings of ±1.5 V at RX+ and RX–.

AC-coupling the input signal to this stage via 0.1 μF coupling capacitors is recommended to ensure that any external dc offset does not become amplified with high RxPGA gain settings, potentially exceeding the ADC input range.

To limit the RxPGA self-induced input offset, an offset cancellation loop is included. This cancellation loop is automatically performed upon power-up and can also be initiated via the SPI. During calibration, the RxPGA first stage is internally shorted, and each gain stage set to a high gain setting. A digital servo loop slaves a calibration DAC, which forces the Rx input offset to be within ±32 LSBs for this particular high gain setting. Although the offset varies for other gain settings, the offset is typically limited to ±5% of the ADC's 2 V input span. Note that the offset cancellation circuitry is intended to reduce the voltage offset attributed to only the RxPGA input stage, not to any dc offsets attributed to an external source.

The gain of the RxPGA should be set to minimize clipping of the ADC while utilizing most of its dynamic range. The maximum peak-to-peak differential voltage that does not result in ADC clipping is shown in Figure 25. Although the graph suggests that the maximum input signal for a gain setting of −12 dB is 8.0 V p-p, the maximum input voltage into the PGA should be limited to less than 6 V p-p to prevent turning on ESD protection diodes. For applications having higher maximum input signals, consider adding an external resistive attenuator network. While the input sensitivity of the Rx path is degraded by the amount of attenuation on a dB-to-dB basis, the low noise characteristics of the RxPGA provide some design margin such that the external line noise remains the dominant source.

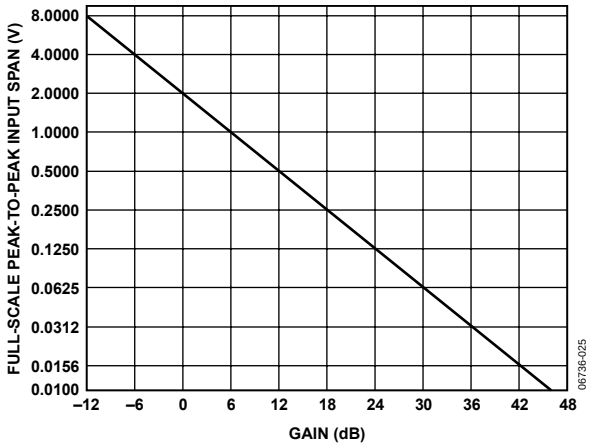

Figure 25. Maximum Peak-to-Peak Input vs. RxPGA Gain Setting that Does Not Result in ADC Clipping

LOW-PASS FILTER

The low-pass filter (LPF) provides a third-order response with a cutoff frequency that is typically programmable over a 15 MHz to 35 MHz span. The first real pole is implemented within the first CPGA gain stage (see Figure 24), and the complex pole pair is implemented in the second CPGA gain stage. Capacitor arrays are used to vary the different RC time constants within these two stages in a manner that changes the cutoff frequency while preserving the normalized frequency response. Because absolute resistor and capacitor values are process-dependent, a calibration routine lasting less than 100 µs automatically occurs each time the target cutoff frequency register (Register 0x08) is updated, ensuring a repeatable cutoff frequency from device to device.

Although the default setting specifies that the LPF be active, it can also be bypassed providing a nominal $f_{-3\,dB}$ of 55 MHz. Table 19 shows the SPI registers pertaining to the LPF.

Table 19. SPI Registers for Rx Low-Pass Filter

Address (Hex)	Bit	Description
0x07	0	Enable Rx LPF.
0x08	7:0	Target value.

The normalized wideband gain response is shown in Figure 26. The normalized pass-band gain and group delay responses are shown in Figure 27. The −3 dB cutoff frequency, $f_{-3\,dB}$, results in −3 dB attenuation. In addition, the actual group delay time (GDT) response can be calculated given a programmed cutoff frequency using the following equation:

$$Actual\ GDT = Normalized\ GDT/(2.45 \times f_{-3dB}) \quad (4)$$

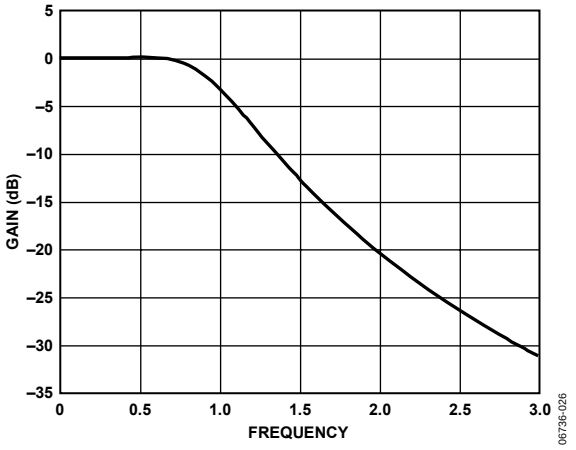

Figure 26. LPF Normalized Wideband Gain Response

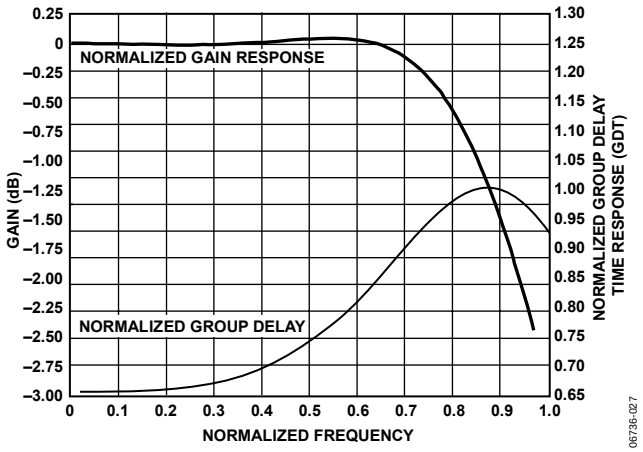

Figure 27. LPF Normalized Pass-Band Gain and Group Delay Responses

The $f_{-3\,dB}$ is programmable by writing an 8-bit word, referred to as the target, to Register 0x08. The cutoff frequency is a function of the ADC sample rate, f_{ADC}, and to a lesser extent, the RxPGA gain setting (in dB). Figure 28 shows how $f_{-3\,dB}$ varies as a function of the RxPGA gain setting.

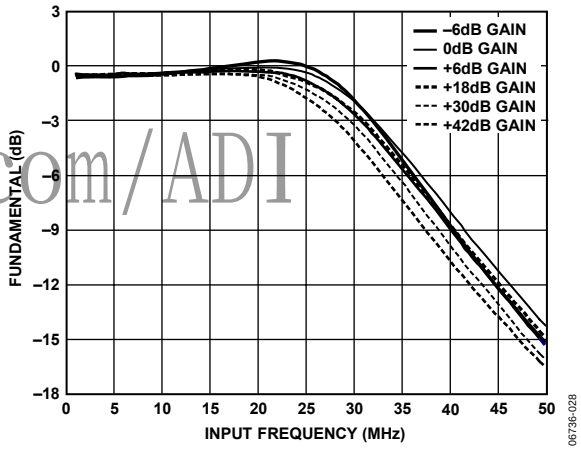

Figure 28. Effects of RxPGA Gain on LPF Frequency Response ($f_{-3\,dB}$ = 32 MHz @ 0 dB and f_{ADC} = 80 MSPS)

The following formula[1] can be used to estimate $f_{-3\,dB}$ for a RxPGA gain setting of 0 dB:

$$f_{-3dB\_0dB} = (128/target) \times (f_{ADC}/80) \times (f_{ADC}/30 + 23.83)\, f \quad (5)$$

Figure 29 compares the measured and calculated $f_{-3\,dB}$ using this formula.

[1] Empirically derived for an $f_{-3\,dB}$ range of 15 MHz to 35 MHz and an f_{ADC} of 40 MSPS to 80 MSPS with an RxPGA = 0 dB.

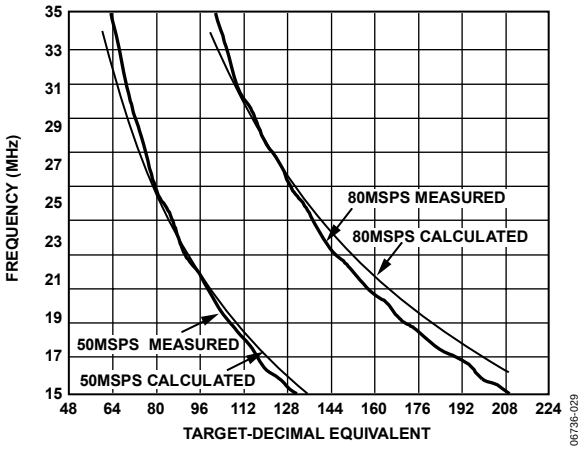

Figure 29. Measured and Calculated $f_{-3\ dB}$ vs. Target Value for f_{ADC} = 50 MSPS and 80 MSPS

The following scaling factor can be applied to the previous formula to compensate for the RxPGA gain setting on $f_{-3\ dB}$:

$$Scale\ Factor = 1 - (RxPGA \text{ in dB})/382 \quad (6)$$

This scaling factor reduces the calculated $f_{-3\ dB}$ as the RxPGA increases. Applications that need to maintain a minimum cutoff frequency, $f_{-3\ dB\_MIN}$, for all RxPGA gain settings should first determine the scaling factor for the highest RxPGA gain setting to be used. Next, the $f_{-3\ dB\_MIN}$ should be divided by this scale factor to normalize to the 0 dB RxPGA gain setting, $f_{-3\ dB\_0\ dB}$. Equation 5 can then be used to calculate the target value.

The LPF frequency response shows a slight sensitivity to temperature, as shown in Figure 30. Applications sensitive to temperature drift can recalibrate the LPF by rewriting the target value to Register 0x08.

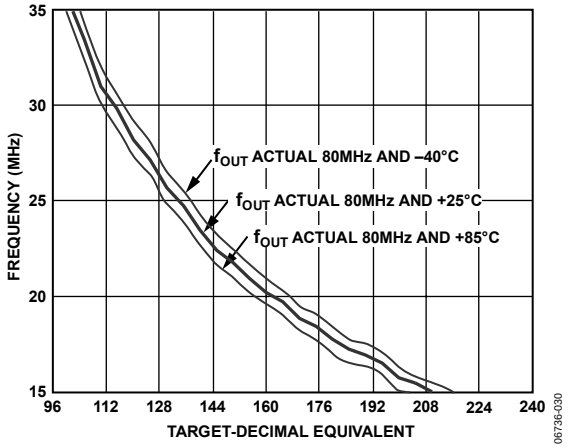

Figure 30. $f_{-3\ dB}$ Temperature Drift for f_{ADC} = 80 MSPS and RxPGA = 0 dB

ANALOG-TO-DIGITAL CONVERTER (ADC)

The AD9869 features a 12-bit analog-to-digital converter (ADC) capable of up to 80 MSPS. As shown in Figure 24, the ADC is driven by the SPGA stage, which performs both the sample-and-hold and the fine gain adjust functions. A buffer amplifier (not shown) isolates the last CPGA gain stage from the dynamic load presented by the SPGA stage. The full-scale input span of the ADC is 2 V p-p, and depending on the PGA gain setting, the full-scale input span into the SPGA is adjustable from 1 V to 2 V in 1 dB increments.

A pipelined, multistage ADC architecture is used to achieve high sample rates while consuming low power. The ADC distributes the conversion over several smaller ADC subblocks, refining the conversion with progressively higher accuracy as it passes the results from stage to stage on each clock edge. The ADC typically performs best when driven internally by a 50% duty cycle clock.

The ADC power consumption can be reduced by 25 mA with minimal effect on its performance by setting Bit 4 of Register 0x07. Alternative power bias settings are also available via Register 0x13, as discussed in the Power Control and Dissipation section. Lastly, the ADC can be completely powered down for half-duplex operation, further reducing the peak power consumption of the AD9869.

The ADC has an internal voltage reference and reference amplifier as shown in Figure 31. The internal band gap reference generates a stable 1 V reference level that is converted to a differential 1 V reference centered about midsupply (AVDD/2). The outputs of the differential reference amplifier are available at the REFT and REFB pins and must be properly decoupled for optimum performance. The REFT and REFB pins are conveniently situated at the corners of the LFCSP package such that C1 (0603 type) can be placed directly across its pins. C3 and C4 can be placed underneath C1, and C2 (10 µF tantalum) can be placed furthest from the package.

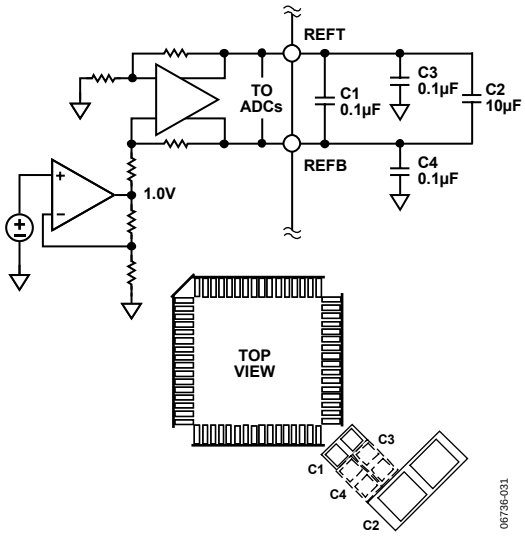

Figure 31. ADC Reference and Decoupling

Table 20 shows the SPI registers pertaining to the ADC.

Table 20. SPI Registers for Rx ADC

Address (Hex)	Bit	Description
0x04	4	ADC clock from PLL.
0x07	4	ADC low power mode.
0x13	2:0	ADC power bias adjust.

AGC TIMING CONSIDERATIONS

When implementing a digital AGC timing loop, it is important to consider the Rx path latency and settling time of the Rx path in response to a change in gain setting. While the RxPGA settling time may also show a slight dependency on the LPF cutoff frequency, the ADC pipeline delay, along with the ADIO bus interface, presents a more significant delay. The amount of delay or latency is dependent on whether a half-duplex or full-duplex is selected. An impulse response at the RxPGA input can be observed after 10.0 ADC clock cycles ($1/f_{ADC}$) in the case of a half-duplex interface, and 10.5 ADC clock cycles in the case of a full-duplex interface. This latency, along with the RxPGA settling time, should be considered to ensure stability of the AGC loop.

CLOCK SYNTHESIZER

The AD9869 generates all its internal sampling clocks, as well as two user-programmable clock outputs appearing at CLKOUT1 and CLKOUT2, from a single reference source (see Figure 32). The reference source can either be a fundamental frequency or an overtone quartz crystal connected between OSCIN and XTAL, with the parallel resonant load components specified by the crystal manufacturer. It can also be a TTL-level clock applied to OSCIN with XTAL left unconnected.

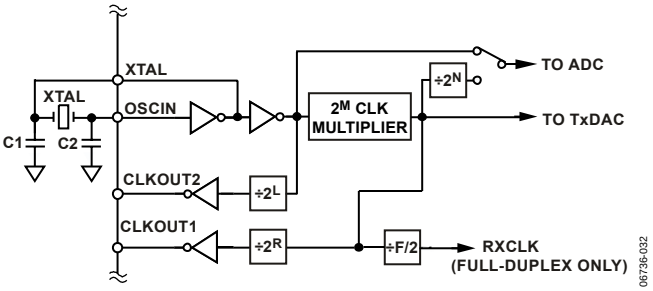

Figure 32. Clock Oscillator and Synthesizer

Special consideration should be given to the design of crystal oscillators using the AD9869 internal CMOS inverter. This is especially true when designing third overtone oscillators where crystal power dissipation and negative resistance upon start-up are a few of the issues to consider. For this reason, a 40 MHz or lower fundamental crystal is preferred with the AD9869.

The CMOS inverter device characteristics are listed in Table 21. It is recommended to consult with the selected crystal manufacturer to ensure that a robust design can be realized with the selected crystal and AD9869 CMOS inverter.

Table 21. CMOS Inverter Device Characteristics

Parameter	Nominal Value	Tolerance %	Description
RF	1.2 MΩ	±25	Feedback resistor.
gm	17 mA/V	±20	At midsupply.
Z_{OUT}	1.6 kΩ	±50	At midsupply.
C_{IN}	2.5 pF	±25	Parasitic capacitance.
C_{OUT}	2.0 pF	±25	Parasitic capacitance.

The data rate, f_{DATA}, for the Tx and Rx data paths must always be equal. Therefore, the ADC sample rate, f_{ADC}, is always equal to f_{DATA}, while the TxDAC update rate is a factor of 1, 2, or 4 of f_{DATA}, depending on the selected interpolation factor. The data rate refers to the word rate and should not be confused with the nibble rate in full-duplex interface.

The 2^M CLK multiplier contains a PLL (with integrated loop filter) and a VCO capable of generating an output frequency that is a multiple of 1, 2, 4, or 8 of its input reference frequency, f_{OSCIN}, appearing at OSCIN. The input frequency range of f_{OSCIN} is between 20 MHz and 80 MHz, and the VCO can operate over an 80 MHz to 200 MHz span. For the best phase noise/jitter characteristics, it is advisable to operate the VCO with a frequency between 100 MHz and 200 MHz. The VCO output drives the TxDAC directly such that its update rate, f_{DAC}, is related to f_{OSCIN} by the following equation:

$$f_{DAC} = 2^M \times f_{OSCIN} \quad (7)$$

where M = 0, 1, 2, or 3.

M is the PLL multiplication factor set in Register 0x04. The value of M is determined by the Tx path's word rate, f_{DATA}, and digital interpolation factor, F, as shown in the following equation:

$$M = \log_2 (F \times f_{DATA}/f_{OSCIN}) \quad (8)$$

Note that if the reference frequency appearing at OSCIN is chosen to be equal to the Tx path and Rx path word rates, M is equal to $\log_2(F)$. Also note that the RXCLK frequency for full-duplex mode (MODE = 1) is a function of the 2^M CLK multiplier setting, as well as the interpolation factor, F. Full-duplex mode requires that RXCLK be equal to 2 × f_{DATA} because data is transferred in nibbles.

The clock source for the ADC can be selected in Register 0x04 as a buffered version of the reference frequency appearing at OSCIN (default setting) or a divided version of the VCO output, f_{DAC}. The first option is the default setting and most desirable if f_{OSCIN} is equal to f_{ADC}. This option typically results in the best jitter/phase noise performance for the ADC sampling clock. The second option is suitable in cases where f_{OSCIN} is a factor of 2 or 4 less than the f_{ADC}. In this case, the divider ratio, N, is chosen such that the divided down VCO output is equal to the ADC sample rate, as shown in the following equation:

$$f_{ADC} = f_{DAC}/2^N \quad (9)$$

where N = 0, 1, or 2.

The CLK synthesizer also has two clock outputs appearing at CLKOUT1 and CLKOUT2. They are programmable via Register 0x06. Both outputs can be inverted or disabled. The voltage levels appearing at these outputs are relative to DRVDD and remain active during a hardware or software reset. Table 22 shows the SPI registers pertaining to the CLK synthesizer.

Table 22. SPI Registers for CLK Synthesizer

Address (Hex)	Bit	Description
0x04	4	ADC CLK from PLL.
	3:2	PLL divide factor (N).
	1:0	PLL multiplication factor (M).
0x06	7:6	CLKOUT2 divide number.
	5	CLKOUT2 invert.
	4	CLKOUT2 disable.
	3:2	CLKOUT1 divide number.
	1	CLKOUT1 invert.
	0	CLKOUT1 disable.

CLKOUT1 is a divided version of the VCO output and can be set to be a submultiple integer of f_{DAC} ($f_{DAC}/2^R$, where R = 0, 1, 2, or 3). Because this clock is derived from the same set of dividers used within the PLL core, it is phase-locked to the dividers such that its phase relationship relative to the signal appearing at OSCIN (or RXCLK) can be determined upon power-up. In addition, this clock has a near 50% duty cycle because it is derived from the VCO. As a result, CLKOUT1 should be selected before CLKOUT2 as the primary source for system clock distribution.

CLKOUT2 is a divided version of the reference frequency, f_{OSCIN}, and can be set to be a submultiple integer of f_{OSCIN} ($f_{OSCIN}/2^L$, where L = 0, 1, or 2). With L set to 0, the output of CLKOUT2 is a delayed version of the signal appearing at OSCIN, exhibiting the same duty cycle characteristics. With L set to 1 or 2, the output of CLKOUT2 is a divided version of the OSCIN signal, exhibiting a near 50% duty cycle, but without having a deterministic phase relationship relative to CLKOUT1 (or RXCLK).

POWER CONTROL AND DISSIPATION

POWER-DOWN

The AD9869 provides the ability to control the power-on state of various functional blocks. The state of the PWRDWN pin, along with the contents of Register 0x01 and Register 0x02, allow two user-defined power settings that are pin-selectable. The default settings[1] are such that Register 0x01 has all blocks powered on (all bits 0), while Register 0x02 has all blocks powered down (excluding the PLL) such that the clock signal remains available at CLKOUT1 and CLKOUT2. When the PWRDWN pin is low, the functional blocks corresponding to the bits in Register 0x01 are powered down. When the PWRDWN is high, the functional blocks corresponding to the bits in Register 0x02 are powered down. PWRDWN immediately affects the designated functional blocks with minimum digital delay.

Table 23. SPI Registers Associated with Power-Down and Half-Duplex Power Savings

Address (Hex)	Bit	Description	Comments
0x01	7	CLK Synthesizer	PWRDWN = 0. Default setting is all functional blocks powered on.
	6	TxDAC/IAMP	
	5	Tx Digital	
	4	REF	
	3	ADC CML	
	2	ADC	
	1	PGA Bias	
	0	RxPGA	
0x02	7	CLK Synthesizer	PWRDWN = 1. Default setting is all functional blocks powered off excluding PLL.
	6	TxDAC/IAMP	
	5	Tx Digital	
	4	REF	
	3	ADC CML	
	2	ADC	
	1	PGA Bias	
	0	RxPGA	
0x03	7:3	Tx OFF Delay	Half-duplex power savings.
	2	Rx PWRDWN via TXEN	
	1	Enable Tx PWRDWN	
	0	Enable Rx PWRDWN	

[1] With MODE = 1 and CONFIG =1, Register 0x02 default settings are with all blocks powered off, with RXCLK providing a buffered version of the signal appearing at OSCIN. This setting results in the lowest power consumption upon power-up, while still allowing AD9869 to generate the system clock via a crystal.

HALF-DUPLEX POWER SAVINGS

Significant power savings can be realized in applications having a half-duplex protocol, allowing only the Rx path or Tx path to be operational at one time. The power-savings method depends on whether the AD9869 is configured for a full-duplex or half-duplex interface. Functional blocks having fast power-on/power-off times for the Tx path and Rx path are controlled by the following bits: TxDAC/IAMP, Tx Digital, ADC, and RxPGA (see Table 23).

In the case of a full-duplex digital interface (MODE = 1), users can set Register 0x01 to Register 0x60 and Register 0x02 to Register 0x05 (or vice versa) such that the Tx path and Rx path are never powered on simultaneously. The PWRDWN pin can then be used to control which path is powered on, depending on the burst type. During a Tx burst, the Rx path PGA and ADC blocks can typically be powered down within 100 ns, while the Tx path DAC, IAMP, and digital filter blocks are powered up within 0.5 µs. For an Rx burst, the Tx circuitry can be powered down within 100 ns, while the Rx circuitry is powered up within 2 µs.

Setting the $\overline{\text{TXQUIET}}$ pin low allows it to be used with the full-duplex interface to quickly power down the IAMP and disable the interpolation filter. This is meant to maintain backward compatibility with the AD9875/AD9876 MxFEs, except that the TxDAC remains powered if its IOUTP outputs are used. In most applications, the interpolation filter needs to be flushed with 0s before or after being powered down. This ensures that upon power-up, the TxDAC (and IAMP) have a negligible differential dc offset, thus preventing spectral splatter due to an impulse transient.

Applications using a half-duplex interface (MODE = 0) can benefit from an additional power-savings feature available in Register 0x03. This register is effective only for a half-duplex interface. In addition to providing power savings for half-duplex applications, this feature allows the AD9869 to be used in applications that need only its Rx (or Tx) path functionality through pin strapping, making a serial port interface (SPI) optional. This feature also allows the PWRDWN pin to retain its default function as a master power control, as defined in Table 10.

The default settings for Register 0x03 provide fast power control of the functional blocks in the Tx signal path and Rx signal path (outlined previously) using the TXEN pin. The TxDAC remains powered on in this mode, while the IAMP is powered down. Significant current savings are typically realized when the IAMP is powered down.

For a Tx burst, the falling edge of TXEN is used to generate an internal delayed signal for powering down the Tx circuitry. Upon receipt of this signal, power-down of the Tx circuitry occurs within 100 ns. The user-programmable delay for the Tx path power-down is meant to match the pipeline delay of the last Tx burst sample such that power-down of the TxDAC and IAMP does not impact its transmission. A 5-bit field in Register 0x03 sets the delay from 0 to 31 TXCLK clock cycles, with the default being 31 (0.62 µs with f_{TXCLK} = 50 MSPS). The digital interpolation filter is automatically flushed with midscale samples prior to power-down if the clock signal into the TXCLK pin is present for 33 additional clock cycles after TXEN returns low. For an Rx burst, the rising edge of TXEN is used to generate an internal signal (with no delay) that powers up the Tx circuitry within 0.5 µs.

The Rx path power-on/power-off can be controlled by either TXEN or RXEN by setting Bit 2 of Register 0x03. In the default setting, the falling edge of TXEN powers up the Rx circuitry within 2 µs, while the rising edge of TXEN powers down the Rx circuitry within 0.5 µs. If RXEN is selected as the control signal, its rising edge powers up the Rx circuitry, and the falling edge powers it down. To disable the fast power-down of the Tx circuitry and/or Rx circuitry, set Bit 1 and/or Bit 0 to 0.

POWER REDUCTION OPTIONS

The power consumption of the AD9869 can be significantly reduced from its default setting by optimizing the power consumption vs. performance of the various functional blocks in the Tx signal path and Rx signal path. On the Tx path, minimum power consumption is realized when the TxDAC output is used directly and its standing current is reduced to as low as 1 mA. Although a slight degradation in THD performance results at reduced standing currents, it often remains adequate for most applications because the op amp driver typically limits the overall linearity performance of the Tx path. The load resistors used at the TxDAC outputs (IOUTP+ and IOUTP−) can be increased to generate an adequate differential voltage that can be further amplified via a power efficient op amp-based driver solution. Figure 33 shows how the supply current for the TxDAC is reduced from 55 mA to 14 mA as the standing current is reduced from 12.5 mA to 1.25 mA. Further Tx power savings can be achieved by bypassing or reducing the interpolation factor of the digital filter as shown in Figure 34.

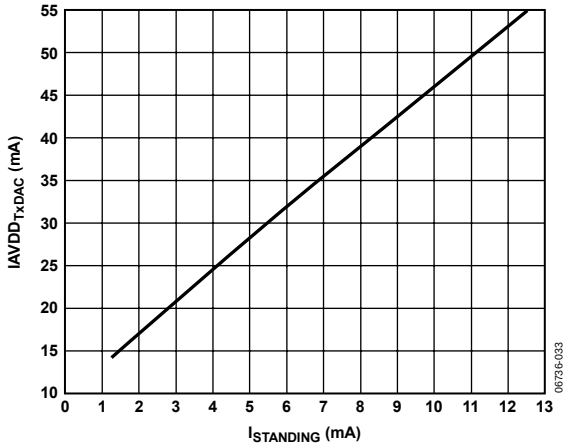

Figure 33. Reduction in TxDAC Supply Current vs. Standing Current

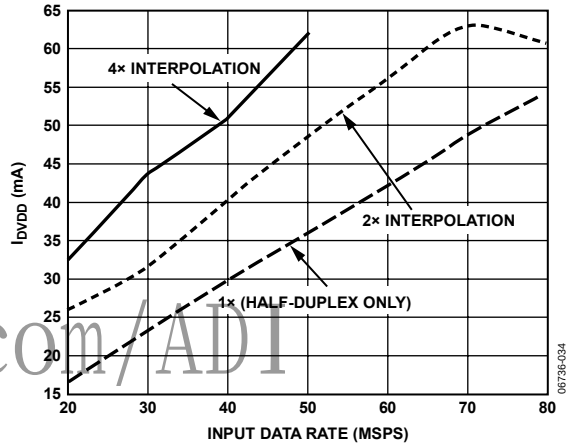

Figure 34. Digital Supply Current Consumption vs. Input Data Rate (DVDD = DRVDD = 3.3 V and $f_{OUT} = f_{DATA}/10$)

Power consumption on the Rx path can be achieved by reducing the bias levels of the various amplifiers contained within the RxPGA and ADC. As previously noted, the RxPGA consists of two CPGA amplifiers and one SPGA amplifier. The bias levels of each of these amplifiers, along with the ADC, can be controlled via Register 0x13 as shown in Table 24. The default setting for Register 0x13 is 0x00.

Table 24. SPI Register for RxPGA and ADC Biasing

Address (Hex)	Bit	Description
0x07	4	ADC low power.
0x13	7:5	CPGA bias adjust.
	4:3	SPGA bias adjust.
	2:0	ADC power bias adjust.

Because the CPGA processes signals in the continuous time domain, its performance vs. bias setting remains mostly independent of the sample rate. Table 25 shows how the typical current consumption seen at AVDD varies as a function of Register 0x13, Bits[7:5], while the remaining bits are maintained at their default settings of 0. Only four of the possible settings result in any reduction in current consumption relative to the default setting. Reducing the bias level typically results in degradation in the THD vs. frequency performance as shown in Figure 35. This is due to a reduction of the amplifier's unity gain bandwidth, while the SNR performance remains relatively unaffected.

Table 25. Analog Supply Current vs. CPGA Bias Settings at f_{ADC} = 65 MSPS

Bit 7	Bit 6	Bit 5	ΔmA
0	0	0	0
0	0	1	−27
0	1	0	−42
0	1	1	−51
1	0	0	−55
1	0	1	+27
1	1	0	+69
1	1	1	+27

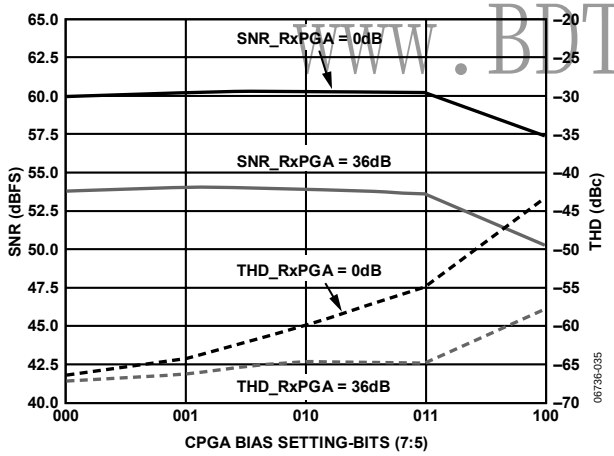

Figure 35. THD vs. f_{IN} Performance and CPGA Bias Settings (000, 001, 010, 100 with RxPGA = 0 and +36 dB, AIN = −1 dBFS, LPF set to 26 MHz, f_{ADC} = 50 MSPS)

The SPGA is implemented as a switched capacitor amplifier, therefore, its performance vs. bias level is mostly dependent on the sample rate. Figure 36 shows how the typical current consumption seen at AVDD varies as a function of Register 0x13, Bits[4:3] and sample rate, while the remaining bits are maintained at the default setting of 0. Figure 37 shows how the SNR and THD performance is affected for a 10 MHz sine wave input as the ADC sample rate is swept from 20 MHz to 80 MHz. The SNR and THD performance remains relatively stable, suggesting that the SPGA bias can often be reduced from its default setting without impacting the device's overall performance.

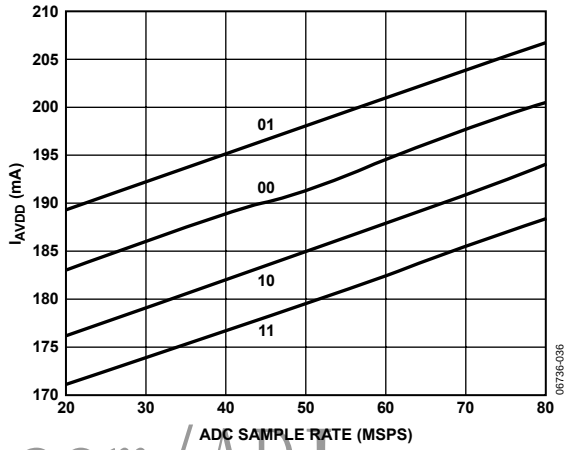

Figure 36. AVDD Current vs. SPGA Bias Setting and Sample Rate

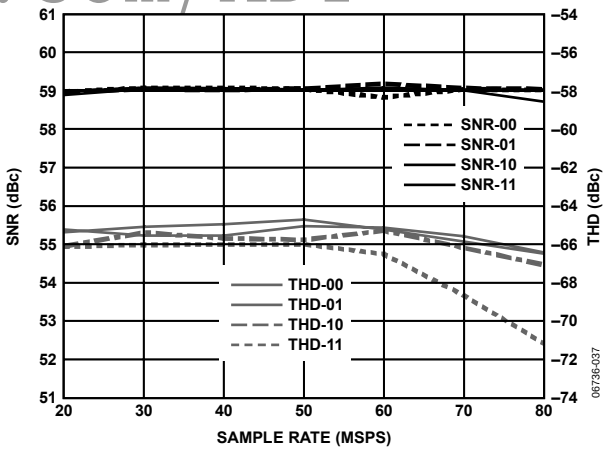

Figure 37. SNR and THD Performance vs. f_{ADC} and SPGA Bias Setting with RxPGA = 0 dB, f_{IN} = 10 MHz, LPF set to 26 MHz, AIN = −1 dBFS

The ADC is based on a pipeline architecture with each stage consisting of a switched capacitor amplifier. Therefore, its performance vs. bias level is mostly dependent on the sample rate. Figure 38 shows how the typical current consumption seen at AVDD varies as a function of Register 0x13, Bits[2:0] and sample rate, while the remaining bits are maintained at the default setting of 0. Setting Bit 4 or Register 0x07 corresponds to the 011 setting, and the settings of 101 and 111 result in higher current consumption. Figure 39 shows how the SNR and THD performance are affected for a 10 MHz sine wave input for the lower power settings as the ADC sample rate is swept from 20 MHz to 80 MHz.

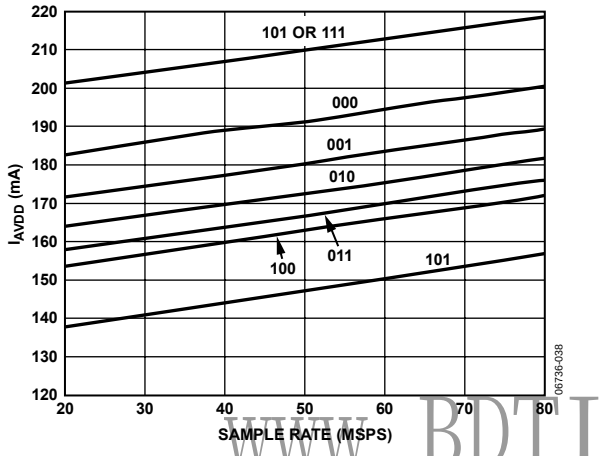

Figure 38. AVDD Current vs. ADC Bias Setting and Sample Rate

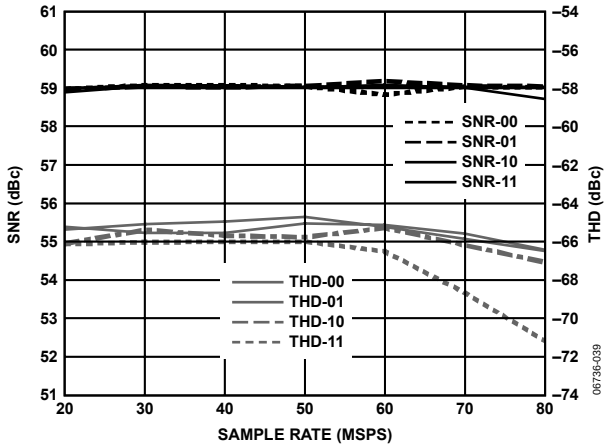

Figure 39. SNR and THD Performance vs. f_{ADC} and ADC Bias Setting with RxPGA = 0 dB, f_{IN} = 10 MHz, AIN = −1 dBFS

A sine wave input is a standard and convenient method of analyzing the performance of a system. However, the amount of power reduction that is possible is application dependent, based on the nature of the input waveform (such as frequency content, and peak-to-rms ratio), the minimum ADC sample, and the minimum acceptable level of performance. Thus, it is advisable that power-sensitive applications optimize the power bias setting of the Rx path using an input waveform that is representative of the application.

POWER DISSIPATION

The power dissipation of the AD9869 can become quite high in full-duplex applications in which the Tx path and Rx path are simultaneously operating with nominal power bias settings. In fact, some applications that use the IAMP may need to either reduce its peak power capabilities or reduce the power consumption of the Rx path so that the device's maximum allowable power consumption, P_{MAX}, is not exceeded.

P_{MAX} is specified at 1.66 W to ensure that the die temperature does not exceed 125°C at an ambient temperature of 85°C. This specification is based on the 64-lead LFSCP having a thermal resistance, θ_{JA}, of 24°C/W with its heat slug soldered. (The θ_{JA} is 30.8°C/W if the heat slug remains unsoldered.) If a particular application's maximum ambient temperature, T_A, falls below 85°C, the maximum allowable power dissipation can be determined by the following equation:

$$P_{MAX} = 1.66 + (85 - T_A)/24 \quad (10)$$

Assuming the IAMP common-mode bias voltage is operating off the same analog supply as the AD9869, the following equation can be used to calculate the maximum total current consumption, I_{MAX}, of the IC:

$$I_{MAX} = (P_{MAX} - P_{IAMP})/3.47 \quad (11)$$

With an ambient temperature of up to 85°C, I_{MAX} is 478 mA.

If the IAMP is operating off a different supply or in the voltage mode configuration, first calculate the power dissipated in the IAMP, P_{IAMP}, using Equation 3, and then recalculate I_{MAX} using Equation 11.

Figure 33, Figure 34, Figure 36, and Figure 38 can be used to calculate the current consumption of the Rx and Tx paths for a given setting.

MODE SELECT UPON POWER-UP AND RESET

The AD9869 power-up state is determined by the logic levels appearing at the MODE and CONFIG pins. The MODE pin is used to select a half- or full-duplex interface by pin strapping it low or high, respectively. The CONFIG pin is used in conjunction with the MODE pin to determine the default settings for the SPI registers as outlined in Table 10.

The intent of these particular default settings is to allow some applications to avoid using the SPI (disabled by pin strapping $\overline{SEN}$ high), thereby reducing implementation costs. For example, setting MODE low and CONFIG high configures the AD9869 to be backward compatible with the AD9975, while setting MODE high and CONFIG low makes it backward compatible with the AD9875. Other applications must use the SPI to configure the device.

A hardware reset ($\overline{\text{RESET}}$ pin) or software reset (Bit 5 of Register 0x00) can be used to place the AD9869 into a known state of operation as determined by the state of the MODE and CONFIG pins. A dc offset calibration and filter tuning routine is also initiated upon a hardware reset, but not with a software reset. Neither reset method flushes the digital interpolation filters in the Tx path. Refer to the Half-Duplex Mode and Full-Duplex Mode sections for information on flushing the digital filters.

A hardware reset can be triggered by pulsing the $\overline{\text{RESET}}$ pin low for a minimum of 50 ns. The SPI registers are instantly reset to their default settings upon $\overline{\text{RESET}}$ going low, whereas the dc offset calibration and filter-tuning routine is initiated upon $\overline{\text{RESET}}$ returning high. To ensure sufficient power-on time of the various functional blocks, $\overline{\text{RESET}}$ returning high should occur no less than 10 ms upon power-up. If a digital reset signal from a microprocessor reset circuit (such as ADM1818) is not available, a simple R-C network referenced to DVDD can be used to hold $\overline{\text{RESET}}$ low for approximately 10 ms upon power-up.

ANALOG AND DIGITAL LOOPBACK TEST MODES

The AD9869 features analog and digital loopback capabilities that can assist in system debug and final test. Analog loopback routes the digital output of the ADC back into the Tx data path prior to the interpolation filters such that the Rx input signal can be monitored at the output of the TxDAC or IAMP. As a result, the analog loopback feature can be used for a half-duplex or full-duplex interface to allow testing of the functionality of the entire IC (excluding the digital data interface).

For example, the user can configure the AD9869 with similar settings as the target system, inject an input signal (sinusoidal waveform) into the Rx input, and monitor the quality of the reconstructed output from the TxDAC or IAMP to ensure a minimum level of performance. In this test, the user can exercise the RxPGA as well as validate the attenuation characteristics of the RxLPF. Note that the RxPGA gain setting should be selected such that the input does not result in clipping of the ADC.

Digital loopback can be used to test the full-duplex digital interface of the AD9869. In this test, data appearing on the Tx[5:0] port is routed back to the Rx[5:0] port, thereby confirming proper bus operation. The Rx port can also be three-stated for half-duplex and full-duplex interfaces.

Table 26. SPI Registers for Test Modes

Address (Hex)	Bit	Description
0x0D	7	Analog loopback.
	6	Digital loopback.
	5	Rx port three-state.

OUTLINE DIMENSIONS

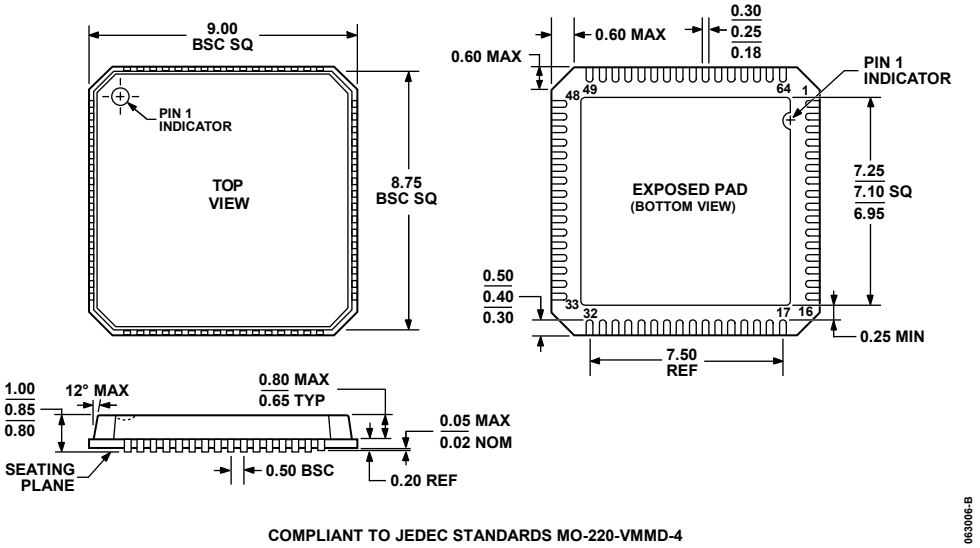

Figure 40. 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
9 mm x 9 mm Body, Very Thin Quad
(CP-64-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9869BCPZ[1]	−40°C to +85°C	64-Lead LFCSP_VQ	CP-64-3
AD9869BCPZRL[1]	−40°C to +85°C	64-Lead LFCSP_VQ	CP-64-3

[1] Z = RoHS Compliant Part.

NOTES

D06736-0-5/07(0)