AMD

Interfacing the AMD-761™ System Controller and the Via Technologies, Inc. VT82C686B Southbridge.

Application Note

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Revision History

Date	Rev	Description
April 2001	A	Initial Release

Application Note

Interfacing the AMD-761™ System Controller and the Via Technologies, Inc. VT82C686B Southbridge

The AMD-761™ System Controller and the Via Technologies, Inc. VT82C686B Southbridge are interoperable core logic solutions. However, two incompatibilities exist that must be considered when implementing the pair in system designs.

Purpose

This document describes two system-level incompatibilities that occur when creating a system with the AMD-761 system controller (Northbridge) and the Via Technologies, Inc. VT82C686B (Southbridge):

1. Incompatibilities in the Write Snoop Complete (WSC#) protocol mandate an alternative configuration for proper function. This impacts compliance with the Microsoft® PC-2001 specification.
2. Potential data corruption when switching into the ACPI S3 power management state (Suspend to RAM) in systems that use registered DDR DIMMs due to incompatible sequencing of the PCIRESET# pin.

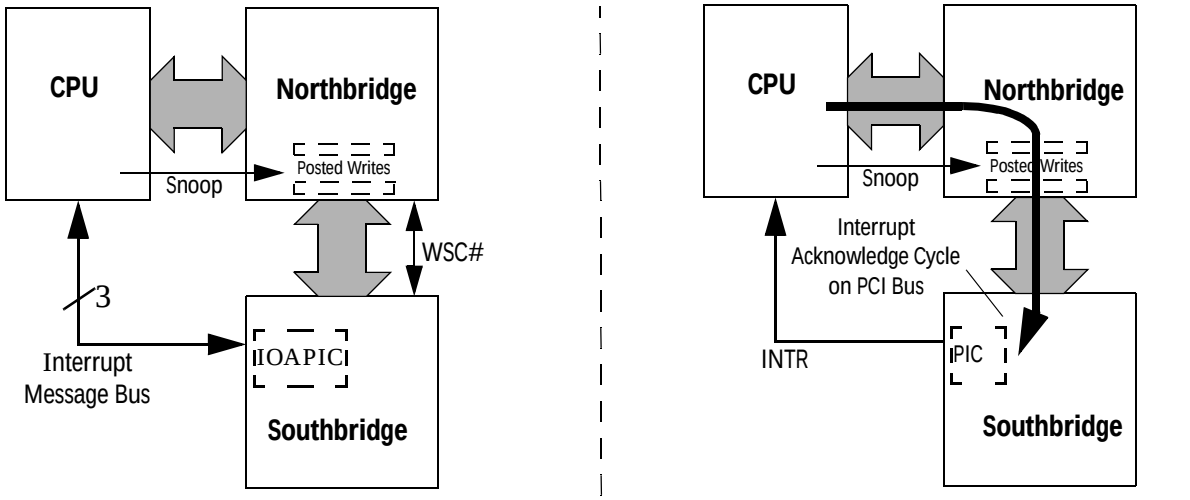
These incompatibilities and their corresponding solutions are discussed in the following sections.

Write Snoop Protocol Incompatibility

Background

The Microsoft Windows® Logo Program Requirements 2.0 v.0.9 requires that all desktop systems must be Advanced Programmable Interrupt Controller (APIC) enabled (SYS-001.3). This requires that all hardware interrupts be connected to the IOAPIC, and that the IOAPIC be connected to the processor's local APIC. The communication between the IOAPIC and the local APIC occurs over a separate sideband bus. A comparison of this configuration to the traditional PIC configuration is shown in Figure 1 on page 3.

Operation with the IOAPIC and the local APIC requires all of the Northbridge's posted write-buffers to be properly flushed to coherent memory before the IOAPIC sends an interrupt message to the processor. This is required to prevent potential data coherency problems that may result when the processor receives an interrupt and reads stale data because the data most recently written by the PCI Bus master still resides in a posted write-buffer in the Northbridge. Non-APIC implementations do not have the potential for this problem because the processor's interrupt acknowledge cycle that traverses the PCI Bus is serializing in nature, thus all posted-write buffers are flushed before the processor reads memory in the interrupt service routine.



IOAPIC System Configuration

1. Peripheral interrupt request occurs, IOAPIC must send interrupt message to the processor
2. WSC# protocol forces Northbridge and CPU to snoop all posted writes and provide a status indicator to the Southbridge.
3. Southbridge/IOAPIC is now free to issue message to CPU on the interrupt bus
4. Processor reads of memory are coherent.

PIC System Configuration

1. Peripheral interrupt request occurs, PIC sends interrupt request to the processor on the INTR pin
2. Processor responds with interrupt acknowledge cycle
3. Interrupt acknowledge cycle forces Northbridge to flush all posted writes.
4. Processor reads of memory are coherent.

Figure 1. IOAPIC vs. Traditional PIC System Configuration

The mechanism typically employed in chipsets to flush the posted write-buffers is a simple protocol between the Northbridge and the Southbridge that signals the completion of processor snooping of all posted write-buffers, indicating that an interrupt message may be safely sent from the IOAPIC to the local APIC. This mechanism is known as “Write Snoop Complete” and is implemented with a pin called WSC#. The WSC# pin is supported on both the AMD-761 system controller and the VT82C686B Southbridge, but the implementations are functionally incompatible as follows:

- The AMD-761 system controller implements WSC# as a bidirectional pin that is first asserted by the Southbridge to request that the posted write-buffers be snooped by the processor, and subsequently asserted by the Northbridge to indicate that the Southbridge's IOAPIC can safely issue an interrupt message to the local APIC. The AMD-761 system controller does not assert the WSC# pin unless it first receives a request on this pin.
- The VT82C686B implements WSC# as a unidirectional pin that is only driven by the Northbridge and must be asserted low unless the Northbridge has outstanding PCI to DRAM posted writes that have not been snooped by the processor. When the VT82C686B is connected to an AMD-761 system controller, the WSC# pin will never be asserted because the VT82C686B does not first assert WSC# to request posted writes to be snooped, thus the system is not able to send interrupt messages to the processor.

Solution

Figure 2 shows an incompatible implementation where the WSC# signal is directly connected between the AMD-761 System Controller and the VT82C686B.

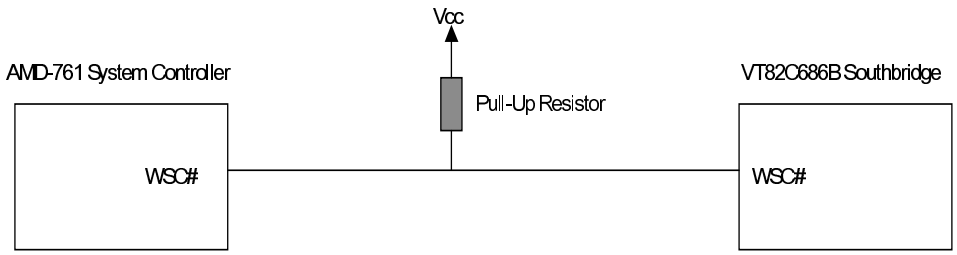


Figure 2. Typical Configuration

To alleviate this incompatibility, AMD recommends that the WSC# signal be connected as shown in Figure 3. In this new configuration, the motherboard must be designed in the following fashion.

- The WSC# pins of the AMD-761 system controller and the VT82C686B southbridge are connected through an unpopulated resistor pad shown as R1 in Figure 3. This configuration allows POP/NOPOP capability. (A zero-ohm resistor can be added in the event of silicon changes that allow direct connection.)

Note: *The WSC# pin of the AMD-761 system controller contains an internal pull-up resistor. No external termination is required on the AMD-761 system controller WSC# pin when it is disconnected from the VT82C686B WSC# input.*

- The WSC# input of the VT82C686B is terminated using a resistor pad populated by a pull-down resistor shown as R2 in Figure 3. This configuration allows POP/NOPOP capability for future changes.

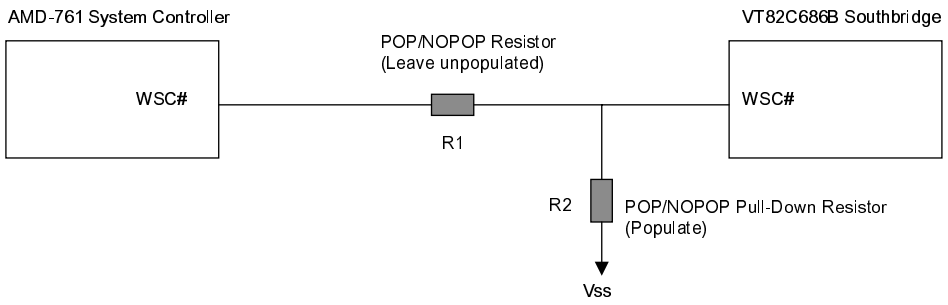


Figure 3. New Configuration

Note: *This solution only applies to uniprocessor applications using the AMD-761 system controller.*

Due to the shared IRQ architecture implemented by Windows® operating systems, the above solution provides proper operation for Windows PC-2001 compliance. How? As ISRs (Interrupt Service Routines) are invoked, the ISRs read the status registers of the various devices to determine the source of the interrupt. The reading of the status registers forces the proper flushing of the posted write-buffers of the AMD-761 system controller before the local APIC sends an interrupt message to the processor. Hence, data coherency issues are avoided.

ACPI S3 Incompatibility with Registered DDR DIMMs

Background

Systems employing registered DDR DIMMs and the AMD-761 system controller/VT82C686B southbridge combination may experience data corruption when entering or exiting the ACPI S3 (Suspend to RAM) power management state. This is due to an incompatibility in the sequencing of the PCIRESET# signal between the Northbridge and the Southbridge.

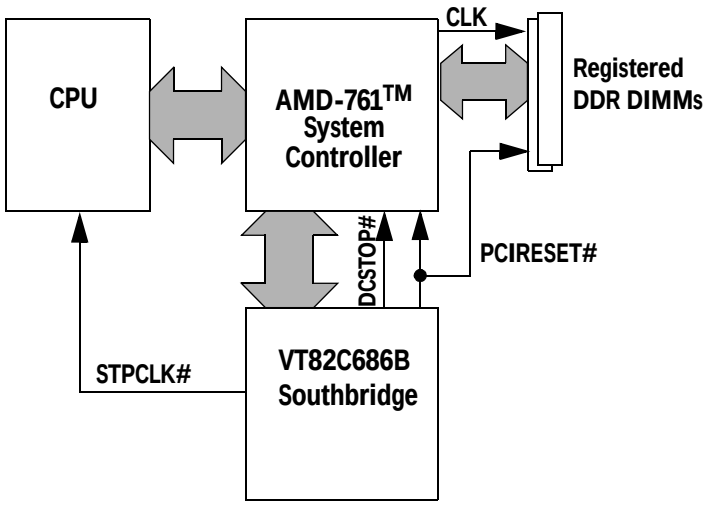


Figure 4. DDR DIMM Reset Connection in AMD-761™ System Controller System

The AMD-761 system controller supports the ACPI S3 state by specific sequencing on the DCSTOP# and PCIRESET# pins. When entering the S3 state the DCSTOP# pin must be asserted followed by the assertion of the PCIRESET# pin one RTC clock later (~30 mS). The PCIRESET# assertion is used by the AMD-761 system controller to gate off its I/O pad ring since the pad ring will be powered off while the core remains powered (the DDR I/O pad ring remains powered). Approximately four clocks later the DDR clocks will be disabled. Since registered DIMMs incorporate PLLs and registers on the module, they require a separate reset pin that must be asserted before its clocks are removed to allow stable operation.

As shown in Figure 4 on page 6, the reset pin on the DDR DIMMs is connected to the Southbridge PCIRESET# pin in a AMD-761 system controller-based system. When entering the Suspend to RAM state, the AMD-761 system controller continues to drive the DDR clocks for at least four clocks after the PCIRST# pin is asserted to meet the DIMM requirements.

- The VT82C686B does not follow the DCSTOP# and PCIRESET# sequencing listed above. The VT82C686B does not assert the PCIRESET# pin low until after the power supply has been turned off (PWRGOOD de-asserted). This means that the system clock generator is already powered off by the time the AMD-761 system controller detects the assertion of PCIRESET#. This potentially results in DDR memory failures since the DIMM was not properly shut down.

Solution

A solution for this incompatibility does not exist at this time. AMD does not recommend the use of the AMD-761 system controller with the VT82C686B Southbridge in registered DIMM applications.

Unbuffered DIMM applications using the AMD-761 system controller with the VT82C686B Southbridge function properly.