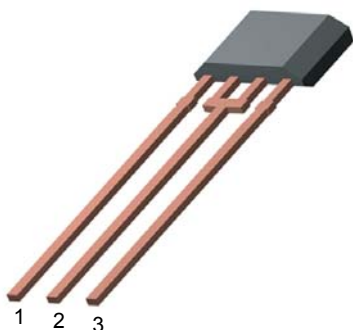


# A1373 and A1374

## High Precision, Output Pin Programmable Linear Hall Effect Sensors

Package KB, 3-pin SIP



1. VCC
2. GND
3. VOUT (Programming)

### ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $V_{CC}$ .....	16 V
Reverse-Supply Voltage, $V_{RCC}$ .....	-16 V
Output Voltage <sup>1</sup> , $V_{OUT}$ .....	16 V
Reverse-Output Voltage, $V_{ROUT}$ .....	-0.1 V
Output Current	
Source, $I_{OUTSOURCE}$ .....	3 mA
Sink, $I_{OUTSINK}$ .....	10 mA
Operating Temperature	
Ambient, $T_A$ , Range E .....	-40°C to 85°C
Ambient, $T_A$ , Range L .....	-40°C to 150°C
Maximum Junction, $T_{J(max)}$ .....	165°C
Storage Temperature, $T_S$ .....	-65°C to 170°C

<sup>1</sup>When blowing fuses during device programming, a voltage of 28 V may be applied to VOUT.

The A1373 and A1374 high precision linear Hall effect sensors are sensitive, temperature stable, linear devices with externally programmable features. This device family incorporates a chopper-stabilized amplifier, voltage regulator, programming logic, and an output amplifier on a single IC. The patented dynamic offset cancellation used with a chopper-stabilization technique provides extremely low offset and minimal temperature drift. A high frequency clock is used for chopping, to ensure high frequency signal processing capability. The A1373 and A1374 are ideal for use in automotive and industrial linear position-sensing applications that require increased reliability and accuracy over conventional contacting-potentiometer solutions. Key applications include: throttle position sensors, pedal position sensors, and suspension height sensors.

The design and manufacturing flexibility of the A1373 and A1374 complement the Allegro linear Hall effect family of devices by offering programmable gain, quiescent offset voltage for unipolar or bipolar operation, temperature coefficient, clamps, and polarity. The device can be set up in a magnetic circuit and programmed with a train of serial pulses via the output pin. Once the right combination of gain, quiescent output voltage, and temperature coefficient has been selected, the codes can be locked for one-time programming. In this manner, manufacturing tolerances can be reduced and the assembly process can be simplified.

These devices are available in the KB package, a 3-pin SIP (single inline package). The lead (Pb) free version has a 100% matte tin plated leadframe.

### Features and Benefits

- Output pin programming
- Field-programmable for optimal application integration
- Selectable coarse and fine gain and quiescent output voltage
- Selectable sensitivity temperature coefficient
- Selectable output clamp voltage level, including no-clamp (rail-to-rail)
- Selectable output polarity
- Unipolar or bipolar operation
- Ratiometric sensitivity, clamps, and quiescent output voltage
- Chopper-stabilized Hall technique
- Wide operating temperature range
- On-chip regulator for over/under voltage protection
- On-chip regulator provides EMI robustness
- Wide lead-spacing with KB package



# A1373 and A1374

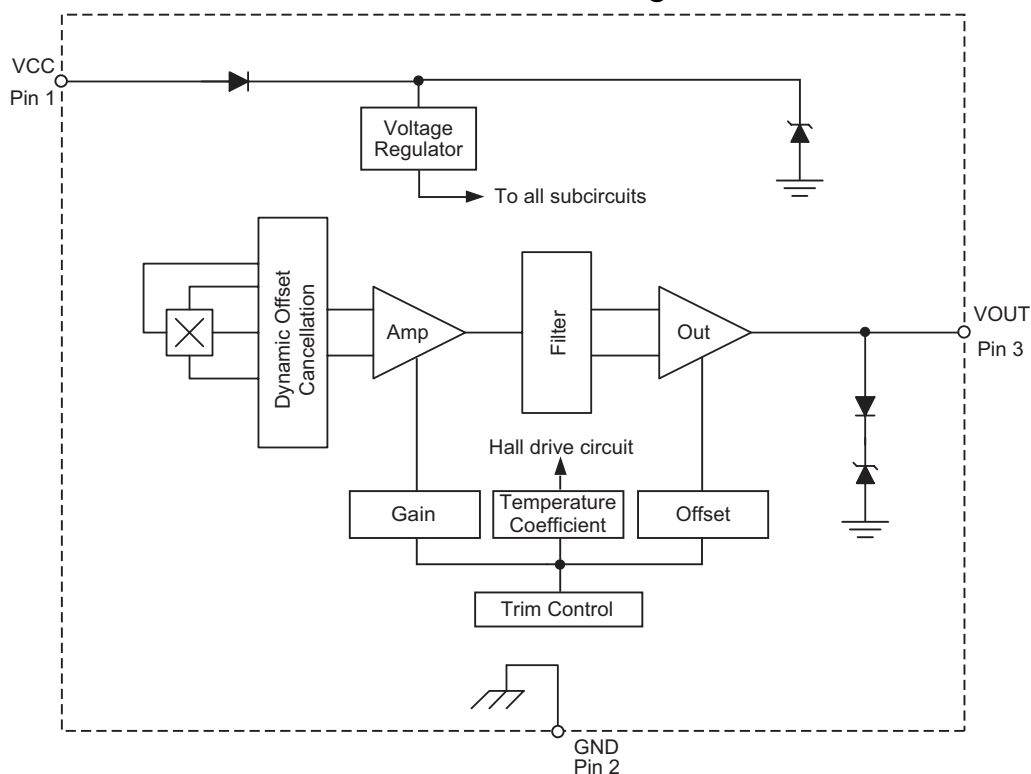
High Precision, Output Pin Programmable, Linear Hall Effect Sensors

## Product Selection Guide

Part Number	Pb-free	Packing*	Ambient, $T_A$ (°C)
A1373EKB	–	Bulk, 500 pcs./bag	–40 to 85
A1373EKB–T	Yes		
A1373EKBTI	–	14.24-in. reel, 2000 pcs/reel	
A1373EKBTI–T	Yes		
A1373LKB	–	Bulk, 500 pcs./bag	–40 to 150
A1373LKB–T	Yes		
A1373LKBTI	–	14.24-in. reel, 2000 pcs/reel	
A1373LKBTI–T	Yes		
A1374EKB	–	Bulk, 500 pcs./bag	–40 to 85
A1374EKB–T	Yes		
A1374EKBTI	–	14.24-in. reel, 2000 pcs/reel	
A1374EKBTI–T	Yes		
A1374LKB	–	Bulk, 500 pcs./bag	–40 to 150
A1374LKB–T	Yes		
A1374LKBTI	–	14.24-in. reel, 2000 pcs/reel	
A1374LKBTI–T	Yes		

\*Contact Allegro for additional packing options

## Functional Block Diagram



# A1373 and A1374

## High Precision, Output Pin Programmable, Linear Hall Effect Sensors

### CHARACTERISTIC PARAMETERS

Characteristic	Symbol	Test Conditions		Min.	Typ.	Max	Units
ELECTRICAL CHARACTERISTICS over operating temperature range, V <sub>CC</sub> =5.0 V, unless otherwise noted							
Supply Voltage	V <sub>CC</sub>	Operation within specification, T <sub>j</sub> < 165°C		4.5	5.0	5.5	V
Supply Current	I <sub>CC</sub>			–	8.2	10	mA
Reverse-Supply Current	I <sub>RCC</sub>	V <sub>CC</sub> = –16 V, T <sub>A</sub> = 25°C		–	–	16	mA
Power-On Time <sup>1</sup>	t <sub>PO</sub>	C <sub>LOAD</sub> = 10 nF, 90% full scale V <sub>OUT</sub>		–	–	300	μs
Chopping Frequency	f <sub>C</sub>			–	200	–	kHz
Internal Bandwidth	BW	A1373	Small signal -3 dB	–	2.5	–	kHz
		A1374		–	20	–	kHz
OUTPUT CHARACTERISTICS over operating temperature range, V <sub>CC</sub> =5.0 V, unless otherwise noted							
Noise <sup>2,3</sup>	V <sub>N</sub>	A1373	peak-to-peak, C <sub>LOAD</sub> > 1 nF, 2.5 mV/G	–	6	16	mV
		A1374		–	14	26	mV
Output Capacitance Load	C <sub>LOAD</sub>	V <sub>OUT</sub> pin to GND pin		–	–	10	nF
Output Resistive Load	R <sub>LOAD</sub>			4700	–	–	Ω
Phase Shift	ΔΦ	A1373	Magnetic signal freq. = 100 Hz	–	3	–	(°)
		A1374	Magnetic signal freq. = 1000 Hz	–	3	–	(°)
Output Voltage	V <sub>OUT(Sat)HIGH</sub>	I <sub>OUTSINK</sub> = 1.2 mA, B(kG) > (V <sub>CC</sub> –V <sub>OUT(Q)</sub> ) / Sens (mV/G)		4.65	4.7	–	V
	V <sub>OUT(Sat)LOW</sub>	I <sub>OUTSOURCE</sub> = 1.2 mA, B(kG) < V <sub>OUT(Q)</sub> / Sens (mV/G)		–	0.2	0.25	V
Output Resistance	R <sub>OUT</sub>			–	1.5	–	Ω
MAGNETIC CHARACTERISTICS							
Magnetic Slew Rate	SLR	V / ms / Sens		–	20	–	G/μs
PRE-PROGRAMMING TARGET (Prior to coarse and fine trim) over operating temperature range, V <sub>CC</sub> =5.0 V, unless otherwise noted							
Pre-Programming Quiescent Output Voltage	V <sub>OUT(Q)PRE</sub>	B = 0 G, T <sub>A</sub> = 25°C		1.62	1.80	1.98	V
Pre-Programming Sensitivity	Sens <sub>PRE</sub>	T <sub>A</sub> = 25°C		1.05	1.31	1.75	mV/G
Pre-Programming Sensitivity Temperature Coefficient	TC <sub>PRE</sub>	T <sub>A</sub> relative to 25°C		–0.016	0.05	0.104	%/°C
INITIAL COARSE PROGRAMMING over operating temperature range, V <sub>CC</sub> =5.0 V, unless otherwise noted							
Initial Coarse Quiescent Output Voltage	V <sub>OUT(Q)INITLOW</sub>	T <sub>A</sub> = 25°C		–	0.55	–	V
	V <sub>OUT(Q)INITMID</sub>	Reference V <sub>OUT(Q)PRE</sub>		–	—	–	V
	V <sub>OUT(Q)INITHIGH</sub>	T <sub>A</sub> = 25°C		–	3.25	–	V
Initial Coarse Sensitivity	Sens <sub>INITLOW</sub>	Reference Sens <sub>PRE</sub>		–	–	–	mV/G
	Sens <sub>INITMID</sub>	T <sub>A</sub> = 25°C		–	2.8	–	mV/G
	Sens <sub>INITHIGH</sub>	T <sub>A</sub> = 25°C		–	5.5	–	mV/G

Continued on the next page...

# A1373 and A1374

## High Precision, Output Pin Programmable, Linear Hall Effect Sensors

### CHARACTERISTIC PARAMETERS (continued)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max	Units	
QUIESCENT OUTPUT VOLTAGE PROGRAMMING over operating temperature range, V <sub>CC</sub> = 5.0 V, unless otherwise noted							
Quiescent Output Voltage Range	V <sub>OUT(Q)LOW</sub>	B = 0 G, T <sub>A</sub> = 25°C	0.7	–	1.9	V	
	V <sub>OUT(Q)MID</sub>		2.0	–	3.2	V	
	V <sub>OUT(Q)HIGH</sub>		3.5	–	4.5	V	
Average Quiescent Output Voltage Step Size <sup>4,5,6</sup>	Step <sub>VOUT(Q)</sub>	T <sub>A</sub> = 25°C	3.0	3.275	3.5	mV	
Quiescent Output Voltage Programming Resolution	Err <sub>PROGVOUT(Q)</sub>	Fine programming value selection accuracy	–	±0.5 × Step <sub>VOUT(Q)</sub>	–	mV	
Quiescent Output Voltage Drift Over Operating Temperature Range	ΔV <sub>OUT(Q)</sub>	V <sub>OUT(Q)</sub> = V <sub>OUT(Q)LOW</sub>	–	–	±40	mV	
		V <sub>OUT(Q)</sub> = V <sub>OUT(Q)MID</sub>	–	–	±40	mV	
		V <sub>OUT(Q)</sub> = V <sub>OUT(Q)HIGH</sub>	–	–	±55	mV	
Quiescent Output Voltage Programming Bits	–	Coarse (Range selection)	–	2	–	Bit	
		Fine (Value selection)	–	9	–	Bit	
10% Output Clamp Option <sup>7</sup>	V <sub>OUTCLP10HIGH</sub>	A1373	High-side output clamp	4.350	–	4.565	V
		A1374		4.300	–	4.650	V
	V <sub>OUTCLP10LOW</sub>	A1373	Low-side output clamp	0.4	–	0.6	V
		A1374		0.3	–	0.6	V
20% Output Clamp Option <sup>7</sup>	V <sub>OUTCLP20HIGH</sub>	A1373	High-side output clamp	3.925	–	4.125	V
		A1374		3.900	–	4.200	V
	V <sub>OUTCLP20LOW</sub>	A1373	Low-side output clamp	0.9	–	1.1	V
		A1374		0.8	–	1.1	V
Delay to Clamp	t <sub>CLP</sub>	A1373	–	–	2	μs	
		A1374	–	–	100	μs	
SENSITIVITY PROGRAMMING over operating temperature range, V <sub>CC</sub> = 5.0 V, unless otherwise noted							
Sensitivity Range <sup>8</sup>	Sens <sub>LOW</sub>	T <sub>A</sub> = 25°C	1.75	–	2.8	mV/G	
	Sens <sub>MID</sub>		3.5	–	5.7	mV/G	
	Sens <sub>HIGH</sub>		7.0	–	11.25	mV/G	
Average Sensitivity Step Size <sup>4,5,6</sup>	Step <sub>SENSLOW</sub>	T <sub>A</sub> = 25°C	6	9.5	14	μV/G	
	Step <sub>SENSMID</sub>		12	18.7	28	μV/G	
	Step <sub>SENSHIGH</sub>		22	37.0	56	μV/G	
Sensitivity Programming Resolution	Err <sub>PROGSENS</sub>	Fine programming value selection accuracy	–	±0.5 × Step <sub>SENS</sub>	–	μV/G	
Sensitivity Programming Bits	–	Coarse (Range selection)	–	2	–	Bit	
		Fine (Value selection)	–	8	–	Bit	
POLARITY PROGRAMMING							
Polarity Programming Bit	–	Negative Sensitivity	–	1	–	Bit	

Continued on the next page...

# A1373 and A1374

## High Precision, Output Pin Programmable, Linear Hall Effect Sensors

### CHARACTERISTIC PARAMETERS (continued)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max	Units
<b>SENSITIVITY TEMPERATURE COEFFICIENT PROGRAMMING</b> over operating temperature range, $V_{CC}=5.0$ V, unless otherwise noted						
Sensitivity Temperature Coefficient Range	TC	Sensitivity T/C codes 0 to 11, minimum (absolute) positive temperature coefficient attainable	–	0.07	–	%/°C
		Sensitivity T/C codes 16 to 27, minimum (absolute) negative temperature coefficient attainable	–	–0.016	–	%/°C
Average Sensitivity Temperature Coefficient Step Size <sup>4,5,6</sup>	Step <sub>TC</sub>	$T_A = 150^{\circ}\text{C}$	–	0.01	–	%/°C
Sensitivity Temperature Coefficient Programming Bits	–		–	5	–	Bit
<b>ONE-TIME PROGRAMMING</b>						
Device Programming Lock Bit	–		–	1	–	Bit
<b>RATIOMETRY</b> over operating temperature range, $V_{CC}=5.0$ V, unless otherwise noted						
Quiescent Voltage Error	Rat <sub>VOUT(Q)</sub>	$V_{CC}$ at $V_{\text{OPERATING}}$	–	±0.25	–	%
Sensitivity Error	Rat <sub>SENS</sub>	$V_{CC}$ at $V_{\text{OPERATING}}$	–	±1.0	–	%
Clamp Error	Rat <sub>VOUTCLP</sub>	$V_{CC}$ at $V_{\text{OPERATING}}$	–	±1.5	–	%
<b>LINEARITY</b> over operating temperature range, $V_{CC}=5.0$ V, unless otherwise noted						
Positive Linearity Error	Lin+	$V_{CC}$ at $V_{\text{OPERATING}}$	–	±0.5	–	%
Negative Linearity Error	Lin–	$V_{CC}$ at $V_{\text{OPERATING}}$	–	±0.5	–	%
<b>SYMMETRY</b> over operating temperature range, $V_{CC}=5.0$ V, unless otherwise noted						
Symmetry Error	Sym	$V_{CC}$ at $V_{\text{OPERATING}} - V_{CC}$	–	±0.35	–	%
<b>ADDITIONAL CHARACTERISTICS</b>						
Sensitivity Drift <sup>9</sup>	ΔSens		–	–	±2	%
<b>FAULT CONDITIONS</b> over operating temperature range, $V_{CC}=5.0$ V, unless otherwise noted						
Shorted Output Wire	I <sub>OUTSHT</sub>	VOUT pin to VCC pin	–	–	18	mA
		VOUT pin to GND pin	–	–	4	mA

<sup>1</sup>  $t_{PO}$  does not include  $t_{CLP}$ , specified in the Quiescent Programming section of this table.

<sup>2</sup> Peak to peak value exceeded: 0.3% (6σ).

<sup>3</sup> For A1373, no digital noise is present at the output.

<sup>4</sup> Step size is larger than required for the specified range, to take into account manufacturing spread.

<sup>5</sup> Individual code step sizes can be greater than 2× larger than the step size at each significant bit rollover.

<sup>6</sup> Average fine code step size in a given range = (Output value at highest fine code in the range – Output value at code 0 of the range) / Total quantity of steps (codes) in the range.

<sup>7</sup> Values indicated are valid if any additional magnetic field does not exceed  $B(kG) = \pm 2 (V) / \text{Sens} (mV/G)$ , after  $V_{\text{OUTCLP}}$  is reached.

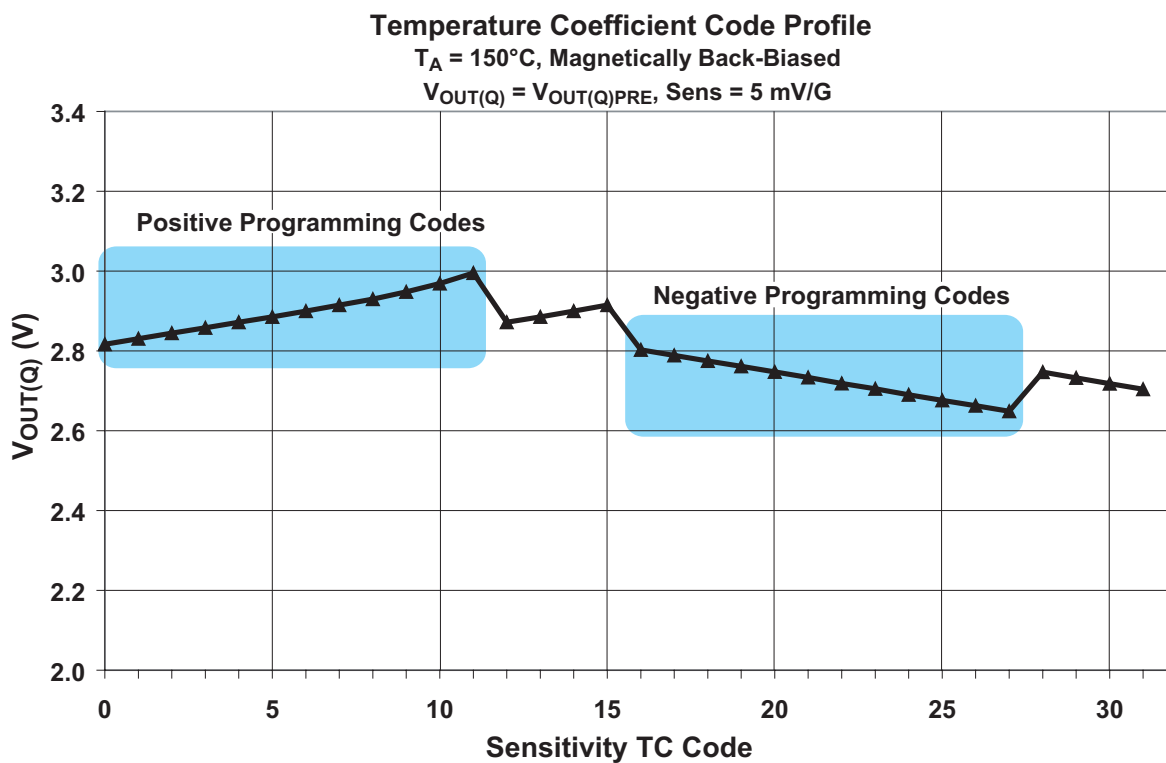
<sup>8</sup> Program the Sensitivity T/C register before programming Sensitivity Coarse and Sensitivity Fine, due to a worst case shift of ±3% in sensitivity at 25°C at the maximum values for Sensitivity T/C: Positive T/C and Sensitivity T/C: Negative T/C. The Programming Guidelines section in this document lists a complete recommended order for programming individual values.

<sup>9</sup> Drift due to temperature cycling is due to package effects on the Hall transducer. The stress is reduced when the package is baked. However, it will recover over time after removal from the bake.

# A1373 and A1374

High Precision, Output Pin Programmable, Linear Hall Effect Sensors

## Typical Characteristics

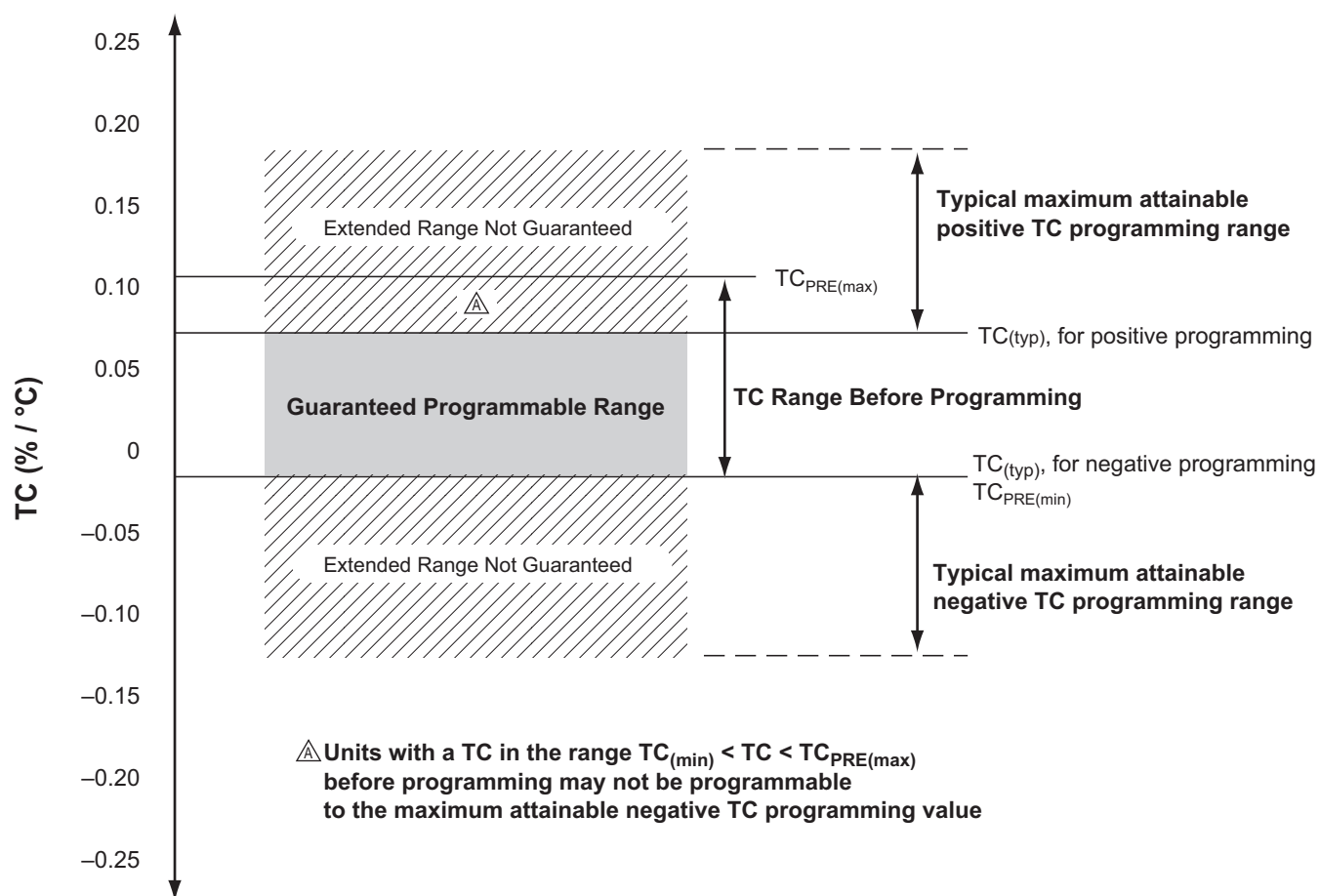


Code	Application
0	Initial code
1 – 11	Positive TC codes, use to increase TC value
12 – 15	[Unused, same effect as 4 – 7, respectively]
16 – 27	Negative TC codes, use to decrease TC value
28 – 31	[Unused, same effect as 20 – 23, respectively]

# A1373 and A1374

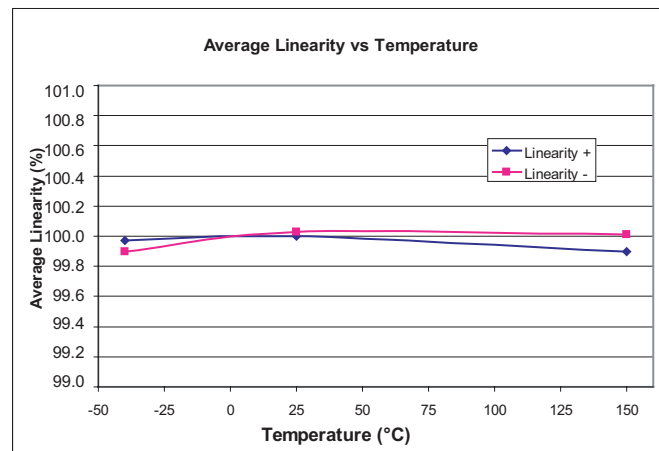
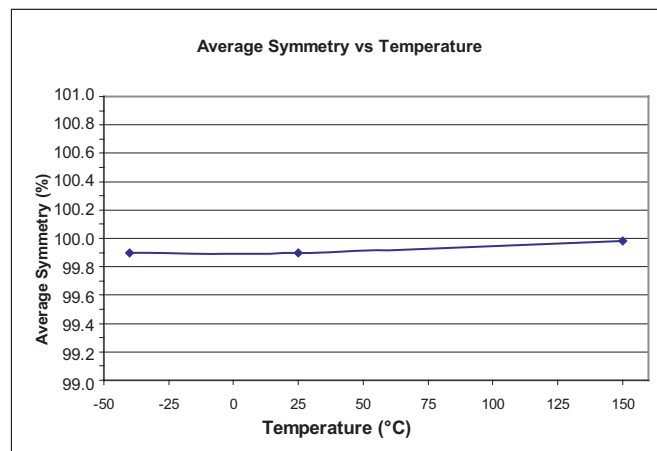
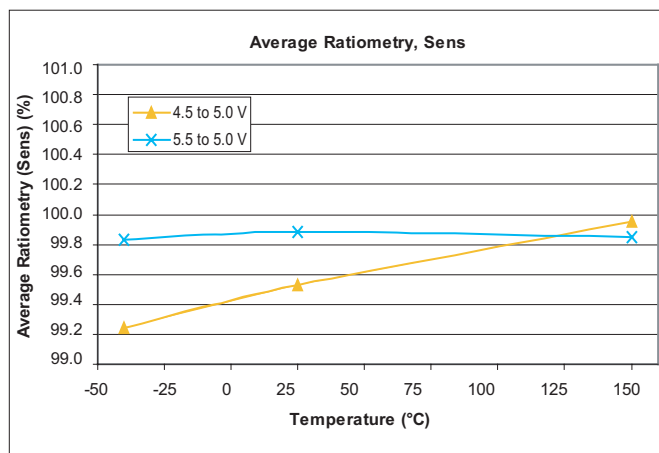
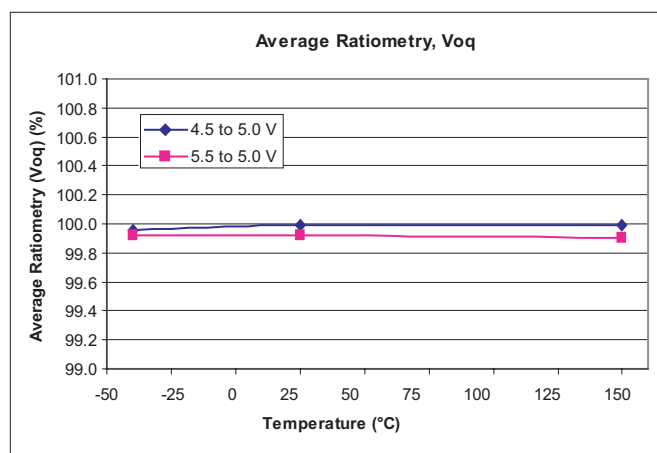
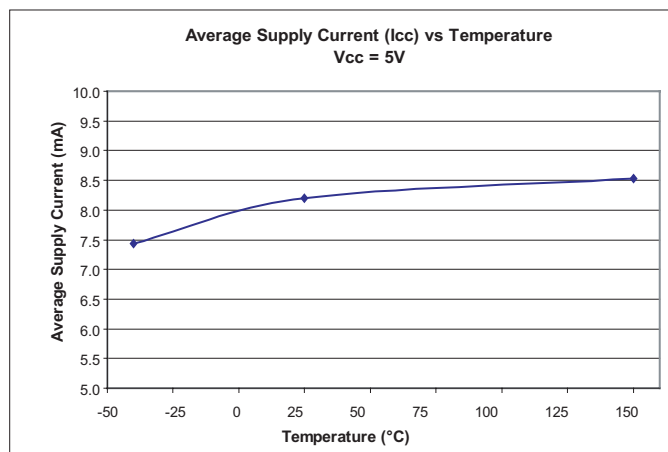
High Precision, Output Pin Programmable, Linear Hall Effect Sensors

## Sensitivity Temperature Coefficient Range, TC



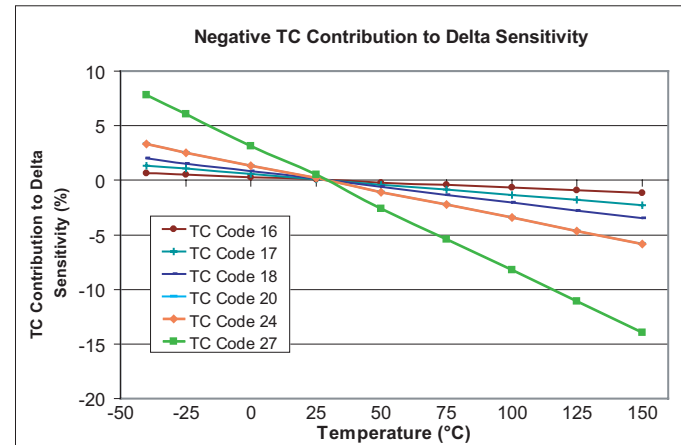
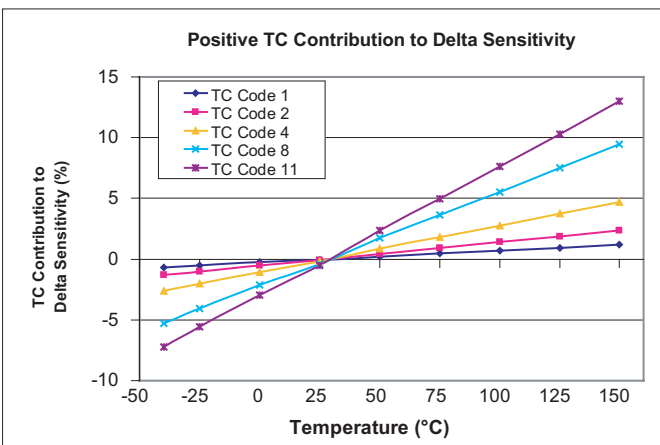
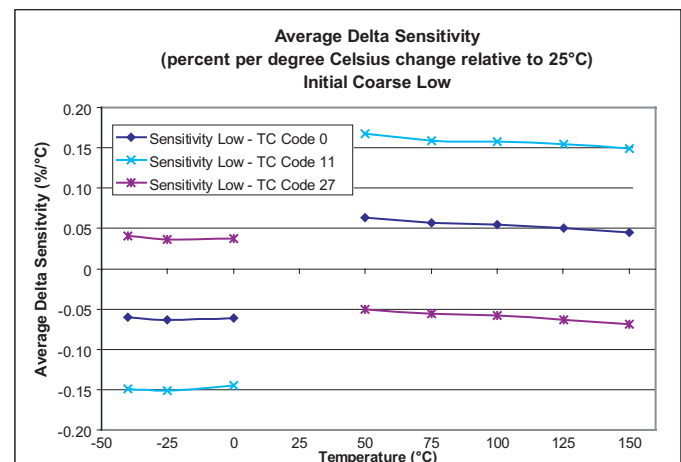
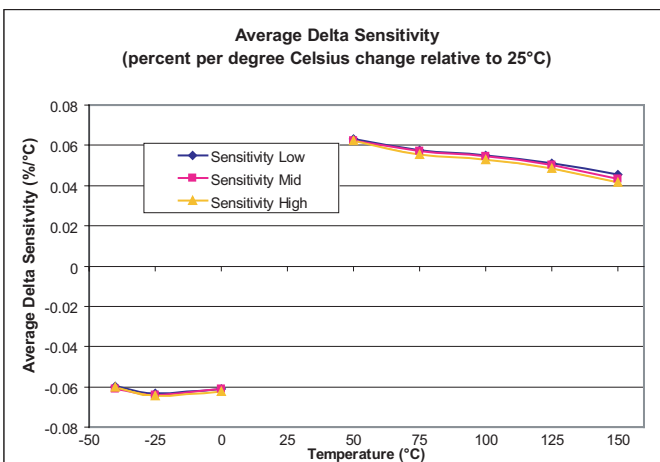
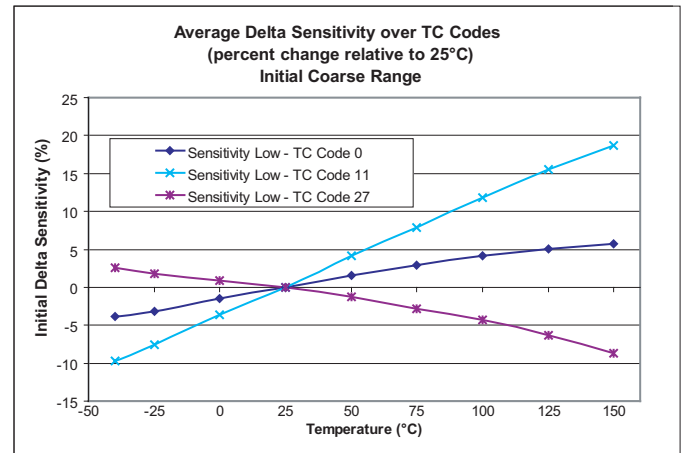
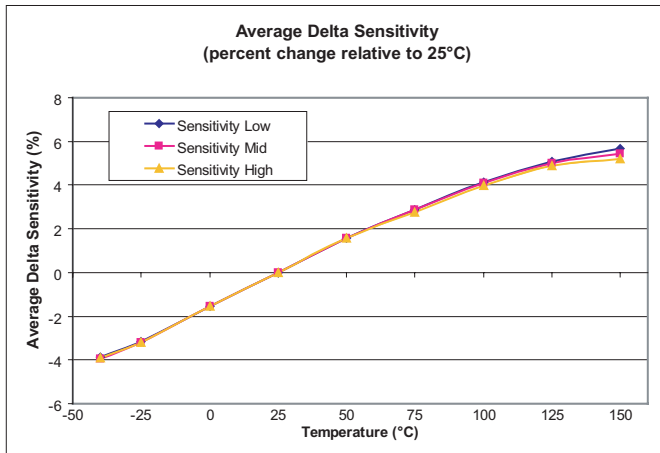
# A1373 and A1374

High Precision, Output Pin Programmable, Linear Hall Effect Sensors



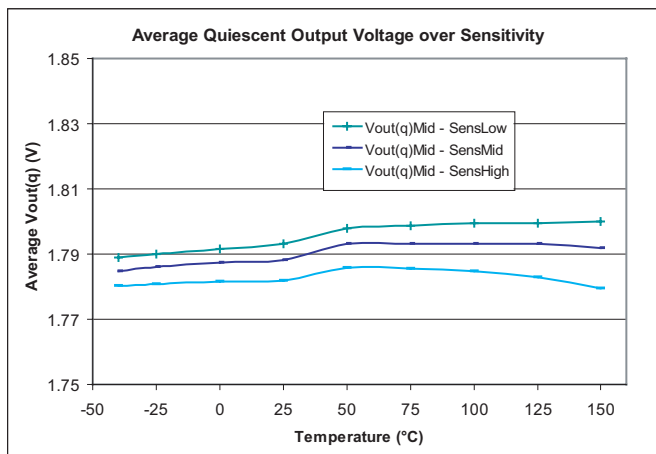
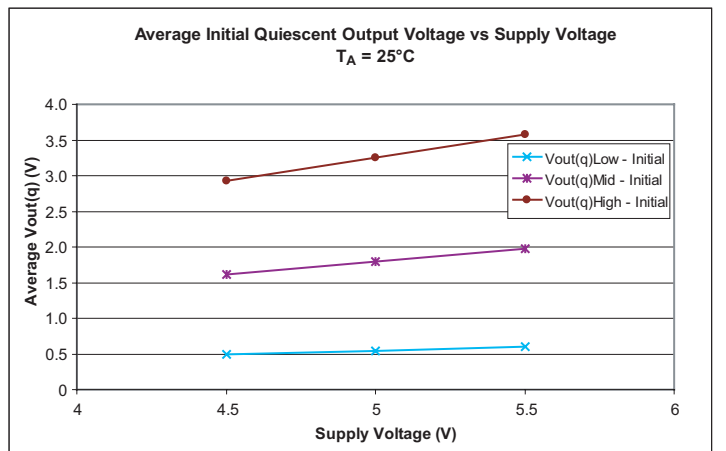
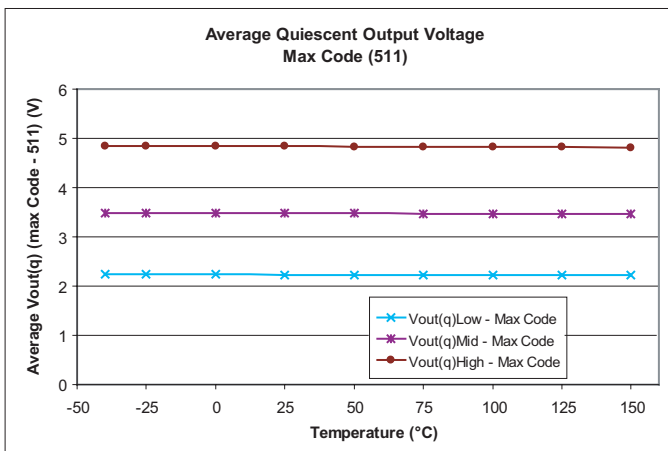
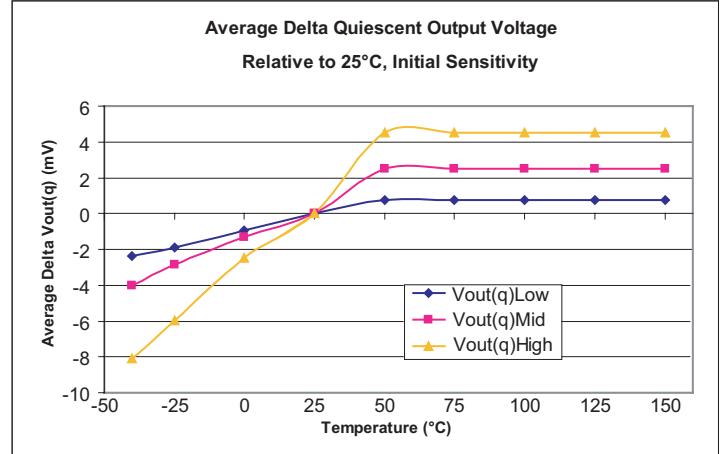
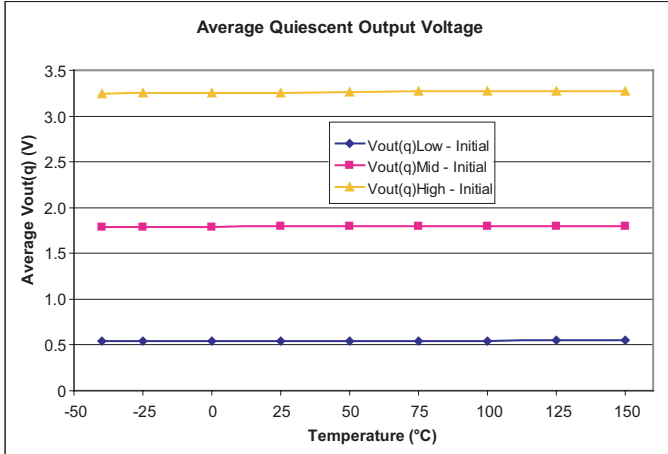
# A1373 and A1374

## High Precision, Output Pin Programmable, Linear Hall Effect Sensors



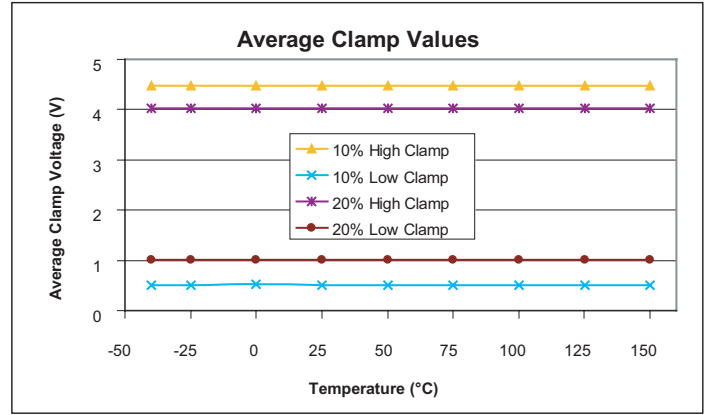
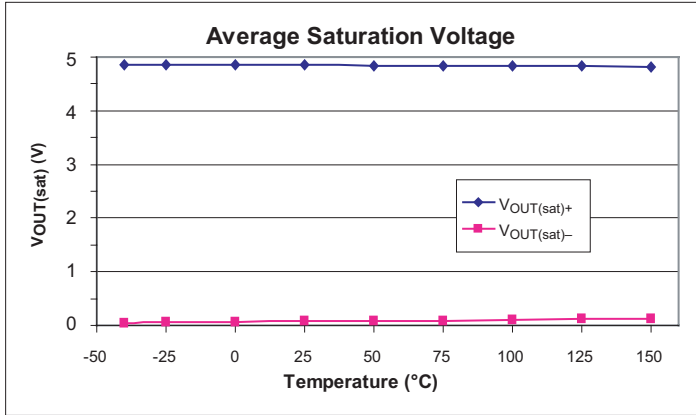
# A1373 and A1374

## High Precision, Output Pin Programmable, Linear Hall Effect Sensors



# A1373 and A1374

High Precision, Output Pin Programmable, Linear Hall Effect Sensors



# A1373 and A1374

## High Precision, Output Pin Programmable, Linear Hall Effect Sensors

### Chopper Stabilization Technique

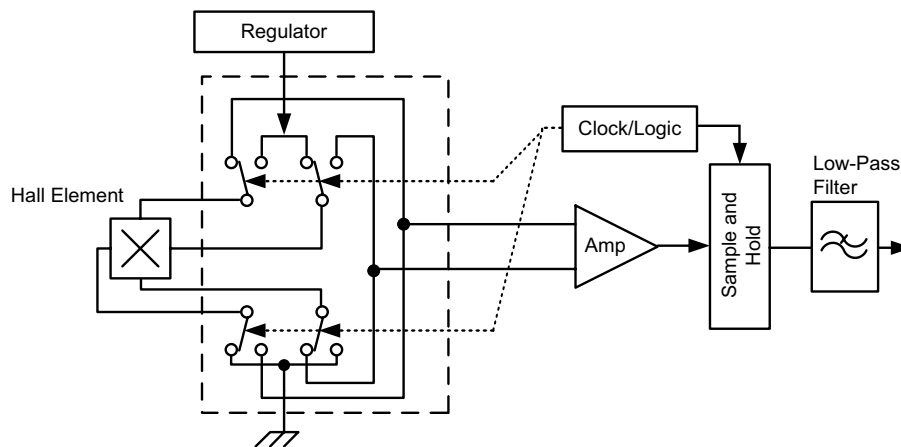
Chopper stabilization is a unique approach used to minimize Hall offset on the chip. The patented Allegro technique, namely Dynamic Quadrature Offset Cancellation, removes key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation.

The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field-induced signal to recover its original spectrum at baseband, while the dc offset becomes a high-frequency signal. The magnetic-sourced signal then can

pass through a low-pass filter, while the modulated dc offset is suppressed.

The chopper stabilization technique uses a 200 kHz high frequency clock. For demodulation process, a sample and hold technique is used, where the sampling is performed at twice the chopper frequency (400 kHz). This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability.

This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.



Concept of Chopper Stabilization Technique

# A1373 and A1374

## High Precision, Output Pin Programmable, Linear Hall Effect Sensors

### Definitions of Terms

**Linear:** A type of Hall-Effect sensor that produces an analog output voltage proportional to the strength of a sensed magnetic field.

**Ratiometric:** A linear Hall-Effect sensor that, when not subjected to a significant magnetic field, has an output that is a ratio of its supply voltage. A ratiometric performance of 100% indicates the output follows the supply with no percentage error.

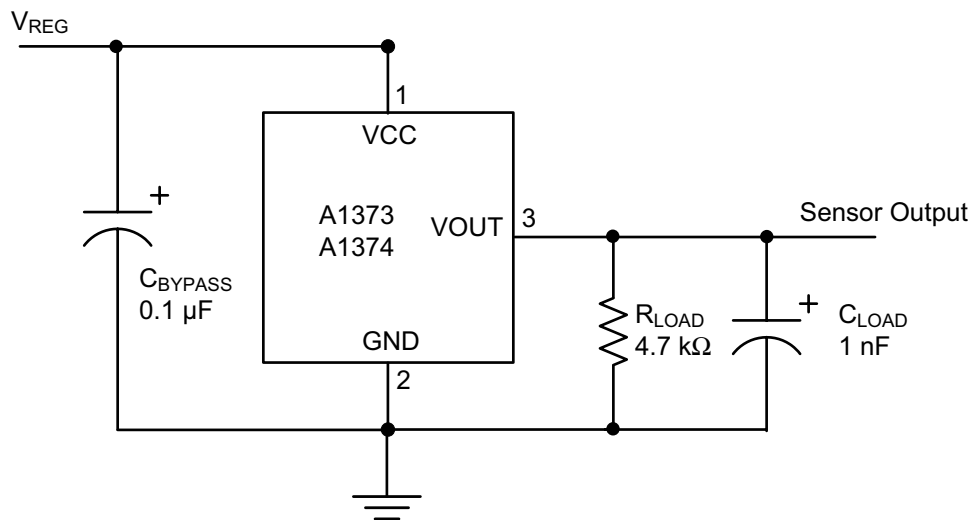
**Gauss:** Standard unit of measuring magnetic flux density. 1 gauss is equal to 1 Maxwell per square centimeter or  $10^{-4}$  tesla. (For reference, the earth's magnetic field is approximately 0.5 gauss.)

**Blowing:** Applying a pulse of sufficient voltage and duration to permanently set a bit, by blowing a fuse internal to the device. Once a bit (fuse) has been blown, it cannot be reset. The terms *trimming* and *programming* can be used interchangeably with *blowing* in this context.

**Programming modes:** Testing the results is the only valid method to guarantee successful programming, and multiple modes are provided to support this. The programming modes are described in the section Mode Selection State.

**Code:** The number used to identify the register and the bitfield to be programmed, expressed as the decimal equivalent of the binary value. The LSB of a register is denoted as bit 0.

### Typical Application Drawing



### Characteristic Definitions

**Quiescent Output Voltage.** In the quiescent state (no significant magnetic field:  $B = 0$ ), the output,  $V_{OUTQ}$ , equals a ratio of the supply voltage,  $V_{CC}$ , throughout the entire operating ranges of  $V_{CC}$  and ambient temperature,  $T_A$ . Due to internal component tolerances and thermal considerations, however, there is a tolerance on the quiescent output voltage,  $\Delta V_{OUTQ}$ , which is a function of both  $\Delta V_{CC}$  and  $\Delta T_A$ . For purposes of specification, the quiescent output voltage as a function of temperature,  $\Delta V_{OUTQ}(\Delta T_A)$ , is defined as:

$$\Delta V_{OUTQ}(\Delta T_A) = \frac{V_{OUTQ}(T_A) - V_{OUTQ}(25^\circ\text{C})}{Sens_{(25^\circ\text{C})}} \quad (1)$$

where Sens is in mV/G, and the result is the device equivalent accuracy, in gauss (G), applicable over the entire operating temperature range.

**Sensitivity.** The presence of a south-polarity (+B) magnetic field, perpendicular to the branded face of the device package, increases the output voltage,  $V_{OUT}$ , in proportion to the magnetic field applied, from  $V_{OUTQ}$  toward the  $V_{CC}$  rail. Conversely, the application of a north polarity (–B) magnetic field, in the same orientation, proportionally decreases the output voltage from its quiescent value. This proportionality is specified as the magnetic sensitivity of the device and is defined as:

$$Sens = \frac{V_{OUT(-B)} - V_{OUT(+B)}}{2B} \quad (2)$$

The stability of the device magnetic sensitivity as a function of ambient temperature,  $\Delta Sens_{(\Delta T_A)}$  (%) is defined as:

$$\Delta Sens_{(\Delta T_A)} = \frac{Sens_{(T_A)} - Sens_{(25^\circ\text{C})}}{Sens_{(25^\circ\text{C})}} \times 100\% \quad (3)$$

**Ratiometric.** The A1373 and A1374 feature ratiometric output. This means that the quiescent voltage output,  $V_{OUTQ}$ , magnetic sensitivity, Sens, and clamp voltage,  $V_{OUTCLP}$ , are

proportional to the supply voltage,  $V_{CC}$ .

The ratiometric change in the quiescent output voltage,  $RAT_{VOUT(Q)}$  (%), is defined as:

$$RAT_{VOUT(Q)} = \frac{V_{OUTQ}(V_{CC}) / V_{OUTQ}(5V)}{V_{CC} / 5V} \times 100\% \quad (4)$$

the ratiometric change in sensitivity is defined as:

$$RAT_{Sens} = \frac{Sens_{(V_{CC})} / Sens_{(5V)}}{V_{CC} / 5V} \times 100\% \quad (5)$$

and the ratiometric change in clamp voltage is defined as:

$$RAT_{VCLP} = \frac{V_{CLP}(V_{CC}) / V_{CLP}(5V)}{V_{CC} / 5V} \times 100\% \quad (6)$$

Note that clamping effect is applicable only when clamping is enabled by programming of the device.

**Linearity and Symmetry.** The on-chip output stage is designed to provide linear output at a supply voltage of 5 V. Although the application of very high magnetic fields does not damage these devices, it does force their output into a nonlinear

$$Lin+ = \frac{V_{OUT(+B)} - V_{OUTQ}}{2(V_{OUT(+B/2)} - V_{OUTQ})} \times 100\% \quad (7)$$

$$Lin- = \frac{V_{OUT(-B)} - V_{OUTQ}}{2(V_{OUT(-B/2)} - V_{OUTQ})} \times 100\% \quad (8)$$

region. Linearity in percent is measured and defined as:

$$Sym = \frac{V_{OUT(+B)} - V_{OUTQ}}{V_{OUTQ} - V_{OUT(-B)}} \times 100\% \quad (9)$$

and output symmetry as:

# A1373 and A1374

## High Precision, Output Pin Programmable, Linear Hall Effect Sensors

### Pulse Generation

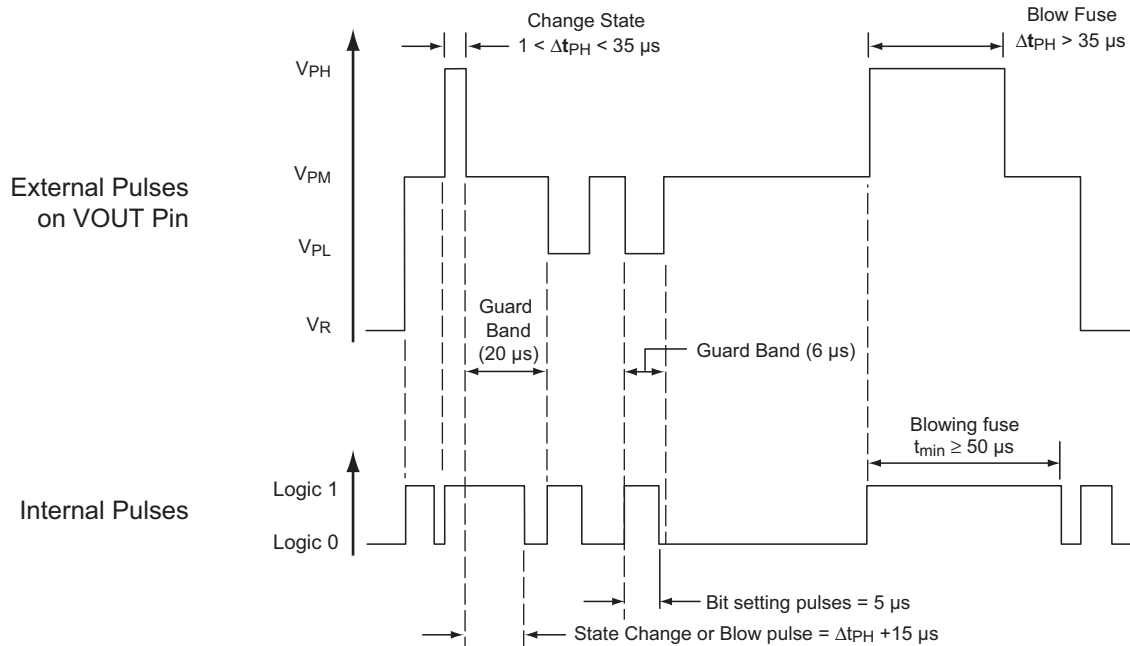
Several parameters can be field-programmed. To do so, a coded series of voltage pulses through the VOUT pin is used to set bitfields in onboard registers. The effect on the device output can be monitored, and the registers can be cleared and set repeatedly until the required output results are achieved. To make the setting permanent, bitfield-level solid state fuses are blown, and finally, a device-level fuse is blown, blocking any further coding.

Although any programmable variable power supply can be used to generate the pulsed waveforms, Allegro highly recommends using the Allegro Sensor Evaluation Kit, available on the Allegro Web site On-line Store. The manual for that kit is available for download free of charge, and provides additional information on programming these devices.

There are four relative nominal voltage levels that must be taken into account when programming. For purposes of explanation in this document, the signal levels are referred to simply as high programming voltage,  $V_{PH}$ , midrange,  $V_{PM}$ , and low,  $V_{PL}$ . The

fourth voltage level,  $V_R$ , is a very low level, near zero volts, used to reset the bitfields that have not yet been isolated by blown fuses.

The high level,  $V_{PH}$ , pulse is maintained either for short duration ( $\Delta t_{PH} = 1$  to  $<<35 \mu s$ ), acting as a strobe to signal the transition between states, or for long duration ( $\Delta t_{PH} \geq 35 \mu s$ ) and used for fuse-blowing. The device generates an internal pulse beginning at the leading (rising) edge of a  $V_{PH}$  pulse. The duration of the internal pulse is the duration of the external  $V_{PH}$  pulse,  $\Delta t_{PH}$ , plus  $15 \mu s$ . The added time is a buffer to compensate for voltage drop when the high current is sourced, ensuring that there is sufficient power to blow the fuse completely. Before sending another pulse, an additional guard band of  $5 \mu s$  is recommended to allow the signal to decay, for a total of at least  $20 \mu s$  after the end of any  $V_{PH}$  pulse.  $\Delta t_{PH}$  is measured from the time when the external signal voltage rises above  $23.6 V$  to the time when it falls below  $19.4 V$ . The nominal level for  $V_{PH}$  is  $28 V$ .



Note: Spurious bit-setting pulses are generated on first  $V > V_{PL}$  after  $V_R$ , and at last  $V_{PL}$ .

### Programming Pulse Waveforms

# A1373 and A1374

## High Precision, Output Pin Programmable, Linear Hall Effect Sensors

The midrange voltage level,  $V_{PM}$ , is a neutral level, used to separate both  $V_{PH}$  and  $V_{PL}$  pulses from each other. The nominal level for  $V_{PM}$  is 15 V.

The low level,  $V_{PL}$ , pulse is used to indicate bitfield addresses that are to be set. The device generates an internal pulse beginning at the leading (falling) edge of a  $V_{PL}$  pulse. The duration of the internal pulse is 5  $\mu$ s. Before allowing the voltage to rise again, an additional guard band of 1  $\mu$ s is recommended to ensure that the pulse completes, for a total of at least 6  $\mu$ s after the start of any  $V_{PL}$  pulse. The duration of the  $V_{PL}$  pulse,  $\Delta t_{PL}$ , is measured from the time when the external signal voltage falls into the range 0 to 7.5 V to the time when it rises above 10 V. If the voltage rises above 10 V before the 5  $\mu$ s period expires, then

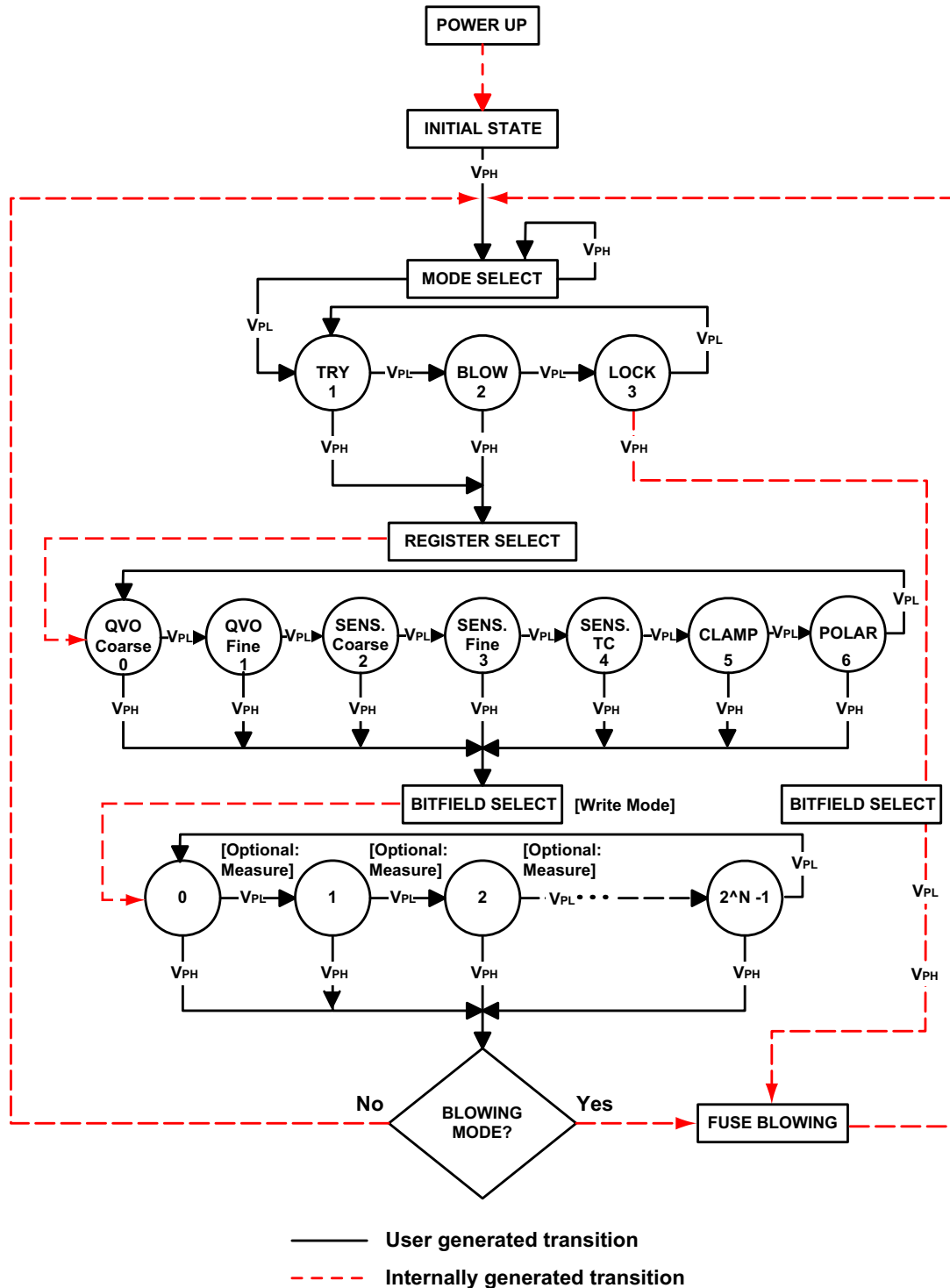
the  $V_{PL}$  pulse will immediately end, with undefined results. The nominal level for  $V_{PH}$  is 5 V.

$V_{PL}$  must always be maintained high enough above  $V_R$  (nominally 0 V) to maintain the settings provisionally latched into registers. Note that, when the external voltage rises from  $V_R$  through the  $V_{PL}$  range, a spurious internal pulse is generated, making Code 0 not available in Mode Selection state. A spurious internal pulse also is generated when the external voltage falls through the  $V_{PL}$  range at the end of a code sequence. For that reason, it is mandatory to ensure that the voltage is dropped fully to  $V_R$ , before every Blow Fuse mode operation, to ensure that the spurious pulse does not affect the next code sequence.

# A1373 and A1374

High Precision, Output Pin Programmable, Linear Hall Effect Sensors

## Programming State Machine



# A1373 and A1374

## High Precision, Output Pin Programmable, Linear Hall Effect Sensors

### Programming Protocol and State Machine Description

#### INITIAL STATE

After system power-up, the programming logic is reset to a known state. This is referred to as the Initial state. All the registers that have intact fuses are set to logic 0.

While in the Initial state, any  $V_{PL}$  pulses on the VOUT pin are ignored.

To enter the Mode Selection state, send one  $V_{PH}$  pulse on the VOUT pin.

#### MODE SELECTION STATE

This state allows the selection of the programming mode:

- Try Value Mode. In this mode, the user provisionally downloads settings to the device registers, without blowing the bits. The user can increment through the codes of each parameter, and evaluate the results of various code settings.
- Blow Fuse Mode. In this mode, after downloading the settings, the user can blow the fuses in specific registers.
- Lock Device Mode. This mode is similar to Blow Fuse mode, except that the fuse that is blown permanently prevents any further programming of any bits in the device.

To select a mode, increment through the register bitfields by sending  $V_{PL}$  pulses on the VOUT pin, as follows:

- 0 pulses – No effect
- 1 pulse – Try Value mode
- 2 pulses – Blow Fuse mode
- 3 pulses – Lock Device mode

This register wraps by default. This means that sending additional  $V_{PL}$  pulses traverses the register again.

Any  $V_{PH}$  pulse sent before a  $V_{PL}$  pulse has no effect.

To enter the Register Selection state, after sending a valid quantity of  $V_{PL}$  pulses, send one  $V_{PH}$  pulse on the VOUT pin.

#### REGISTER SELECTION STATE

This state allows the selection of the register containing the bitfields to be programmed. Selecting the register corresponds to selecting the parameter to be set. For bit codes, see the section Programming Logic.

- QVO [ $V_{OUT(Q)}$ ] Coarse. Register for setting the range of the operating dc point (2 bits)
- QVO Fine. Register for setting the value within the range set in the QVO Coarse register (9 bits)
- Sens. [Sensitivity] Coarse. Register for setting the overall gain of the

device (2 bits)

- Sens. Fine. Register for setting the value within the range set in the Sens. Coarse register (8 bits)
- [Sensitivity] TC Register. Register for setting the temperature coefficient for the device (5 bits).
- Clamp [ $V_{OUTCLP}$ ] Bit. Register for setting the clamping voltage of the output (2 bits)
- Polarity Bit. Register setting the polarity of the output (1 bit)

To select a register, increment through the register bitfields by sending  $V_{PL}$  pulses on the VOUT pin. Note that the programming of registers should follow the order shown in item 7 in the section Programming Guidelines, not the bitfield selection order shown here. The bitfield selection order is:

- 0 pulses – QVO Coarse register
- 1 pulse – QVO Fine register
- 2 pulses – Sens. Coarse register
- 3 pulses – Sens. Fine register
- 4 pulses – TC Register register
- 5 pulses – Clamp Bit register
- 6 pulses – Polarity Bit register

This register wraps by default.

To enter the Register Selection state, send one  $V_{PH}$  pulse on the VOUT pin.

#### BITFIELD SELECTION STATE (Write Mode)

This state allows the selection of the individual bitfields to be programmed, in the register selected in the Register Selection state.

In Try Value mode, the total value of the bitfields selected increments by 1 with each  $V_{PL}$  pulse on the VOUT pin. The parameter being programmed changes with each additional pulse, so measurements can be taken after each pulse to determine if the desired result has been acquired.

In Blow Fuses mode, each bitfield to be blown must be selected individually.

For bit codes and wrapping for these registers, see the section Programming Logic.

To leave this state, send one  $V_{PH}$  pulse on the VOUT pin. If the current mode is Try Value, the bitfields remain set and the device reverts to the Mode Selection state. If the current mode is Blow Fuse, the selected bitfield fuse is blown, and the device reverts to the Mode Selection state.

# A1373 and A1374

High Precision, Output Pin Programmable, Linear Hall Effect Sensors

## Programming Logic

Binary Bitfield Address	Decimal Equivalent Code	Description
QVO Coarse register		
00	0	$V_{OUT(Q)}$ mid range
01	1	$V_{OUT(Q)}$ low range
10	2	$V_{OUT(Q)}$ high range
11	3	Register wraps to 00
QVO Fine register		
00000000	0	Initial value in selected QVO Coarse range
11111111	511	Maximum value in selected QVO Coarse range
Sens. Coarse register		
00	0	Sens low range
01	1	Sens mid range
10	2	Sens high range
11	3	Register wraps to 00
Sens. Fine register		
00000000	0	Initial value in selected Sens. Coarse range
11111111	255	Maximum value in selected Sens. Coarse range
TC Register register (See also chart Sensitivity Temperature Coefficient Code Profile in Typical Characteristics section)		
00000	0	initial TC
00001 through 01011	1 through 11	Positive TC programming range
01100 through 01111	12 through 15	Unused: equal to codes 4 to 7, respectively
10000 through 11011	16 through 27	Negative TC programming range; Value for 16 equals 1 step less than the value for the Initial TC Value (00000)
11100 through 11111	28 through 31	Unused: equal to codes 20 to 23, respectively
Clamp Bit register		
00	0	Rail-to-rail output swing
01	1	0.5 V and $V_{CC} - 0.5V$ rails
10	2	1 V and $V_{CC} - 1 V$ rails
00	3	Register wraps to 00
Polarity Bit register		
0	0	Positive ( $V_{OUT}$ increases when a positive (south) magnetic field is applied to the device )
1	1	Negative ( $V_{OUT}$ increases when a negative (north) magnetic field is applied to the device )

# A1373 and A1374

## High Precision, Output Pin Programmable, Linear Hall Effect Sensors

### Programming Guidelines

- A bypass capacitor rated at 0.1 $\mu$ F must be mounted between the VOUT pin and the GND pin during programming. The power supply used for programming should be capable of delivering 28 V and 300 mA.

- Before beginning any Blow Fuse mode or Lock Device mode code sequence, the device MUST be reset by cycling V<sub>CC</sub> power-off and power-on again. Cycling power resets the device by setting all bitfields that have intact fuses to 0. Bitfields with blown fuses are unaffected.

In Try Value mode, to retain register settings from previous code sequences, do not cycle power between sequences.

When a register is selected in Register Selection mode, when the V<sub>PH</sub> pulse is sent to enter the Bitfield Selection mode, the bitfields with intact fuses in that register are reset to 0.

- In Try Value mode, all bits in the register can be set in one code sequence. For example, setting the binary value 0110 and sending a V<sub>PH</sub> pulse sets code 6. However, because of the power requirement, blowing fuses must be performed one bitfield at a time. In order to program (blow fuses) for binary 0110, the bitfields MUST be programmed (blown) in two different code sequences: one setting the 0100 bit, and the other setting the 0010 bit (in either order). Power must be cycled before each of the two sequences.

- Although a bitfield cannot be reset once its fuse is blown, additional bitfields can be blown at any time, until the device is locked by setting the Lock bit. For example, if bit 1 (0010) has been blown, it is possible to blow bit 0 (0001). Because bit 1 was

already blown, the end result will be 0011 (code 3).

- Before powering down the device after programming, observe the recommended delay, to ensure that the last V<sub>PH</sub> pulse has decayed before voltage drops to the V<sub>PL</sub> voltage. This will avoid the generation of overlapping V<sub>PL</sub> and V<sub>PH</sub> pulses. At the end of a Lock Device mode code sequence, the delay is not necessary.

- Programming order is important in both Try Value mode and in Blow Fuse mode. There will be a slight parametric shift in sensitivity after programming the temperature coefficient, and a slight quiescent voltage shift with polarity. Subsequent changes to sensitivity can cause a shift in the quiescent output voltage.

The following order is recommended:

- a. Polarity
- b. TC Register
- c. Sens Coarse
- d. QVO Coarse
- e. Sens Fine
- g. QVO Fine

The Clamp Bit register can be programmed at any point in the order, as no parametric shift is observed due to clamps.

- The actual distribution of parametric programming ranges are wider than the specified programming ranges, in order to take into account manufacturing spread. The maximum possible attainable range can be used with the understanding that other specified parameters might be out of datasheet specification in the extended range. (For an example, see the chart Sensitivity Temperature Coefficient Range, in the Typical Characteristics section.)

# A1373 and A1374

## High Precision, Output Pin Programmable, Linear Hall Effect Sensors

### Programming Example

This example demonstrates the programming of the devices by setting the register for Sensitivity Temperature Coefficient to 00110.

1. Power-on the system. This will reset the unprogrammed bits in all registers to 0. The device enters the Initial state.
2. Send one  $V_{PH}$  pulse to enter the Mode Selection state.
3. Send one  $V_{PL}$  pulse to select Try Value mode.
4. Send one  $V_{PH}$  pulse to enter the Register Selection state.
5. Send four  $V_{PL}$  pulses to select the TC register.
6. Send one  $V_{PH}$  pulse to enter Bitfield Selection state (Write mode). The TC register is reset to 00000 (assuming all of those bitfields have intact fuses).
7. Send five  $V_{PL}$  pulses to set bitfields 0 and 2 (00101).

Now we can measure the device output to see if this is the desired value. We may find that the value we programmed is not correct. So we will proceed to change it, as follows:

8. Send one  $V_{PL}$  pulse to increase the code to 6 (setting bitfields 1 and 2: 00110).

We measure the device and find that this is the correct TC we require. We are finished with trying values, and now want to set the value permanently. In the following steps, remember that blowing fuses is done one bit at a time.

9. Send one  $V_{PH}$  pulse to exit Bitfield Selection mode. (The device returns to the Mode Selection state.)
10. RESET the device by powering it off and on.
11. Send one  $V_{PH}$  pulse to enter the Mode Selection state.
12. Send two  $V_{PL}$  pulses to select Blow Fuse mode.

13. Send one  $V_{PH}$  pulse to enter the Register Selection state.
14. Send four  $V_{PL}$  pulses to select the TC register.
15. Send one  $V_{PH}$  pulse to enter Bitfield Selection state (Write Mode). The TC register is reset to 00000.
16. Send four  $V_{PL}$  pulses to set bit 2 (00100, decimal 4).
17. Send one  $V_{PH}$  pulse to exit Bitfield Selection state. The bitfield fuse is blown, and the device returns to the Mode Selection state.

One of the two bitfields is programmed. Now we program the other bitfield.

18. Repeat steps 10 to 15 to select the TC register again. This time, however, the register resets to 00100, because bit 2 has been permanently set.
19. Send two  $V_{PL}$  pulses to set bit 1 (00010, decimal 2).
20. Send one  $V_{PH}$  pulse to exit Bitfield Selection state. The bitfield fuse is blown, and the device returns to the Mode Selection state.

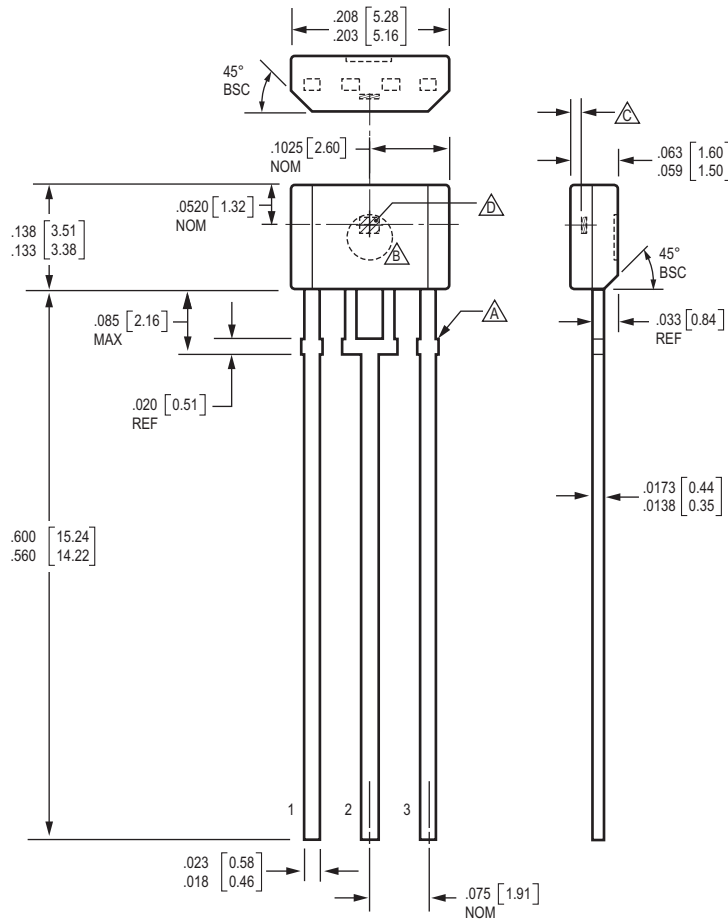
After repeating the above steps to program all parameters, we can lock the device:

21. RESET the device by powering it off and on.
22. Send one  $V_{PH}$  pulse to enter the Mode Selection state.
23. Send three  $V_{PL}$  pulses to select Lock Device mode.
24. Send one  $V_{PH}$  pulse to enter the Bitfield Selection state. (We do not need to select a register for locking the device).
25. Send one  $V_{PL}$  pulse to set the Lock bit to 1.
26. Send one  $V_{PH}$  pulse to exit Bitfield Selection state. The bitfield fuse is blown, and the device returns to the Mode Selection state.
27. Programming the device is complete. Optionally, test the results, or power-off the device.





# A1373 and A1374

High Precision, Output Pin Programmable, Linear Hall Effect Sensors

## Package KB, 3-Pin SIP



Dimensions in inches  
 Millimeters in brackets, for reference only  
 Dimensions exclusive of mold flash, gate burrs, or dambar protrusions  
 Exact case and lead configuration at supplier discretion within limits shown

-  Dambar removal protrusion (6X)
-  Ejector mark on opposite side
-  Active Area Depth .0165 [0.42] NOM
-  Hall element (not to scale)

# A1373 and A1374

High Precision, Output Pin Programmable, Linear Hall Effect Sensors

*The products described herein are manufactured under one or more of the following U.S. patents: 5,045,920; 5,264,783; 5,442,283; 5,389,889; 5,581,179; 5,517,112; 5,619,137; 5,621,319; 5,650,719; 5,686,894; 5,694,038; 5,729,130; 5,917,320; and other patents pending.*

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