

ACT-S512K8 High Speed 4 Megabit Monolithic SRAM

Features

- Low Power Monolithic CMOS 512K x 8 SRAM
- Full Military (-55°C to +125°C) Temperature Range
- Input and Output TTL Compatible Design
- Fast 17,20,25,35,45 & 55ns Maximum Access Times
- +5 V Power Supply
- MIL-PRF-38534 Compliant MCMs Available
- Industry Standard Pinouts
- Packaging – Hermetic Ceramic
 - 36 Lead, .92" x .51" x .13" Flat Package (FP), Aeroflex code# "F3"
 - 36 Lead, .92" x .43" x .184" Small Outline J lead (CSOJ), Aeroflex code# "F4"
 - (.155 MAX thickness available, contact factory for details)
 - 32 Lead, 1.6" x .60" x .20" Dual-in-line (DIP), Aeroflex code# "P4"
- DESC SMD# 5962-95613 Released(F3,F4,P4)



General Description

The ACT-S512K8 is a high speed, 4 Megabit CMOS Monolithic SRAM designed for full temperature range military, space, or high reliability mass memory and fast cache applications.

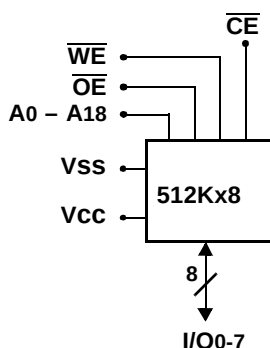
The MCM is input and output TTL compatible. Writing is executed when the write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are low and output enable ($\overline{OE}$) is high. Reading is accomplished when $\overline{WE}$ is high and $\overline{CE}$ and $\overline{OE}$ are both low. Access time grades of 17ns, 20ns, 25ns, 35ns, 45ns and 55ns maximum are standard.

The +5 Volt power supply version is standard and +3.3 Volt lower power model is a future optional product.

The products are designed for operation over the temperature range of -55°C to +125°C and under the full military environment. A DESC Standard Military Drawing (SMD) number is released.

The ACT-S512K8 is manufactured in Aeroflex's 80,000 square foot MIL-PRF-38534 certified facility in Plainview, N.Y.

Block Diagram – Flat Package(F3,F16), DIP(P4) & CSOJ(F4)



Pin Description

I/O0-7	Data I/O
A0-18	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
Vcc	Power Supply
Vss	Ground
NC	Not Connected

Absolute Maximum Ratings

Symbol	Parameter	MINIMUM	MAXIMUM	Units
T_C	Case Operating Temp.	-55	+125	°C
T_{STG}	Storage Temperature	-65	+150	°C
P_D	Maximum Package Power Dissipation	-	1.1	W
V_G	Maximum Signal Voltage to Ground	-0.5	$V_{CC} + 0.5$	V
V_{CC}	Power Supply Voltage	-0.5	+7.0	V
T_J	Junction Temperature	-	+150	°C

Recommended Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units
V_{CC}	Power Supply Voltage	+4.5	+5.5	V
V_{IH}	Input High Voltage	+2.2	$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage	-0.5	+0.8	V
T_A	Operating Temp. (Mil)	-55	+125	°C

Truth Table

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Data I/O	Power
Standby	H	X	X	High Z	Standby (deselect/power down)
Read	L	L	H	Data OUT	Active
Output Disable	L	H	H	High Z	Active (deselected)
Write	L	X	L	Data IN	Active

Capacitance

($V_{IN} = 0V$, $f = 1MHz$, $T_c = 25^\circ C$, unless otherwise noted, Guaranteed but not tested)

Symbol	Parameter	Maximum	Units
C_{IN}	Input Capacitance (A_{0-18} , $\overline{WE}$ & $\overline{OE}$)	20	pF
C_{OUT}	Output Capacitance (I/O_{0-7} & $\overline{CE}$)	20	pF

DC Characteristics

($V_{CC} = 5.0V$, $V_{SS} = 0V$, $T_c = -55^\circ C$ to $+125^\circ C$, unless otherwise specified)

Parameter	Sym	Conditions	ALL SPEEDS		Units
			Min	Max	
Input Leakage Current	I_{LI}	$V_{CC} = \text{Max}$, $V_{IN} = 0$ to V_{CC}	-10	+10	μA
Output Leakage Current	I_{LO}	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IH}$, $V_{OUT} = 0$ to V_{CC}	-10	+10	μA
Operating Supply Current	I_{CC}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$, $V_{CC}=5.5V$, $f=5MHz$ CMOS Compatible	-	170	mA
Standby Current	I_{SB}	$\overline{CE} = V_{CC}$, $\overline{OE} = V_{IH}$, $V_{CC}=5.5V$, $f=5MHz$ CMOS Compatible	-	20	mA
Output Low Voltage	V_{OL}	$I_{OL} = 8$ mA, $V_{CC} = 4.5V$	-	0.4	V
Output High Voltage	V_{OH}	$I_{OH} = -4$ mA, $V_{CC} = 4.5V$	2.4	-	V

AC Characteristics

(V_{CC} = 5.0V, V_{SS} = 0V, T_c = -55°C to +125°C)

Read Cycle

Parameter	Sym	-017		-020		-025		-035		-045		-055		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	17	-	20	-	25	-	35	-	45	-	55	-	ns
Address Access Time	t _{AA}	-	17	-	20	-	25	-	35	-	45	-	55	ns
Chip Select Access Time	t _{ACS}	-	17	-	20	-	25	-	35	-	45	-	55	ns
Output Hold from Address Change	t _{OH}	0	-	0	-	0	-	0	-	0	-	0	-	ns
Output Enable to Output Valid	t _{OE}	-	9	-	10	-	12	-	25	-	25	-	25	ns
Chip Select to Output in Low Z (1)	t _{CLZ}	2	-	2	-	2	-	4	-	4	-	4	-	ns
Output Enable to Output in Low Z (1)	t _{OLZ}	0	-	0	-	0	-	0	-	0	-	0	-	ns
Chip Deselect to Output in High Z (1)	t _{CHZ}	-	9	-	10	-	12	-	15	-	20	-	20	ns
Output Disable to Output in High Z (1)	t _{OHZ}	-	9	-	10	-	12	-	15	-	20	-	20	ns

Note 1. Guaranteed by design, but not tested

Write Cycle

Parameter	Sym	-017		-020		-025		-035		-045		-055		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{WC}	17	-	20	-	25	-	35	-	45	-	55	-	ns
Chip Select to End of Write	t _{CW}	15	-	15	-	20	-	25	-	35	-	50	-	ns
Address Valid to End of Write	t _{AW}	15	-	15	-	20	-	25	-	35	-	50	-	ns
Data Valid to End of Write	t _{DW}	12	-	12	-	15	-	20	-	25	-	25	-	ns
Write Pulse Width	t _{WP}	14	-	14	-	15	-	25	-	35	-	40	-	ns
Address Setup Time	t _{AS}	2	-	2	-	2	-	2	-	2	-	2	-	ns
Address Hold Time	t _{AH}	0	-	0	-	0	-	0	-	5	-	5	-	ns
Output Active from End of Write (1)	t _{OW}	0	-	0	-	0	-	0	-	5	-	5	-	ns
Write to Output in High Z (1)	t _{WHZ}	-	9	-	9	-	10	-	15	-	20	-	25	ns
Data Hold from Write Time	t _{DH}	0	-	0	-	0	-	0	-	0	-	0	-	ns

Note 1. Guaranteed by design, but not tested

Data Retention Electrical Characteristics (Special Order Only)

(T_c = -55°C to +125°C)

Parameter	Sym	Test Conditions	ALL SPEEDS			Units
			Min	Typ	Max	
V _{CC} for Data Retention	V _{DR}	$\overline{CE} \geq V_{CC} - 0.2V$	2	-	5.5	V
Data Retention Current (1)	I _{CCDR1}	V _{CC} = 3V	-	0.5	7.0	mA

Available in Low Power version. Call For Information.

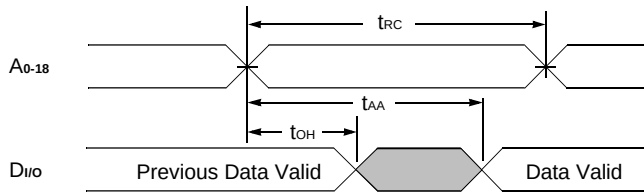
Truth Table

Mode	CE	OE	WE	Data I/O	Power
Standby	H	X	X	High Z	Standby (deselect/power down)
Read	L	L	H	Data Out	Active
Output Disable	L	H	H	High Z	Active (deselected)
Write	L	X	L	Data In	Active

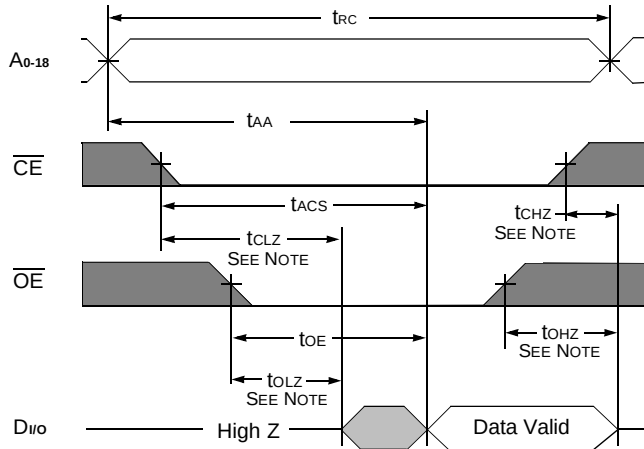
Timing Diagrams

Read Cycle Timing Diagrams

Read Cycle 1 ($\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$)



Read Cycle 2 ($\overline{WE} = V_{IH}$)

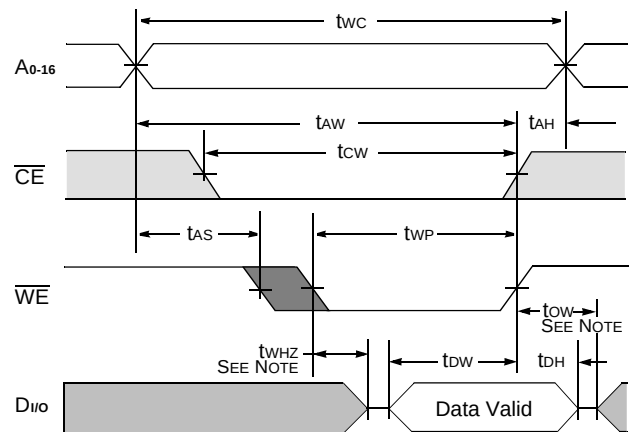


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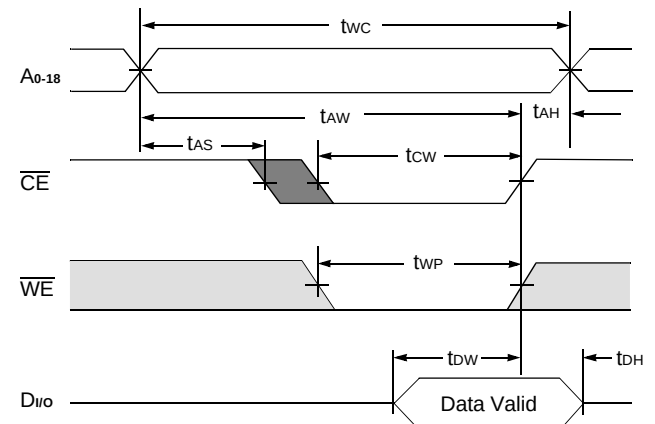
DON'T CARE

Write Cycle Timing Diagrams

Write Cycle 1 ($\overline{WE}$ Controlled, $\overline{OE} = V_{IL}$)

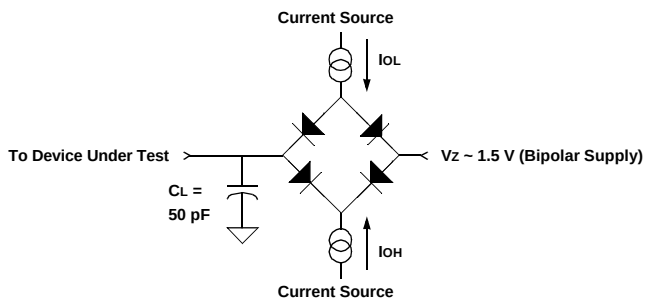


Write Cycle 2 ($\overline{CE}$ Controlled, $\overline{OE} = V_{IH}$)



Note: Guaranteed by design, but not tested.

AC Test Circuit



Parameter	Typical	Units
Input Pulse Level	0 – 3.0	V
Input Rise and Fall	5	ns
Input and Output Timing Reference Level	1.5	V

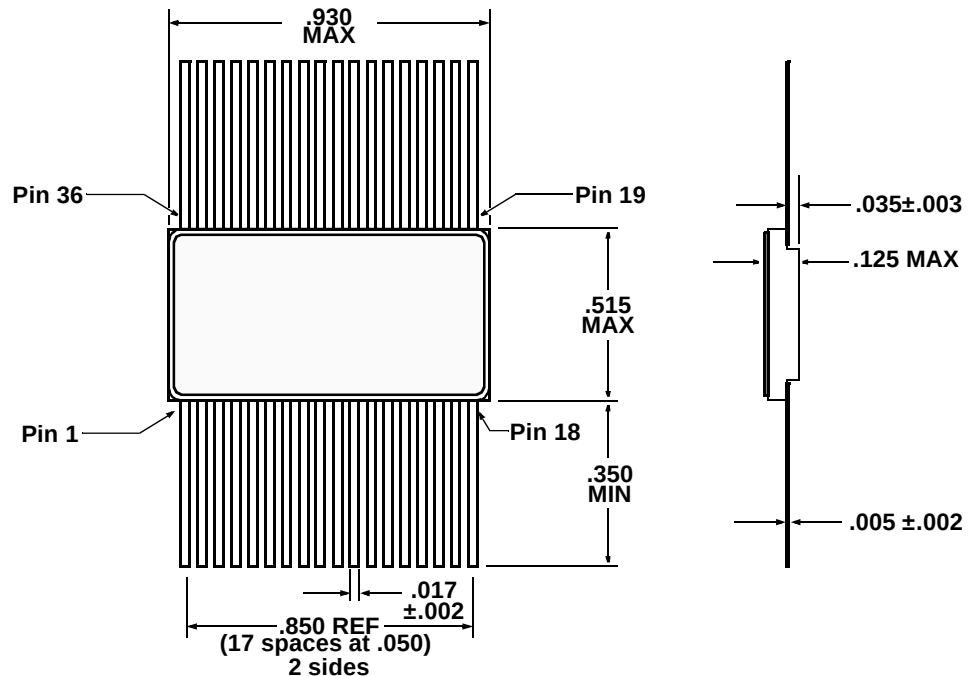
Notes:

- 1) V_Z is programmable from -2V to +7V.
- 2) I_{OL} and I_{OH} programmable from 0 to 16 mA.
- 3) Tester Impedance $Z_O = 75\Omega$.
- 4) V_Z is typically the midpoint of V_{OH} and V_{OL} .
- 5) I_{OL} and I_{OH} are adjusted to simulate a typical resistance load circuit.
- 6) ATE Tester includes jig capacitance.

Pin Numbers & Functions

36 Pins — Flat Package			
Pin #	Function	Pin #	Function
1	A ₀	19	NC
2	A ₁	20	A ₁₀
3	A ₂	21	A ₁₁
4	A ₃	22	A ₁₂
5	A ₄	23	A ₁₃
6	$\overline{\text{CE}}$	24	A ₁₄
7	I/O ₀	25	I/O ₄
8	I/O ₁	26	I/O ₅
9	V _{CC}	27	V _{CC}
10	V _{SS}	28	V _{SS}
11	I/O ₂	29	I/O ₆
12	I/O ₃	30	I/O ₇
13	$\overline{\text{WE}}$	31	$\overline{\text{OE}}$
14	A ₅	32	A ₁₅
15	A ₆	33	A ₁₆
16	A ₇	34	A ₁₇
17	A ₈	35	A ₁₈
18	A ₉	36	NC

Package Outline "F3" — Small Flat Package, 36 Leads

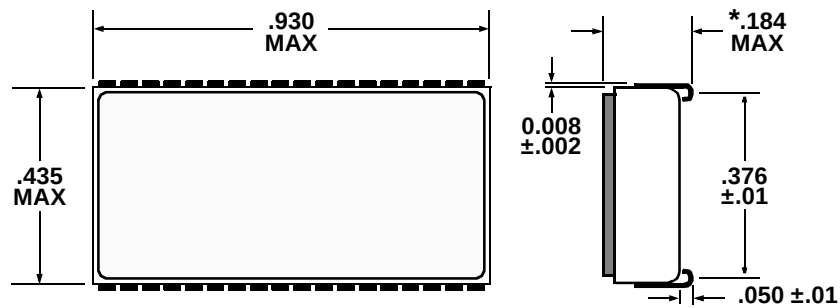


All dimensions in inches

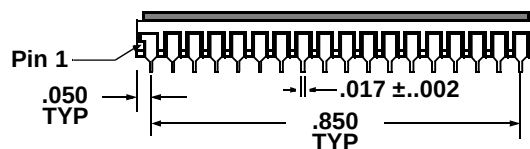
Pin Numbers & Functions

36 Pins — CSOJ			
1	A0	19	NC
2	A1	20	A10
3	A2	21	A11
4	A3	22	A12
5	A4	23	A13
6	$\overline{CE}$	24	A14
7	I/O0	25	I/O4
8	I/O1	26	I/O5
9	V _{CC}	27	V _{CC}
10	V _{SS}	28	V _{SS}
11	I/O2	29	I/O6
12	I/O3	30	I/O7
13	$\overline{WE}$	31	$\overline{OE}$
14	A5	32	A15
15	A6	33	A16
16	A7	34	A17
17	A8	35	A18
18	A9	36	NC

Package Outline "F4" — .435" x .920" CSOJ, 36 Pins



All dimensions in inches

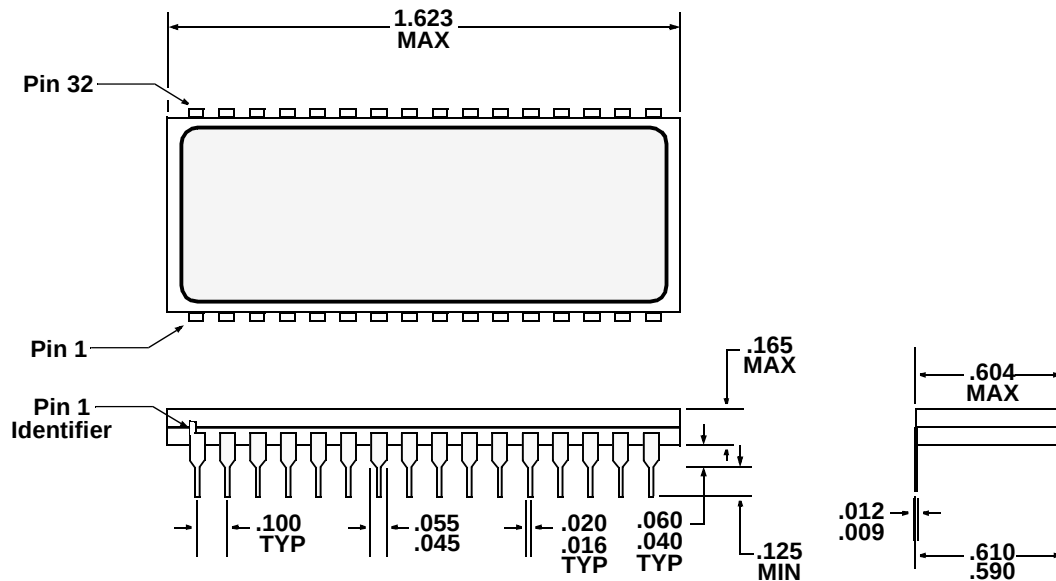


*.155 MAX thickness available, contact factory for details

Pin Numbers & Functions

32 Pins — DIP			
1	A18	17	I/O3
2	A16	18	I/O4
3	A14	19	I/O5
4	A12	20	I/O6
5	A7	21	I/O7
6	A6	22	$\overline{CE}$
7	A5	23	A10
8	A4	24	$\overline{OE}$
9	A3	25	A11
10	A2	26	A9
11	A1	27	A8
12	A0	28	A13
13	I/O0	29	$\overline{WE}$
14	I/O1	30	A17
15	I/O2	31	A15
16	V _{SS}	32	V _{CC}

Package Outline "P4" — .590" x 1.67" DIP Package, 32 Leads



All dimensions in inches

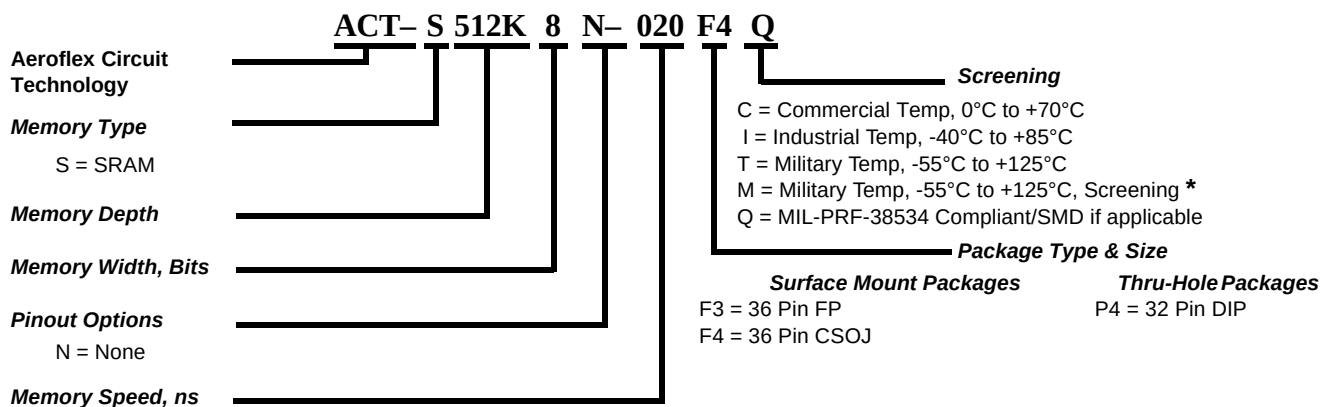


Ordering Information

Model Number	DESC Part Number	Speed	Package
ACT-S512K8N-017F3Q	5962-9561310HUC	17ns	36 Lead Flat
ACT-S512K8N-020F3Q	5962-9561309HUC	20ns	36 Lead Flat
ACT-S512K8N-025F3Q	5962-9561308HUC	25ns	36 Lead Flat
ACT-S512K8N-035F3Q	5962-9561307HUC	35ns	36 Lead Flat
ACT-S512K8N-045F3Q	5962-9561306HUC	45ns	36 Lead Flat
ACT-S512K8N-055F3Q	5962-9561305HUC	55ns	36 Lead Flat
ACT-S512K8N-017P4Q	5962-9561310HYC	17ns	32 Pin DIP
ACT-S512K8N-020P4Q	5962-9561309HYC	20ns	32 Pin DIP
ACT-S512K8N-025P4Q	5962-9561308HYC	25ns	32 Pin DIP
ACT-S512K8N-035P4Q	5962-9561307HYC	35ns	32 Pin DIP
ACT-S512K8N-045P4Q	5962-9561306HYC	45ns	32 Pin DIP
ACT-S512K8N-055P4Q	5962-9561305HYC	55ns	32 Pin DIP
ACT-S512K8N-017F4Q	5962-9561310HZC	17ns	36 Lead CSOJ
ACT-S512K8N-020F4Q	5962-9561309HZC	20ns	36 Lead CSOJ
ACT-S512K8N-025F4Q	5962-9561308HZC	25ns	36 Lead CSOJ
ACT-S512K8N-035F4Q	5962-9561307HZC	35ns	36 Lead CSOJ
ACT-S512K8N-045F4Q	5962-9561306HZC	45ns	36 Lead CSOJ
ACT-S512K8N-055F4Q	5962-9561305HZC	55ns	36 Lead CSOJ

* Pending

Model Number Breakdown



Specification subject to change without notice

* Screened to the individual test methods of MIL-STD-883

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