



ProASIC™ 500K Family

Features and Benefits

High Capacity

- 98,000 to 1.1 Million System Gates
- 14k to 138k Bits of Two-Port SRAM
- 210 to 623 User I/Os

Performance

- 33 MHz PCI 32-Bit
- Internal System Performance up to 250 MHz
- External System Performance up to 100 MHz

Low Power

- Low Impedance Flash Switches
- Segmented Hierarchical Routing Structure
- Small Efficient Logic Cells

High Performance Routing Hierarchy

- Ultra Fast Local Network
- Efficient Long Line Network
- High Speed Bus Network
- High Performance Global Network

Nonvolatile and Reprogrammable Flash Technology

- Live at Power-Up
- No Configuration Boot Device Required
- Retains Programmed Design During Power-Down/Power-Up Cycles

I/O

- Mixed 2.5/3.3 Volt Support
- 3.3V, 33 MHz PCI Compliance (PCI Revision 2.2)
- Individually Selectable 2.5V or 3.3V I/Os and Slew Rate (25, 50, and 100 mA/nsec)

Secure Programming

- Security Bit Prevents Read Back of Programming Bit Stream

Standard FPGA and ASIC Design Flow

- Flexibility to Choose Vendor-Specific Front-End Tools
- Provide Efficient Design Through Front-End Timing and Gate Optimization

ISP Support

- In-System Programming (ISP) with Silicon Sculptor and Silicon Explorer II

Embedded Memory Netlist Generator for SRAMs and FIFOs

- Ensures Optimal Usage of Embedded Memory Blocks
- Up to 133 MHz Synchronous and Asynchronous Operation

JTAG Support

- IEEE Std. 1149.1 (JTAG) Compliant

Individual ProASIC Device ID

- Control and Restrict IP Delivery to Individual ProASIC Device

ProASIC Product Profile

Device	A500K050	A500K130	A500K180	A500K270	A500K350	A500K440	A500K510
Maximum System Gates	98,000	287,000	369,000	473,000	638,000	956,000	1,100,000
Typical Gates	43,000	105,000	150,000	215,000	280,000	350,000	410,000
Maximum Flip-Flops	5,376	12,800	18,432	26,880	34,816	43,776	51,200
Embedded RAM Bits	14k	46k	55k	65k	74k	124k	138k
Embedded RAM Blocks (256 X 9)	6	20	24	28	32	54	60
Logic Tiles	5,376	12,800	18,432	26,880	34,816	43,776	51,200
Global Clocks	4	4	4	4	4	4	4
Maximum User I/Os	210	312	368	446	496	570	623
JTAG	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PCI	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Package (by Pin Count)							
PQFP	208	208	208	208			
PBGA	272	272, 456	456	456			
FBGA			580	580	580	580	580

General Description

The ProASIC 500K family combines the advantages of ASICs with the benefits of programmable devices through its nonvolatile Flash technology. ProASIC 500K devices make it possible to create high-density systems using existing ASIC or FPGA design flows and tools, shortening time-to-production. ASIC migration is not necessary for any volume because the family offers cost effective reprogrammable solutions, ideal for applications in the networking, telecom, computer, and consumer markets.

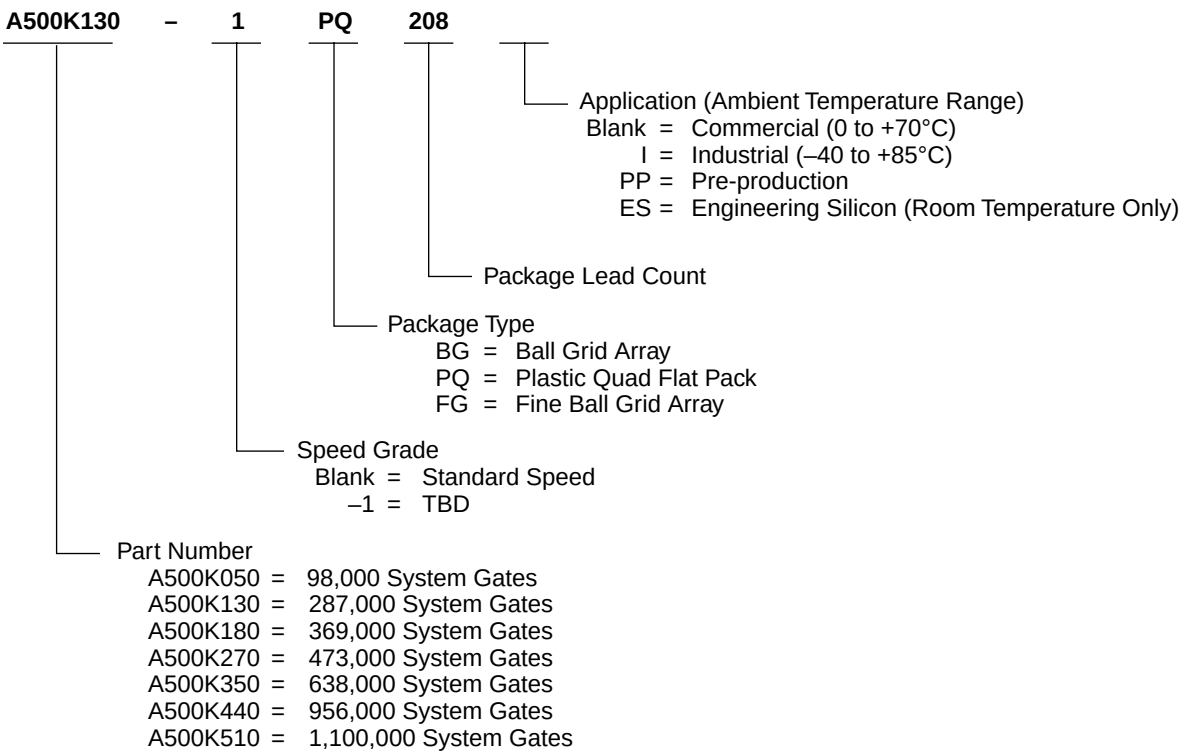
The ProASIC 500K family offers seven devices with 98k to 1.1M system gates and includes up to 138k bits of embedded

two-port memory. These memory blocks include hardwired FIFO circuitry as well as circuits to generate or check parity. This minimizes external logic gate count and complexity while maximizing flexibility and utility.

Process Technology

The ProASIC 500K family achieves its non-volatility and reprogrammability through an advanced 4LM Flash-based 0.25µ channel length LVCMOS technology process. Standard CMOS design techniques are used to implement logic and control functions resulting in highly predictable performance and gate array compatibility.

Ordering Information



	Speed Grade		Application	
	Std	–1*	C	I
A500K050 Device				
208-Pin Plastic Quad Flat Pack (PQFP)	✓	P	P	P
272-Pin Plastic Ball Grid Array (PBGA)	✓	P	P	P
A500K130 Device				
208-Pin Plastic Quad Flat Pack (PQFP)	✓	P	P	P
272-Pin Plastic Ball Grid Array (PBGA)	✓	P	P	P
456-Pin Plastic Ball Grid Array (PBGA)	✓	P	P	P
A500K180 Device				
208-Pin Plastic Quad Flat Pack (PQFP)	✓	P	P	P
456-Pin Plastic Ball Grid Array (PBGA)	✓	P	P	P
580-Pin Fine Ball Grid Array (FBGA)	P	P	P	P
A500K270 Device				
208-Pin Plastic Quad Flat Pack (PQFP)	✓	P	P	P
456-Pin Plastic Ball Grid Array (PBGA)	✓	P	P	P
580-Pin Fine Ball Grid Array (FBGA)	P	P	P	P
A500K350 Device				
580-Pin Fine Ball Grid Array (FBGA)	P	P	P	P
A500K440 Device				
580-Pin Fine Ball Grid Array (FBGA)	P	P	P	P
A500K510 Device				
580-Pin Fine Ball Grid Array (FBGA)	P	P	P	P

Applications: C = Commercial *Availability:* ✓ = Limited Availability. Contact your Actel Sales representative for the latest
I = Industrial availability information.

	User I/Os			
Device	PQFP 208-Pin	PBGA 272-Pin	PBGA 456-Pin	FBGA 580-Pin
A500K050	170	210	—	—
A500K130	170	210	312	—
A500K180	170	—	368	368
A500K270	170	—	368	446
A500K350	—	—	—	496
A500K440	—	—	—	496
A500K510	—	—	—	496

PQFP = Plastic Quad Flat Pack, PBGA = Plastic Ball Grid Array, FBGA = Fine Ball Grid Array

ProASIC 500K Architecture

The ProASIC 500K family utilizes a proprietary architecture that results in granularity comparable to gate arrays. Unlike SRAM-based FPGAs, ProASIC devices do not utilize look-up tables or architectural mapping during design. Instead, designs are directly synthesized to gates that streamline the design flow, increase design productivity, and eliminate dependencies on vendor-specific design tools.

The ProASIC 500K device core consists of a Sea-of-Tiles™ (Figure 1). Each tile (Figure 2) can be configured into a 3-input logic function (i.e. NAND gate, D-Flip-Flop, etc.) by programming the appropriate interconnect Flash switches, shown in Figure 3 on page 5. Gates and larger functions are connected together, utilizing the four levels of routing

hierarchy. Flash memory bits are distributed throughout each device providing non-volatile, reconfigurable interconnect programming. Flash switches are programmed to connect signal lines to the appropriate logic cell inputs and outputs. Dedicated high-performance lines are connected as needed for fast, low-skew clock distribution throughout the core. Maximum core utilization is possible for virtually any design.

The ProASIC 500K devices also contain embedded two-port SRAM blocks that have built in FIFO/RAM control logic. Programming options include synchronous or asynchronous operation, two-port RAM configurations, user defined depth and width, and parity generation or checking. Table 2 on page 9 lists the 24 basic memory configurations.

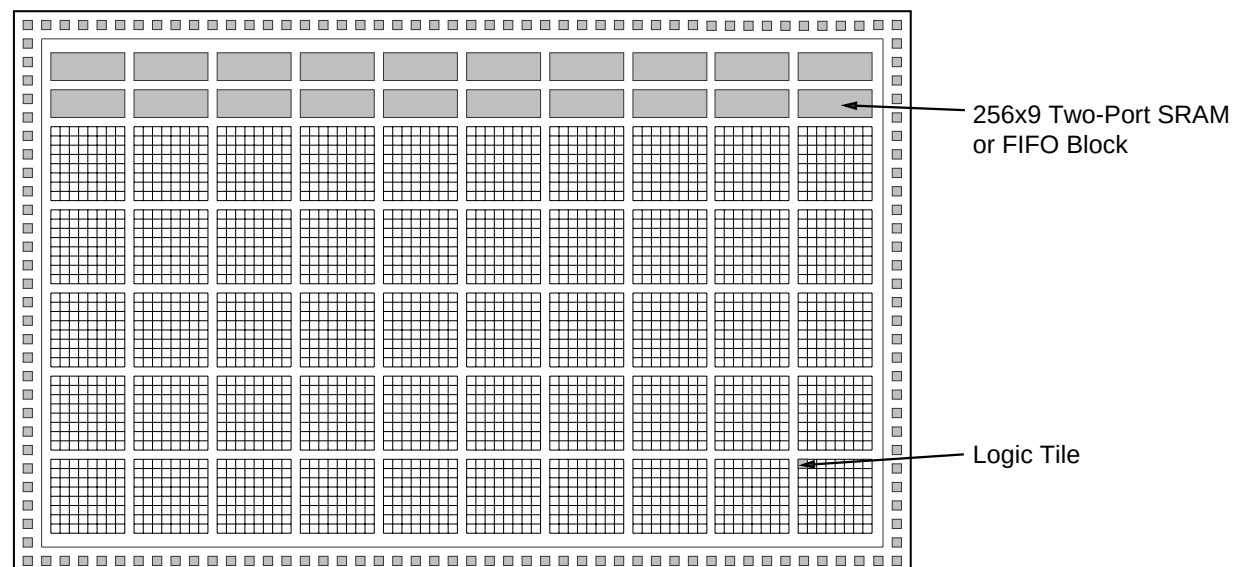


Figure 1 • The ProASIC Device Architecture

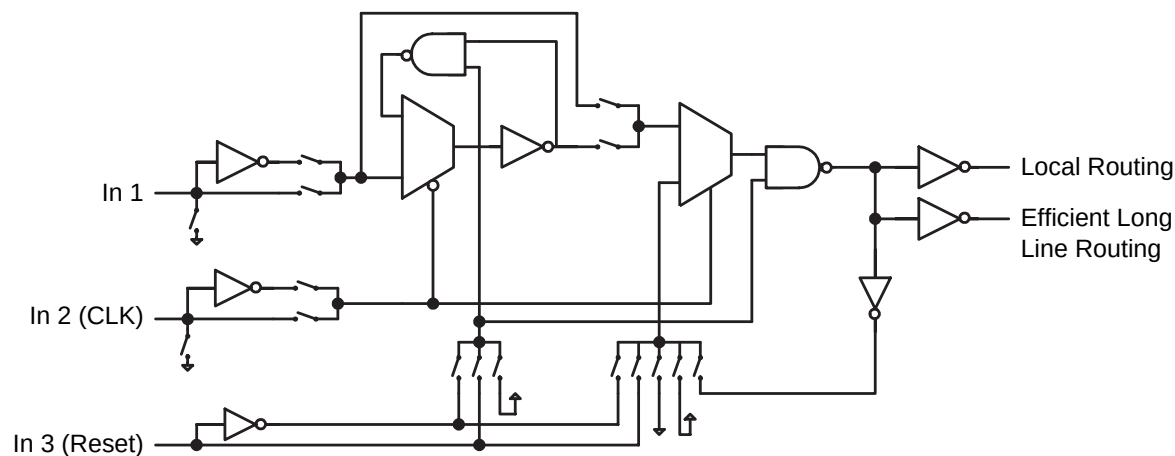


Figure 2 • Core Logic Tile

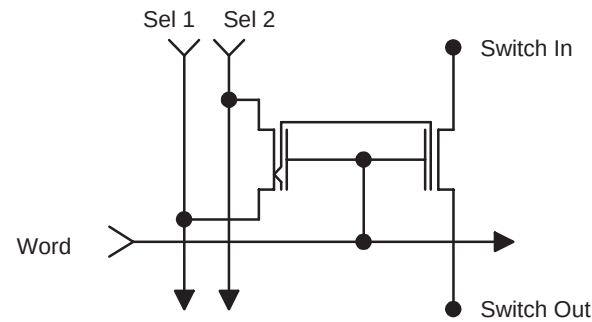


Figure 3 • Flash Switch

Routing Resources

The routing structure of the ProASIC 500K devices is designed to provide high performance through routing flexibility. It is composed of four levels of hierarchical resources: ultra fast local resources, efficient long line resources, high speed bus resources, and high performance global networks.

The ultra fast local resources are high speed dedicated lines that allow the output of each tile to directly connect to every input of the eight surrounding tiles (Figure 4).

The efficient long line resources provide routing for longer distance and higher fanout connections. These resources vary in length (spanning 1, 2, or 4 tiles), run both vertically and horizontally, and cover the entire ProASIC device (Figure 5 on page 6). Each tile can drive signals onto the efficient long line resources, and the resources can access every input of a tile. Active buffers are inserted automatically by the ASICmaster software to limit the effects of loading due to distance and fanout.

The high speed bus resources span across the entire device with minimal delay and are used to route very long or very high fanout nets. These resources run vertically and horizontally, and provide multiple access to each group of tiles throughout the device (Figure 6 on page 6).

The high performance global networks are low skew, high fanout nets that are accessible from four dedicated pins or from internal logic (Figure 7 on page 7). These nets are typically used to distribute clocks, resets, and other high fanout nets requiring a minimum skew. The global networks are implemented as clock trees, and signals can be introduced at any junction. These can be used hierarchically, with signals accessing every input on all tiles.

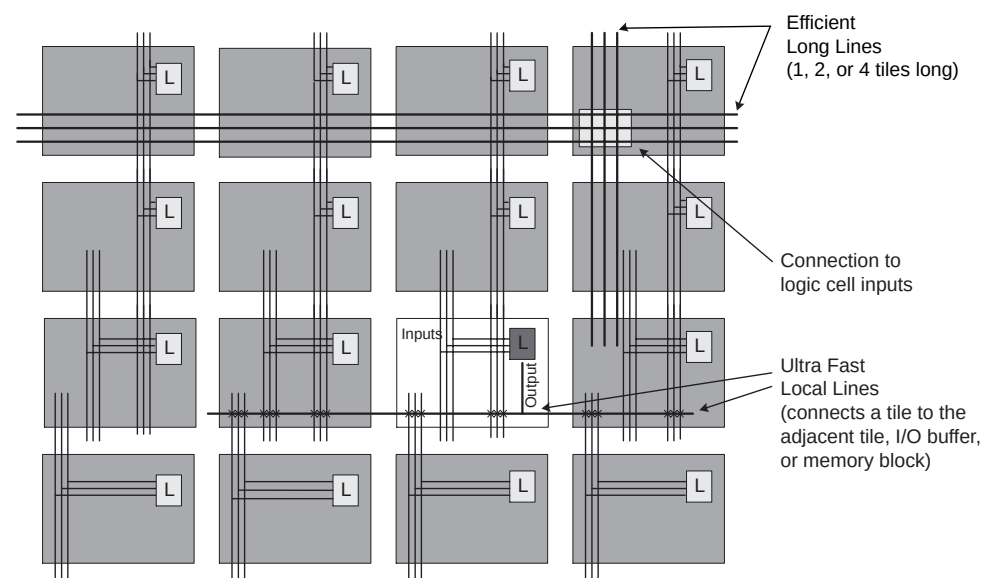


Figure 4 • Ultra Fast Local Resources

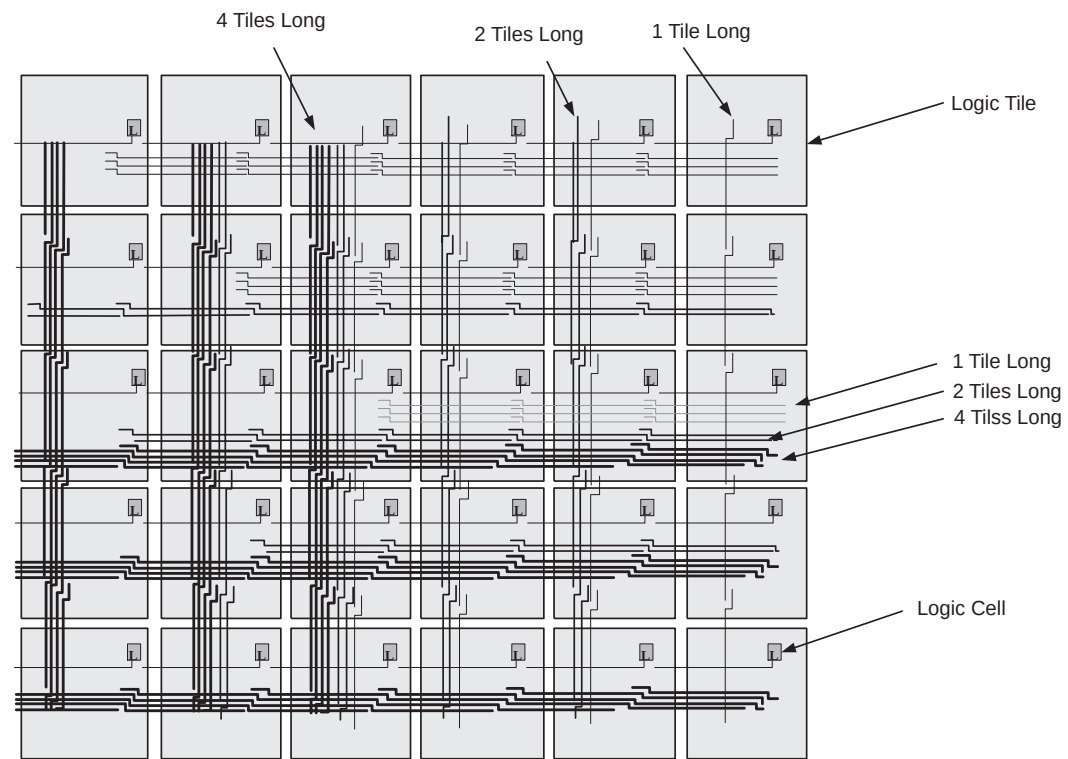


Figure 5 • Efficient Long Line Resources

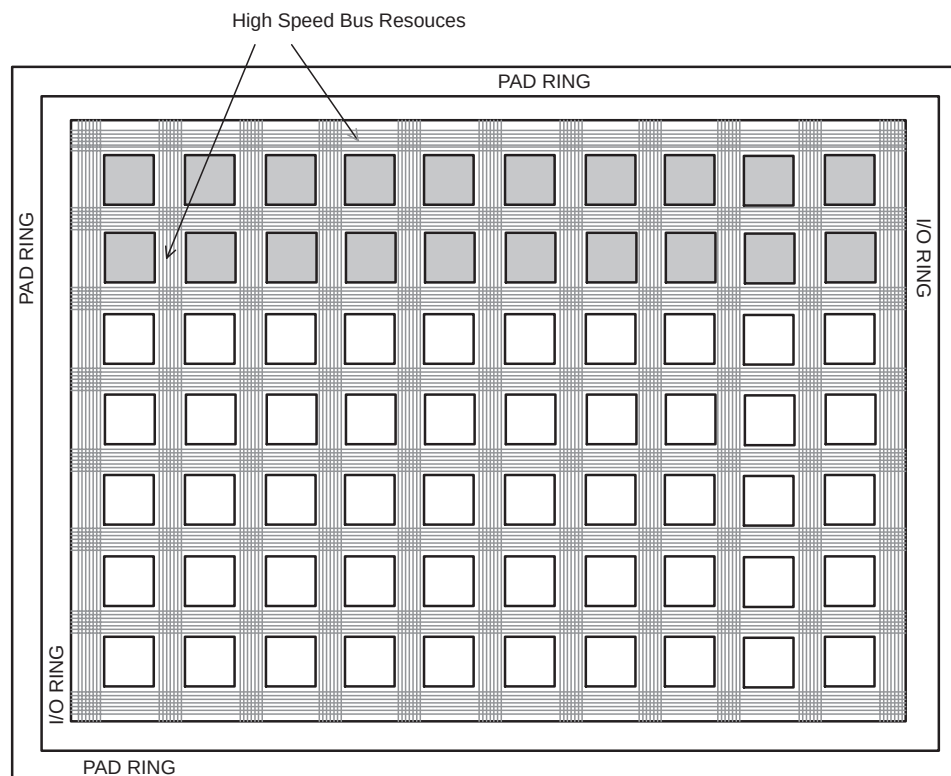


Figure 6 • High Speed Bus Resources

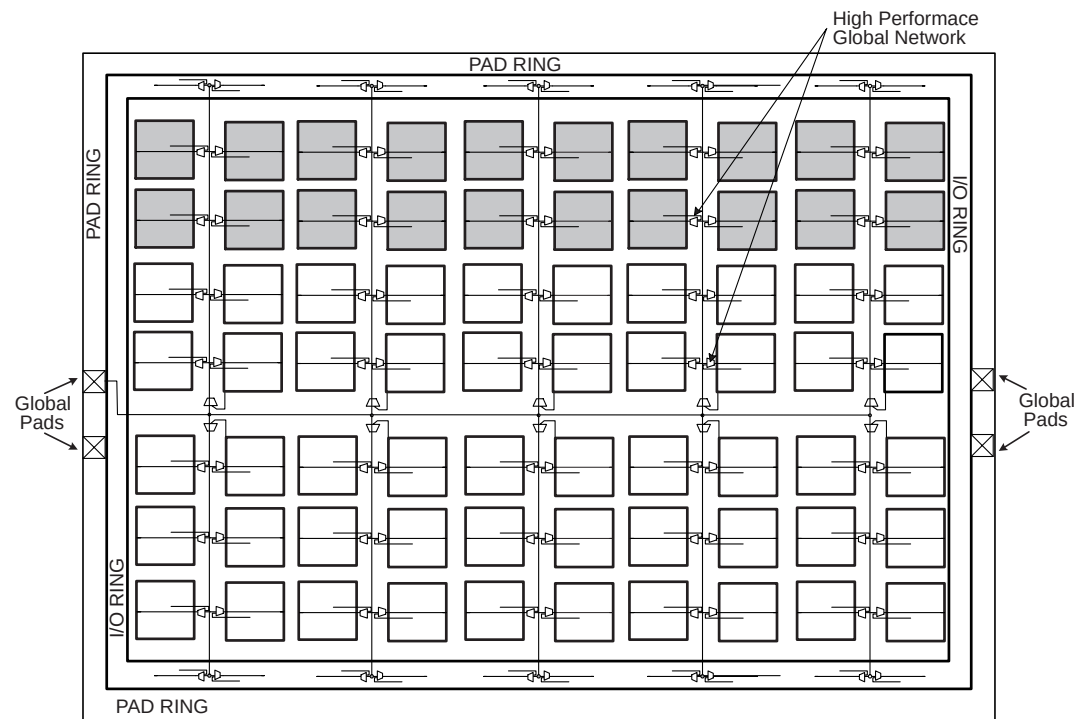


Figure 7 • High Performance Global Network

Input/Output Blocks

To meet the needs of complex system designs, the ProASIC 500K family offers devices with a large number of I/O pins, with the A500K510 device offering up to 623 user I/O pins. If the I/O pad is powered at 3.3V, each I/O can be selectively configured at 2.5V and 3.3V compliant threshold levels. Table 1 shows the various supply voltage configurations available in the ProASIC devices. Figure 8 illustrates I/O interfaces with other devices. All I/Os also include an ESD protection circuit. Each I/O is tested according to the following models:

Human Body Model (HBM)	1500V
(Per Mil Std 883 Method 3015)	
Machine Model	200V

Table 1 • ProASIC Power Supply Voltages

V_{DDP}	2.5V	3.3V
Input Tolerance	2.5V	3.3V, 2.5V
Output Drive	2.5V	3.3V, 2.5V

Note: V_{DDL} is always 2.5V.

The I/O pads are fully configurable to provide the maximum flexibility and speed. Each pad can be configured as an input, an output, a three-state driver, or a bi-directional buffer (Figure 9). I/O pads configured as inputs have the following features:

- Individually selectable 2.5V or 3.3V compliant threshold levels¹
- Optional pull-up resistor

I/O pads configured as outputs have the following features:

- Individually selectable 2.5V or 3.3V compliant output signals¹
- 3.3V PCI compliant
- Ability to drive LVTTL and LVCMOS levels
- Selectable drive strengths
- Selectable slew rates (25mA/s, 50mA/s, 100mA/s)
- Three-state enable

I/O pads configured as bi-directional buffers have the following features:

- Individually selectable 2.5V or 3.3V compliant output signals and threshold levels¹
- 3.3V PCI compliant
- Ability to drive LVTTL and LVCMOS levels
- Optional pull-up resistor

1. If $V_{DDP} = 2.5V$, pads are compliant to 2.5V level signals as defined by JEDEC JESD 8-5.

- Selectable drive strengths
- Selectable slew rates (25mA/s, 50mA/s, 100mA/s)
- Three-state enable

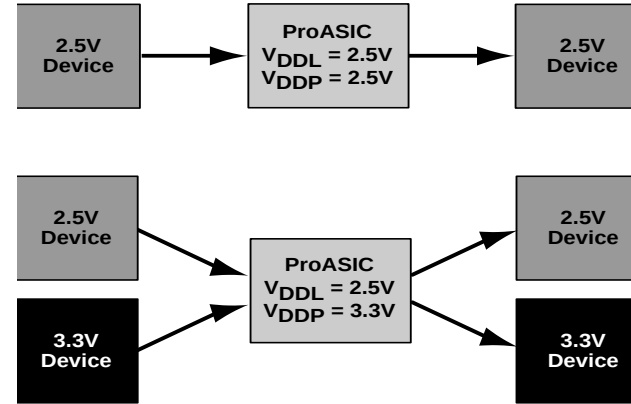


Figure 8 • I/O Interfaces

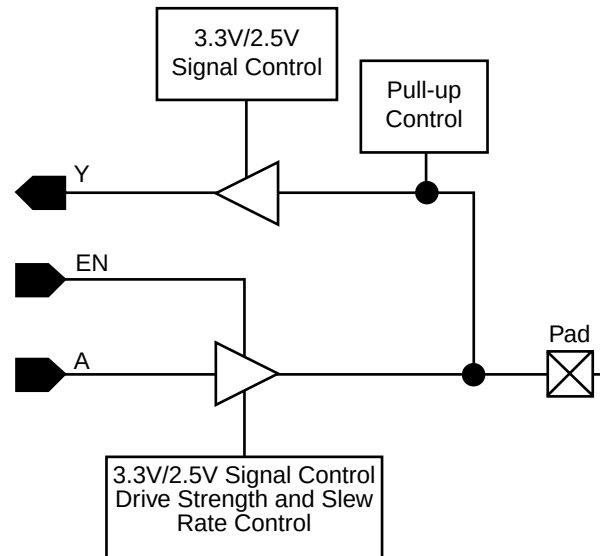


Figure 9 • I/O Block Schematic Representation

User Security and Traceability²

The ProASIC 500K devices have a read-protect bit that, once programmed, prevents the programmed contents from being read from the part. To clear the read-protect bit, the entire part must be erased. This capability lets you secure the programmed design and prevent it from being read back and duplicated. For traceability a 12-character alphanumeric user part number field allows the user to assign a user part ID, which can subsequently be read back by the programmer.

2. Available after completion of full qualification/characterization 2H, 2000.

Embedded Memory Floorplan

The embedded memory is located across the top of the device (see [Figure 1 on page 4](#)). Depending upon the device, 6 to 60 (256x9) blocks of memory are available to support a variety of possible memory configurations. Each block can be programmed as an independent memory or combined, using dedicated memory routing resources, to form larger and more complex memories.

Embedded Memory Configurations

The embedded memory in the ProASIC 500K family offers great flexibility in memory configuration. Whereas other programmable vendors typically provide single port memories that can be transformed into a two-port memory at the loss of half the memory, each ProASIC block is designed and optimized as a two-port memory (1r1w). This provides 138k total memory bits for two-port and single port memory usage in the A500K510 device.

Each memory can be configured as a FIFO or SRAM, with independent selection of synchronous or asynchronous read and write ports ([Table 2](#)). However, multiple write ports are not supported. Additional characteristics include programmable FIFO flags and selectable depth, and parity check and generation. [Figure 10](#) and [Figure 11 on page 10](#)

show the block diagram of the basic SRAM and FIFO blocks. These memories are designed to operate at up to 133 MHz when operated individually. Each block contains a 256 word deep by 9-bit wide (1r, 1w) memory. The memory blocks, shown in [Figure 12 on page 11](#), may be combined in parallel to form wider memories or stacked to form deeper memories. This provides optimal bit widths of 9 (1 block), 18, 36, and 72, and optimal depths of 256, 572, 768, and 1024. Refer to the *ProASIC Macro Library Guide* for more information.

[Figure 13 on page 11](#) shows an example of optimal memory usage. Three memories have been compiled with various widths and depths using 10 blocks and consuming all 23,040 bits. [Figure 14 on page 11](#) shows an example of doubling up memory to create extra read ports. In this example, 10 out of 60 blocks of the A500K510 are fully used, but yield an effective 6,912 bits of multiple port memories. The MEMORYmaster™ software facilitates an easy means of building wider and deeper memories for optimal memory usage.

Table 2 • Basic Memory Configurations

Type	Write Access	Read Access	Parity	Library Cell Name
RAM	Asynchronous	Asynchronous	Checked	RAM256x9AA
RAM	Asynchronous	Asynchronous	Generated	RAM256x9AAP
RAM	Asynchronous	Synchronous Transparent	Checked	RAM256xAST
RAM	Asynchronous	Synchronous Transparent	Generated	RAM256xASTP
RAM	Asynchronous	Synchronous Pipelined	Checked	RAM256x9ASR
RAM	Asynchronous	Synchronous Pipelined	Generated	RAM256x9ASRP
RAM	Synchronous	Asynchronous	Checked	RAM256x9SA
RAM	Synchronous	Asynchronous	Generated	RAM256xSAP
RAM	Synchronous	Synchronous Transparent	Checked	RAM256x9SST
RAM	Synchronous	Synchronous Transparent	Generated	RAM256x9SSTP
RAM	Synchronous	Synchronous Pipelined	Checked	RAM256x9SSR
RAM	Synchronous	Synchronous Pipelined	Generated	RAM256x9SSRP
FIFO	Asynchronous	Asynchronous	Checked	FIFO256xAA
FIFO	Asynchronous	Asynchronous	Generated	FIFO256x9AAP
FIFO	Asynchronous	Synchronous Transparent	Checked	FIFO256xAST
FIFO	Asynchronous	Synchronous Transparent	Generated	FIFO256x9ASTP
FIFO	Asynchronous	Synchronous Pipelined	Checked	FIFO256x9ASR
FIFO	Asynchronous	Synchronous Pipelined	Generated	FIFO256x9ASRP
FIFO	Synchronous	Asynchronous	Checked	FIFO256x9SA
FIFO	Synchronous	Asynchronous	Generated	FIFO256xSAP
FIFO	Synchronous	Synchronous Transparent	Checked	FIFO256x9SST
FIFO	Synchronous	Synchronous Transparent	Generated	FIFO256x9SSTP
FIFO	Synchronous	Synchronous Pipelined	Checked	FIFO256x9SSR
FIFO	Synchronous	Synchronous Pipelined	Generated	FIFO256x9SSRP

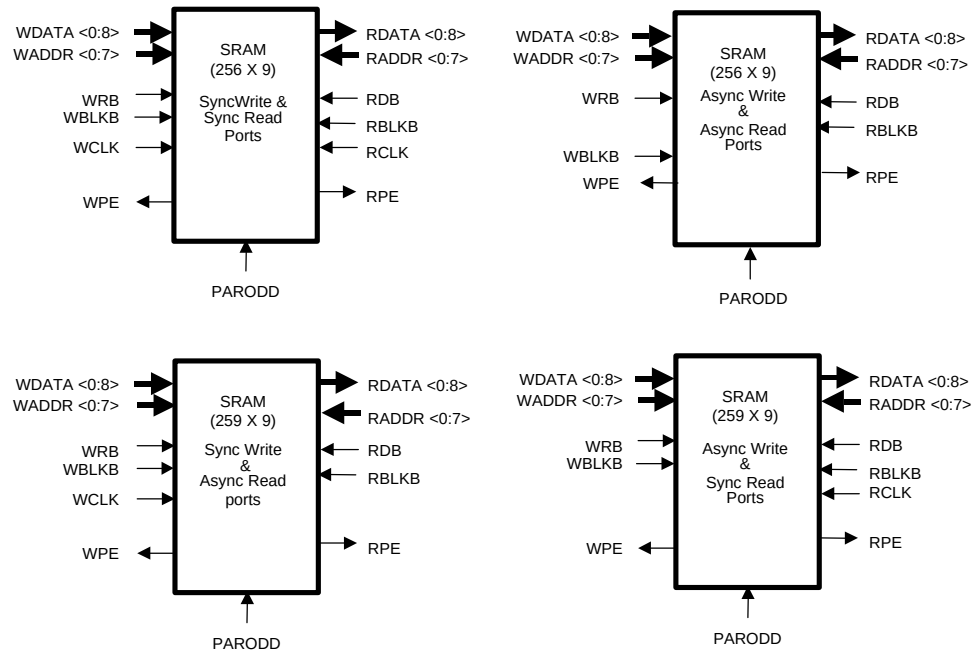


Figure 10 • Example SRAM Block Diagrams

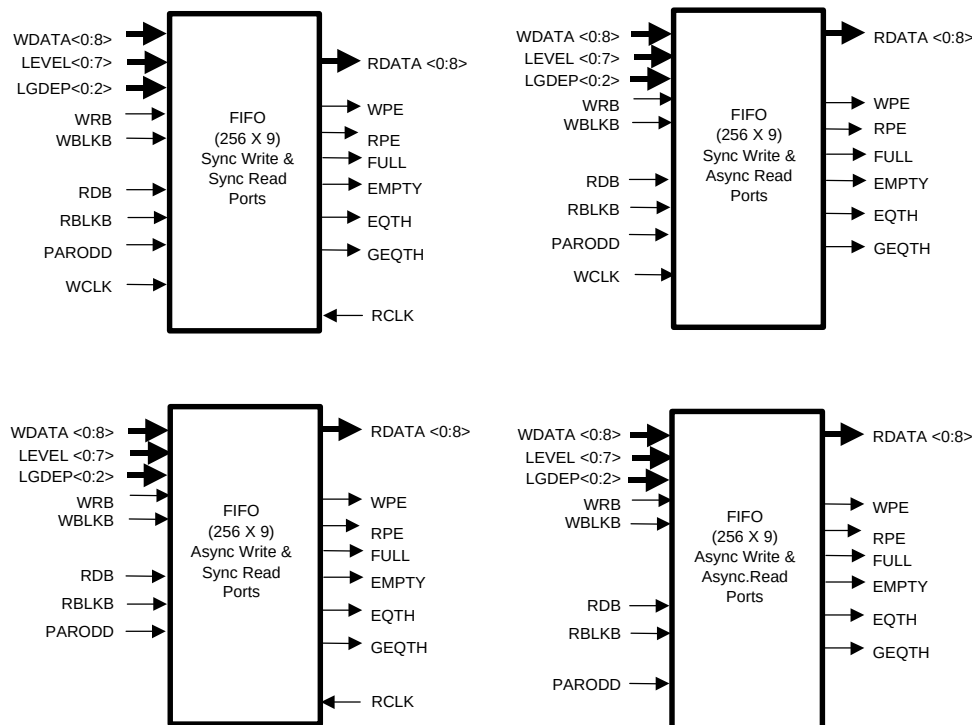


Figure 11 • Basic FIFO Block Diagrams

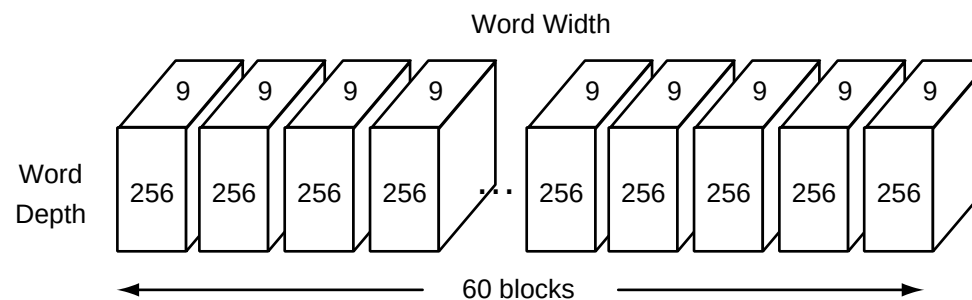


Figure 12 • A500K510 Memory Block Architecture

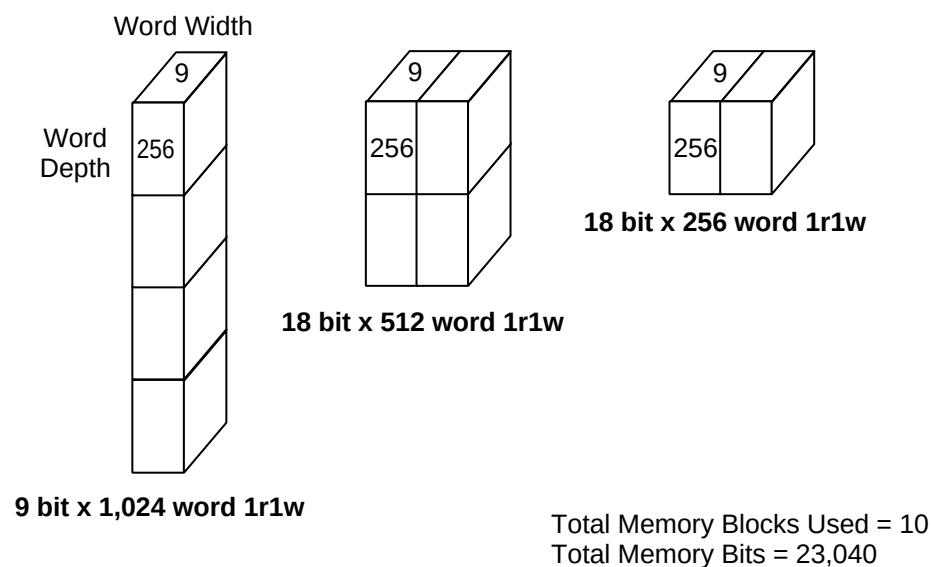


Figure 13 • Memories with Different Width and Depth

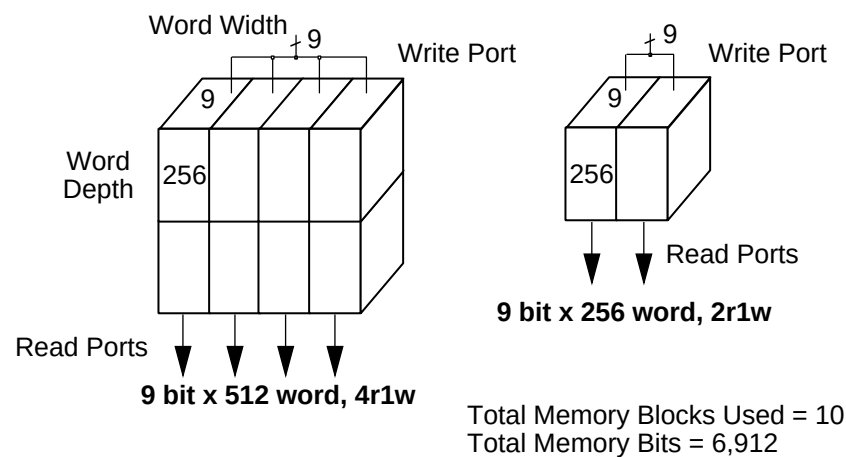


Figure 14 • Multiport Memory Usage

Design Environment

ProASIC devices are supported by Actel's ASICmaster and MEMORYmaster software, as well as third party CAE tools. Using the standard VHDL or Verilog HDL descriptions, no special HDL design techniques, as required by some FPGA vendors, are needed. This allows designers to use technology independent HDL code for ProASIC devices. This and the ProASIC design flow ensure a seamless transition to an ASIC, should production volumes warrant a migration to a gate array or a standard cell product (Figure 15).

MEMORYmaster automatically generates memories from inputs given by the designer. The designer can select the depth and width, usage of parity generation or check, and synchronous or asynchronous functionality of the ports. If it is a synchronous read port, the designer can choose whether the output is pipelined or transparent. MEMORYmaster allows any bit width up to 252 (for the A500K270 device), but if an intermediate bit width is chosen, such as 16 bits, the remaining two bits are no longer accessible for other

memories. MEMORYmaster also enables optimal memory stacking in 256 word increments. However, any word depth may be compiled for up to 7,168 words.

Place and route is performed by Actel's ASICmaster software. Available for SunOS®, Solaris®, HP®, and Windows NT®, it accepts standard netlists in Verilog, VHDL, and in EDIF 2.0.0, performs place and route of the design into the selected device, and provides post layout delay information for back annotation simulation or static timing analysis. The ASICmaster software also contains very powerful interactive layout capabilities for the experienced user.

Once the design is finalized, the programming bitstream is downloaded into the device programmer for ProASIC part programming. ProASIC 500K devices can be programmed with the Silicon Sculptor programmer. In-system programming is also available using the Silicon Sculptor programmer or Silicon Explorer II.

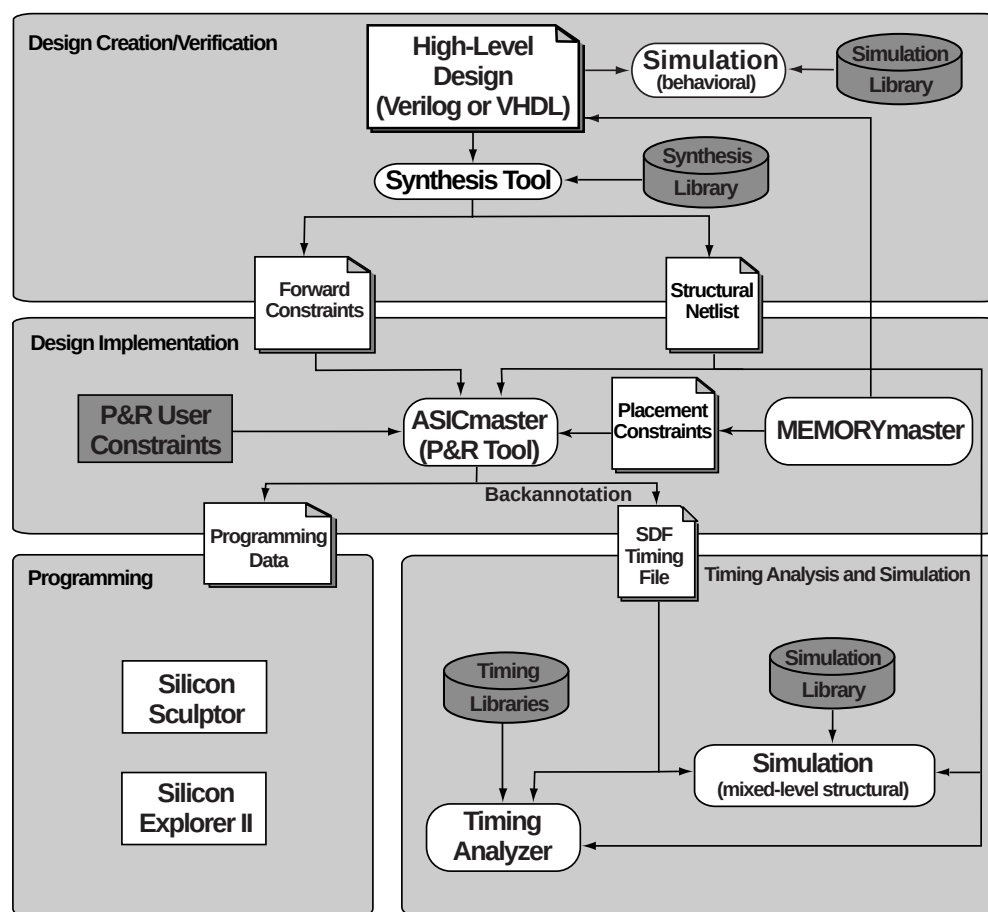


Figure 15 • Design Flow

Package Thermal Characteristics

The ProASIC 500K family is available in a number of package types. Actel has selected packages based on high pin count, reliability factors, and superior thermal characteristics.

The ability of a package to conduct heat away from the silicon, through the package, to the surrounding air is expressed in terms of thermal resistance. This junction-to-ambient thermal resistance is measured in degrees Celsius/Watt and is represented as Theta ja (Θ_{ja}). The lower this thermal resistance, the easier it is for the package to dissipate heat.

The maximum allowed power (P) for a package is a function of the maximum junction temperature (T_J), the maximum ambient operating temperature (T_A), and the

junction-to-ambient thermal resistance Θ_{ja} . Maximum junction temperature is the maximum temperature on the active surface of the IC and is 110° C. P is defined as:

$$P = \frac{T_J - T_A}{\Theta_{ja}}$$

Θ_{ja} is a function of the rate of airflow in contact with the package, in linear feet per minute (lfpm). When the estimated power consumption exceeds the maximum allowed power, other means of cooling must be used, such as increasing the airflow rate.

Package Type	Pin Count	Θ_{jc}	Θ_{ja} Still Air	Θ_{ja} 300 ft/min	Units
Plastic Quad Flat Pack (PQFP)	208	3.5	20	17	°C/W
Plastic Ball Grid Array (PBGA)	272	3	20	16.5	°C/W
Plastic Ball Grid Array (PBGA)	456	3	18	14.5	°C/W

Calculating Power Dissipation

ProASIC device power is calculated in the same manner as LVC MOS gate arrays and includes both a static and an active component. The active component is a function of both the number of tiles utilized and the system speed. ASICmaster provides an automatic power calculator that can be used to quickly and easily calculate power dissipation. Power dissipation can also be calculated using the following formula:

$$P = V_{DD} * I_{DD}$$

where:

$$I_{DD} = I_{STATIC} + I_{OUTPUT} + I_{LOGIC}$$

and

$$I_{STATIC} = I_{STATIC\ CORE} + I_{STATIC\ I/O}$$

I_{OUTPUT} is the current due to the outputs switching.

I_{LOGIC} is the current due to the internal logic signals switching.

The static power (I_{STATIC}) is the amount of current drawn when no inputs are switching. This is equal to the Quiescent Supply Current I_{DDQ} specified under DC Electrical Specifications beginning on [page 16](#).

Active power includes both the current due to outputs switching and the current due to internal logic signals switching.

$$I_{OUTPUT} = \sum_{i=1}^n (C_i \cdot V_i \cdot f_i + I_{DCi})$$

where:

C_i = Capacitance on the i th output pad

V_i = Voltage swing on the i th output pad

f_i = Switching frequency on the i th output pad

n = Number of outputs

I_{DCi} = Average DC load on each pad, if any

In most cases I_{OUTPUT} can be approximated by the following formula, measured in mA:

$$I_{OUTPUT} = n * C_{typ} * V * f_{avg}$$

where:

n = Number of active outputs

C_{typ} = Typical capacitance load on an output

V = Average voltage swing

f_{avg} = Average switching frequency of the outputs. Typically this is less than 25% of the clock frequency

I_{LOGIC} is represented by this formula, measured in mA:

$$I_{LOGIC} = I_E * G * f * F$$

where:

I_E = Effective μA per gate per MHz of the Actel parts. For the ProASIC products the value is 1.2

G = Number of gates used in the design, in thousands

f = Operating frequency in MHz
 F = Fraction of devices active on each clock edge. F varies for different designs, but 0.15 is a conservative and commonly used value.

For an A500K130 design that has 47,000 used gates, 20 memory blocks, 150 active outputs, an average load of 20pF, and a 66 MHz clock, resulting in an average switching frequency of 16.5 MHz, the power calculation appears below.

$$I_{\text{OUTPUT}} = 150 * 20 * 10^{-12} * 3.6 * 16.5 * 10^6 \text{ mA} \\ = 140 \text{ mA}$$

$$P_{\text{OUTPUT}} = 3.6\text{V} * 140 \text{ mA} = .5\text{W}$$

$$I_{\text{LOGIC}} = 1.2 * 47 * 66 * 0.15 \text{ mA} \\ = 558 \text{ mA}$$

Therefore

$$I_{\text{LOGIC}} = 558 \text{ mA}$$

$$P_{\text{Logic}} = 2.75\text{V} * 558 \text{ mA} \\ = 1.5\text{W}$$

Assumptions .5k gates per 256x9 block

$$I_{\text{memory}} = 1.2 * .5 * 66 * .15 * 20 \text{ mA} \\ = 118 \text{ mA}$$

$$P_{\text{memory}} = 2.75\text{V} * 143 \text{ mA} = .326$$

$$P = 1.5\text{W} + .5\text{W} + .32\text{W} = 2.32\text{W}$$

$I_{\text{STATIC CORE}}$ and $I_{\text{STATIC I/O}}$ are not included in this calculation.

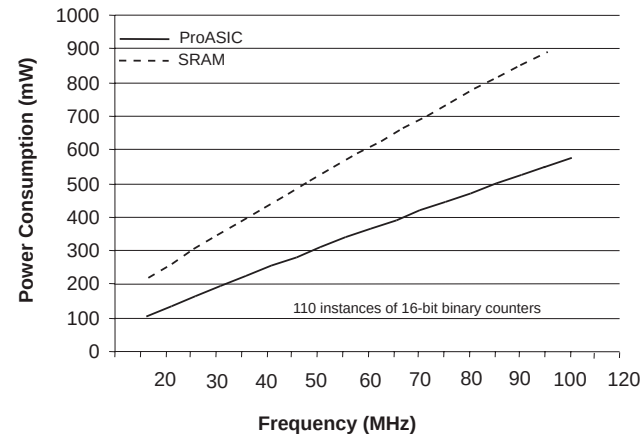


Figure 16 • Power Consumption of a 500K Device

Operating Conditions

Absolute Maximum Ratings

Parameter	Condition	Minimum	Maximum	Units
Supply Voltage Core (V_{DDL})		-0.3	3.0	V
Supply Voltage IO Ring (V_{DDP})		-0.3	4.0	V
DC Input Voltage		-0.3	$V_{\text{DDP}} + 0.3$	V
PCI DC Input Voltage		-0.5	$V_{\text{DDP}} + 0.5$	V
DC Input Clamp Current (I _{IK})	$V_{\text{IN}} < 0$ or $> V_{\text{DDP}}$	-10	+10	mA

Note: Stresses beyond those listed under Absolute Maximum ratings can cause permanent damage to the device. Exposure to maximum rated conditions for extended periods can adversely affect device reliability. Operation of the device at these conditions or any others beyond those listed in the Recommended Operating Conditions table on page 15 is not implied.

Temperature Maximums

Parameter	Min.	Max.	Units	Program Retention
Storage Temperature	–65	+150	°C	N/A
Storage Temperature—Programmed	–65	+110	°C	20 years

Programming Limits and Recommended Operating Conditions

Product Grade	Programming Cycles	Program Retention	Junction Temperature	
			Min.	Max.
Commercial	500	20 years	0°C	110°C
Industrial	500	20 years	–40°C	110°C

Supply Voltages

Mode	V _{DDL}	V _{DDP}	V _{PP}	V _{PN}
Single Voltage	2.5V	2.5V	$2.5V \leq V_{PP} \leq 16.5V$	$-12V \leq V_{PN} \leq 0V$
Mixed Voltage	2.5V	3.3V	$3.3V \leq V_{PP} \leq 16.5V$	$-12V \leq V_{PN} \leq 0V$

Recommended Operating Conditions

Parameter	Symbol	Limits
Commercial		
DC Supply Voltage (2.5V I/Os)	V _{DDL} & V _{DDP}	2.3V to 2.7V
DC Supply Voltage (3.3V, 2.5V I/Os)	V _{DDP} V _{DDL}	3.0V to 3.6V 2.3V to 2.7V
Operation Ambient Temperature Range	T _A	0°C to 70°C
Operation Junction Temperature (maximum)	T _J	≤ 110°C
Industrial		
DC Supply Voltage (2.5V I/Os)	V _{DDL} & V _{DDP}	2.3V to 2.7V
DC Supply Voltage (2.5V, 3.3V I/Os)	V _{DDP} V _{DDL}	3.0V to 3.6V 2.3V to 2.7V
Operation Ambient Temperature Range	T _A	–40°C to 85°C
Operation Junction Temperature (maximum)	T _J	≤ 110°C

DC Electrical Specifications ($V_{DDP} = 2.5V$)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DDP} V_{DDL}	Supply Voltage		2.3		2.7	V
V_{OH}	Output High Voltage High Drive Low Drive	$I_{OH} = -2.0$ mA $I_{OH} = -4.0$ mA $I_{OH} = -8.0$ mA $I_{OH} = -1.0$ mA $I_{OH} = -2.0$ mA $I_{OH} = -4.0$ mA	2.1 2.0 1.7 2.1 2.0 1.7			V
V_{OL}	Output Low Voltage High Drive Low Drive	$I_{OL} = 5.0$ mA $I_{OL} = 10.0$ mA $I_{OL} = 15.0$ mA $I_{OL} = 2.0$ mA $I_{OL} = 3.5$ mA $I_{OL} = 5.0$ mA			0.2 0.4 0.7 0.2 0.4 0.7	V
V_{IH}	Input High Voltage		1.7		$V_{DDP} + 0.3$	V
V_{IL}	Input Low Voltage		-0.3		.7	V
I_{IN}	Input Current Input Current	with pull-up without pull-up	-20 -10		-100 10	μ A μ A
I_{DDQ}	Quiescent Supply Current	$V_{IN} = V_{SS}^{\dagger}$ or V_{DDL}		1.0	10	mA
I_{OZ}	3-State Output Leakage Current	$V_{OH} = V_{SS}$ or V_{DDL}	-10		+10	μ A
I_{OSH}	Output Short Circuit Current High High Drive Low Drive				-120 -100	mA
I_{OSL}	Output Short Circuit Current Low High Drive Low Drive				100 30	mA
$C_{I/O}$	I/O Pad Capacitance				8	pF
C_{CLK}	Clock Input Pad Capacitance				8	pF

Notes: All process conditions. Junction Temperature: -40 to +110°C.

$\dagger$ No pull-up resistor.

DC Electrical Specifications ($V_{DDP} = 3.3V$)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DDP}	Supply Voltage		3.0		3.6	V
V_{DDL}	Supply Voltage, Logic Array		2.3		2.7	V
V_{OH}	Output High Voltage					V
	3.3V I/O, High Drive	$I_{OH} = -3.0\text{ mA}$ $I_{OH} = -5.0\text{ mA}$ $I_{OH} = -10.0\text{ mA}$	$V_{DDP} - 0.2$ $0.9 \times V_{DDP}$ 2.4			
	3.3V I/O, Low Drive	$I_{OH} = -2.0\text{ mA}$ $I_{OH} = -3.0\text{ mA}$ $I_{OH} = -6.0\text{ mA}$	$V_{DDP} - 0.2$ $0.9 \times V_{DDP}$ 2.4			
	2.5V I/O, High Drive	$I_{OH} = -0.5\text{ mA}$ $I_{OH} = -1.0\text{ mA}$ $I_{OH} = -2.0\text{ mA}$	2.1 2.0 1.7			V
	2.5V I/O, Low Drive	$I_{OH} = -0.5\text{ mA}$ $I_{OH} = -1.0\text{ mA}$ $I_{OH} = -2.0\text{ mA}$	2.1 2.0 1.7			
V_{OL}	Output Low Voltage					V
	3.3V I/O, High Drive	$I_{OL} = 7.5\text{ mA}$ $I_{OL} = 12.0\text{ mA}$ $I_{OL} = 15.0\text{ mA}$			0.2 $0.1 \times V_{DDP}$ 0.4	
	3.3V I/O, Low Drive	$I_{OL} = 2.5\text{ mA}$ $I_{OL} = 4.0\text{ mA}$ $I_{OL} = 5.0\text{ mA}$			0.2 $0.1 \times V_{DDP}$ 0.4	
	2.5V I/O, High Drive	$I_{OL} = 7.5\text{ mA}$ $I_{OL} = 15.0\text{ mA}$ $I_{OL} = 24.0\text{ mA}$			0.2 0.4 0.7	V
	2.5V I/O, Low Drive	$I_{OL} = 2.5\text{ mA}$ $I_{OL} = 5.0\text{ mA}$ $I_{OL} = 8.0\text{ mA}$			0.2 0.4 0.7	
V_{IH}	Input High Voltage					V
	LVTTL/LVCMOS		2		$V_{DDP} + 0.3$	
	2.5V Mode		1.7		$V_{DDP} + 0.3$	
V_{IL}	Input Low Voltage					V
	LVTTL/LVCMOS		-0.3		0.8	
	2.5V Mode		-0.3		0.7	
I_{IN}	Input Current					
	LVTTL/LVCMOS	with pull-up	-40		-200	μA
	LVTTL/LVCMOS	without pull-up	-10		10	μA
I_{DDQ}	Quiescent Supply Current	$V_{IN} = V_{SS}^{\dagger}$ or V_{DD}		1.0	10	mA

Notes: Refer to PCI Specifications Revision 2.2. for 3.3V high drive, high slew-rate output pads, and all 3.3V input/clock pads.

$\dagger$ No pull-up resistor.

DC Electrical Specifications ($V_{DDP} = 3.3V$) (Continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{OZ}	3-State Output Leakage Current	$V_{OH} = V_{SS}^{\dagger}$ or V_{DD}	-10		+10	μA
I_{OSH}	Output Short Circuit Current High 3.3V I/O, High Drive 3.3V I/O, Low Drive 2.5V I/O, High Drive 2.5V I/O, Low Drive				-200 -140 -100 -100	mA
I_{OSL}	Output Short Circuit Current Low 3.3V I/O, High Drive 3.3V I/O, Low Drive 2.5V I/O, High Drive 2.5V I/O, Low Drive				160 50 160 50	mA
$C_{I/O}$	I/O Pad Capacitance				8	pF
C_{CLK}	Clock Input Pad Capacitance				8	pF

Notes: Refer to PCI Specifications Revision 2.2, for 3.3V high drive, high slew-rate output pads, and all 3.3V input/clock pads.

$\dagger$ No pull-up resistor.

Timing Characteristics

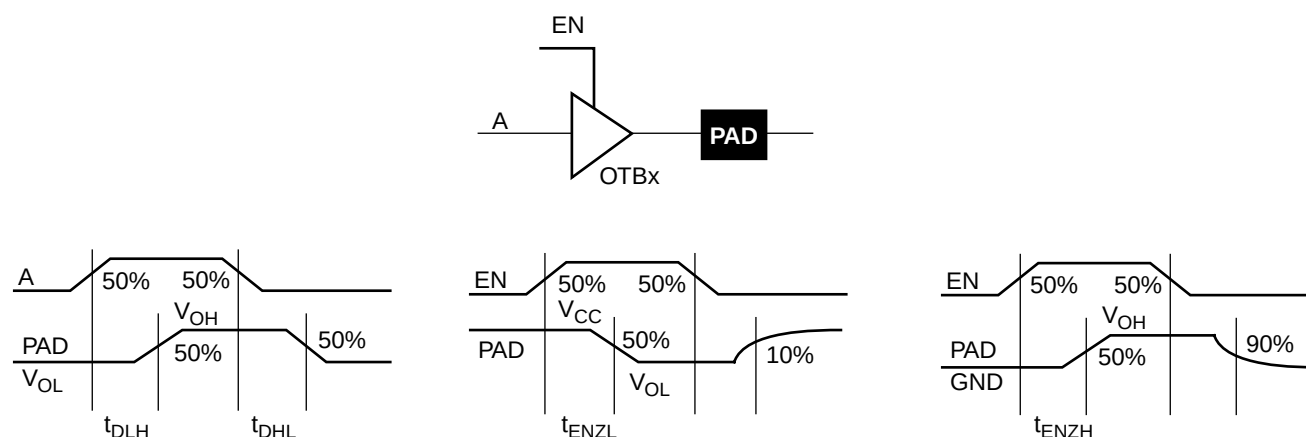


Figure 17 • Tri-State Buffer Delays

Table 3 • Tri-State Buffer Delays

(Worst-Case Commercial Conditions, $V_{DDP} = 3.0V$, $V_{DDL} = 2.3V$, 35 pF load, $T_J = 70^{\circ}C$)

Macro Type	Description	Max t_{DLH}	Max t_{DHL}	Max t_{ENZH}	Max t_{ENZL}	Units
OTB33PH	3.3V, PCI Output Current, High Slew Rate	4.41	4.28	4.40	3.71	ns
OTB33PN	3.3V, PCI Output Current, Nominal Slew Rate	4.91	6.08	4.90	5.46	ns
OTB33PL	3.3V, PCI Output Current, Low Slew Rate	5.51	7.41	5.50	6.86	ns
OTB33LH	3.3V, Low Output Current, High Slew Rate	6.23	6.90	6.24	6.09	ns
OTB33LN	3.3V, Low Output Current, Nominal Slew Rate	6.98	9.63	6.98	9.26	ns
OTB33LL	3.3V, Low Output Current, Low Slew Rate	7.80	12.56	7.80	12.28	ns
OTB25HH	2.5V, High Output Current, High Slew Rate	7.15	3.73	7.15	3.48	ns
OTB25HN	2.5V, High Output Current, Nominal Slew Rate	7.54	5.41	7.54	5.14	ns
OTB25HL	2.5V, High Output Current, Low Slew Rate	8.45	6.66	8.45	6.38	ns
OTB25LH	2.5V, Low Output Current, High Slew Rate	10.77	5.74	10.76	5.37	ns
OTB25LN	2.5V, Low Output Current, Nominal Slew Rate	11.54	8.60	11.52	8.35	ns
OTB25LL	2.5V, Low Output Current, Low Slew Rate	12.39	11.37	12.38	11.12	ns
OTB25LPHH	2.5V, Low Power, High Output Current, High Slew Rate	5.30	5.29	5.27	4.57	ns
OTB25LPHN	2.5V, Low Power, High Output Current, Nominal Slew Rate	6.27	7.99	6.24	7.46	ns
OTB25LPHL	2.5V, Low Power, High Output Current, Low Slew Rate	7.15	10.20	7.12	9.74	ns
OTB25LPLH	2.5V, Low Power, Low Output Current, High Slew Rate	7.74	9.02	7.71	8.10	ns
OTB25LPLN	2.5V, Low Power, Low Output Current, Nominal Slew Rate	8.96	13.11	8.93	12.76	ns
OTB25LPLL	2.5V, Low Power, Low Output Current, Low Slew Rate	10.24	17.72	10.21	17.38	ns

Notes:

1. t_{DLH} = Data-to-Pad HIGH
2. t_{DHL} = Data-to-Pad LOW
3. t_{ENZH} = Enable-to-Pad, Z to HIGH
4. t_{ENZL} = Enable-to-Pad, Z to LOW

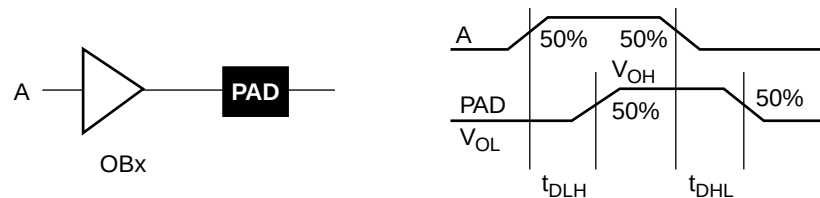


Figure 18 • Output Buffer Delays

Table 4 • Output Buffer Delays

(Worst-Case Commercial Conditions, $V_{DDP} = 3.0V$, $V_{DDL} = 2.3V$, 35 pF load, $T_J = 70^\circ C$)

Macro Type	Description	Max. t_{DLH}	Max. t_{DHL}	Units
OB33PH	3.3V, PCI Output Current, High Slew Rate	4.41	4.28	ns
OB33PN	3.3V, PCI Output Current, Nominal Slew Rate	4.91	6.08	ns
OB33PL	3.3V, PCI Output Current, Low Slew Rate	5.51	7.41	ns
OB33LH	3.3V, Low Output Current, High Slew Rate	6.23	6.90	ns
OB33LN	3.3V, Low Output Current, Nominal Slew Rate	6.98	9.63	ns
OB33LL	3.3V, Low Output Current, Low Slew Rate	7.80	12.56	ns
OB25HH	2.5V, High Output Current, High Slew Rate	7.15	3.73	ns
OB25HN	2.5V, High Output Current, Nominal Slew Rate	7.54	5.41	ns
OB25HL	2.5V, High Output Current, Low Slew Rate	8.45	6.66	ns
OB25LH	2.5V, Low Output Current, High Slew Rate	10.77	5.74	ns
OB25LN	2.5V, Low Output Current, Nominal Slew Rate	11.54	8.60	ns
OB25LL	2.5V, Low Output Current, Low Slew Rate	12.39	11.37	ns
OB25LPHH	2.5V, Low Power, High Output Current, High Slew Rate	5.30	5.29	ns
OB25LPHN	2.5V, Low Power, High Output Current, Nominal Slew Rate	6.27	7.99	ns
OB25LPHL	2.5V, Low Power, High Output Current, Low Slew Rate	7.15	10.20	ns
OB25LPLH	2.5V, Low Power, Low Output Current, High Slew Rate	7.74	9.02	ns
OB25LPLN	2.5V, Low Power, Low Output Current, Nominal Slew Rate	8.96	13.11	ns
OB25LPLL	2.5V, Low Power, Low Output Current, Low Slew Rate	10.24	17.72	ns

Notes:

1. t_{DLH} = Data-to-Pad HIGH
2. t_{DHL} = Data-to-Pad LOW

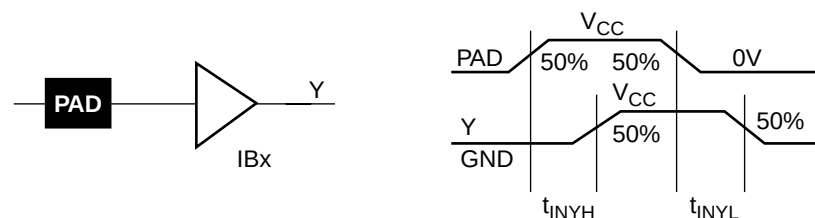


Figure 19 • Input Buffer Delays

Table 5 • Input Buffer Delays

(Worst-Case Commercial Conditions, $V_{DDP} = 3.0V$, $V_{DDL} = 2.3V$, $T_J = 70^{\circ}C$)

Macro Type	Description	Max. t_{INYH}	Max. t_{INYL}	Units
IB25	2.5V, CMOS Input Levels, No Pull-up Resistor	2.26	0.70	ns
IB25LP	2.5V, CMOS Input Levels, Low Power	2.25	1.51	ns
IB33	3.3V, CMOS Input Levels, No Pull-up Resistor	1.98	1.02	ns

Notes:

1. t_{INYH} = Input Pad-to-Y HIGH
2. t_{INYL} = Input Pad-to-Y LOW

Table 6 • Global Input Buffer Delays

(Worst-Case Commercial Conditions, $V_{DDP} = 3.0V$, $V_{DDL} = 2.3V$, $T_J = 70^{\circ}C$)

Macro Type	Description	Max. t_{INYH}	Max. t_{INYL}	Units
GL25	2.5V, CMOS Input Levels	2.17	1.74	ns
GL25LP	2.5V, CMOS Input Levels	2.38	2.37	ns
GL33	3.3V, CMOS Input Levels	3.97	1.17	ns
GL25U	2.5V, CMOS Input Levels, with Pull-up Resistor	2.17	1.74	ns
GL25LPU	2.5V, CMOS Input Levels, Low Power, with Pull-up Resistor	2.38	2.37	ns
GL33U	3.3V, CMOS Input Levels, with Pull-up Resistor	3.97	1.17	ns

Table 7 • Predicted Global Routing Delay*

(Worst-Case Commercial Conditions, $V_{DDP} = 3.0V$, $V_{DDL} = 2.3V$, $T_J = 70^{\circ}C$)

Parameter	Description	Max.	Units
t_{RCKH}	Input Low to High (fully loaded row—32 inputs)	1.19	ns
t_{RCKL}	Input High to Low (fully loaded row—32 inputs)	1.1	ns
t_{RCKH}	Input Low to High (minimally loaded row—1 input)	0.89	ns
t_{RCKL}	Input High to Low (minimally loaded row—1 input)	0.85	ns

*The timing delay difference between tile locations is less than 15ps.

Table 8 • Global Routing Skew

(Worst-Case Commercial Conditions, $V_{DDP} = 3.0V$, $V_{DDL} = 2.3V$, $T_J = 70^{\circ}C$)

Parameter	Description	Max.	Units
t_{RCKSWH}	Maximum Skew Low to High	0.30	ns
t_{RCKSHH}	Maximum Skew High to Low	0.26	ns

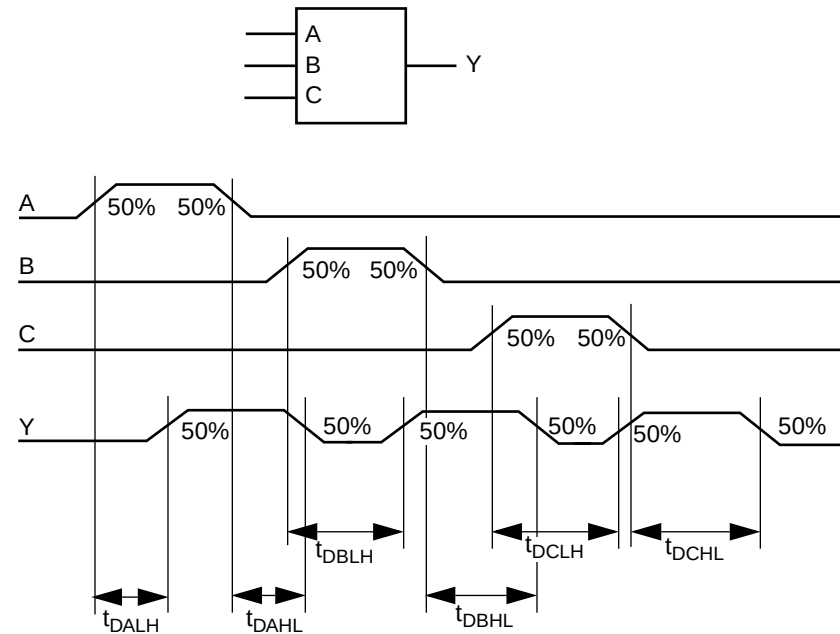


Figure 20 • Module Delays

Table 9 • Sample Macrocell Library Listing
(Worst-Case Commercial Conditions, $V_{DDL} = 2.3V$, $T_J = 70^\circ C$)

Cell Name	Description	Maximum Intrinsic Delay	Minimum Setup/Hold	Units
NAND2	2-Input NAND	0.42		ns
AND2	2-Input AND	0.40		ns
NOR3	3-Input NOR	0.42		ns
MUX2L	2-1 Mux with Active Low Select	0.42		ns
OA21	2-Input OR into a 2-Input AND	0.40		ns
XOR2	2-Input Exclusive OR	0.34		ns
LDL	Active Low Latch (LH/HL)	D: 0.26/0.21	t_{setup} 0.54 t_{hold} 0.20	ns
DFFL	Negative Edge-Triggered D-type Flip-Flop (LH/HL)	CLK-Q: 0.42/0.37	t_{setup} 0.43 t_{hold} 0.20	ns

Note: Assumes fanout of two.

Embedded Memory Specifications

This section focuses on the embedded memory of the ProASIC 500K family. It describes the SRAM and FIFO interface signals and includes timing diagrams that show the relationships of signals as they pertain to single embedded memory blocks (Table 10). Refer to Table 2 on page 9 for basic RAM configurations.

Enclosed Timing Diagrams—SRAM Mode:

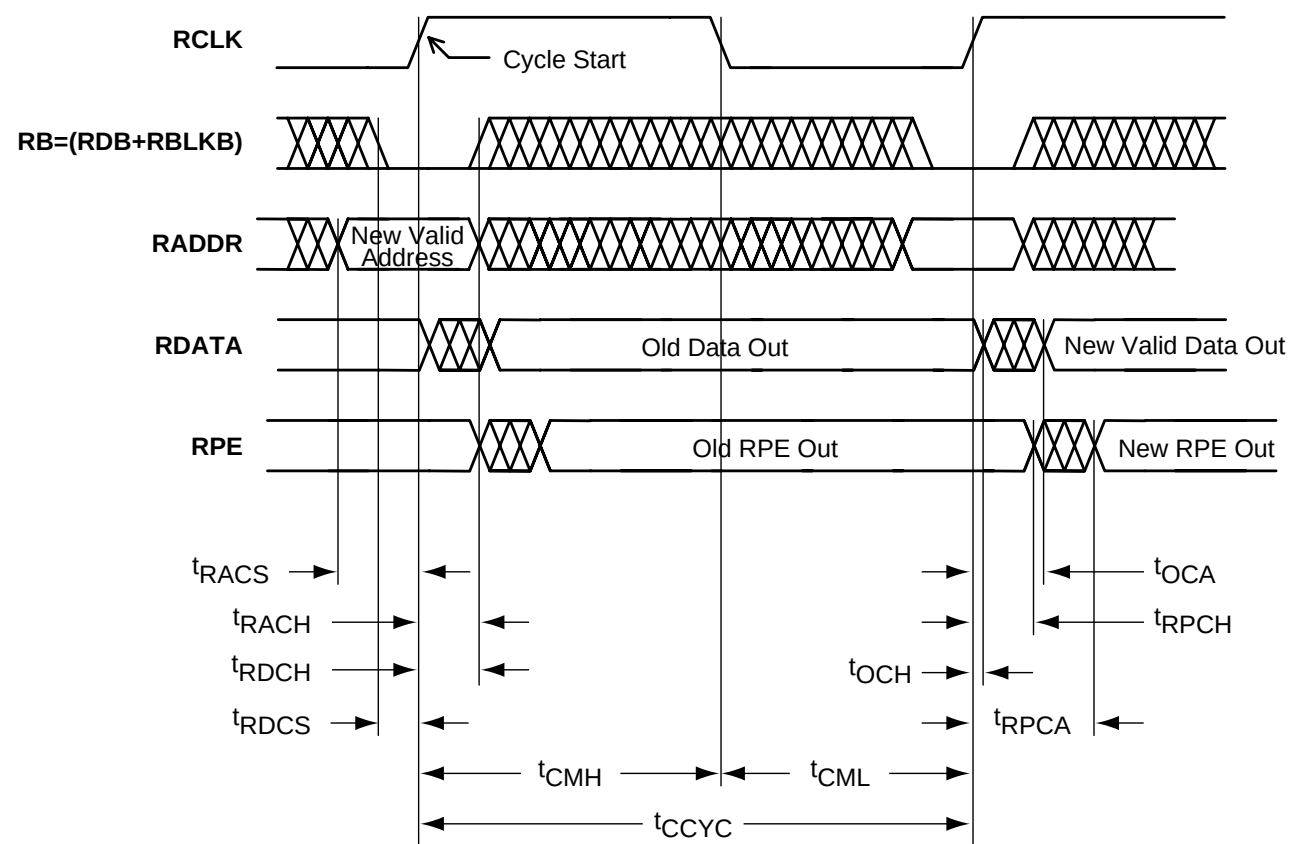
- Asynchronous RAM Read, Address Controlled, RDB=0
- Asynchronous RAM Read, RDB Controlled
- Asynchronous RAM Write
- Synchronous RAM Read, Access Timed Output Strobe (Synchronous Transparent)
- Synchronous RAM Read, Pipeline Mode Outputs (Synchronous Pipelined)
- Synchronous RAM Write
- Synchronous Write & Read to the Same Location
- Asynchronous Write & Synchronous Read to the Same Location
- Asynchronous Write & Read to the Same Location
- Synchronous Write & Asynchronous Read to the Same Location

Note: The difference between synchronous transparent and pipeline modes is the timing of all the output signals from the memory. In transparent mode the outputs will change within the same clock cycle to reflect the data requested by the currently valid access to the memory. However, if clock cycles are short (high clock speed) the data requires most of the clock cycle to change to valid values (stable signals). This makes processing of this data in the same clock cycle nearly impossible. Most designers solve this problem by adding registers at all outputs of the memory to push the data processing into the next clock cycle. In this setup, the whole cycle time can be used to process the data. To simplify the use of this kind of memory setup these registers have been implemented as part of the memory primitive and are available to the user in the synchronous pipeline mode. In this mode the output signals will change shortly after the second rising edge following the initiation of the read access.

Table 10 • Memory Block SRAM Interface Signals

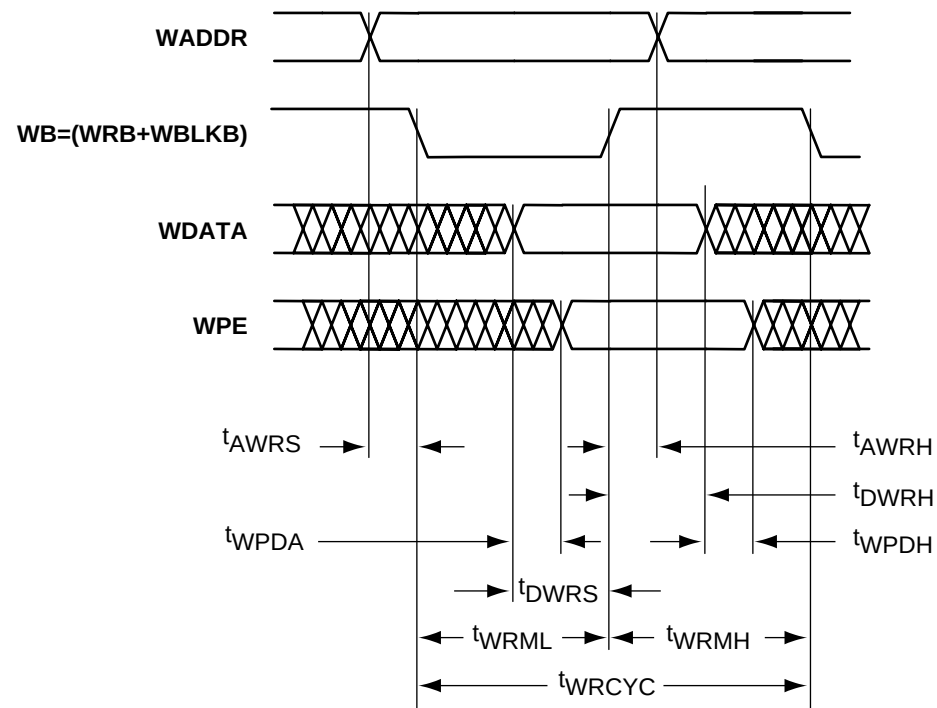
SRAM Signal	Bits	In/Out	Description
WCLKS	1	IN	Write clock used on synchronization on write side
RCLKS	1	IN	Read clock used on synchronization on read side
RADDR<0:7>	8	IN	Read address
RBLKB	1	IN	Negative true read block select
RDB	1	IN	Negative true read pulse
WADDR<0:7>	8	IN	Write address
WBLKB	1	IN	Negative true write block select
DI<0:8>	9	IN	Input data bits <0:8>, <8> will be generated if PARGEN is true
WRB	1	IN	Negative true write pulse
DO<0:8>	9	OUT	Output data bits <0:8>
RPE	1	OUT	Read parity error
WPE	1	OUT	Write parity error
PARODD	1	IN	Selects odd parity generation/detect when high, even when low

Notes: Not all signals shown are used in all modes.

Synchronous RAM Read, Pipeline Mode Outputs (Synchronous Pipelined) **$T_J = 0^{\circ}\text{C}$ to 110°C ; $V_{DDL} = 2.3\text{V}$ to 2.7V**

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
OCA	New RDATA access from RCLK $\uparrow$	2.0		ns	
OCH	Old RDATA valid from RCLK $\uparrow$		.75	ns	
RACH	RADDR hold from RCLK $\uparrow$	0.5		ns	
RACS	RADDR setup to RCLK $\uparrow$	1.0		ns	
RDCH	RDB hold from RCLK $\uparrow$	0.5		ns	
RDCS	RDB setup to RCLK $\uparrow$	1.0		ns	
RPCA	New RPE access from RCLK $\uparrow$	4.0		ns	
RPCH	Old RPE valid from RCLK $\uparrow$		1.0	ns	

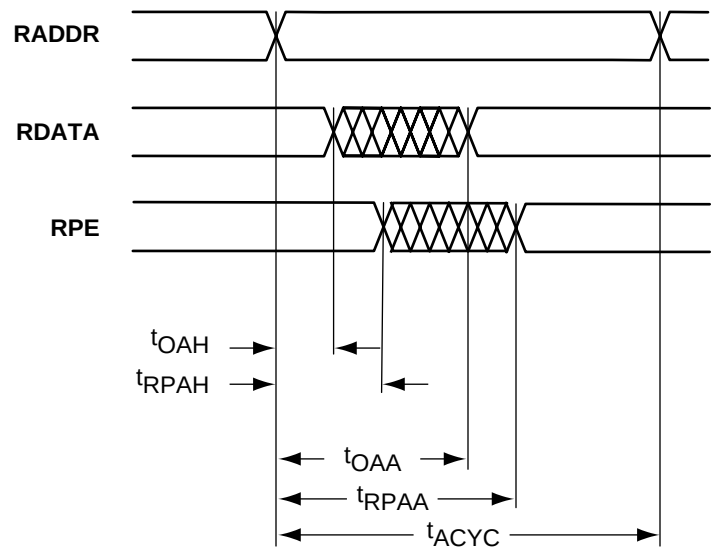
Asynchronous RAM Write



$T_J = 0^{\circ}\text{C}$ to 110°C ; $V_{DDL} = 2.3\text{V}$ to 2.7V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
AWRH	WADDR hold from WB $\uparrow$	1.0		ns	
AWRS	WADDR setup to WB $\downarrow$	0.5		ns	
DWRH	WDATA hold from WB $\uparrow$	1.5		ns	
DWRS	WDATA setup to WB $\uparrow$	0.5		ns	PARGEN is inactive
DWRS	WDATA setup to WB $\uparrow$	2.5		ns	PARGEN is active
WPDA	WPE access from WDATA	3.0		ns	WPE is invalid while
WPDH	WPE hold from WDATA		1.0	ns	PARGEN is active
WRCYC	Cycle time	7.5		ns	
WRMH	WB high phase	3.0		ns	Inactive
WRML	WB low phase	3.0		ns	Active

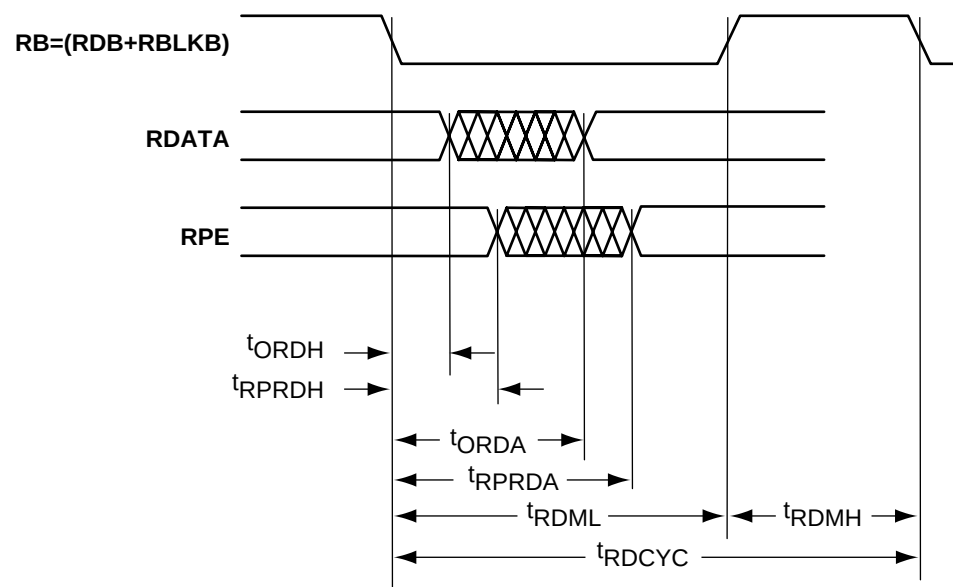
Asynchronous RAM Read, Address Controlled, RDB=0



T_J = 0°C to 110°C; V_{DDL} = 2.3V to 2.7V

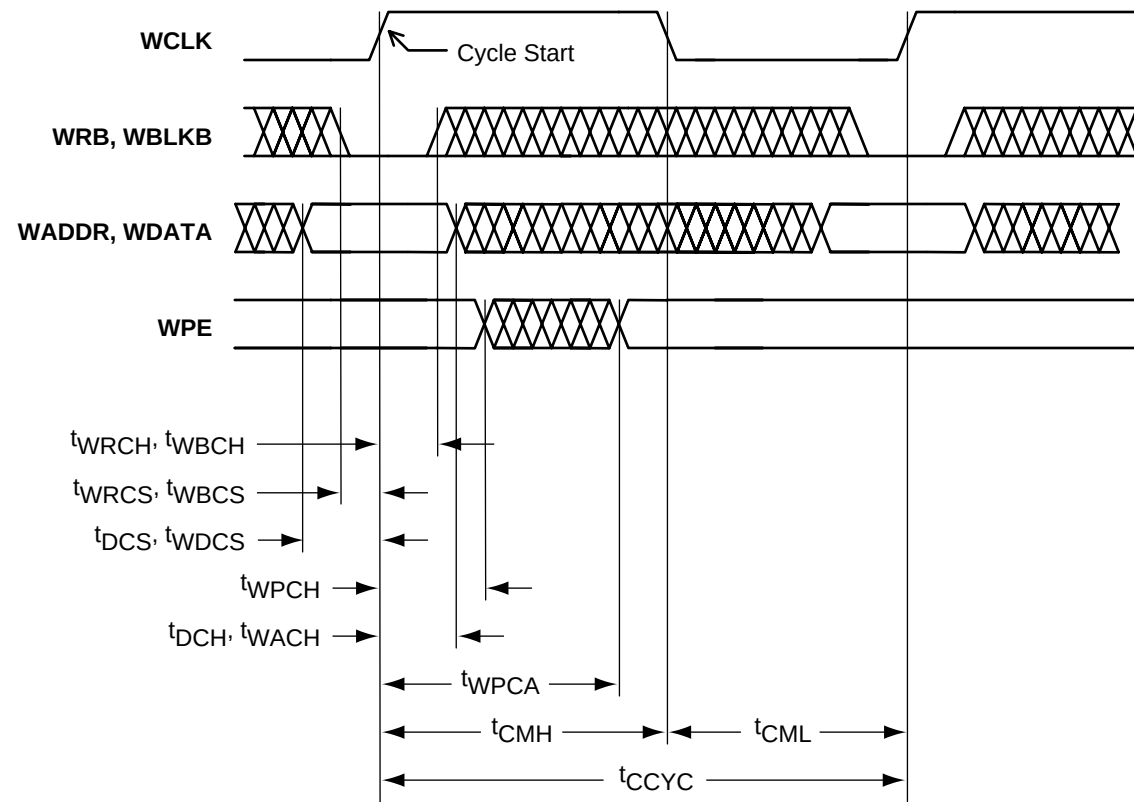
Symbol t _{xxx}	Description	Min.	Max.	Units	Notes
ACYC	Read cycle time	7.5		ns	
OAA	New RDATA access from RADDR stable	7.5		ns	
OA H	Old RDATA hold from RADDR stable		3.0	ns	
RPAA	New RPE access from RADDR stable	10.0		ns	
RPAA H	Old RPE hold from RADDR stable		3.0	ns	

Asynchronous RAM Read, RDB Controlled



$T_J = 0^{\circ}\text{C}$ to 110°C ; $V_{DDL} = 2.3\text{V}$ to 2.7V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ORDA	New RDATA access from RB ↓	7.5		ns	
ORDH	Old RDATA valid from RB ↓		3.0	ns	
RDCYC	Read cycle time	7.5		ns	
RDMH	RB high phase	3.0		ns	Inactive setup to new cycle
RDML	RB low phase	3.0		ns	Active
RPRDA	New RPE access from RB ↓	9.5		ns	
RPRDH	Old RPE valid from RB ↓		3.0	ns	

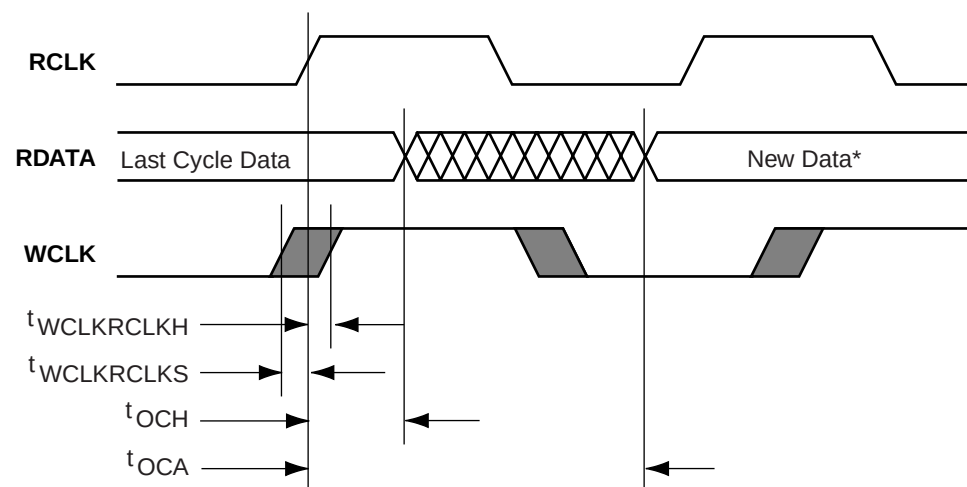
Synchronous RAM Write

$T_J = 0^{\circ}\text{C to } 110^{\circ}\text{C}; V_{DDL} = 2.3\text{V to } 2.7\text{V}$

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
DCH	WDATA hold from WCLK ↑	0.5		ns	
DCS	WDATA setup to WCLK ↑	1.0		ns	
WACH	WADDR hold from WCLK ↑	0.5		ns	
WACS	WADDR setup to WCLK ↑	1.0		ns	
WPCA	New WPE access from WCLK ↑	3.0		ns	WPE is invalid while PARGEN is active
WPCH	Old WPE valid from WCLK ↑		0.5	ns	
WRCH, WBCH	WRB & WBLKB hold from WCLK ↑	0.5		ns	
WRCS, WBCS	WRB & WBLKB setup to WCLK ↑	1.0		ns	

Note: On simultaneous read and write accesses to the same location WDATA is output to RDATA.

Synchronous Write & Read to the Same Location



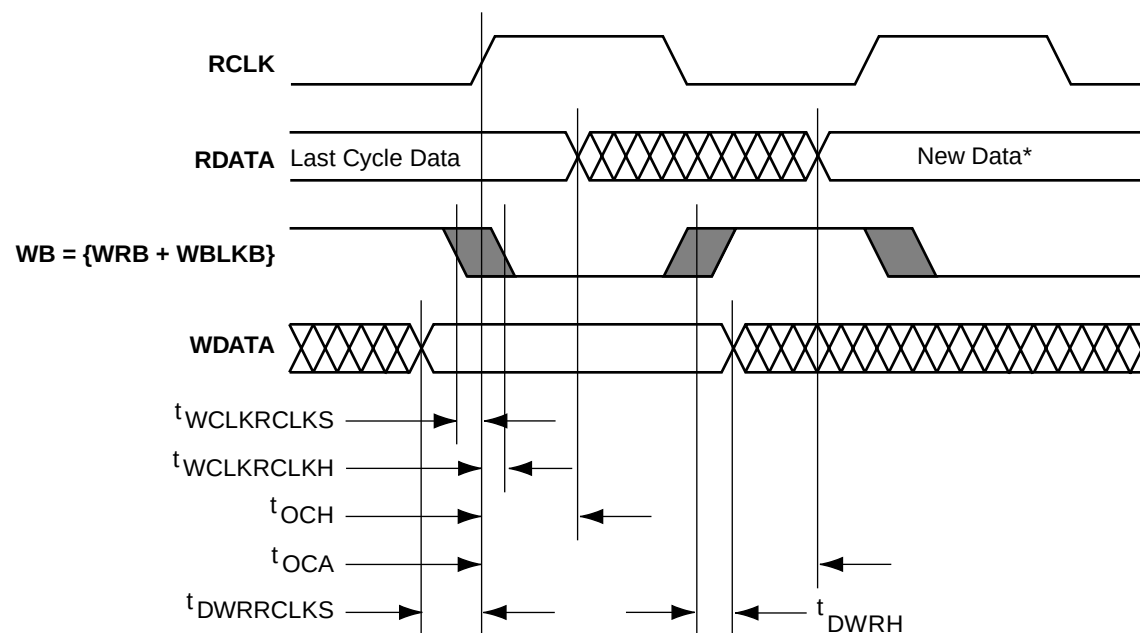
* New data is read if WCLK ↑ occurs before setup time.
The data stored is read if WCLK ↑ occurs after hold time.

T_J = 0°C to 110°C; V_{DDL} = 2.3V to 2.7V

Symbol t _{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
WCLKRCLKS	WCLK ↑ to RCLK ↑ setup time	- 0.1		ns	
WCLKRCLKH	WCLK ↑ to RCLK ↑ hold time		7.0	ns	
OCH	Old RDATA valid from RCLK ↑		3.0	ns	OCA/OCH displayed for Access Timed Output
OCA	New RDATA valid from RCLK ↑	7.5		ns	

Notes:

1. This behavior is valid for Access Timed Output and Pipelined Mode Output. Shown are the timings of an access timed output.
2. During synchronous write and synchronous read access to the same location, the new write data will be read out if the active write clock edge occurs before or at the same time as the active read clock edge. The negative setup time insures this behavior for WCLK and RCLK driven by the same design signal.
3. If WCLK changes after the hold time, the data will be read.
4. A setup or hold time violation will result in unknown output data.

Asynchronous Write & Synchronous Read to the Same Location

* New data is read if WB ↓ occurs before setup time.
 The stored data is read if WB ↓ occurs after hold time.

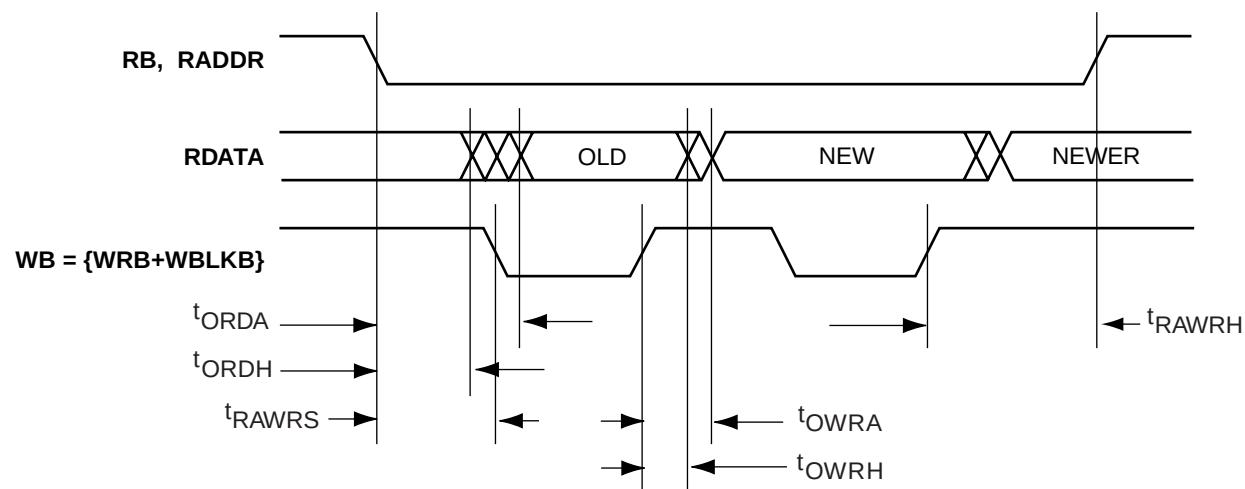
$T_J = 0^{\circ}\text{C to } 110^{\circ}\text{C}; V_{DDL} = 2.3\text{V to } 2.7\text{V}$

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
WBRCLKS	WB ↓ to RCLK ↑ setup time	-0.1		ns	
WBRCLKH	WB ↓ to RCLK ↑ hold time		7.0	ns	
OCH	Old RDATA valid from RCLK ↑		3.0	ns	OCA/OCH displayed for Access Timed Output
OCA	New RDATA valid from RCLK ↑	7.5		ns	
DWRRCLKS	WDATA to RCLK ↑ setup time	0		ns	
DWRH	WDATA to WB ↑ hold time		1.5	ns	

Notes:

1. This behavior is valid for Access Timed Output and Pipelined Mode Output. Shown are the timings of an access timed output.
2. In asynchronous write and synchronous read access to the same location, the new write data will be read out if the active write signal edge occurs before or at the same time as the active read clock edge. If WB changes to low after hold time, the data will be read.
3. A setup or hold time violation will result in unknown output data.

Asynchronous Write & Read to the Same Location

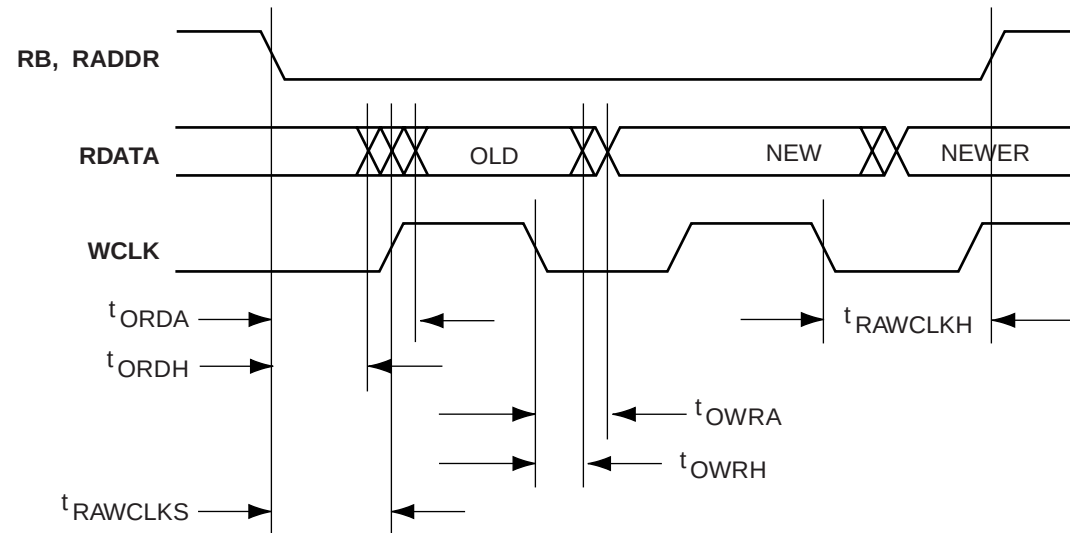


$T_J = 0^{\circ}\text{C}$ to 110°C ; $V_{DDL} = 2.3\text{V}$ to 2.7V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ORDA	New RDATA access from RB ↓	7.5		ns	
ORDH	Old RDATA valid from RB ↓		3.0	ns	
OWRA	New RDATA access from WB ↑	3.0		ns	
OWRH	Old RDATA valid from WB ↑		0.5	ns	
RAWRS	RB ↓ or RADDR from WB ↓	5.0		ns	
RAWRH	RB ↑ or RADDR from WB ↑	5.0		ns	

Notes:

1. During an asynchronous read cycle, each write operation (sync. or async.) to the same location will automatically trigger a read operation which updates the read data.
2. Violation of RAWRS will disturb access to the OLD data.
3. Violation of RAWRH will disturb access to the NEWER data.

Synchronous Write & Asynchronous Read to the Same Location

$T_J = 0^{\circ}\text{C}$ to 110°C ; $V_{DDL} = 2.3\text{V}$ to 2.7V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ORDA	New RDATA access from RB ↓	7.5		ns	
ORDH	Old RDATA valid from RB ↓		3.0	ns	
OWRA	New RDATA access from WCLK ↓	3.0		ns	
OWRH	Old RDATA valid from WCLK ↓		0.5	ns	
RAWCLKS	RB ↓ or RADDR from WCLK ↑	5.0		ns	
RAWCLKH	RB ↑ or RADDR from WCLK ↓	5.0		ns	

Notes:

1. During an asynchronous read cycle, each write operation (sync. or async.) to the same location will automatically trigger a read operation which updates the read data.
2. Violation of RAWCLKS will disturb access to OLD data.
3. Violation of RAWCLKH will disturb access to NEWER data.

Asynchronous FIFO Full and Empty Transitions

The asynchronous FIFO accepts writes and reads while not full or not empty, respectively. When the FIFO is full, all writes are inhibited. Conversely, when the FIFO is empty, all reads are inhibited. A problem is created if the FIFO is written during the transition out of full to not full or read during the transition out of empty to not empty. The exact time at which the write (read) operation changes from inhibited to accepted after the read (write) signal which causes the transition from full (empty) to not full (empty) is indeterminate. This indeterminate period starts 1 ns after the RB (WB) transition which deactivates full (not empty) and ends 3 ns after the RB (WB) transition, for slow cycles. For fast cycles, the indeterminate period ends 3 ns (7.5 ns – RDL (WRL)) after the RB (WB) transition, whichever is later.

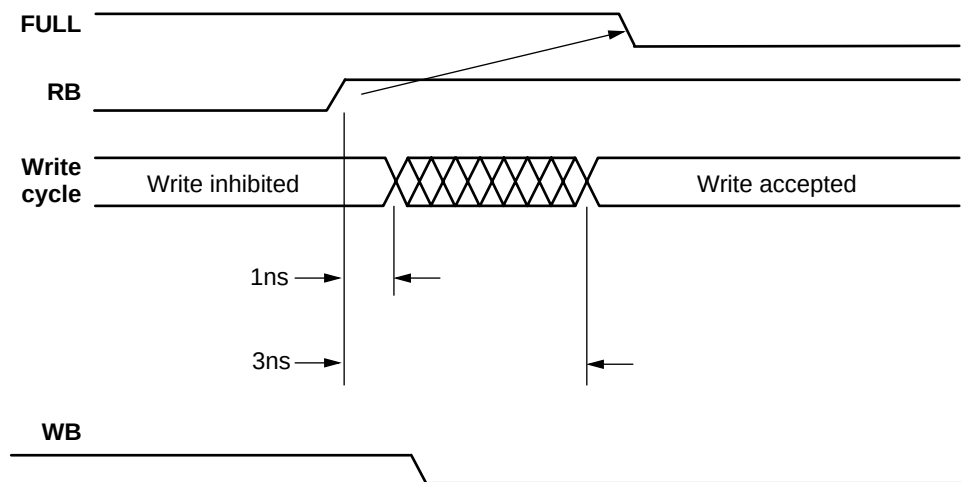
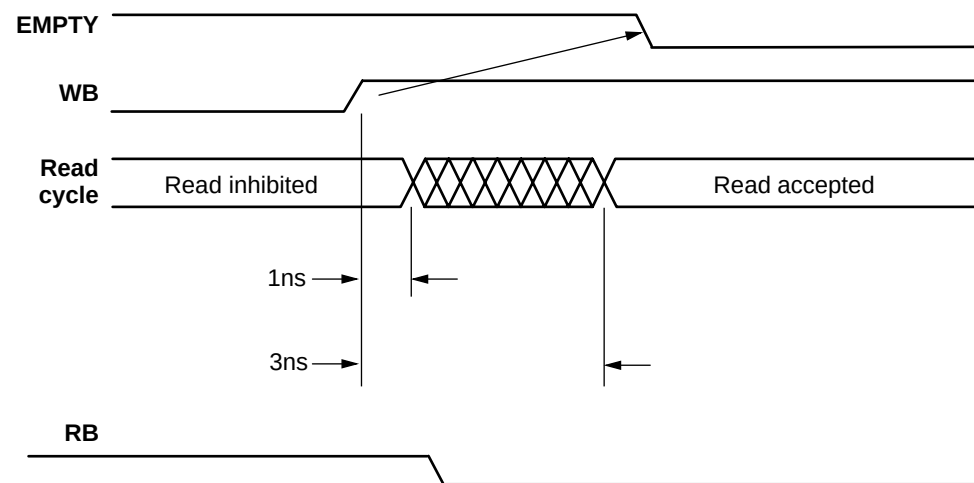
The timing diagram for write is shown in [Figure 21 on page 35](#). The timing diagram for read is shown in [Figure 22 on page 35](#). For basic RAM configurations, see [Table 2 on page 9](#).

Enclosed Timing Diagrams—FIFO Mode:

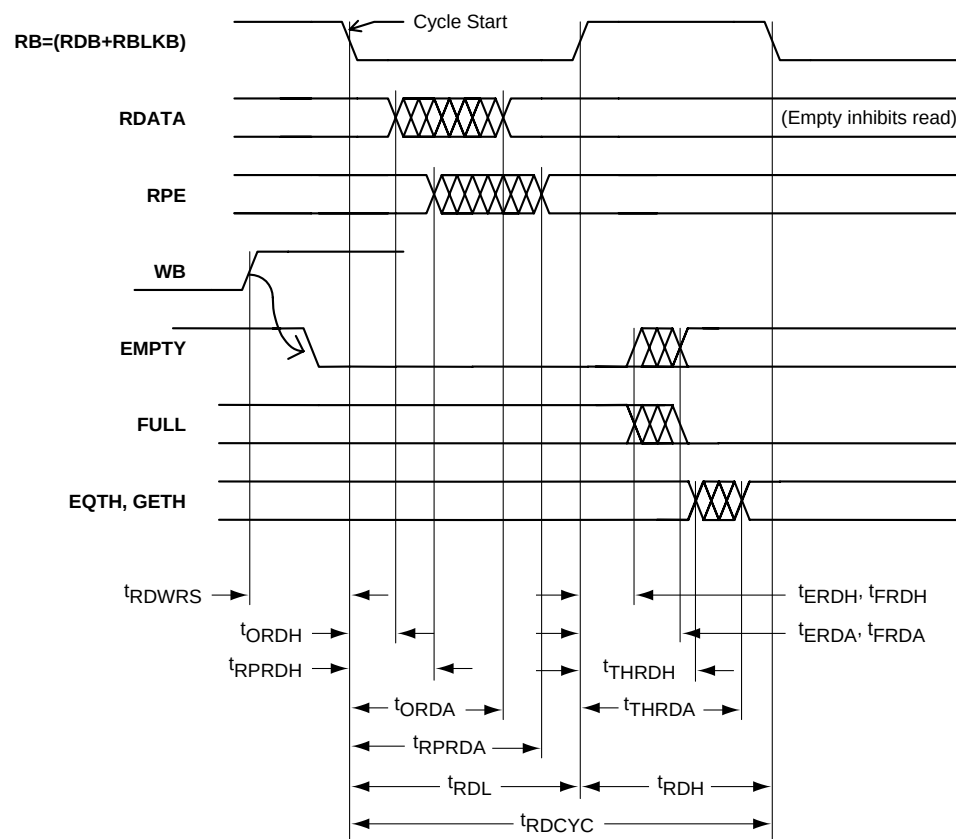
- Asynchronous FIFO Read
- Asynchronous FIFO Write
- Synchronous FIFO Read, Access Timed Output Strobe (Synchronous Transparent)
- Synchronous FIFO Read, Pipeline Mode Outputs (Synchronous Pipelined)
- Synchronous FIFO Write
- FIFO Reset

Table 11 • Memory Block FIFO Interface Signals

FIFO Signal	Bits	In/Out	Description
WCLK	1	IN	Write clock used on synchronization on write side
RCLK	1	IN	Read clock used on synchronization on read side
LEVEL <0:7>	8	IN	Direct configuration implements static flag logic.
RBLKB	1	IN	Negative true read block select.
RDB	1	IN	Negative true read pulse.
RESET	1	IN	Negative true reset for FIFO pointers.
WBLKB	1	IN	Negative true write block select.
DI<0:8>	9	IN	Input data bits <0:8>, <8> will be generated if PARGEN is true.
WRB	1	IN	Negative true write pulse.
FULL, EMPTY	2	OUT	FIFO flags. FULL prevents write and EMPTY prevents read.
EQTH, GEQTH	2	OUT	EQTH is true when the FIFO holds (LEVEL) words. GEQTH is true when the FIFO holds (LEVEL) words or more.
DO<0:8>	9	OUT	Output data bits <0:8>
RPE	1	OUT	Read parity error.
WPE	1	OUT	Write parity error.
LGDEP <0:2>	3	IN	Configures DEPTH of the FIFO to 2 ^(LGDEP+1)
PARODD	1	IN	Selects odd parity generation/detect when high, even when low.

*Figure 21 • Write Timing Diagram**Figure 22 • Read Timing Diagram*

Asynchronous FIFO Read



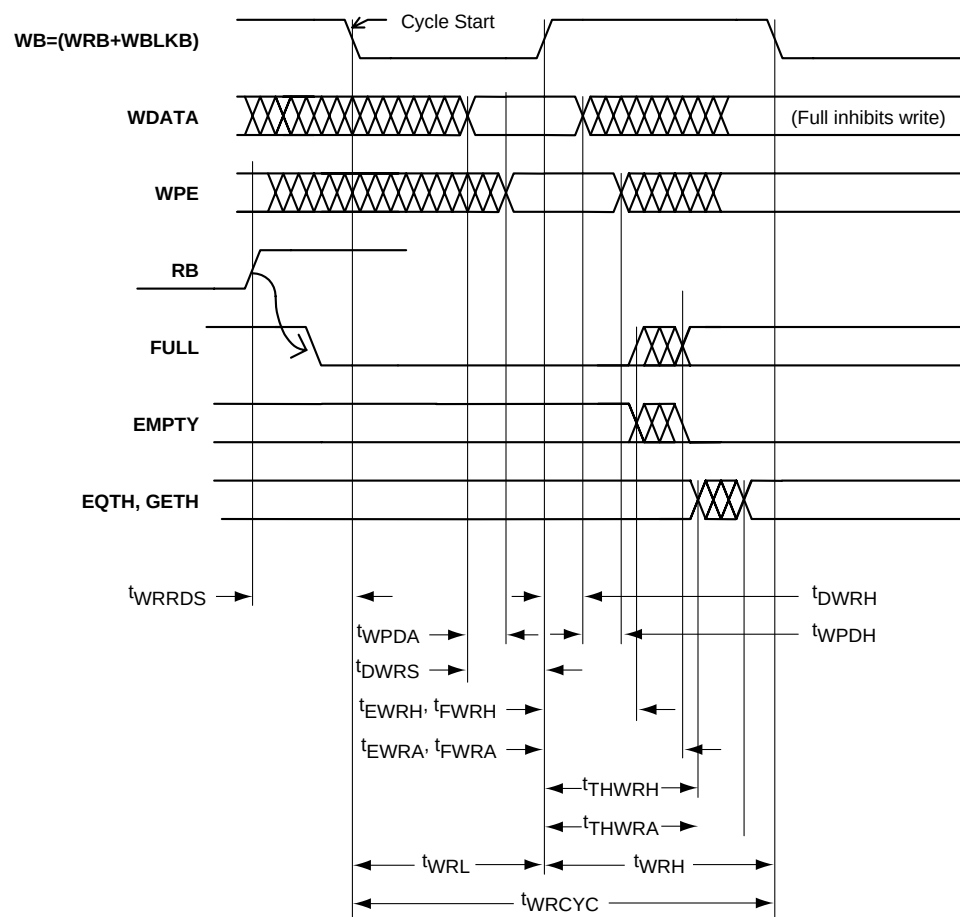
T_J = 0°C to 110°C; V_{DDL} = 2.3V to 2.7V

Symbol t _{xxx}	Description	Min.	Max.	Units	Notes
ERDH, FRDH, THRDH	Old EMPTY, FULL, EQTH, & GETH valid hold time from RB ↑		0.5	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
ERDA	New EMPTY access from RB ↑	3.0 ¹		ns	
FRDA	FULL ↓ access from RB ↑	3.0 ¹		ns	
ORDA	New RDATA access from RB ↓	7.5		ns	
ORDH	Old RDATA valid from RB ↓		3.0	ns	
RDCYC	Read cycle time	7.5		ns	
RDWRS	WB ↑, clearing EMPTY, setup to RB ↓	3.0 ²		ns	Enabling the read operation
			1.0	ns	Inhibiting the read operation
RDH	RB high phase	3.0		ns	Inactive
RDL	RB low phase	3.0		ns	Active
RPRDA	New RPE access from RB ↓	9.5		ns	
RPRDH	Old RPE valid from RB ↓		4.0	ns	
THRDA	EQTH or GETH access from RB ↑	4.5		ns	

Notes:

- At fast cycles, ERDA & FRDA = MAX (7.5 ns – RDL), 3.0 ns
- At fast cycles, RDWRS (for enabling read) = MAX (7.5 ns – WRL), 3.0 ns

Asynchronous FIFO Write



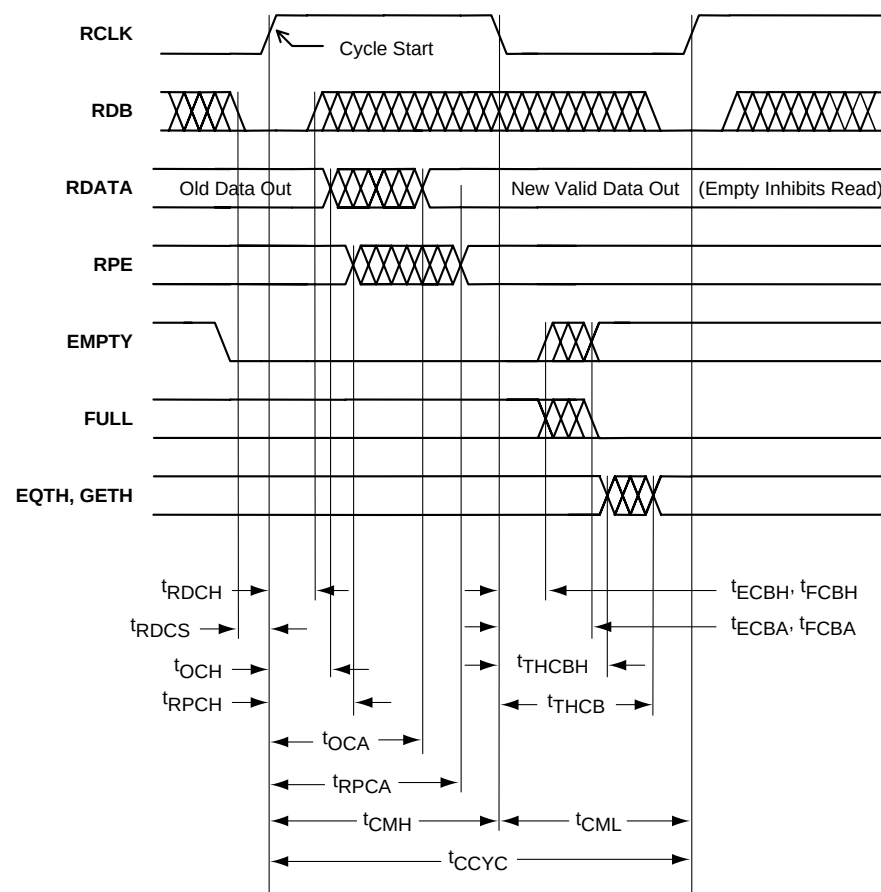
$T_J = 0^{\circ}\text{C}$ to 110°C ; $V_{DDL} = 2.3\text{V}$ to 2.7V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
DWRH	WDATA hold from WB $\uparrow$	1.5		ns	
DWRS	WDATA setup to WB $\uparrow$	0.5		ns	PARGEN is inactive.
DWRS	WDATA setup to WB $\uparrow$	2.5		ns	PARGEN is active.
EWRH, FWRH, THWRH	Old EMPTY, FULL, EQTH, & GETH valid hold time after WB $\uparrow$		0.5	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete.
EWRA	EMPTY $\downarrow$ access from WB $\uparrow$	3.0^1		ns	
FWRA	New FULL access from WB $\uparrow$	3.0^1		ns	
THWRA	EQTH or GETH access from WB $\uparrow$	4.5		ns	
WPDA	WPE access from WDATA	3.0		ns	WPE is invalid while PARGEN is active.
WPDH	WPE hold from WDATA		1.0	ns	
WRCYC	Cycle time	7.5		ns	
WRRDS	RB $\uparrow$, clearing FULL, setup to WB $\downarrow$	3.0^2		ns	Enabling the write operation.
			1.0		Inhibiting the write operation.
WRH	WB high phase	3.0		ns	Inactive
WRL	WB low phase	3.0		ns	Active

Notes:

- At fast cycles, $EWRA, FWRA = \text{MAX}(7.5 \text{ ns} - WRL), 3.0 \text{ ns}$
- At fast cycles, $WRRDS$ (for enabling write) = $\text{MAX}(7.5 \text{ ns} - RDL), 3.0 \text{ ns}$

Synchronous FIFO Read, Access Timed Output Strobe (Synchronous Transparent)



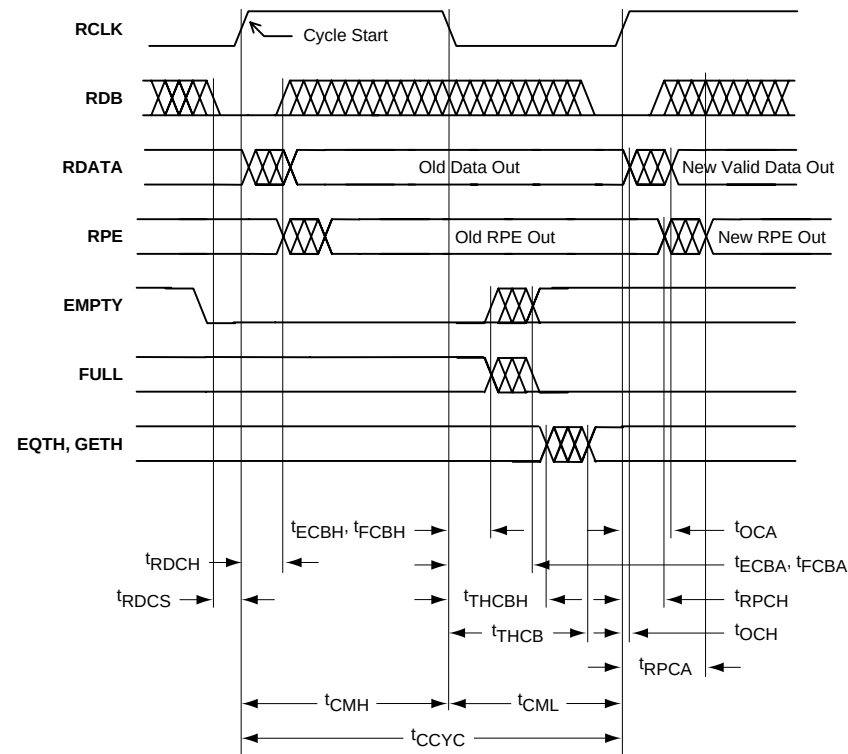
T_J = 0°C to 110°C; V_{DDL} = 2.3V to 2.7V

Symbol t _{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
ECBA	New EMPTY access from RCLK ↓	3.0 ¹		ns	
FCBA	FULL ↓ access from RCLK ↓	3.0 ¹		ns	
ECBH, FCBH, THCBH	Old EMPTY, FULL, EQTH, & GETH valid hold time from RCLK ↓		1.0	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
OCA	New RDATA access from RCLK ↑	7.5		ns	
OCH	Old RDATA valid from RCLK ↑		3.0	ns	
RDCH	RDB hold from RCLK ↑	0.5		ns	
RDCS	RDB setup to RCLK ↑	1.0		ns	
RPCA	New RPE access from RCLK ↑	9.5		ns	
RPCH	Old RPE valid from RCLK ↑		3.0	ns	
THCBA	EQTH or GETH access from RCLK ↓	4.5		ns	

Note:

1. At fast cycles, ECBA & FCBA = MAX(7.5 ns – CMH), 3.0 ns

Synchronous FIFO Read, Pipeline Mode Outputs (Synchronous Pipelined)



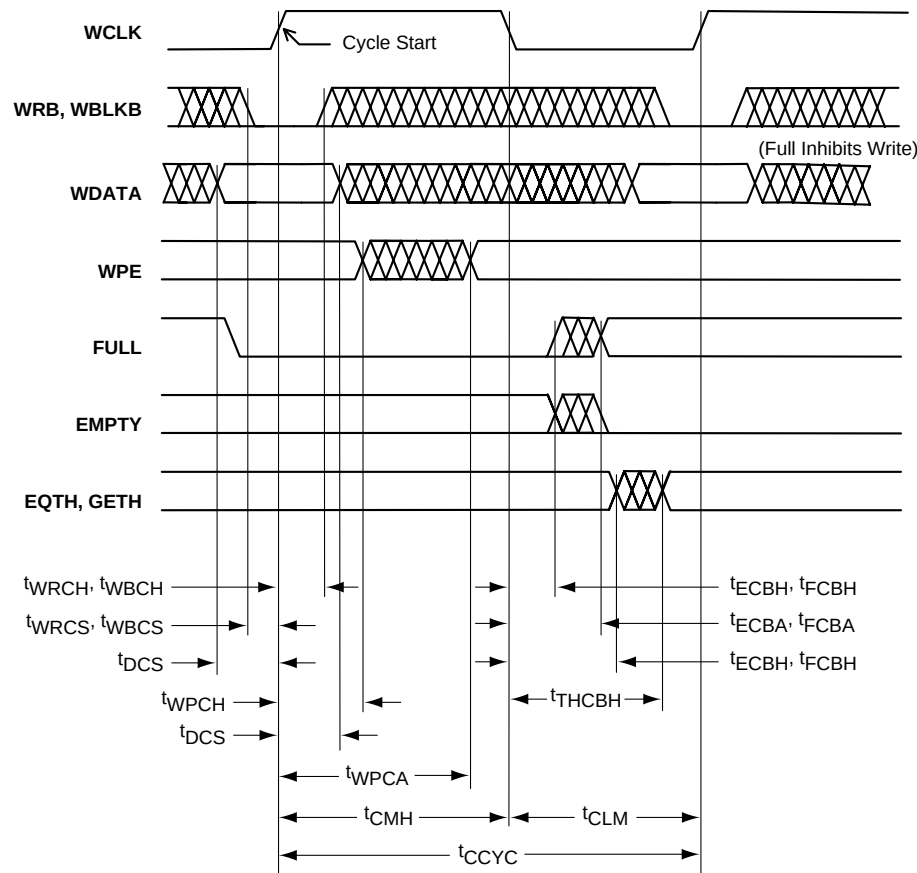
T_J = 0°C to 110°C; V_{DDL} = 2.3V to 2.7V

Symbol t _{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
ECBA	New EMPTY access from RCLK ↓	3.0 ¹		ns	
FCBA	FULL ↓ access from RCLK ↓	3.0 ¹		ns	
ECBH, FCBH, THCBH	Old EMPTY, FULL, EQTH, & GETH valid hold time from RCLK ↓		1.0	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
OCA	New RDATA access from RCLK ↑	2.0		ns	
OCH	Old RDATA valid from RCLK ↑		0.75	ns	
RDCH	RDB hold from RCLK ↑	0.5		ns	
RDCS	RDB setup to RCLK ↑	1.0		ns	
RPCA	New RPE access from RCLK ↑	4.0		ns	
RPCH	Old RPE valid from RCLK ↑		1.0	ns	
THCBA	EQTH or GETH access from RCLK ↓	4.5		ns	

Note:

1. *At fast cycles, ECBA & FCBA = MAX(7.5 ns – CMS), 3.0 ns*

Synchronous FIFO Write

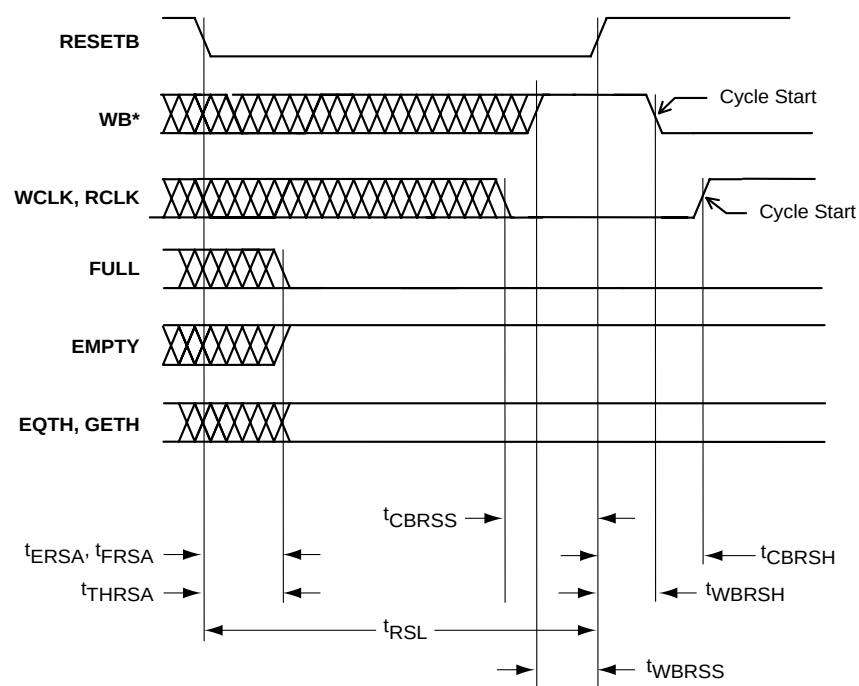


$T_J = 0^\circ\text{C to } 110^\circ\text{C}; V_{DDL} = 2.3\text{V to } 2.7\text{V}$

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
DCH	WDATA hold from WCLK $\uparrow$	0.5		ns	
DCS	WDATA setup to WCLK $\uparrow$	1.0		ns	
FCBA	New FULL access from WCLK $\downarrow$	3.0 ¹		ns	
ECBA	EMPTY $\downarrow$ access from WCLK $\downarrow$	3.0 ¹		ns	
ECBH, FCBH, THCBH	Old EMPTY, FULL, EQTH, & GETH valid hold time from WCLK $\downarrow$		1.0	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
THCBA	EQTH or GETH access from WCLK $\downarrow$	4.5		ns	
WPCA	New WPE access from WCLK $\uparrow$	3.0		ns	WPE is invalid while PARGEN is active
WPCH	Old WPE valid from WCLK $\uparrow$		0.5	ns	
WRCH, WBCH	WRB & WBLKB hold from WCLK $\uparrow$	0.5		ns	
WRCS, WBCS	WRB & WBLKB setup to WCLK $\uparrow$	1.0		ns	

Note:

1. At fast cycles, ECBA & FCBA = MAX (7.5 ns – CMH), 3.0 ns

FIFO Reset

$$*WB = WRB + WBLRB$$

$T_J = 0^{\circ}\text{C}$ to 110°C ; $V_{DDL} = 2.3\text{V}$ to 2.7V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CBRSH	WCLK or RCLK $\uparrow$ hold from RESETB $\uparrow$	1.5		ns	Synchronous mode only
CBRSS	WCLK or RCLK $\downarrow$ setup to RESETB $\uparrow$	1.5		ns	Synchronous mode only
ERSA	New EMPTY $\uparrow$ access from RESETB $\downarrow$	3.0		ns	
FRSA	FULL $\downarrow$ access from RESETB $\downarrow$	3.0		ns	
RSL	RESETB low phase	7.5		ns	
THRSA	EQTH or GETH access from RESETB $\downarrow$	4.5		ns	
WBRSH	WB $\downarrow$ hold from RESETB $\uparrow$	1.5		ns	Asynchronous mode only
WBRSS	WB $\uparrow$ setup to RESETB $\uparrow$	1.5		ns	Asynchronous mode only

Pin Description

I/O **User Input/Output**

The I/O pin functions as an input, output, three-state, or bi-directional buffer. Input and output signal levels are compatible with standard LVTTTL and LVCMOS specifications. Unused I/O pins are configured as inputs with pull-up resistor.

N/C **No Connect**

To maintain compatibility with future Actel ProASIC products it is recommended that this pin not be connected to the circuitry on the board.

GL **Global Input Pin**

Low skew input pin for clock or other global signals. Input only. This pin can be configured with a pull-up resistor.

GND **Ground**

Common ground supply voltage.

V_{DDL} **Logic Array Power Supply Pin**

2.5V supply voltage.

V_{DDP} **I/O Pad Power Supply Pin**

2.5V or 3.3V supply voltage.

V_{PP} **Programming Supply Pin**

This pin must be connected to V_{DDP} during normal operation, or it can remain at 16.5V in an ISP application. This pin must not float.

V_{PN} **Programming Supply Pin**

This pin must be connected to GND during normal operation, or it can remain at -12V in an ISP application. This pin must not float.

TMS **Test Mode Select**

The TMS pin controls the use of JTAG circuitry.

TCK **Test Clock**

Clock input pin for JTAG.

TDI **Test Data In**

Serial input for JTAG.

TDO **Test Data Out**

Serial output for JTAG.

TRST **Test Reset Input**

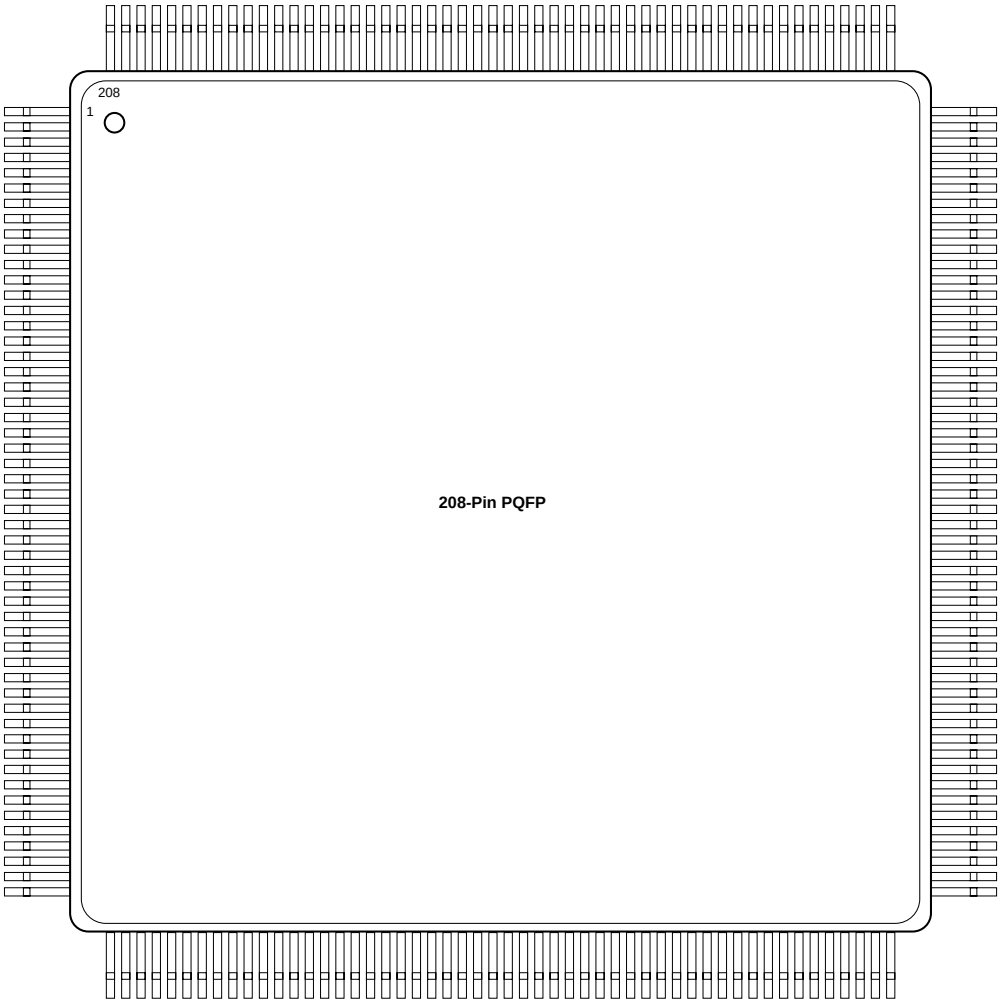
An optimal JTAG reset pin.

RCK **Running Clock**

A free running clock is needed during programming if the programmer cannot guarantee that TCK will be uninterrupted.

Package Pin Assignments

208-Pin PQFP



208-Pin PQFP

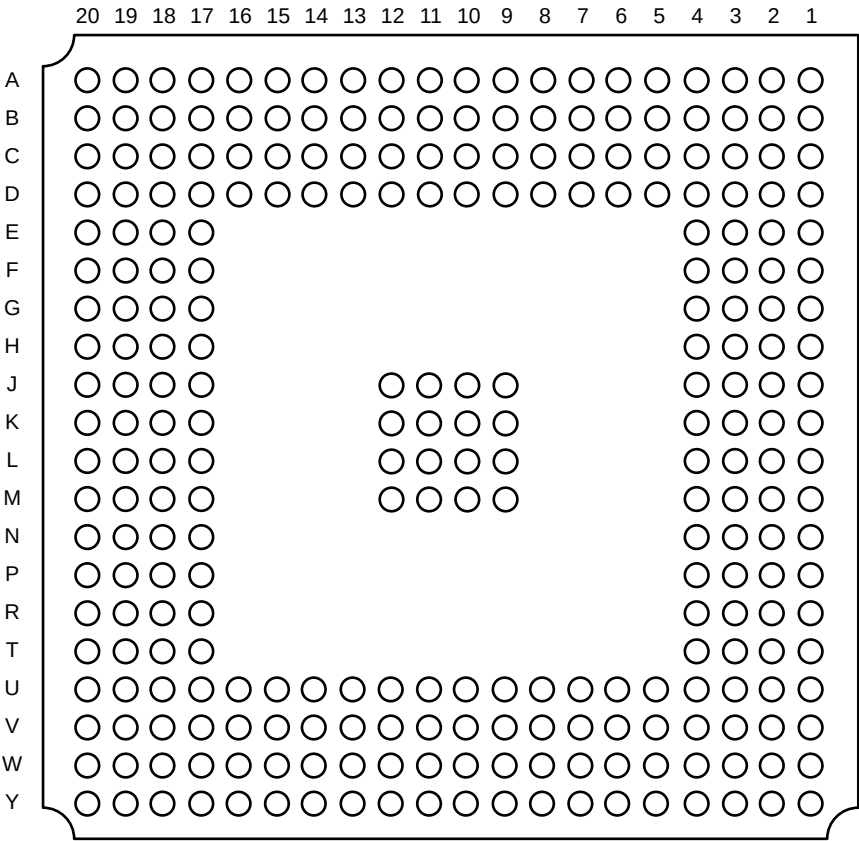
Pin Number	A500K050 Function	A500K130 Function	A500K180 Function	A500K270 Function
1	GND	GND	GND	GND
2	I/O	I/O	I/O	I/O
3	I/O	I/O	I/O	I/O
4	I/O	I/O	I/O	I/O
5	I/O	I/O	I/O	I/O
6	I/O	I/O	I/O	I/O
7	I/O	I/O	I/O	I/O
8	I/O	I/O	I/O	I/O
9	I/O	I/O	I/O	I/O
10	I/O	I/O	I/O	I/O
11	I/O	I/O	I/O	I/O
12	I/O	I/O	I/O	I/O
13	I/O	I/O	I/O	I/O
14	I/O	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O
16	V _{DDL}	V _{DDL}	V _{DDL}	V _{DDL}
17	GND	GND	GND	GND
18	I/O	I/O	I/O	I/O
19	I/O	I/O	I/O	I/O
20	I/O	I/O	I/O	I/O
21	I/O	I/O	I/O	I/O
22	V _{DDP}	V _{DDP}	V _{DDP}	V _{DDP}
23	I/O	I/O	I/O	I/O
24	I/O	I/O	I/O	I/O
25	GL	GL	GL	GL
26	GL	GL	GL	GL
27	I/O	I/O	I/O	I/O
28	I/O	I/O	I/O	I/O
29	GND	GND	GND	GND
30	I/O	I/O	I/O	I/O
31	I/O	I/O	I/O	I/O
32	I/O	I/O	I/O	I/O
33	I/O	I/O	I/O	I/O
34	I/O	I/O	I/O	I/O
35	I/O	I/O	I/O	I/O
36	V _{DDL}	V _{DDL}	V _{DDL}	V _{DDL}
37	I/O	I/O	I/O	I/O
38	I/O	I/O	I/O	I/O
39	I/O	I/O	I/O	I/O
40	V _{DDP}	V _{DDP}	V _{DDP}	V _{DDP}
41	GND	GND	GND	GND
42	I/O	I/O	I/O	I/O
43	I/O	I/O	I/O	I/O
44	I/O	I/O	I/O	I/O
45	I/O	I/O	I/O	I/O
46	I/O	I/O	I/O	I/O
47	I/O	I/O	I/O	I/O
48	I/O	I/O	I/O	I/O
49	I/O	I/O	I/O	I/O
50	I/O	I/O	I/O	I/O
51	I/O	I/O	I/O	I/O
52	GND	GND	GND	GND

Pin Number	A500K050 Function	A500K130 Function	A500K180 Function	A500K270 Function
53	V _{DDP}	V _{DDP}	V _{DDP}	V _{DDP}
54	I/O	I/O	I/O	I/O
55	I/O	I/O	I/O	I/O
56	I/O	I/O	I/O	I/O
57	I/O	I/O	I/O	I/O
58	I/O	I/O	I/O	I/O
59	I/O	I/O	I/O	I/O
60	I/O	I/O	I/O	I/O
61	I/O	I/O	I/O	I/O
62	I/O	I/O	I/O	I/O
63	I/O	I/O	I/O	I/O
64	I/O	I/O	I/O	I/O
65	GND	GND	GND	GND
66	I/O	I/O	I/O	I/O
67	I/O	I/O	I/O	I/O
68	I/O	I/O	I/O	I/O
69	I/O	I/O	I/O	I/O
70	I/O	I/O	I/O	I/O
71	V _{DDL}	V _{DDL}	V _{DDL}	V _{DDL}
72	V _{DDP}	V _{DDP}	V _{DDP}	V _{DDP}
73	I/O	I/O	I/O	I/O
74	I/O	I/O	I/O	I/O
75	I/O	I/O	I/O	I/O
76	I/O	I/O	I/O	I/O
77	I/O	I/O	I/O	I/O
78	I/O	I/O	I/O	I/O
79	I/O	I/O	I/O	I/O
80	I/O	I/O	I/O	I/O
81	GND	GND	GND	GND
82	I/O	I/O	I/O	I/O
83	I/O	I/O	I/O	I/O
84	I/O	I/O	I/O	I/O
85	I/O	I/O	I/O	I/O
86	I/O	I/O	I/O	I/O
87	I/O	I/O	I/O	I/O
88	V _{DDL}	V _{DDL}	V _{DDL}	V _{DDL}
89	V _{DDP}	V _{DDP}	V _{DDP}	V _{DDP}
90	I/O	I/O	I/O	I/O
91	I/O	I/O	I/O	I/O
92	I/O	I/O	I/O	I/O
93	I/O	I/O	I/O	I/O
94	I/O	I/O	I/O	I/O
95	I/O	I/O	I/O	I/O
96	I/O	I/O	I/O	I/O
97	GND	GND	GND	GND
98	I/O	I/O	I/O	I/O
99	I/O	I/O	I/O	I/O
100	I/O	I/O	I/O	I/O
101	TCK, I/O	TCK, I/O	TCK, I/O	TCK, I/O
102	TDI, I/O	TDI, I/O	TDI, I/O	TDI, I/O
103	TMS, I/O	TMS, I/O	TMS, I/O	TMS, I/O
104	V _{DDP}	V _{DDP}	V _{DDP}	V _{DDP}

208-Pin PQFP (Continued)

Pin Number	A500K050 Function	A500K130 Function	A500K180 Function	A500K270 Function	Pin Number	A500K050 Function	A500K130 Function	A500K180 Function	A500K270 Function
105	GND	GND	GND	GND	157	V _{DDP}	V _{DDP}	V _{DDP}	V _{DDP}
106	V _{PP}	V _{PP}	V _{PP}	V _{PP}	158	I/O	I/O	I/O	I/O
107	V _{PN}	V _{PN}	V _{PN}	V _{PN}	159	I/O	I/O	I/O	I/O
108	TDO, I/O	TDO, I/O	TDO, I/O	TDO, I/O	160	I/O	I/O	I/O	I/O
109	TRST, I/O	TRST, I/O	TRST, I/O	TRST, I/O	161	I/O	I/O	I/O	I/O
110	RCK, I/O	RCK, I/O	RCK, I/O	RCK, I/O	162	GND	GND	GND	GND
111	I/O	I/O	I/O	I/O	163	I/O	I/O	I/O	I/O
112	I/O	I/O	I/O	I/O	164	I/O	I/O	I/O	I/O
113	I/O	I/O	I/O	I/O	165	I/O	I/O	I/O	I/O
114	I/O	I/O	I/O	I/O	166	I/O	I/O	I/O	I/O
115	I/O	I/O	I/O	I/O	167	I/O	I/O	I/O	I/O
116	I/O	I/O	I/O	I/O	168	I/O	I/O	I/O	I/O
117	I/O	I/O	I/O	I/O	169	I/O	I/O	I/O	I/O
118	I/O	I/O	I/O	I/O	170	V _{DDP}	V _{DDP}	V _{DDP}	V _{DDP}
119	I/O	I/O	I/O	I/O	171	V _{DDL}	V _{DDL}	V _{DDL}	V _{DDL}
120	I/O	I/O	I/O	I/O	172	I/O	I/O	I/O	I/O
121	I/O	I/O	I/O	I/O	173	I/O	I/O	I/O	I/O
122	GND	GND	GND	GND	174	I/O	I/O	I/O	I/O
123	V _{DDP}	V _{DDP}	V _{DDP}	V _{DDP}	175	I/O	I/O	I/O	I/O
124	I/O	I/O	I/O	I/O	176	I/O	I/O	I/O	I/O
125	I/O	I/O	I/O	I/O	177	I/O	I/O	I/O	I/O
126	V _{DDL}	V _{DDL}	V _{DDL}	V _{DDL}	178	GND	GND	GND	GND
127	I/O	I/O	I/O	I/O	179	I/O	I/O	I/O	I/O
128	I/O	I/O	I/O	I/O	180	I/O	I/O	I/O	I/O
129	I/O	I/O	I/O	I/O	181	I/O	I/O	I/O	I/O
130	GND	GND	GND	GND	182	I/O	I/O	I/O	I/O
131	I/O	I/O	I/O	I/O	183	I/O	I/O	I/O	I/O
132	I/O	I/O	I/O	I/O	184	I/O	I/O	I/O	I/O
133	GL	GL	GL	GL	185	I/O	I/O	I/O	I/O
134	GL	GL	GL	GL	186	V _{DDP}	V _{DDP}	V _{DDP}	V _{DDP}
135	I/O	I/O	I/O	I/O	187	V _{DDL}	V _{DDL}	V _{DDL}	V _{DDL}
136	I/O	I/O	I/O	I/O	188	I/O	I/O	I/O	I/O
137	I/O	I/O	I/O	I/O	189	I/O	I/O	I/O	I/O
138	V _{DDP}	V _{DDP}	V _{DDP}	V _{DDP}	190	I/O	I/O	I/O	I/O
139	I/O	I/O	I/O	I/O	191	I/O	I/O	I/O	I/O
140	I/O	I/O	I/O	I/O	192	I/O	I/O	I/O	I/O
141	GND	GND	GND	GND	193	I/O	I/O	I/O	I/O
142	V _{DDL}	V _{DDL}	V _{DDL}	V _{DDL}	194	I/O	I/O	I/O	I/O
143	I/O	I/O	I/O	I/O	195	GND	GND	GND	GND
144	I/O	I/O	I/O	I/O	196	I/O	I/O	I/O	I/O
145	I/O	I/O	I/O	I/O	197	I/O	I/O	I/O	I/O
146	I/O	I/O	I/O	I/O	198	I/O	I/O	I/O	I/O
147	I/O	I/O	I/O	I/O	199	I/O	I/O	I/O	I/O
148	I/O	I/O	I/O	I/O	200	I/O	I/O	I/O	I/O
149	I/O	I/O	I/O	I/O	201	I/O	I/O	I/O	I/O
150	I/O	I/O	I/O	I/O	202	I/O	I/O	I/O	I/O
151	I/O	I/O	I/O	I/O	203	I/O	I/O	I/O	I/O
152	I/O	I/O	I/O	I/O	204	I/O	I/O	I/O	I/O
153	I/O	I/O	I/O	I/O	205	I/O	I/O	I/O	I/O
154	I/O	I/O	I/O	I/O	206	I/O	I/O	I/O	I/O
155	I/O	I/O	I/O	I/O	207	I/O	I/O	I/O	I/O
156	GND	GND	GND	GND	208	V _{DDP}	V _{DDP}	V _{DDP}	V _{DDP}

Package Pin Assignments (Continued)
272-Pin PBGA (Bottom View)



272-Pin PBGA

Pin Number	A500K050 Function	A500K130 Function	Pin Number	A500K050 Function	A500K130 Function	Pin Number	A500K050 Function	A500K130 Function
A1	I/O	I/O	C7	I/O	I/O	F17	V _{DDP}	V _{DDP}
A2	I/O	I/O	C8	I/O	I/O	F18	I/O	I/O
A3	I/O	I/O	C9	I/O	I/O	F19	I/O	I/O
A4	I/O	I/O	C10	I/O	I/O	F20	I/O	I/O
A5	I/O	I/O	C11	I/O	I/O	G1	I/O	I/O
A6	I/O	I/O	C12	I/O	I/O	G2	I/O	I/O
A7	I/O	I/O	C13	I/O	I/O	G3	I/O	I/O
A8	I/O	I/O	C14	I/O	I/O	G4	I/O	I/O
A9	I/O	I/O	C15	I/O	I/O	G17	I/O	I/O
A10	I/O	I/O	C16	I/O	I/O	G18	I/O	I/O
A11	I/O	I/O	C17	I/O	I/O	G19	I/O	I/O
A12	I/O	I/O	C18	I/O	I/O	G20	I/O	I/O
A13	I/O	I/O	C19	I/O	I/O	H1	I/O	I/O
A14	I/O	I/O	C20	I/O	I/O	H2	I/O	I/O
A15	I/O	I/O	D1	I/O	I/O	H3	I/O	I/O
A16	I/O	I/O	D2	I/O	I/O	H4	I/O	I/O
A17	I/O	I/O	D3	I/O	I/O	H17	I/O	I/O
A18	I/O	I/O	D4	V _{DDP}	V _{DDP}	H18	I/O	I/O
A19	I/O	I/O	D5	V _{DDP}	V _{DDP}	H19	I/O	I/O
A20	I/O	I/O	D6	V _{DDP}	V _{DDP}	H20	GL	GL
B1	I/O	I/O	D7	I/O	I/O	J1	I/O	I/O
B2	I/O	I/O	D8	V _{DDL}	V _{DDL}	J2	GL	GL
B3	I/O	I/O	D9	V _{DDL}	V _{DDL}	J3	GL	GL
B4	I/O	I/O	D10	V _{DDL}	V _{DDL}	J4	V _{DDL}	V _{DDL}
B5	I/O	I/O	D11	V _{DDL}	V _{DDL}	J9	GND	GND
B6	I/O	I/O	D12	V _{DDL}	V _{DDL}	J10	GND	GND
B7	I/O	I/O	D13	V _{DDL}	V _{DDL}	J11	GND	GND
B8	I/O	I/O	D14	I/O	I/O	J12	GND	GND
B9	I/O	I/O	D15	V _{DDP}	V _{DDP}	J17	V _{DDL}	V _{DDL}
B10	I/O	I/O	D16	V _{DDP}	V _{DDP}	J18	GL	GL
B11	I/O	I/O	D17	V _{DDP}	V _{DDP}	J19	I/O	I/O
B12	I/O	I/O	D18	I/O	I/O	J20	I/O	I/O
B13	I/O	I/O	D19	I/O	I/O	K1	I/O	I/O
B14	I/O	I/O	D20	I/O	I/O	K2	I/O	I/O
B15	I/O	I/O	E1	I/O	I/O	K3	I/O	I/O
B16	I/O	I/O	E2	I/O	I/O	K4	V _{DDL}	V _{DDL}
B17	I/O	I/O	E3	I/O	I/O	K9	GND	GND
B18	I/O	I/O	E4	V _{DDP}	V _{DDP}	K10	GND	GND
B19	I/O	I/O	E17	V _{DDP}	V _{DDP}	K11	GND	GND
B20	I/O	I/O	E18	I/O	I/O	K12	GND	GND
C1	I/O	I/O	E19	I/O	I/O	K17	V _{DDL}	V _{DDL}
C2	I/O	I/O	E20	I/O	I/O	K18	I/O	I/O
C3	I/O	I/O	F1	I/O	I/O	K19	I/O	I/O
C4	I/O	I/O	F2	I/O	I/O	K20	I/O	I/O
C5	I/O	I/O	F3	I/O	I/O	L1	I/O	I/O
C6	I/O	I/O	F4	V _{DDP}	V _{DDP}	L2	I/O	I/O

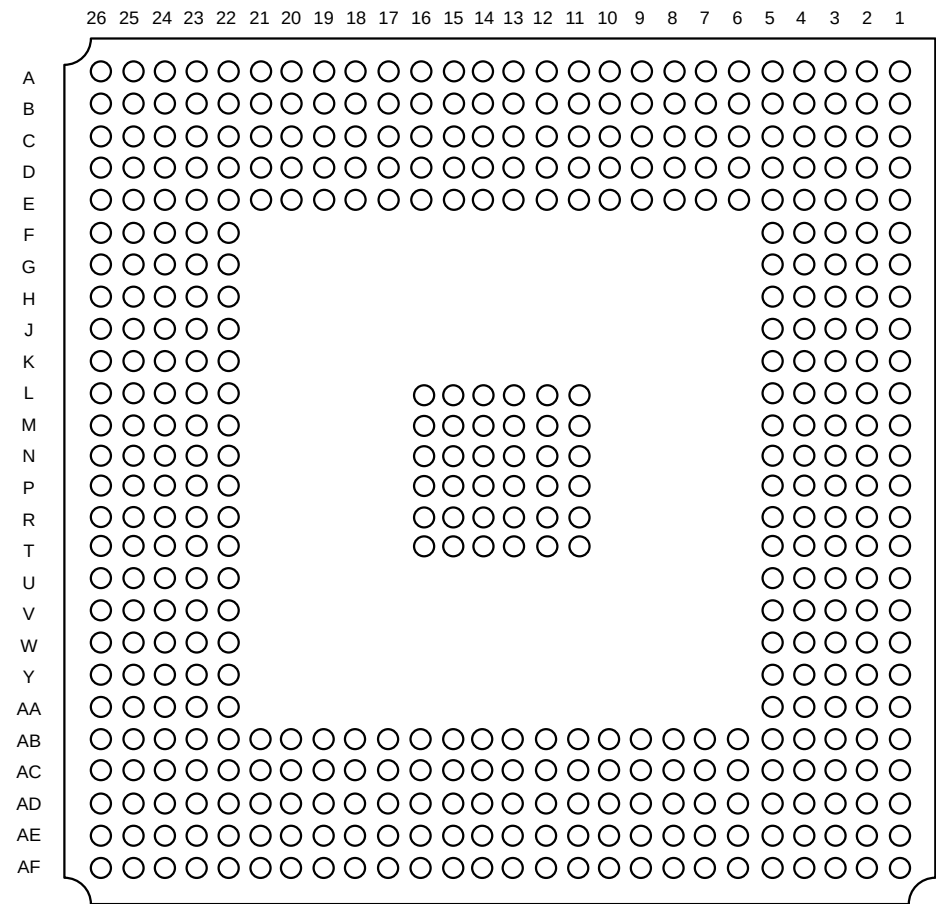
272-Pin PBGA (Continued)

Pin Number	A500K050 Function	A500K130 Function
L3	I/O	I/O
L4	V _{DDL}	V _{DDL}
L9	GND	GND
L10	GND	GND
L11	GND	GND
L12	GND	GND
L17	V _{DDL}	V _{DDL}
L18	I/O	I/O
L19	I/O	I/O
L20	I/O	I/O
M1	I/O	I/O
M2	I/O	I/O
M3	I/O	I/O
M4	V _{DDL}	V _{DDL}
M9	GND	GND
M10	GND	GND
M11	GND	GND
M12	GND	GND
M17	V _{DDL}	V _{DDL}
M18	I/O	I/O
M19	I/O	I/O
M20	I/O	I/O
N1	I/O	I/O
N2	I/O	I/O
N3	I/O	I/O
N4	V _{DDL}	V _{DDL}
N17	V _{DDL}	V _{DDL}
N18	I/O	I/O
N19	I/O	I/O
N20	I/O	I/O
P1	I/O	I/O
P2	I/O	I/O
P3	I/O	I/O
P4	V _{DDP}	V _{DDP}
P17	V _{DDP}	V _{DDP}
P18	I/O	I/O
P19	I/O	I/O
P20	I/O	I/O
R1	I/O	I/O
R2	I/O	I/O
R3	I/O	I/O
R4	V _{DDP}	V _{DDP}
R17	V _{DDP}	V _{DDP}
R18	I/O	I/O
R19	I/O	I/O
R20	I/O	I/O

Pin Number	A500K050 Function	A500K130 Function
T1	I/O	I/O
T2	I/O	I/O
T3	I/O	I/O
T4	V _{DDP}	V _{DDP}
T17	V _{DDP}	V _{DDP}
T18	I/O	I/O
T19	I/O	I/O
T20	I/O	I/O
U1	I/O	I/O
U2	I/O	I/O
U3	I/O	I/O
U4	V _{DDP}	V _{DDP}
U5	V _{DDP}	V _{DDP}
U6	V _{DDP}	V _{DDP}
U7	I/O	I/O
U8	V _{DDL}	V _{DDL}
U9	V _{DDL}	V _{DDL}
U10	V _{DDL}	V _{DDL}
U11	V _{DDL}	V _{DDL}
U12	V _{DDL}	V _{DDL}
U13	V _{DDL}	V _{DDL}
U14	I/O	I/O
U15	V _{DDP}	V _{DDP}
U16	V _{DDP}	V _{DDP}
U17	V _{DDP}	V _{DDP}
U18	RCK, I/O	RCK, I/O
U19	I/O	I/O
U20	I/O	I/O
V1	I/O	I/O
V2	I/O	I/O
V3	I/O	I/O
V4	I/O	I/O
V5	I/O	I/O
V6	I/O	I/O
V7	I/O	I/O
V8	I/O	I/O
V9	I/O	I/O
V10	I/O	I/O
V11	I/O	I/O
V12	I/O	I/O
V13	I/O	I/O
V14	I/O	I/O
V15	I/O	I/O
V16	I/O	I/O
V17	TMS, I/O	TMS, I/O
V18	TDO, I/O	TDO, I/O

Pin Number	A500K050 Function	A500K130 Function
V19	I/O	I/O
V20	I/O	I/O
W1	I/O	I/O
W2	I/O	I/O
W3	I/O	I/O
W4	I/O	I/O
W5	I/O	I/O
W6	I/O	I/O
W7	I/O	I/O
W8	I/O	I/O
W9	I/O	I/O
W10	I/O	I/O
W11	I/O	I/O
W12	I/O	I/O
W13	I/O	I/O
W14	I/O	I/O
W15	I/O	I/O
W16	I/O	I/O
W17	TCK, I/O	TCK, I/O
W18	V _{PP}	V _{PP}
W19	TRST, I/O	TRST, I/O
W20	I/O	I/O
Y1	I/O	I/O
Y2	I/O	I/O
Y3	I/O	I/O
Y4	I/O	I/O
Y5	I/O	I/O
Y6	I/O	I/O
Y7	I/O	I/O
Y8	I/O	I/O
Y9	I/O	I/O
Y10	I/O	I/O
Y11	I/O	I/O
Y12	I/O	I/O
Y13	I/O	I/O
Y14	I/O	I/O
Y15	I/O	I/O
Y16	I/O	I/O
Y17	I/O	I/O
Y18	TDI, I/O	TDI, I/O
Y19	V _{PN}	V _{PN}
Y20	I/O	I/O

Package Pin Assignments (Continued)
456-Pin PBGA (Bottom View)



456-Pin PBGA

Pin Number	A500K130 Function	A500K180 Function	A500K270 Function
A1	V _{DDP}	V _{DDP}	V _{DDP}
A2	V _{DDP}	V _{DDP}	V _{DDP}
A3	NC	I/O	I/O
A4	I/O	I/O	I/O
A5	I/O	I/O	I/O
A6	NC	I/O	I/O
A7	I/O	I/O	I/O
A8	NC	I/O	I/O
A9	NC	I/O	I/O
A10	I/O	I/O	I/O
A11	NC	I/O	I/O
A12	NC	I/O	I/O
A13	I/O	I/O	I/O
A14	NC	I/O	I/O
A15	NC	I/O	I/O
A16	I/O	I/O	I/O
A17	NC	I/O	I/O
A18	NC	I/O	I/O
A19	I/O	I/O	I/O
A20	NC	I/O	I/O
A21	NC	I/O	I/O
A22	I/O	I/O	I/O
A23	NC	I/O	I/O
A24	NC	I/O	I/O
A25	V _{DDP}	V _{DDP}	V _{DDP}
A26	V _{DDP}	V _{DDP}	V _{DDP}
AA1	I/O	I/O	I/O
AA2	I/O	I/O	I/O
AA3	I/O	I/O	I/O
AA4	I/O	I/O	I/O
AA5	V _{DDL}	V _{DDL}	V _{DDL}
AA22	V _{DDL}	V _{DDL}	V _{DDL}
AA23	I/O	I/O	I/O
AA24	I/O	I/O	I/O
AA25	I/O	I/O	I/O
AA26	NC	I/O	I/O
AB1	NC	I/O	I/O
AB2	I/O	I/O	I/O
AB3	I/O	I/O	I/O
AB4	I/O	I/O	I/O
AB5	V _{DDL}	V _{DDL}	V _{DDL}
AB6	V _{DDL}	V _{DDL}	V _{DDL}
AB7	V _{DDL}	V _{DDL}	V _{DDL}
AB8	I/O	I/O	I/O
AB9	I/O	I/O	I/O
AB10	I/O	I/O	I/O

Pin Number	A500K130 Function	A500K180 Function	A500K270 Function
AB11	I/O	I/O	I/O
AB12	I/O	I/O	I/O
AB13	I/O	I/O	I/O
AB14	I/O	I/O	I/O
AB15	I/O	I/O	I/O
AB16	I/O	I/O	I/O
AB17	I/O	I/O	I/O
AB18	I/O	I/O	I/O
AB19	I/O	I/O	I/O
AB20	V _{DDL}	V _{DDL}	V _{DDL}
AB21	V _{DDL}	V _{DDL}	V _{DDL}
AB22	V _{DDL}	V _{DDL}	V _{DDL}
AB23	I/O	I/O	I/O
AB24	I/O	I/O	I/O
AB25	I/O	I/O	I/O
AB26	I/O	I/O	I/O
AC1	I/O	I/O	I/O
AC2	I/O	I/O	I/O
AC3	I/O	I/O	I/O
AC4	V _{DDP}	V _{DDP}	V _{DDP}
AC5	I/O	I/O	I/O
AC6	I/O	I/O	I/O
AC7	I/O	I/O	I/O
AC8	I/O	I/O	I/O
AC9	I/O	I/O	I/O
AC10	I/O	I/O	I/O
AC11	I/O	I/O	I/O
AC12	I/O	I/O	I/O
AC13	I/O	I/O	I/O
AC14	I/O	I/O	I/O
AC15	I/O	I/O	I/O
AC16	I/O	I/O	I/O
AC17	I/O	I/O	I/O
AC18	I/O	I/O	I/O
AC19	I/O	I/O	I/O
AC20	I/O	I/O	I/O
AC21	TMS, I/O	TMS, I/O	TMS, I/O
AC22	TDO, I/O	TDO, I/O	TDO, I/O
AC23	V _{DDP}	V _{DDP}	V _{DDP}
AC24	RCK, I/O	RCK, I/O	RCK, I/O
AC25	I/O	I/O	I/O
AC26	NC	I/O	I/O
AD1	NC	I/O	I/O
AD2	I/O	I/O	I/O
AD3	V _{DDP}	V _{DDP}	V _{DDP}
AD4	I/O	I/O	I/O

456-Pin PBGA (Continued)

Pin Number	A500K130 Function	A500K180 Function	A500K270 Function	Pin Number	A500K130 Function	A500K180 Function	A500K270 Function
AD5	I/O	I/O	I/O	AE25	V _{DDP}	V _{DDP}	V _{DDP}
AD6	I/O	I/O	I/O	AE26	V _{DDP}	V _{DDP}	V _{DDP}
AD7	I/O	I/O	I/O	AF1	V _{DDP}	V _{DDP}	V _{DDP}
AD8	I/O	I/O	I/O	AF2	V _{DDP}	V _{DDP}	V _{DDP}
AD9	I/O	I/O	I/O	AF3	NC	I/O	I/O
AD10	I/O	I/O	I/O	AF4	NC	I/O	I/O
AD11	I/O	I/O	I/O	AF5	I/O	I/O	I/O
AD12	I/O	I/O	I/O	AF6	NC	I/O	I/O
AD13	I/O	I/O	I/O	AF7	NC	I/O	I/O
AD14	I/O	I/O	I/O	AF8	I/O	I/O	I/O
AD15	I/O	I/O	I/O	AF9	NC	I/O	I/O
AD16	I/O	I/O	I/O	AF10	NC	I/O	I/O
AD17	I/O	I/O	I/O	AF11	I/O	I/O	I/O
AD18	I/O	I/O	I/O	AF12	NC	I/O	I/O
AD19	I/O	I/O	I/O	AF13	NC	I/O	I/O
AD20	I/O	I/O	I/O	AF14	I/O	I/O	I/O
AD21	TCK, I/O	TCK, I/O	TCK, I/O	AF15	NC	I/O	I/O
AD22	V _{PP}	V _{PP}	V _{PP}	AF16	NC	I/O	I/O
AD23	I/O	I/O	I/O	AF17	I/O	I/O	I/O
AD24	V _{DDP}	V _{DDP}	V _{DDP}	AF18	NC	I/O	I/O
AD25	I/O	I/O	I/O	AF19	NC	I/O	I/O
AD26	NC	I/O	I/O	AF20	I/O	I/O	I/O
AE1	V _{DDP}	V _{DDP}	V _{DDP}	AF21	NC	I/O	I/O
AE2	V _{DDP}	V _{DDP}	V _{DDP}	AF22	I/O	I/O	I/O
AE3	I/O	I/O	I/O	AF23	TDI, I/O	TDI, I/O	TDI, I/O
AE4	I/O	I/O	I/O	AF24	NC	I/O	I/O
AE5	I/O	I/O	I/O	AF25	V _{DDP}	V _{DDP}	V _{DDP}
AE6	I/O	I/O	I/O	AF26	V _{DDP}	V _{DDP}	V _{DDP}
AE7	I/O	I/O	I/O	B1	V _{DDP}	V _{DDP}	V _{DDP}
AE8	I/O	I/O	I/O	B2	V _{DDP}	V _{DDP}	V _{DDP}
AE9	I/O	I/O	I/O	B3	I/O	I/O	I/O
AE10	I/O	I/O	I/O	B4	I/O	I/O	I/O
AE11	I/O	I/O	I/O	B5	I/O	I/O	I/O
AE12	I/O	I/O	I/O	B6	I/O	I/O	I/O
AE13	I/O	I/O	I/O	B7	I/O	I/O	I/O
AE14	I/O	I/O	I/O	B8	I/O	I/O	I/O
AE15	I/O	I/O	I/O	B9	I/O	I/O	I/O
AE16	I/O	I/O	I/O	B10	I/O	I/O	I/O
AE17	I/O	I/O	I/O	B11	I/O	I/O	I/O
AE18	I/O	I/O	I/O	B12	I/O	I/O	I/O
AE19	I/O	I/O	I/O	B13	I/O	I/O	I/O
AE20	I/O	I/O	I/O	B14	I/O	I/O	I/O
AE21	I/O	I/O	I/O	B15	I/O	I/O	I/O
AE22	I/O	I/O	I/O	B16	I/O	I/O	I/O
AE23	V _{PN}	V _{PN}	V _{PN}	B17	I/O	I/O	I/O
AE24	TRST, I/O	TRST, I/O	TRST, I/O	B18	I/O	I/O	I/O

456-Pin PBGA (Continued)

Pin Number	A500K130 Function	A500K180 Function	A500K270 Function	Pin Number	A500K130 Function	A500K180 Function	A500K270 Function
B19	I/O	I/O	I/O	D13	I/O	I/O	I/O
B20	I/O	I/O	I/O	D14	I/O	I/O	I/O
B21	I/O	I/O	I/O	D15	I/O	I/O	I/O
B22	I/O	I/O	I/O	D16	I/O	I/O	I/O
B23	I/O	I/O	I/O	D17	I/O	I/O	I/O
B24	I/O	I/O	I/O	D18	I/O	I/O	I/O
B25	V _{DDP}	V _{DDP}	V _{DDP}	D19	I/O	I/O	I/O
B26	V _{DDP}	V _{DDP}	V _{DDP}	D20	I/O	I/O	I/O
C1	V _{DDP}	V _{DDP}	V _{DDP}	D21	I/O	I/O	I/O
C2	I/O	I/O	I/O	D22	I/O	I/O	I/O
C3	V _{DDP}	V _{DDP}	V _{DDP}	D23	V _{DDP}	V _{DDP}	V _{DDP}
C4	I/O	I/O	I/O	D24	I/O	I/O	I/O
C5	I/O	I/O	I/O	D25	I/O	I/O	I/O
C6	I/O	I/O	I/O	D26	I/O	I/O	I/O
C7	I/O	I/O	I/O	E1	NC	I/O	I/O
C8	I/O	I/O	I/O	E2	I/O	I/O	I/O
C9	I/O	I/O	I/O	E3	I/O	I/O	I/O
C10	I/O	I/O	I/O	E4	I/O	I/O	I/O
C11	I/O	I/O	I/O	E5	V _{DDL}	V _{DDL}	V _{DDL}
C12	I/O	I/O	I/O	E6	V _{DDL}	V _{DDL}	V _{DDL}
C13	I/O	I/O	I/O	E7	V _{DDL}	V _{DDL}	V _{DDL}
C14	I/O	I/O	I/O	E8	V _{DDL}	V _{DDL}	V _{DDL}
C15	I/O	I/O	I/O	E9	I/O	I/O	I/O
C16	I/O	I/O	I/O	E10	I/O	I/O	I/O
C17	I/O	I/O	I/O	E11	I/O	I/O	I/O
C18	I/O	I/O	I/O	E12	I/O	I/O	I/O
C19	I/O	I/O	I/O	E13	I/O	I/O	I/O
C20	I/O	I/O	I/O	E14	I/O	I/O	I/O
C21	I/O	I/O	I/O	E15	I/O	I/O	I/O
C22	I/O	I/O	I/O	E16	I/O	I/O	I/O
C23	I/O	I/O	I/O	E17	I/O	I/O	I/O
C24	V _{DDP}	V _{DDP}	V _{DDP}	E18	I/O	I/O	I/O
C25	I/O	I/O	I/O	E19	I/O	I/O	I/O
C26	NC	I/O	I/O	E20	V _{DDL}	V _{DDL}	V _{DDL}
D1	NC	I/O	I/O	E21	V _{DDL}	V _{DDL}	V _{DDL}
D2	I/O	I/O	I/O	E22	V _{DDL}	V _{DDL}	V _{DDL}
D3	I/O	I/O	I/O	E23	I/O	I/O	I/O
D4	V _{DDP}	V _{DDP}	V _{DDP}	E24	I/O	I/O	I/O
D5	I/O	I/O	I/O	E25	I/O	I/O	I/O
D6	I/O	I/O	I/O	E26	I/O	I/O	I/O
D7	I/O	I/O	I/O	F1	I/O	I/O	I/O
D8	I/O	I/O	I/O	F2	I/O	I/O	I/O
D9	I/O	I/O	I/O	F3	I/O	I/O	I/O
D10	I/O	I/O	I/O	F4	I/O	I/O	I/O
D11	I/O	I/O	I/O	F5	V _{DDL}	V _{DDL}	V _{DDL}
D12	I/O	I/O	I/O	F22	V _{DDL}	V _{DDL}	V _{DDL}

456-Pin PBGA (Continued)

Pin Number	A500K130 Function	A500K180 Function	A500K270 Function	Pin Number	A500K130 Function	A500K180 Function	A500K270 Function
F23	I/O	I/O	I/O	L3	I/O	I/O	I/O
F24	I/O	I/O	I/O	L4	I/O	I/O	I/O
F25	I/O	I/O	I/O	L5	I/O	I/O	I/O
F26	NC	I/O	I/O	L11	GND	GND	GND
G1	NC	I/O	I/O	L12	GND	GND	GND
G2	I/O	I/O	I/O	L13	GND	GND	GND
G3	I/O	I/O	I/O	L14	GND	GND	GND
G4	I/O	I/O	I/O	L15	GND	GND	GND
G5	V _{DDL}	V _{DDL}	V _{DDL}	L16	GND	GND	GND
G22	V _{DDL}	V _{DDL}	V _{DDL}	L22	I/O	I/O	I/O
G23	I/O	I/O	I/O	L23	I/O	I/O	I/O
G24	I/O	I/O	I/O	L24	I/O	I/O	I/O
G25	I/O	I/O	I/O	L25	I/O	I/O	I/O
G26	I/O	I/O	I/O	L26	NC	I/O	I/O
H1	NC	I/O	I/O	M1	GL	GL	GL
H2	I/O	I/O	I/O	M2	GL	GL	GL
H3	I/O	I/O	I/O	M3	I/O	I/O	I/O
H4	I/O	I/O	I/O	M4	I/O	I/O	I/O
H5	V _{DDL}	V _{DDL}	V _{DDL}	M5	I/O	I/O	I/O
H22	V _{DDL}	V _{DDL}	V _{DDL}	M11	GND	GND	GND
H23	I/O	I/O	I/O	M12	GND	GND	GND
H24	I/O	I/O	I/O	M13	GND	GND	GND
H25	I/O	I/O	I/O	M14	GND	GND	GND
H26	NC	I/O	I/O	M15	GND	GND	GND
J1	I/O	I/O	I/O	M16	GND	GND	GND
J2	I/O	I/O	I/O	M22	GL	GL	GL
J3	I/O	I/O	I/O	M23	I/O	I/O	I/O
J4	I/O	I/O	I/O	M24	I/O	I/O	I/O
J5	I/O	I/O	I/O	M25	I/O	I/O	I/O
J22	I/O	I/O	I/O	M26	NC	I/O	I/O
J23	I/O	I/O	I/O	N1	NC	I/O	I/O
J24	I/O	I/O	I/O	N2	I/O	I/O	I/O
J25	I/O	I/O	I/O	N3	I/O	I/O	I/O
J26	NC	I/O	I/O	N4	I/O	I/O	I/O
K1	NC	I/O	I/O	N5	I/O	I/O	I/O
K2	I/O	I/O	I/O	N11	GND	GND	GND
K3	I/O	I/O	I/O	N12	GND	GND	GND
K4	I/O	I/O	I/O	N13	GND	GND	GND
K5	I/O	I/O	I/O	N14	GND	GND	GND
K22	I/O	I/O	I/O	N15	GND	GND	GND
K23	I/O	I/O	I/O	N16	GND	GND	GND
K24	I/O	I/O	I/O	N22	I/O	I/O	I/O
K25	I/O	I/O	I/O	N23	GL	GL	GL
K26	I/O	I/O	I/O	N24	I/O	I/O	I/O
L1	NC	I/O	I/O	N25	I/O	I/O	I/O
L2	I/O	I/O	I/O	N26	I/O	I/O	I/O

456-Pin PBGA (Continued)

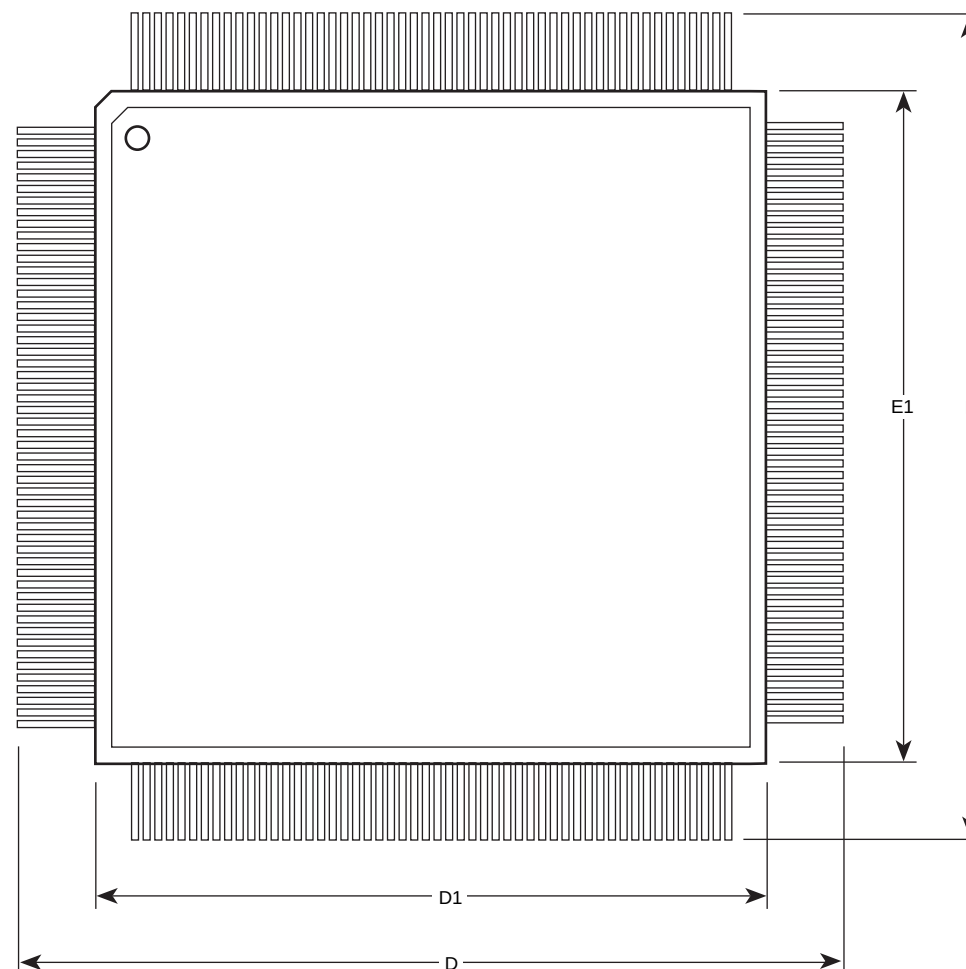
Pin Number	A500K130 Function	A500K180 Function	A500K270 Function
P1	NC	I/O	I/O
P2	I/O	I/O	I/O
P3	I/O	I/O	I/O
P4	I/O	I/O	I/O
P5	I/O	I/O	I/O
P11	GND	GND	GND
P12	GND	GND	GND
P13	GND	GND	GND
P14	GND	GND	GND
P15	GND	GND	GND
P16	GND	GND	GND
P22	I/O	I/O	I/O
P23	I/O	I/O	I/O
P24	I/O	I/O	I/O
P25	I/O	I/O	I/O
P26	NC	I/O	I/O
R1	I/O	I/O	I/O
R2	I/O	I/O	I/O
R3	I/O	I/O	I/O
R4	I/O	I/O	I/O
R5	I/O	I/O	I/O
R11	GND	GND	GND
R12	GND	GND	GND
R13	GND	GND	GND
R14	GND	GND	GND
R15	GND	GND	GND
R16	GND	GND	GND
R22	I/O	I/O	I/O
R23	I/O	I/O	I/O
R24	I/O	I/O	I/O
R25	I/O	I/O	I/O
R26	NC	I/O	I/O
T1	NC	I/O	I/O
T2	I/O	I/O	I/O
T3	I/O	I/O	I/O
T4	I/O	I/O	I/O
T5	I/O	I/O	I/O
T11	GND	GND	GND
T12	GND	GND	GND
T13	GND	GND	GND
T14	GND	GND	GND
T15	GND	GND	GND
T16	GND	GND	GND
T22	I/O	I/O	I/O

Pin Number	A500K130 Function	A500K180 Function	A500K270 Function
T23	I/O	I/O	I/O
T24	I/O	I/O	I/O
T25	I/O	I/O	I/O
T26	I/O	I/O	I/O
U1	NC	I/O	I/O
U2	I/O	I/O	I/O
U3	I/O	I/O	I/O
U4	I/O	I/O	I/O
U5	I/O	I/O	I/O
U22	I/O	I/O	I/O
U23	I/O	I/O	I/O
U24	I/O	I/O	I/O
U25	I/O	I/O	I/O
U26	NC	I/O	I/O
V1	I/O	I/O	I/O
V2	I/O	I/O	I/O
V3	I/O	I/O	I/O
V4	I/O	I/O	I/O
V5	I/O	I/O	I/O
V22	I/O	I/O	I/O
V23	I/O	I/O	I/O
V24	I/O	I/O	I/O
V25	I/O	I/O	I/O
V26	NC	I/O	I/O
W1	NC	I/O	I/O
W2	I/O	I/O	I/O
W3	I/O	I/O	I/O
W4	I/O	I/O	I/O
W5	V _{DDL}	V _{DDL}	V _{DDL}
W22	V _{DDL}	V _{DDL}	V _{DDL}
W23	I/O	I/O	I/O
W24	I/O	I/O	I/O
W25	I/O	I/O	I/O
W26	I/O	I/O	I/O
Y1	NC	I/O	I/O
Y2	I/O	I/O	I/O
Y3	I/O	I/O	I/O
Y4	I/O	I/O	I/O
Y5	V _{DDL}	V _{DDL}	V _{DDL}
Y22	V _{DDL}	V _{DDL}	V _{DDL}
Y23	I/O	I/O	I/O
Y24	I/O	I/O	I/O
Y25	I/O	I/O	I/O
Y26	NC	I/O	I/O

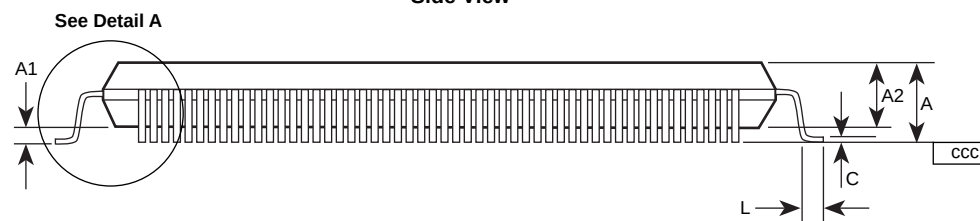
Package Mechanical Drawings

208-Pin PQFP

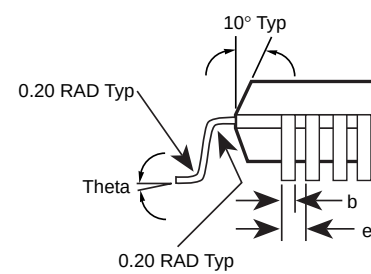
Top View



Side View



Detail A



Plastic Quad Flat Pack

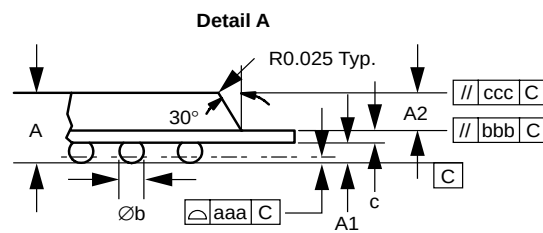
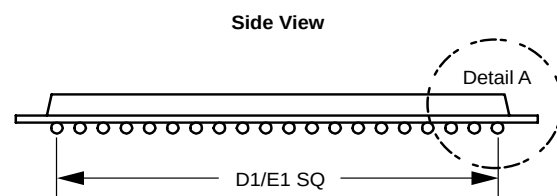
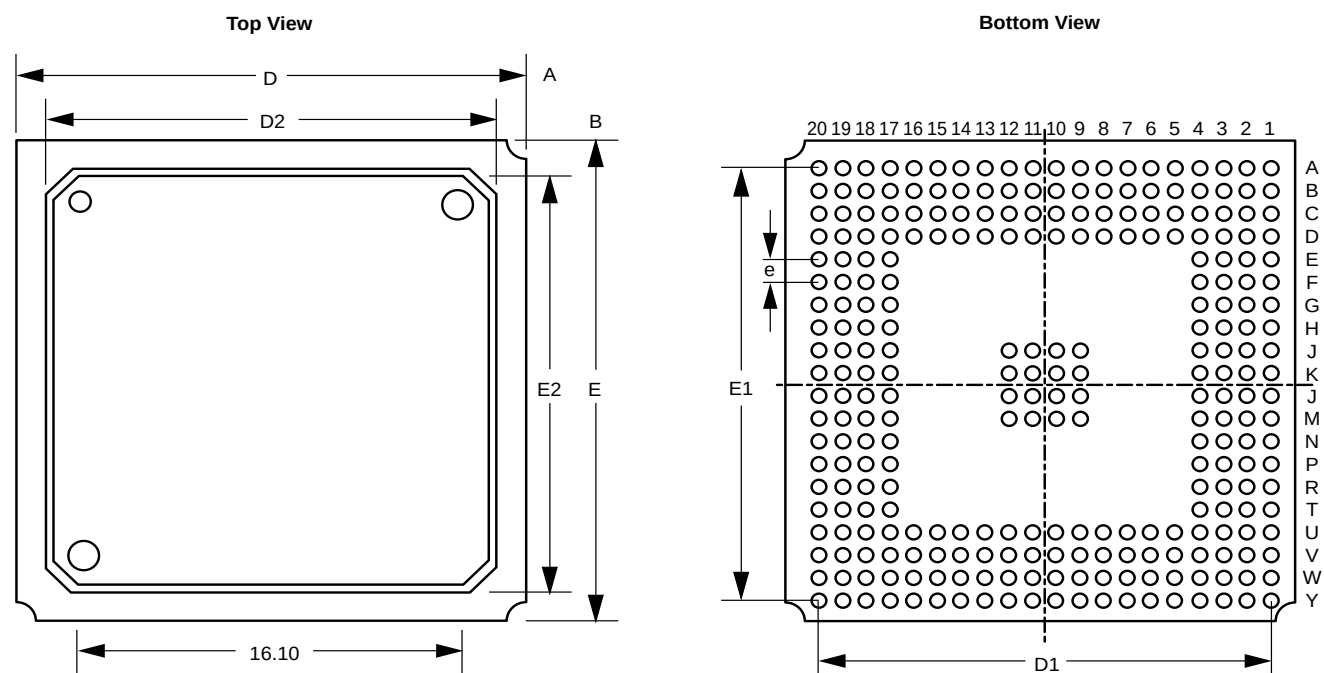
Jedec Equiv	PQFP 208		
Dimension	Min.	Nom.	Max.
A		3.70	4.10
A1	0.25	0.38	
A2	3.20	3.40	3.60
b	0.17		0.27
C	0.09		0.20
ccc			0.10
D/E	30.25	30.60	30.85
D1/E1	27.90	28.00	28.10
e	0.50 BSC		
L	0.50	0.60	0.75
Theta	0		7 deg.

Notes:

1. All dimensions are in millimeters.
2. BSC – Basic Spacing between Centers.

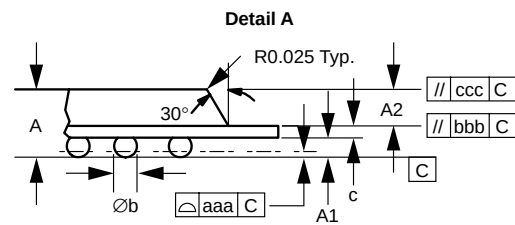
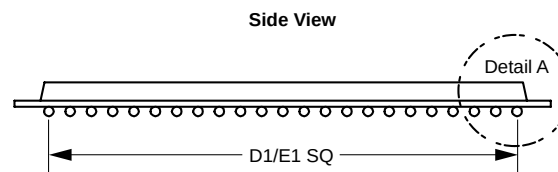
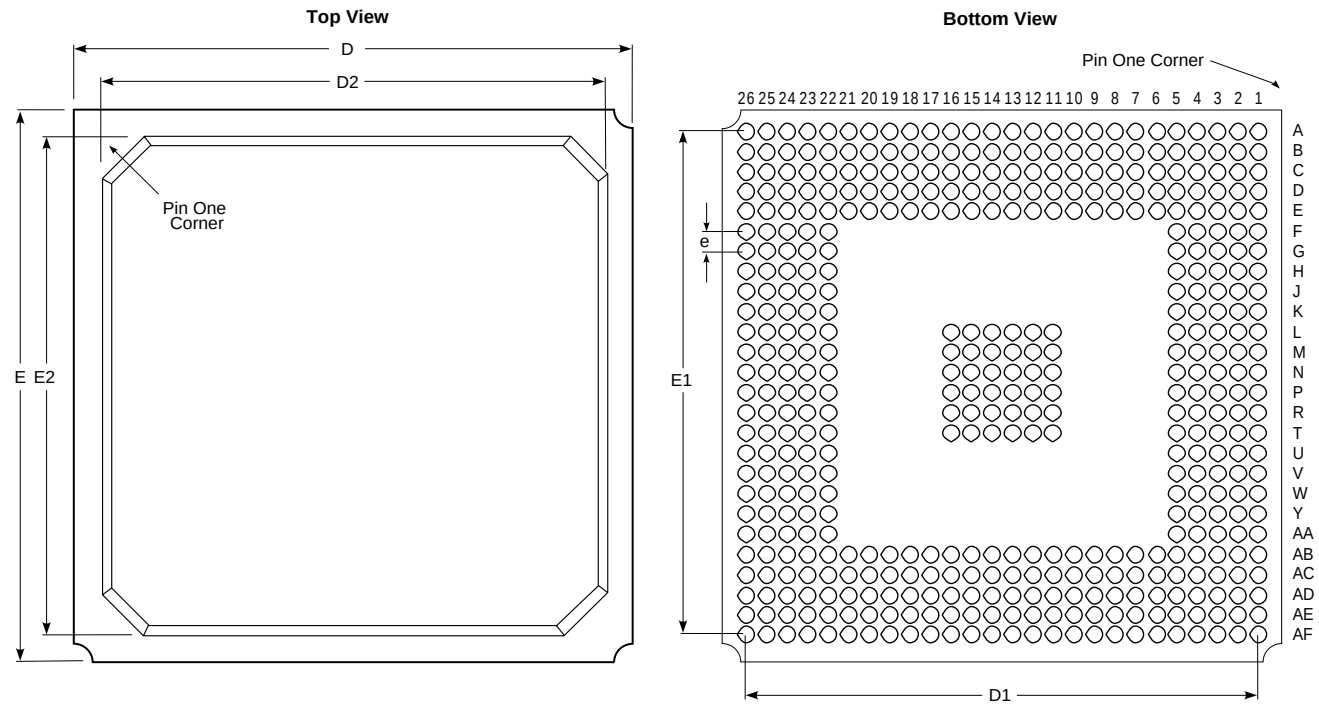
Package Mechanical Drawings (Continued)

272-Pin PBGA



Package Mechanical Drawings (Continued)

456-Pin PBGA



Plastic Ball Grid Array

JEDEC Equivalent	PBGA 272			PBGA 456		
Dimension	Min.	Nom.	Max.	Min.	Nom.	Max.
A	2.18	2.33	2.50	2.13	2.33	2.50
A1	0.50	0.60	0.70	0.50	0.60	0.70
A2	1.15	1.17	1.19	1.12	1.17	1.19
aaa			0.15			0.15
b	0.60	0.75	0.90	0.60	0.75	0.90
bbb			0.20			0.20
c	0.53	0.56	0.61	0.51	0.56	0.61
ccc			0.25			0.25
D	26.80	27.00	27.20	34.80	35.00	35.20
D1	24.13 BSC			31.75 BSC		
D2	23.90	24.00	24.10	29.80	30.00	30.20
E	26.80	27.00	27.20	34.80	35.00	35.20
E1	24.13 BSC			31.75 BSC		
E2	23.90	24.00	24.10	29.80	30.00	30.20
e	1.27 typ.			1.27 typ.		
Theta	30° typ.			30° typ.		

- Notes:
- 1. All dimensions are in millimeters
 - 2. BSC – Basic Spacing between Centers

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