SSI 32D531
Data Separator and Write Precompensation Device

May, 1989

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DESCRIPTION

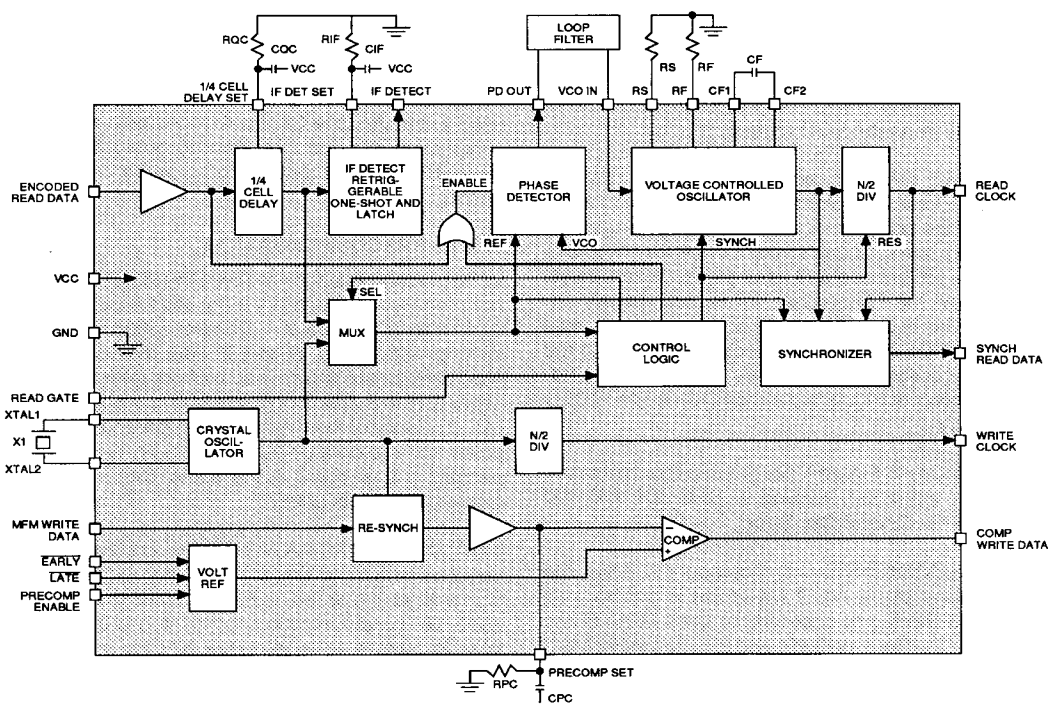
The SSI 32D531 Data Separator performs data synchronization and write precompensation of encoded data. The interface of the SSI 32D531 is optimum for use with Western Digital's WD1010/WD2010 controller family.

The SSI 32D531 contains a high performance Phase Locked Loop for read data synchronization, a crystal controlled reference oscillator for write data synchronization, and write precompensation circuitry. The SSI 32D531 employs an advanced bipolar technology which affords precise bit cell control without the need for external active components. The SSI 32D531 requires a single +5V power supply and is available in 24-pin DIP and 28-pin PLCC packages.

FEATURES

- **MFM & RLL Data Synchronization.**
- **Optimized for use with the WD1010/WD2010 controller family**
- **Fast acquisition Phase Locked Loop**
- **1F detection**
- **Write precompensation**
- **Write data resynchronized for reduced jitter**
- **No external delay line or varactor diode required**
- **Single +5V power supply**

BLOCK DIAGRAM



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FUNCTIONAL DESCRIPTION

DATA SYNCHRONIZATION

Read Data synchronization is accomplished with a high performance, fast acquisition Phase Locked Loop (PLL). The input from the disk drive, ENCODED READ DATA, is phase locked with the VCO clock. The synchronized Read Data and the VCO clock divided by two are made available for external data extraction at the SYNCH READ DATA and READ CLOCK pins, respectively.

The synchronized Read Data is synchronized in a jitter-free manner such that leading edge transitions occur at the center of READ CLOCK half cycles. This is accomplished by internally decoding and re-encoding using the READ CLOCK as a reference.

When READ GATE changes state, the VCO is stopped and restarted in phase with the PLL input which can be either the internal Crystal Oscillator or ENCODED READ DATA. In this manner the lock time is reduced due to small angles of phase error. Limiting the phase error by restarting the VCO in phase with the input prevents the PLL from locking to harmonics and short lock times are assured. The correct phase of READ CLOCK is also ensured by resetting the n/2 Divider at the same time as the VCO restart.

When READ GATE is high, the 1/4 CELL DELAY allows the Phase Detector to be enabled prior to when an edge of the encoded input is to occur. This updates the PLL on a sampled basis and corrects for any phase error with each subsequent input pulse. When READ GATE is low the Phase Detector is continuously enabled and the PLL is both phase and frequency locked to the reference oscillator. By locking the VCO to the reference oscillator it is virtually at the correct frequency when the PLL is switched to track ENCODED READ DATA.

The waveforms in Figure 1 are graphic representation of the PLL alternately locking to ENCODED READ DATA and the Crystal Oscillator.

With an ENCODED READ DATA input of 5 MHz, the final DC level of the VCO waveform is constant as shown with transients occurring at each edge of the READ GATE. The amplitude and duration of the VCO locking transient is dependent on the initial phase error on switching (max is 0.5 rad.) as well as the damping factor and natural frequency of the loop. The lower two waveforms in Figure 1 are an expansion of the ENCODED READ DATA and VCO IN signals showing the effect of disabling the VCO during reference switching and the subsequent stairstep characteristic of the VCO waveform as the PLL locks to the new input.

The synchronizer circuit separates the data and clock pulses using windows derived from the VCO output. The window edges are aligned with the opposite edge from that used to phase lock the VCO. Using a VCO running at twice the expected input frequency allows accurate centering of these windows about the expected bit positions.

1F DATA DETECTION

The SSI 32D531 provides a flag, 1F DETECT, that indicates a continuous stream of "1's" or "0's."

The period of the 1F Detect Retriggerable One-Shot is set so that the sum of the 1/4 Cell Delay and the One-Shot is nominally 1-1/4 time the 2F frequency data period. This results in the 1F DETECT output remaining high during a continuous high frequency input representing a field of "1's" and "0's." External components R1F and C1F at the 1F DETECT SET pin are used to set the One-Shot delay. A Latch operates in conjunction with the One-Shot to guarantee a minimum 1F DETECT output pulse width of one data period.

WRITE PRECOMPENSATION

Write precompensation reduces the effect of intersymbol interference caused by magnetic transition proximity in the disk medial. Compensation consists of shifting written data pulses in time to counteract the read back bit shifting caused by such interaction. The severity of the intersymbol interference is a function of radial velocity of the media, the magnitude of the write pulse and the data pattern. Typically, write precompensation is enabled at the same time as the write current level is reduced.

The COMP WRITE DATA output is a re-synchronized version of the MFM WRITE DATA input that has been time shifted, if needed, to reduce intersymbol interference. Re-synchronization, to the internal crystal oscillator, is performed to minimize bit jitter in the output waveform. The magnitude of the time shift, TC, is

determined by the RC network at the PRECOMP SET pin and is applied as noted in Table 1 according to the states of $\overline{EARLY}$, $\overline{LATE}$ and PRECOMP ENABLE. Figure 2 is a further illustration of these timing relationships.

TABLE 1: Write Precompensation Truth Table

PRECOMP ENABLE	EARLY	LATE	DELAY
0	X	X	Constant
1	0	0	Illegal State
1	0	1	TN-TC
1	1	0	TN + TC
1	1	1	TN

TN = Nominal Pulse Delay
TC = Magnitude of Time Shift

REFERENCE OSCILLATOR

The crystal controlled oscillator serves as the system master clock for the write functions. Its frequency divided by two provides a WRITE CLOCK for an external MFM encoder. It is also used to re-synchronize the MFM WRITE DATA for precise timing control when writing data to the disk. A series resonant crystal should be used.

Additionally, the oscillator output is used as a standby reference for the PLL when READ GATE is low. This enables the PLL to lock rapidly to incoming data when required.

When an external system clock, is available it may be connected to XTAL1, and XTAL2 should be left open.

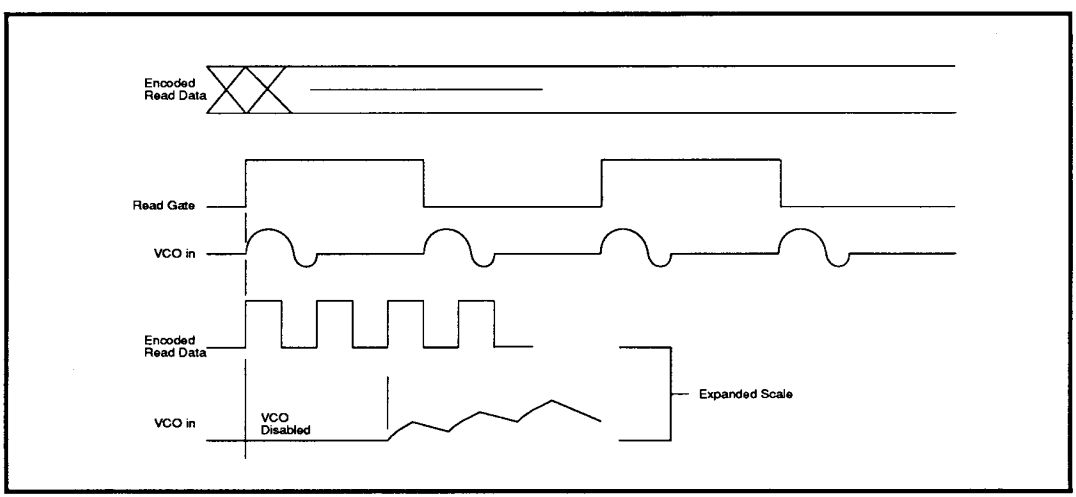


FIGURE 1 : Encoded Read Data Waveforms

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
MFM WRITE DATA	I	Write data to be resynchronized and precompensated. Synchronous with WRITE CLOCK.
PRECOMP ENABLE	I	Enables precompensation to be controlled by -EARLY or –LATE.
EARLY	I	When low causes the MFM WRITE DATA pulses to be written late.
ENCODED READ DATA	I	MFM encoded read data pulses from the read amplifier circuits.
READ GATE	I	Selects the reference input to the PLL. Selects ENCODED READ DATA when high, crystal oscillator when low.
VCC	I	+5V
GND	I	Power and signal ground connection.
WRITE CLOCK	O	Crystal-controlled reference oscillator frequency divided by two. Used by the controller to generate MFM WRITE DATA.
COMP WRITE DATA	O	Re-synchronized and precompensated write data.
READ CLOCK	O	Voltage-controlled oscillator output divided by two. SYNC READ DATA is synchronized to this signal.
SYNC READ DATA	O	Synchronized read data output. Leading-edge transitions occur at center of READ CLOCK half cycles.
1F DETECT	O	Flag used to locate strings of MFM-encoded 1's or 0's in the ENCODED READ DATA input.
XTAL1, XTAL2	I/O	Connections for oscillator crystal. If oscillator is not required, XTAL1 may be driven by TTL logic signal at twice the data rate and XTAL2 left open.
PRECOMP SET	I/O	Pin for R-C network to control write precompensation early and late times
1F DETECT SET	I/O	Pin for R-C network to control the 1F detect period. Component values are dependent on the minimum data period that will keep 1F DETECT high.
1/4 CELL DELAY SET	I/O	Pin for R-C network to control the 1/4 CELL DELAY. This allows the Phase Detector to be enabled 1/4 of the data period prior to receiving an MFM data input.
CF1,CF2	I/O	Pins for the capacitor used in conjunction with RF and RS to set the VCO center frequency.
RF, RS	I/O	Pin for resistors used in conjunction with capacitor to set the VCO center frequency.
PD OUT	I/O	Output of phase detector, input to loop filter.
VCO IN	I/O	Control input of the VCO, for connection of the loop filter output.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Operation above absolute maximum ratings may permanently damage the device.

PARAMETER	RATING	UNIT
Storage Temperature	-65 to +150	°C
Ambient Operating Temperature, TA	0 to +70	°C
Junction Operating Temperature	0 to +130	°C
Supply Voltage, VCC	-0.5 to +7.0	Vdc
Voltage Applied to Logic Inputs	-0.5 Vdc to VCC +0.5	Vdc
Maximum Power Dissipation	800	mW

DC CHARACTERISTICS

Unless otherwise specified 4.75 < VCC < 5.25V, Ta = 0 to 50 °C, RPC = 3.3K, CPC = 24 pF, R1F = 16K, C1F = 120 pF, RQC = 8.2K, CQC = 56 pF, RF = 499, RS = 499, CF = 56 pF, and X1 = 8 MHz to 10.5 MHz crystal conforming to military type HC19A/U.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
High Level Input Voltage, VIH		2.0			V
Low Level Input Voltage, VIL				0.8	V
High Level Input Current, IIH	VIH = 2.7V			20	µA
Low Level Input Current IIL	VIL = 0.4V			-0.36	mA
High Level Output Voltage, VOH					
Comp Write Data	IOH = -400 µA	2.7			V
All Others	IOH = -50 µA	4.6			V
Low Level Output Voltage, VOL					
Comp Write Data	IOL = 4 mA			0.4	V
All Others	IOL = 1 mA			0.4	
Power Supply Current, Icc	All Outputs Open			100	mA

DATA DETECTION CHARACTERISTICS (SEE FIGURE 1)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
ENCODED READ DATA Pulse Width, TERD		10		$\frac{TRCF}{2}+10$	ns
ENCODED READ DATA Positive Transition Time, TERDPT	0.8V to 2.0V, CL = 15 pF			20	ns
READ CLOCK Repetition Period Range, TRCF		0.85 TWCF		1.15 TWCF	ns

DATA DETECTION CHARACTERISTICS (SEE FIGURE 1)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
READ CLOCK Pulse Width, TRC		$\frac{TRCF}{2}$ -1		$\frac{TRCF}{2}$ +7	ns
READ CLOCK Positive Transition Time, TRCPT	0.9V to 4.2V, CL = 15 pF			15	ns
READ CLOCK Negative Transition Time, TRCNT	4.2V to 0.9V, CL = 15 pF			10	ns
SYNC READ DATA TSRDD1		0		TRCF -20	ns
Delay TSRDD2		0		TRCF-TRC -20	ns
SYNC READ DATA Pulse width, TSRD1,2		19		$\frac{TRCF}{2}$	ns
SYNC READ DATA Positive Transition Time, TSRDPT	0.9V to 4.2V, CL = 15 pF			15	ns
1F DETECT Delay T1FD Accuracy	TD = 0.086 (RIF) (CIF + 7pF) +TQC,C1F = 100 pF to 180 pF	0.9TD		1.1TD	sec
1/4 CELL DELAY, TQC Accuracy	TDQ = 0.095 (RQC)(CQC + 7pF) CQC = 43 pF to 82 pF	0.85 TDQ		1.15 TDQ	sec
PHASE LOCKED LOOP CHARACTERISTICS					
VCO Period Accuracy, TVCO	Oscillator period, TO = 1.7(RF + RS) CF, CF = 20 pF to 82 pF, RF = RS = 499Ω	0.9TO		1.1TO	sec
VCO Frequency Range	VCO IN = 0.85V to Vcc -0.85V, Vcc = 5.0V	±20		±30	%
Phase Detector Gain, KD	w/respect to 5 Mbit/sec data rate, Vcc = 5.0V	30		45	µA/rad
VCO Control Gain, KVCO	Wo = Vco radian center frequency V=VCO IN voltage change VCO IN = 0.85V to Vcc -0.85V	$\frac{0.12Wo}{V}$		$\frac{0.18Wo}{V}$	rad/ (sec.V)
VCO Phase Preset Error				±0.5	rad
Data Detection Window Centering Accuracy		±0.02 TRCF ±4			ns
Number of Read Clock Period Delay From ENC RD DATA Input to SYNC RD DATA Output				2	
Number of READ CLOCK periods that VCO may be disabled during reference switching				3	

WRITE PRECOMPENSATION SWITCHING CHARACTERISTICS (SEE FIGURE 2)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
WRITE CLOCK Repetition Period, TWCF	Controlled by X1 Freq.	190		250	ns
WRITE CLOCK Pulse, Width, TWC		$\frac{TWCF}{2} - 15$		$\frac{TWCF}{2} + 10$	ns
WRITE CLOCK Positive Transition Time, TWCPT	0.9V to 4.2V, CL = 15 pF			15	ns
WRITE CLOCK Negative Transition Time, TWCNT	4.2V to 0.9V, CL = 15 pF			10	ns
MFM WRITE DATA Set Up Time, TWDS1,2		15			ns
MFM WRITE DATA Hold Time, TWDH1,2		10			ns
MFM WRITE DATA Release Time, TWDR1, 2		15			ns
$\overline{EARLY}$ or $\overline{LATE}$ Set Up Time TELS1,2		125			ns
$\overline{EARLY}$ or $\overline{LATE}$ Hold Time TELH1,2		10			ns
COMPENSATED WRITE DATA, Pulse Width, TCWD	CL = 15 pF	40		$\frac{TWCF}{2}$	ns
COMPENSATED WRITE DATA "Nom" Pulse Width Delay, TN				$\frac{TWCF}{2}$	ns
COMPENSATION WRITE DATA Compensation Accuracy, TE, TL	TC = 0.15 (RCP) (CPC) CPC = 15 pF to 36 pF	0.8TC		1.2TC	sec
COMPENSATED WRITE DATA Positive Transition Time, TCWDPT	0.8V to 2.0V, CL = 15 pF			10	ns

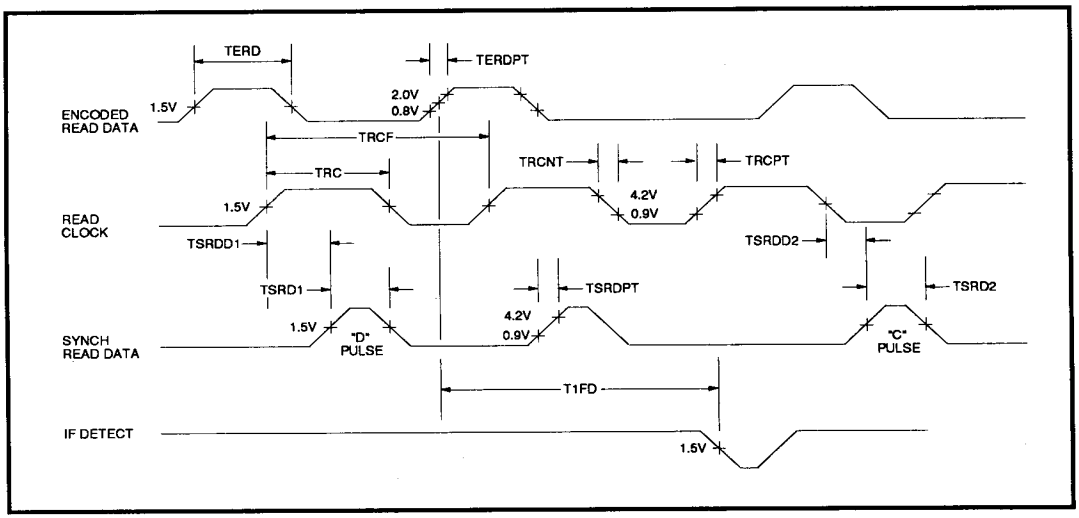


FIGURE 2: Data Detection and Synchronizing Waveforms

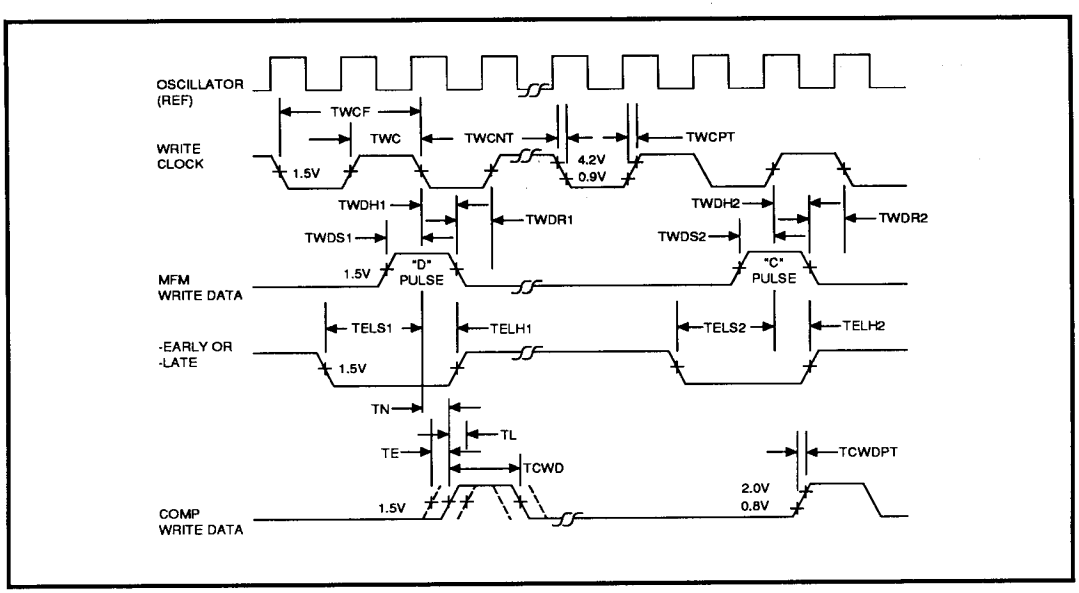


FIGURE 3: Write Precompensation Waveforms

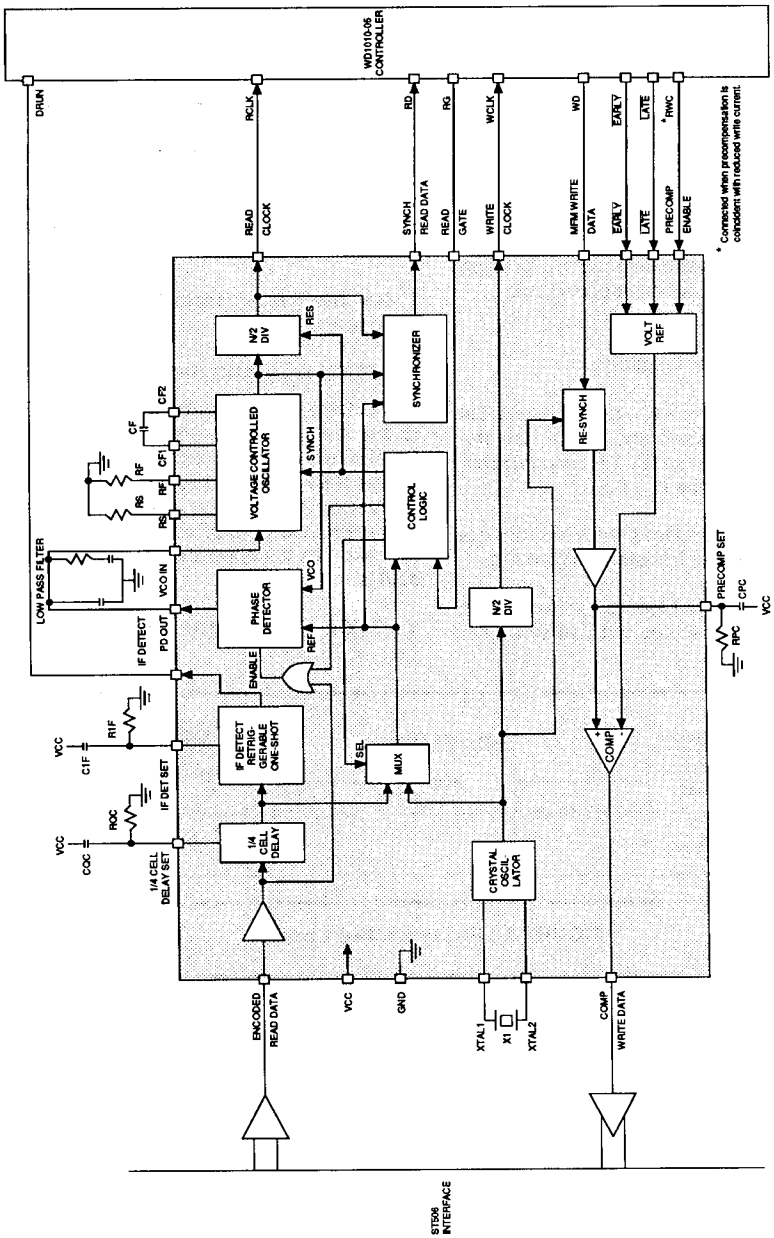


FIGURE 4: Typical System Connections

Application Information

In a typical application the SSI 32D531 is used with a Western Digital WD1010-05 Winchester Disk Controller as shown in Figure 4. Interface to the disk drive consists of the Read data input signal from the drive and the Write data output signal from the SSI 32D531. All the other connections are with the WD1010 and external components.

LOOP FILTER

The low pass filter serves several purposes, it attenuates high frequency components of the phase error signal from the phase detector and modifies the dynamics of the PLL. In lock mode, the PLL can be approximated by the linear model shown in Figure 5.

Standard linear system analysis methods can then be used for analysis. The transfer functions of each of the blocks are as follows:
KD = conversion factor for phase detector in μA/radian
KVCO = VCO gain factor in radians/second volt
F(s) = Low pass filter transfer function

Thus the closed loop transfer function is

$$H(s) = \frac{\frac{KDKVCO}{N} F(s)}{S + \frac{KDKVCO}{N} F(s)}$$

where N = ratio between 5M bit/sec and f_{in} (i.e. for preamble N = 1,for crystal reference N = 0.5)

The transient performance and frequency response is highly dependent on the filter transfer function F(s).

To obtain a zero phase error, a type 2 or higher system must be used. This necessitates the use of a filter transfer function with at least one pole at the origin to obtain two poles at the loop gain origin. A detailed analysis supporting this choice can be found in Phase-lock Techniques by Gardner[1]. The filter shown in Figure 6 can be used which will give independent control of the damping factor and natural frequency of the closed loop function. Proper choice of capacitors C1 and C2 will effect loop settling time and stability. More complex filters can be used that give finer control over loop parameters and enhance performance even further.

1. Gardner F.M. Phaselock Techniques, Wiley N.Y., Second Ed., 1967

Vco FREE RUNNING FREQUENCY

The external components RF, RS and CF, are chosen to set the VCO frequency at twice the ENCODED READ DATA bit rate. For a symmetrical window, equal values of RF and RS are used. Increasing the ratio RF/RS causes the detection window to occur earlier in time with respect to ENCODED READ DATA. Decreasing the ratio has the opposite effect, the value of the time shift is:

T = TVCO (RF - RS)/(RF + RS)

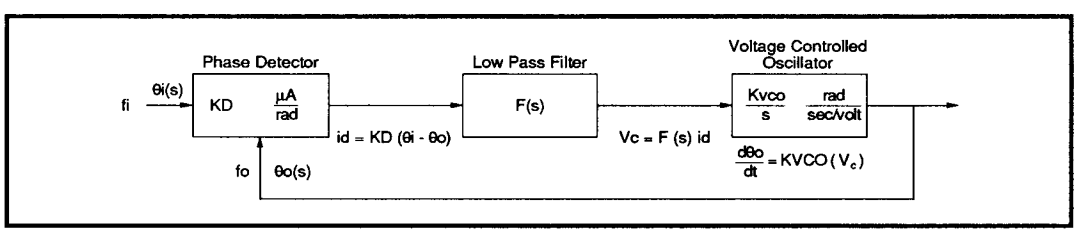


FIGURE 5 : Phase Locked Loop

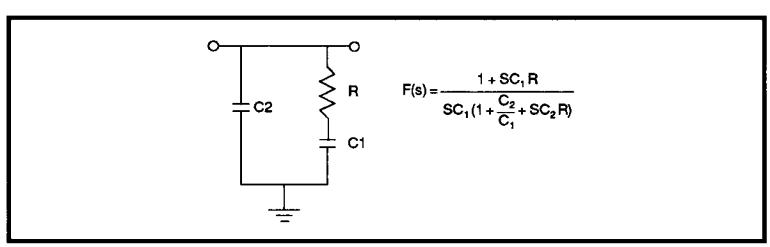
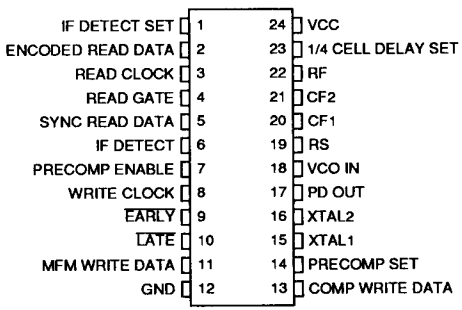


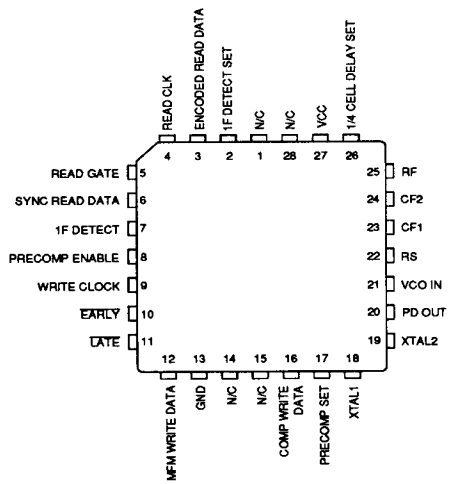
FIGURE 6 : Loop Filter Example

PACKAGE PIN DESIGNATIONS
(TOP VIEW)

CAUTION: Use handling procedures necessary for a static sensitive component.



24-Lead PDIP



28-Lead PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32D531		
24-Pin PDIP	32D531-CP	32D531-CP
28-Pin PLCC	32D531-CH	32D531-CH

