

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R106-94	94-01-20	M. L. Poelking
B	Changes in accordance with NOR 5962-R044-95	94-12-27	M. L. Poelking
C	Add device types 04, 05, and 06. Update boilerplate.	97-04-17	M. L. Poelking

REV																													
SHEET																													
REV	C	C	C	C	C	C	C	C	C																				
SHEET	15	16	17	18	19	20	21	22	23																				
REV STATUS OF SHEETS				REV			C	C	C	C	C	C	C	C	C	C	C	C	C	C									
				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14									
PMIC N/A				PREPARED BY Greg A. Pitz						DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216																			
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A				CHECKED BY Charles Reusing																									
				APPROVED BY Michael A Frye																									
				DRAWING APPROVAL DATE 12 September 1988																									
				REVISION LEVEL C																									
				SIZE A		CAGE CODE 67268		5962-87686																					
				SHEET 1 OF 23																									

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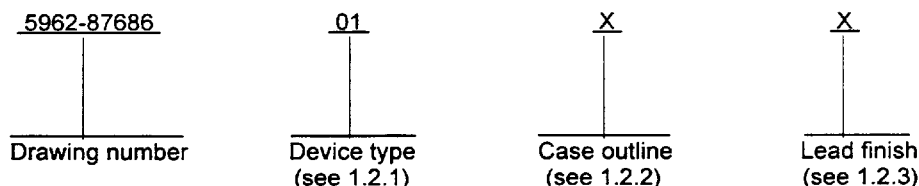
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DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited..

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	7C517-42, 7217L-40	16 X 16 multiplier
02	7C517-55, 7217L-55	16 X 16 multiplier
03	7C517-75, 7217L-75	16 X 16 multiplier
04	7C517-25, 7217L-25	16 X 16 multiplier
05	7C517-30, 7217L-30	16 X 16 multiplier
06	7C517-40, 7217L-40	16 X 16 multiplier

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
U	See figure 1	64	quad flat package
X	CDIP1-T64	64	dual-in-line package
Y	CQCC1-N68	68	square chip carrier package
Z	CMGA15-PN	68	pin grid array
T	CMGA3-PN	68	pin grid array

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/

Supply voltage range -----	-0.5 V dc to +7.0 V dc
DC voltage applied to outputs -----	-0.5 V dc to +7.0 V dc
DC input voltage -----	-0.5 V dc to +7.0 V dc
DC output current -----	10 mA
Maximum power dissipation 2/ -----	1.2 W
Lead temperature (soldering, 10 seconds) ----	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases X, Y, Z, and T -----	See MIL-STD-1835
Case U -----	30°C CW 3/
Junction temperature (T_J) -----	+175°C
Storage temperature range -----	-65°C to +150°C

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1.4 Recommended operating conditions.

Supply voltage (V_{CC})	-----	+4.5 V dc to +5.5 V dc
Ground voltage (GND)	-----	0 V dc
Input high voltage (V_{IH})	-----	2.0 V dc to 6.0 V dc
Input low voltage (V_{IL})	-----	-0.5 V dc to +0.8 V dc
Case operating temperature range (T_C)	-----	-55° C to +125° C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

MIL-STD-973 - Configuration Management.

MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- 2/ Must withstand the added P_D due to short-circuit test, e. g., I_{OS} .
- 3/ When a thermal resistance value is included in MIL-STD-1835, it shall supersede the value stated herein.

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Input-output data format. The input-output data format shall be as specified on figure 3.

3.2.4 Block diagram. The block diagram shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output high voltage	V_{OH}	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -0.4\text{ mA}$	1, 2, 3	All	2.4		V
Output low voltage	V_{OL}	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 4.0\text{ mA}$	1, 2, 3	All		0.4	V
Input high voltage	V_{IH}		1, 2, 3	All	2.0		V
Input low voltage	V_{IL}		1, 2, 3	All		0.8	V
Input leakage current	I_{IX}	$V_{CC} = 5.5\text{ V}$ $GND \leq V_{IN} \leq V_{CC}$	1, 2, 3	All	-10	+10	μA
Output leakage current	I_{OZ}	$V_{CC} = 5.5\text{ V}$ $OE = 2.0\text{ V}$	1, 2, 3	All	-25	+25	μA
Output short-circuit current 2/	I_{OS}	$V_{CC} = 5.5\text{ V}$, $V_{OUT} = GND$	1, 2, 3	All		-110	mA
Supply current (quiescent) 3/	I_{CC1}	$V_{CC} = 5.5\text{ V}$, $V_{IH} \leq V_{IN} \leq V_{CC}$ or GND $\leq V_{IN} \leq V_{IL}$, $OE = \text{high}$	1, 2, 3	All		50	mA
Supply current (quiescent) 3/	I_{CC2}	$V_{CC} = 5.5\text{ V}$ $V_{CC} - 0.2 \leq V_{IN} \leq V_{CC}$ or $GND \leq V_{IN} \leq 0.2\text{ V}$, $OE = \text{high}$	1, 2, 3	All		25	mA
Dynamic supply current 3/	I_{CC3}	$V_{CC} = 5.5\text{ V}$, $f_{CLK} = 10$ MHz, $OE = \text{high}$ $V_{IN} = 0$ to 3.0 V	1, 2, 3	All		110	mA
Input capacitance	C_{IN}	$f = 1.0\text{ MHz}$ $T_C = +25^{\circ}\text{C}$ $V_{CC} = 5.0\text{ V}$ See 4.3.1c	$V_{IN} = 0\text{ V}$ 4	All		10	pF
Output capacitance	C_{OUT}		$V_{OUT} = 0\text{ V}$ 4	All		12	pF
Functional testing		See 4.3.1d	7, 8	All			
Unlocked multiply time	t_{MUC}	See figure 5	9, 10, 11	01 02 03 04 05 06		65 75 100 38 43 60	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics. Continued

Test	Symbol	Conditions 1/ -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Clocked multiply time	t _{MC}	See figure 5	9, 10, 11	01 02 03 04 05 06		42 55 75 25 30 40	ns
Setup time X _i , Y _i , RND, TCX, TCY	t _S		9, 10, 11	01 02 03 04,05 06	15 20 25 12 15		ns
Hold time X _i , Y _i , RND, TCX, TCY	t _H		9, 10, 11	01,02 03,06	3		ns
				04,05	2		
Clock pulse width (high, low)	t _{PWH} , t _{PWL}		9, 10, 11	01,06 02 03 04,05	15 25 30 10		ns
MSPSEL to product out	t _{PDSEL}		9, 10, 11	01,06 02 03 04,05		25 30 35 20	ns
Output clock to P	t _{PDP}		9, 10, 11	01,02 03 04,05 06		30 35 20 25	ns
Output clock to Y	t _{PDY}		9, 10, 11	01,02 03 04,05 06		30 40 20 25	ns
OEP, OEL disable time	t _{PHZ} , t _{PLZ}		9, 10, 11	01,06 02 03 04,05		25 31 36 22	ns
OEP, OEL enable time	t _{PZH} , t _{PZL}		9, 10, 11	01,06 02 03 04,05		25 30 40 22	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics. Continued

Test	Symbol	Conditions 1/ $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Clock enable setup time $\overline{\text{ENX}}, \overline{\text{ENY}}, \overline{\text{ENP}}$	t_{SE}	See figure 5	9, 10, 11	01 02 03 04,05 06	16 20 25 12 15		ns
Clock enable hold time $\overline{\text{ENX}}, \overline{\text{ENY}}, \overline{\text{ENP}}$	t_{HE}			01,02 03,06	3		
				04,05	2		

1/ Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V and output loading of the specified $I_{\text{OL}}/I_{\text{OH}}$ and 40 pF load capacitance.

2/ For test-purposes, not more than one output should be tested at a time. Duration of the short-circuit should not be more than one second.

3/ Two quiescent figures are given for different input voltage ranges. To calculate I_{CC} at any given clock frequency, use $30 \text{ mA} + I_{\text{CC}}(\text{ac})$, where $I_{\text{CC}}(\text{ac}) = (8 \text{ mA/MHz}) \times \text{clock frequency}$.

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Case U

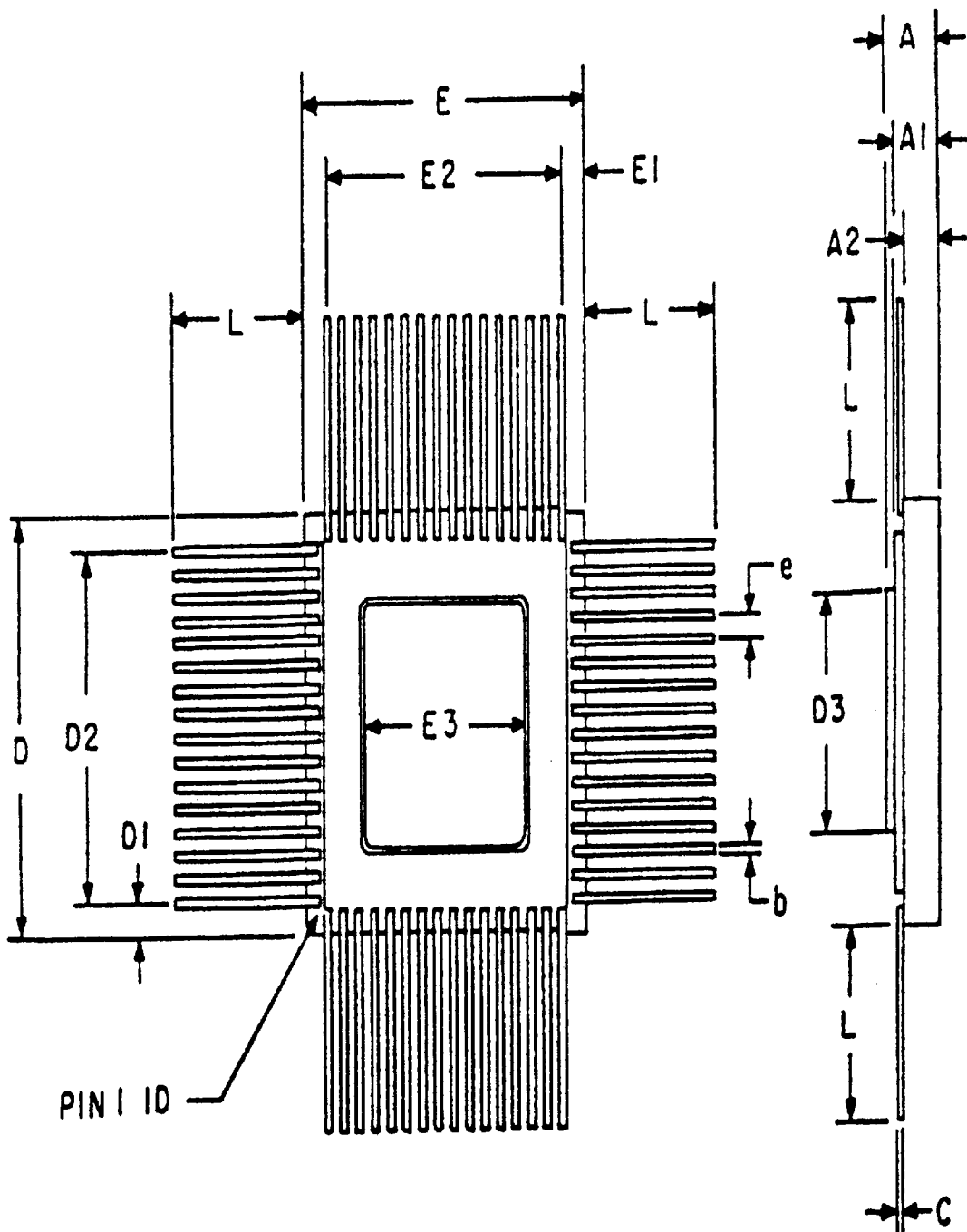


FIGURE 1. Case outline.

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Case U				
Dimensions	Millimeters		Inches	
	Min	Max	Min	Max
A	.1778	.2286	.070	.090
A1	.1524	.19812	.060	.078
A2	.0762	.1143	.030	.045
b	.04064	.0508	.016	.020
C	.02286	.03048	.009	.012
D	2.2479	2.3241	.885	.915
D1	.1905 REF		.075 REF	
D2	1.905 BSC		.750 BSC	
D3	1.2827	1.3589	.505	.535
e	0.127 BSC		.050 BSC	
E	2.2479	2.3241	.885	.915
E1	.1905 REF		.075 REF	
E2	1.905 BSC		.750 BSC	
E3	1.2827	1.3589	.505	.535
L	.889	1.143	.350	.450
ND	40.64		16	
NE	40.64		16	

NOTES:

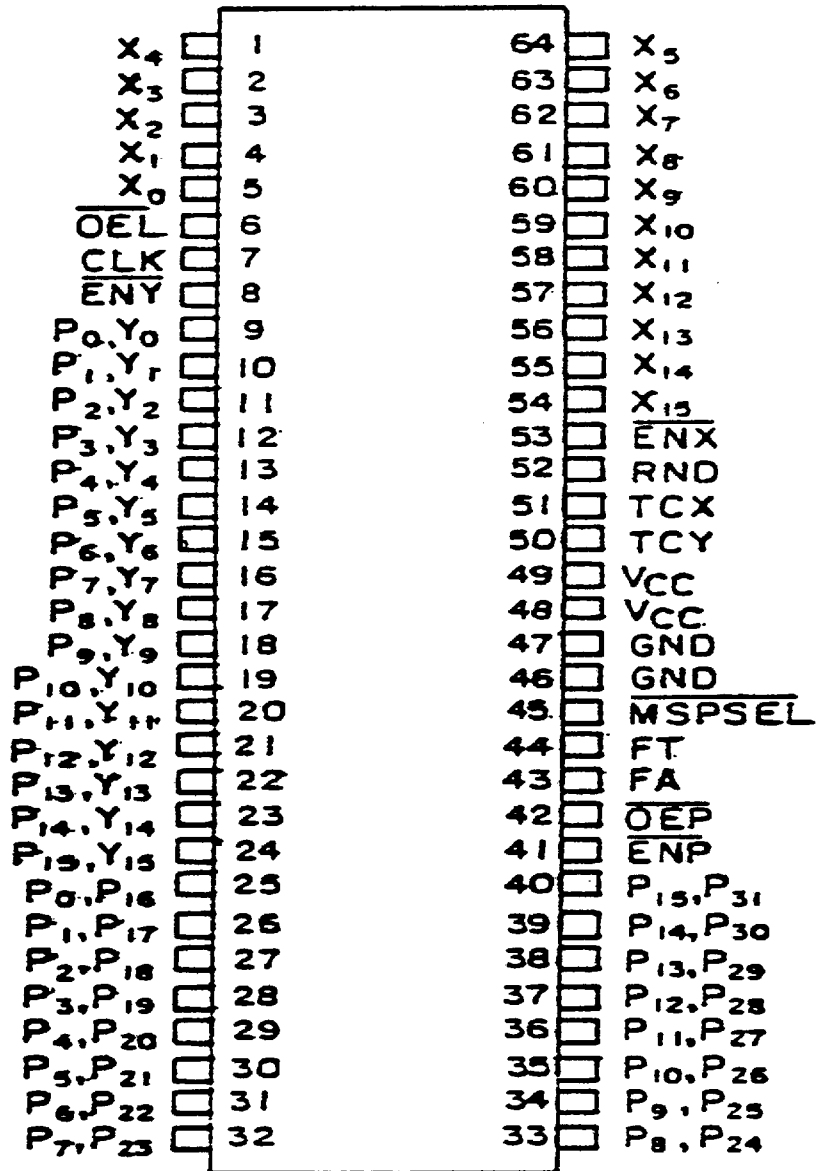
1. The preferred unit of measurement is millimeters. However, this item was designed using inch-pound units of measurements. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Lead number 1 is identified by a tab located on the lead.
3. Lead numbers are shown for reference only and do not appear on package.
4. BSC - Basic pin spacing between centers.

FIGURE 1. Case outline. - Continued

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TOP VIEW

FIGURE 2. Terminal connections

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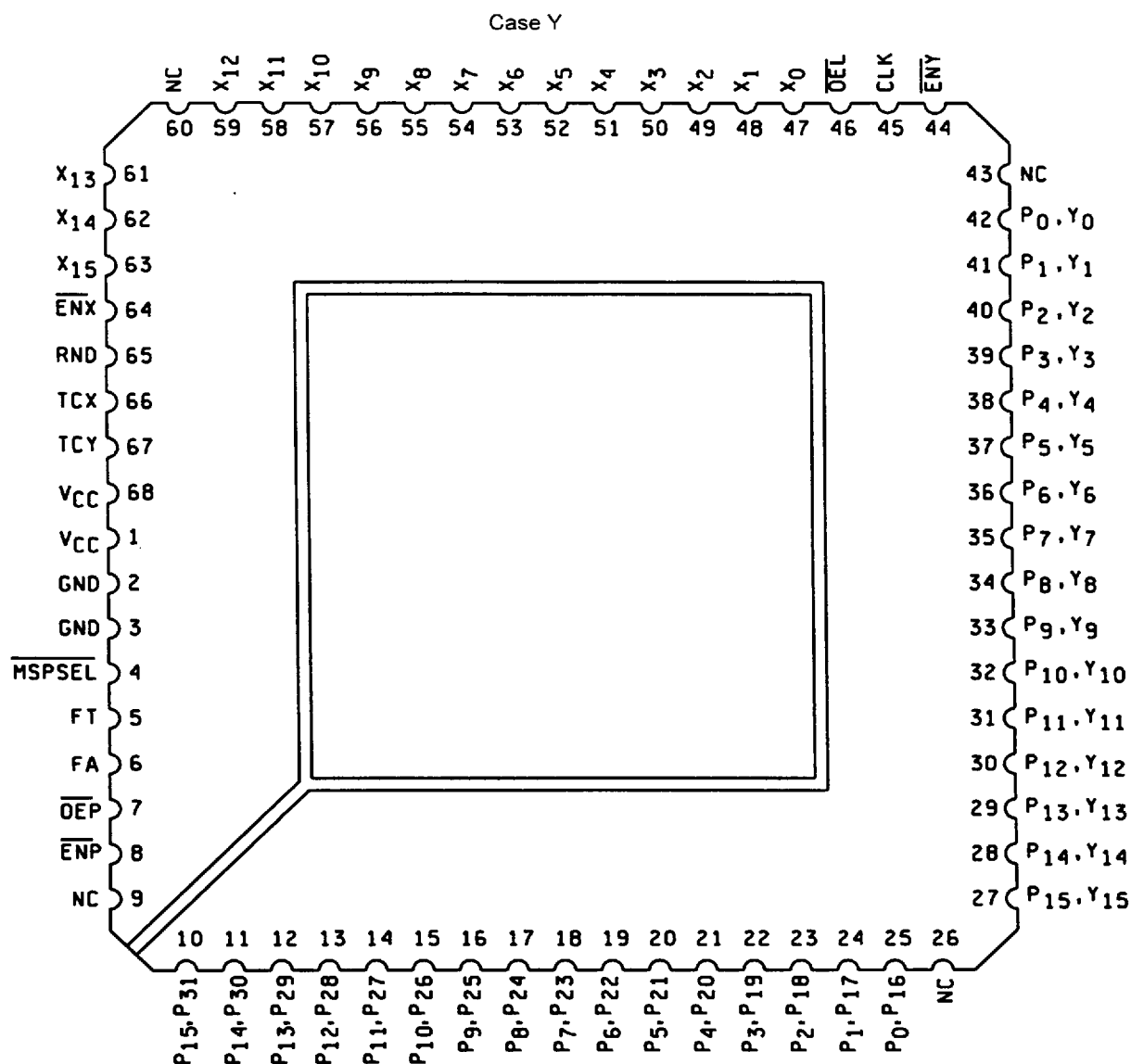


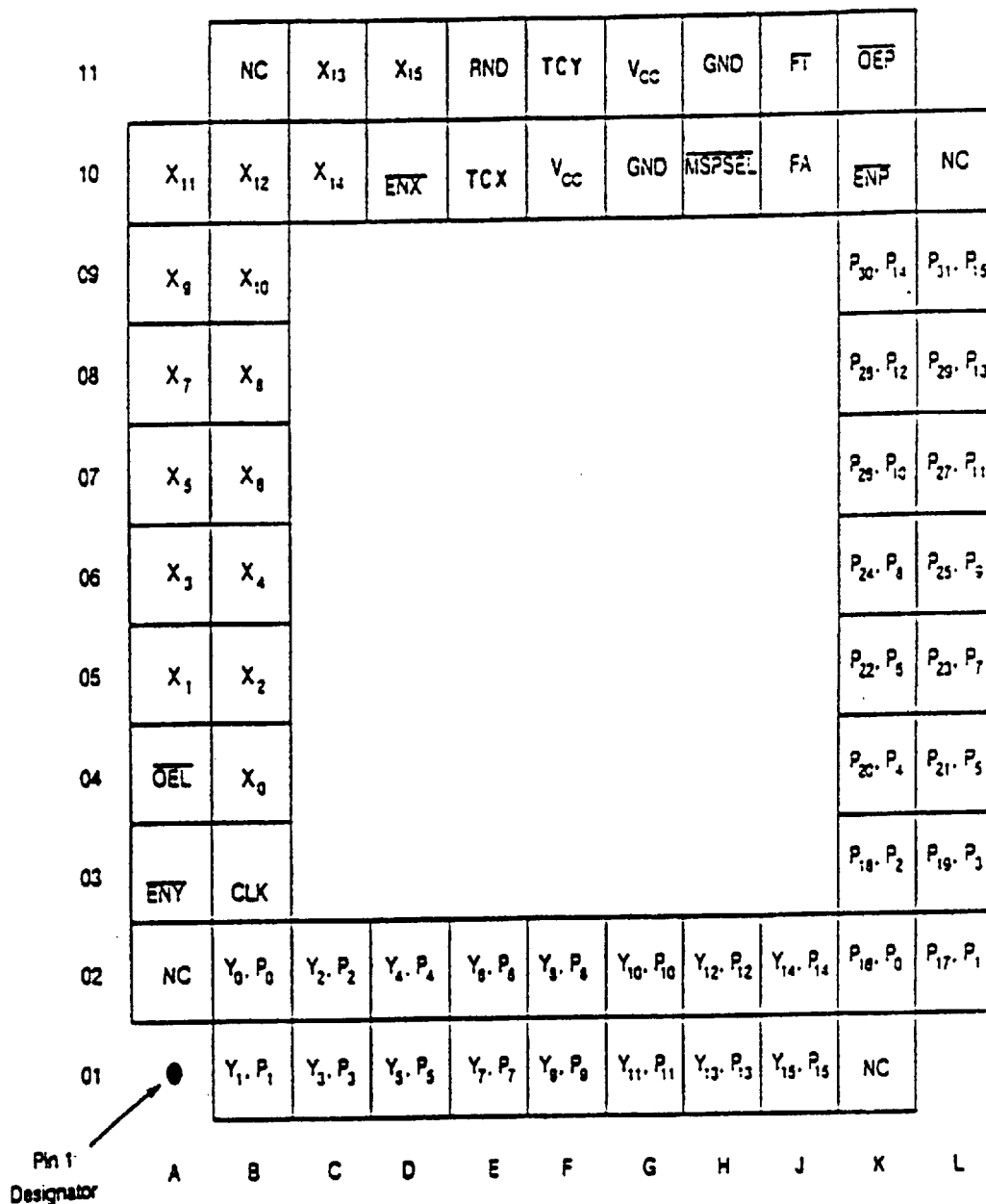
FIGURE 2. Terminal connections. - Continued

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Cases Z and T



TOP VIEW

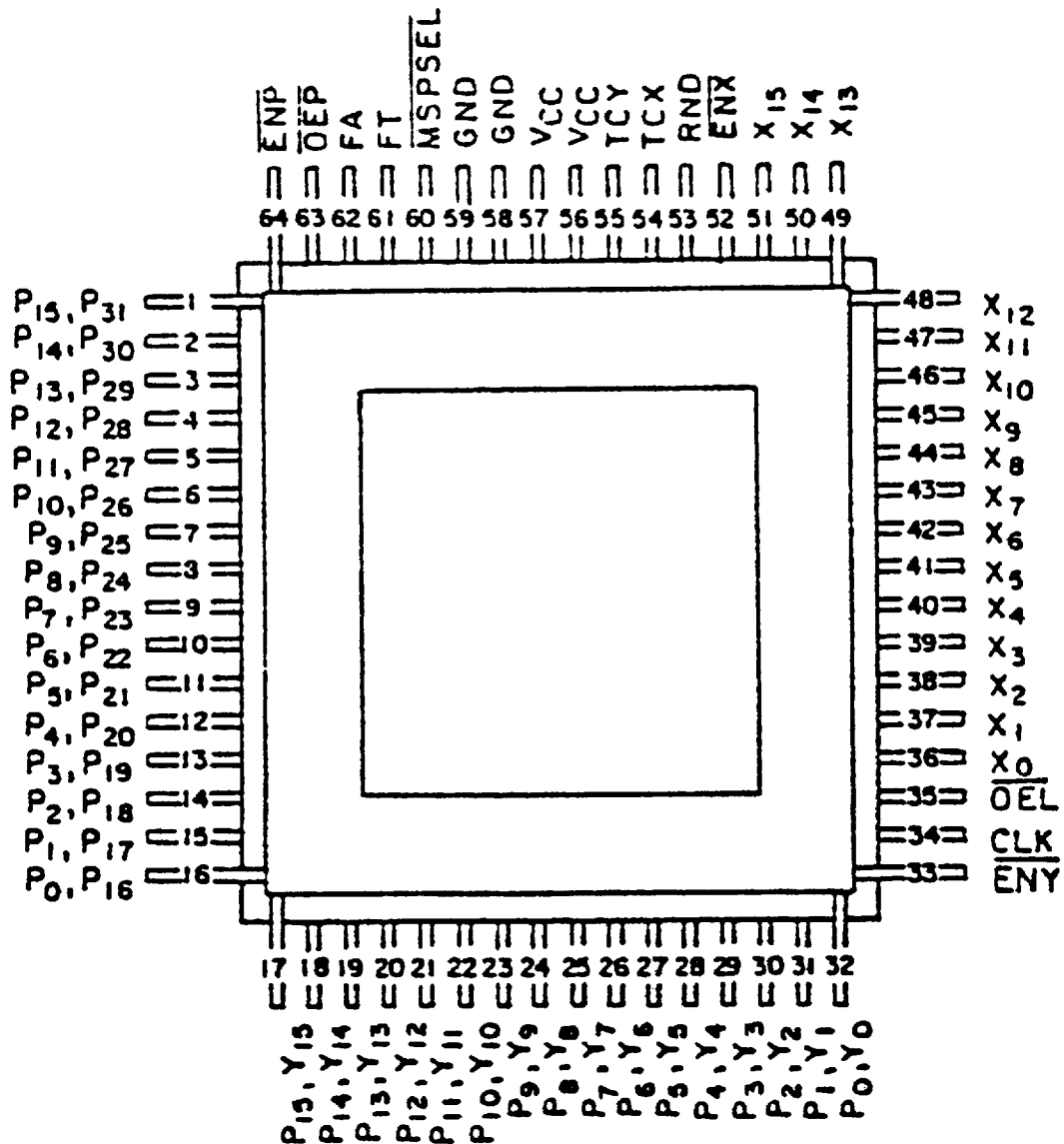
FIGURE 2. Terminal connections. - Continued

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Case U



(TOP VIEW)

FIGURE 2. Terminal connections. - Continued

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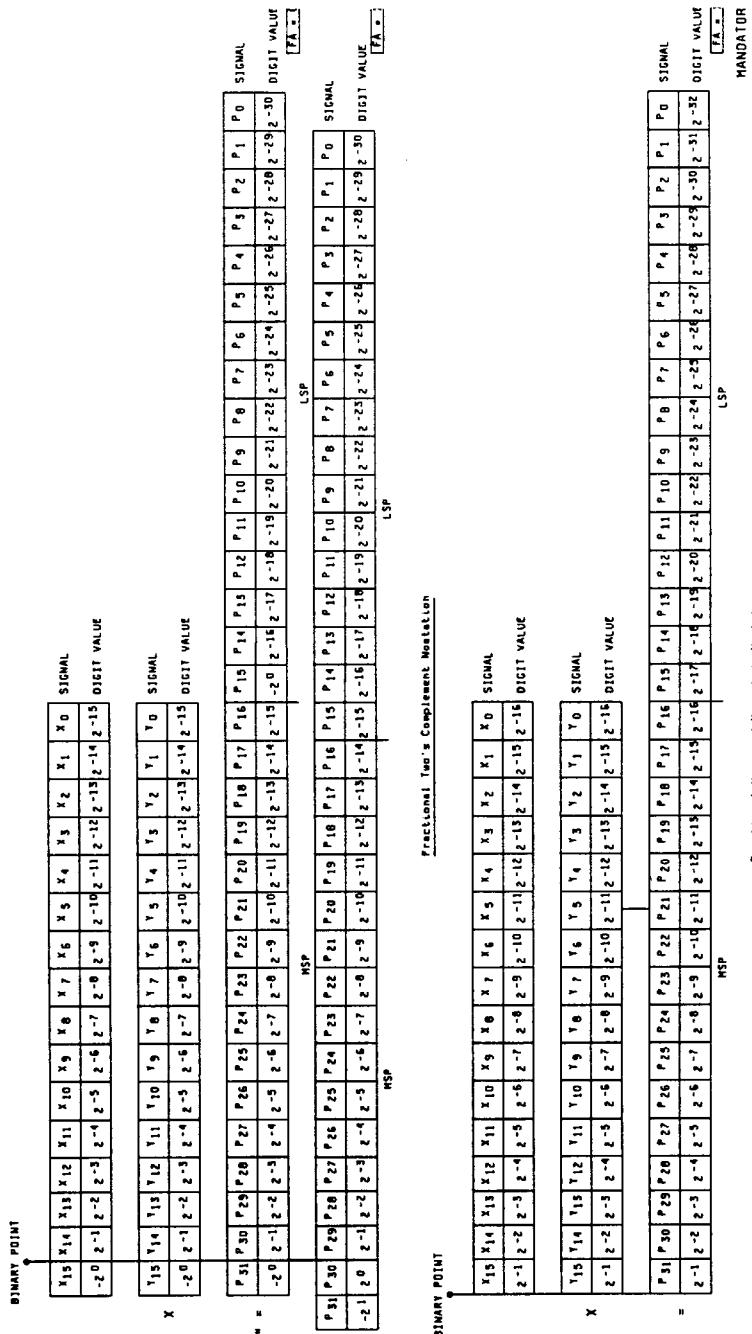


FIGURE 3. Input/output data formats

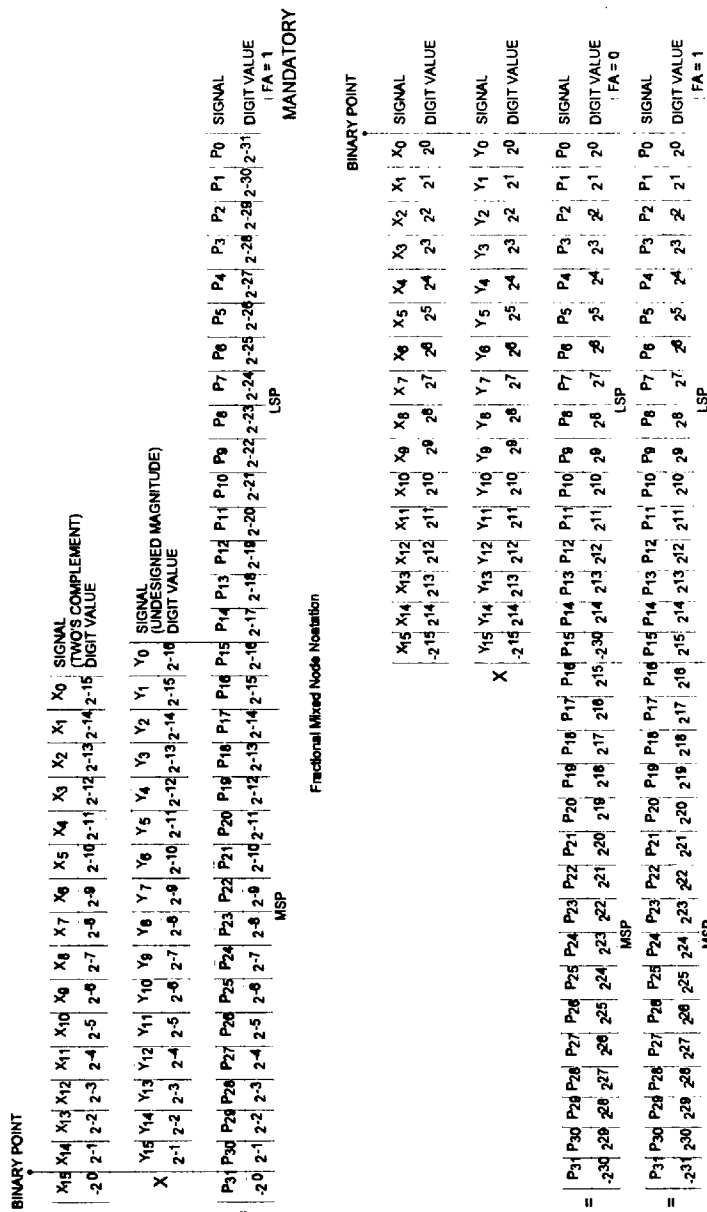
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* In this format an overflow occurs in the attempted multiplication of the two's complement number 1,000...0 with 1,000.0 yielding an erroneous product of -1 in the fraction case and -2^{30} in the integer case.

FIGURE 3. Input/output data formats. - Continued

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FIGURE 3. Input/output data formats. - Continued

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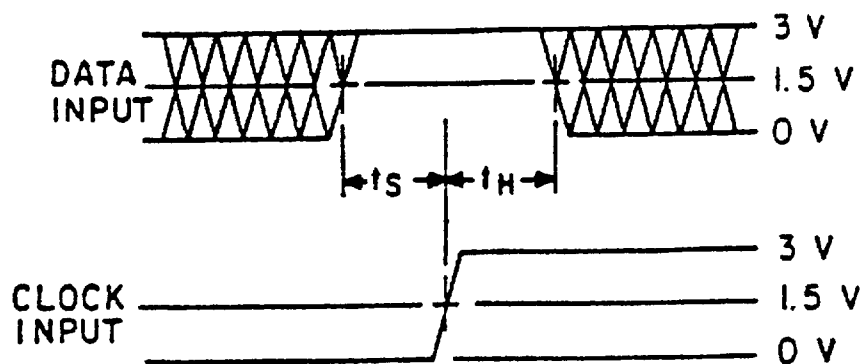
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Setup and hold times



NOTE: Diagram shown for HIGH data only.
Output transition may be opposite sense.

Three-state control timing diagram

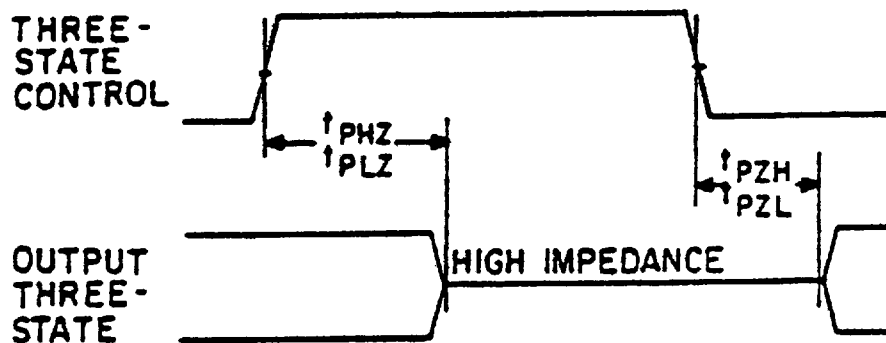


FIGURE 5. Timing waveforms.

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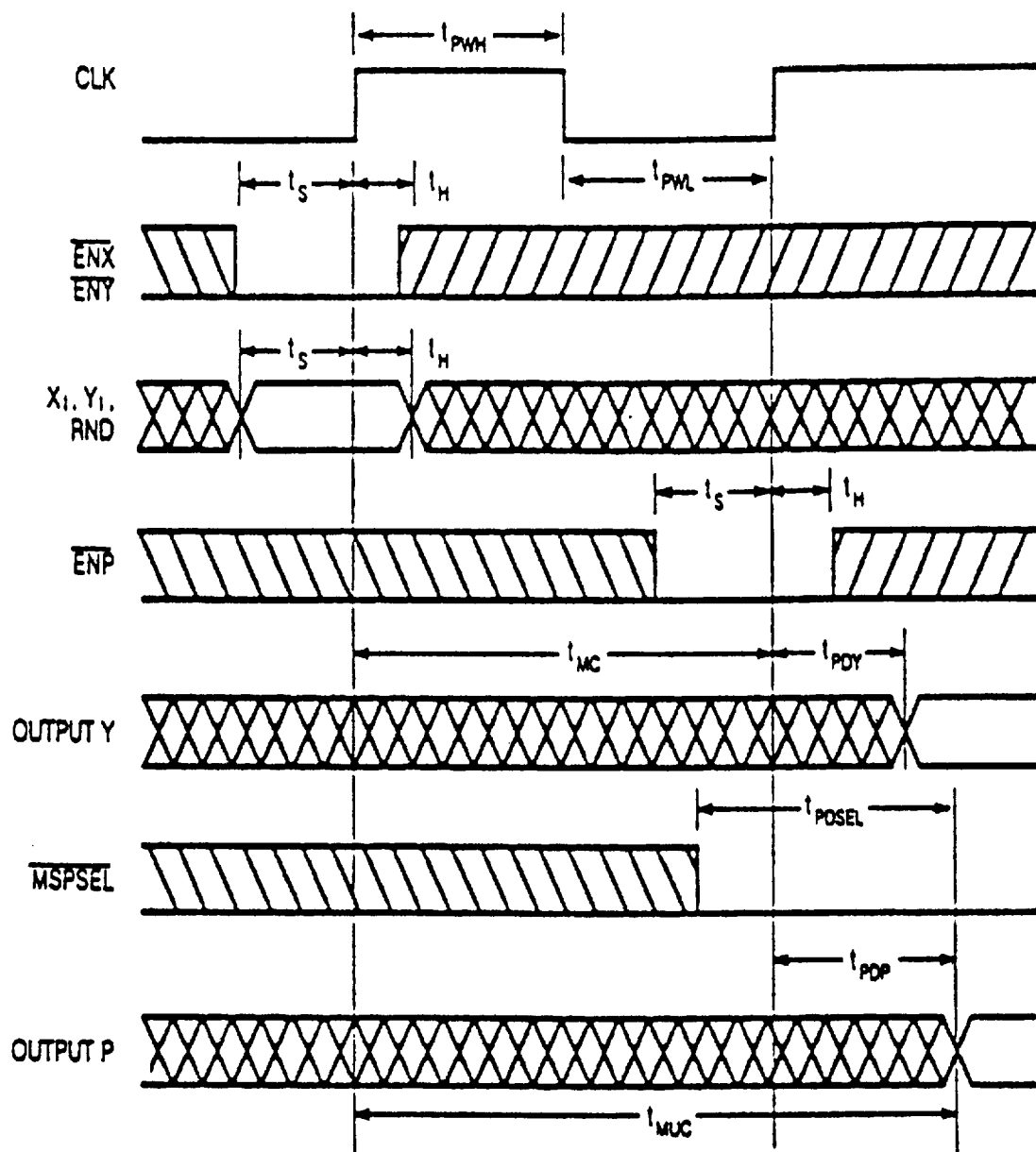


FIGURE 5. Timing waveforms. - Continued

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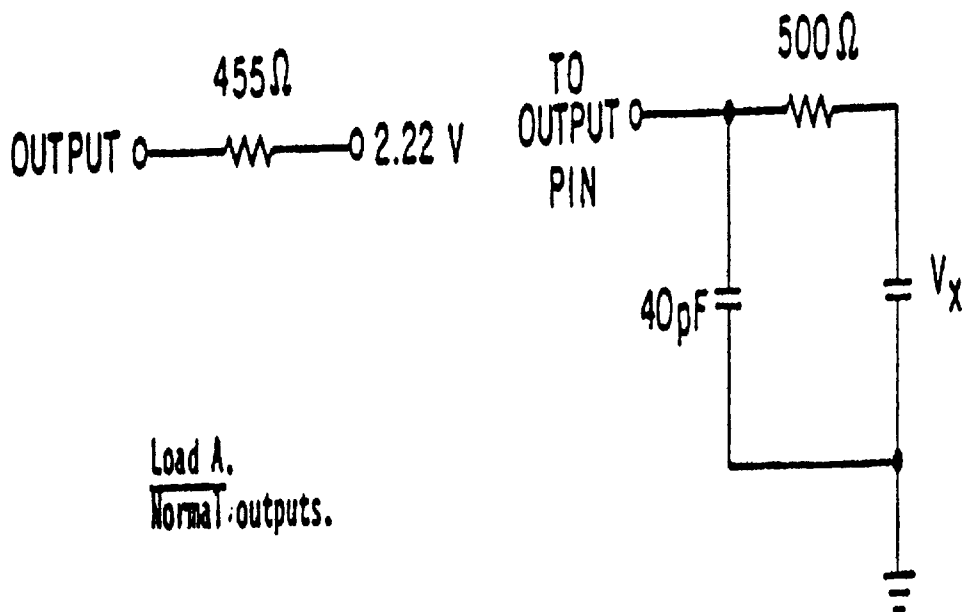
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THEVENIN EQUIVALENT



Load A.
Normal outputs.

Load B. Output three-state
Delay load (V_x = 0 V or 2.6 V)
(or equivalent)

AC TEST CONDITIONS

Input pulse levels	GND to 3.0 V
Input rise/fall times	5 ns
Input timing references levels	1.5 V
Output reference levels	1.5 V

FIGURE 5. Timing waveforms. - Continued

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4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) $T_A = +125^\circ\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	-----
Final electrical test parameters (method 5004)	*1, 2, 3, 7, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- Tests shall be as specified in table II herein.
- Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.
- Subgroups 7 and 8 shall include verification of the functionality of the device. These tests form a part of the vendor's test tape and shall be maintained and available from the approved source of supply.

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4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
 - (2) $T_A = +125^\circ\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0674.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

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6.6 Pin descriptions.

PIN	I/O	Description
X ₁₅₋₀	I	X input data. This 16-bit number may be interpreted as two's complement or unsigned magnitude.
Y ₁₅₋₀ (P ₁₅₋₀)	I/O	Y input/LSP output data. This 16-bit number may be interpreted as two's complement or unsigned magnitude. The Y input port may be multiplexed with the LSP output (P ₁₅₋₀).
P ₃₁₋₁₆ (P ₁₅₋₀)	O	Output data. This 16-bit port may carry either the MSP (P ₃₁₋₁₆) or the LSP (P ₁₅₋₀).
FT	I	The MSP and LSP registers are made transparent (asynchronous operation) if FT is high.
FA	I	Format adjust control. If FA is high, a full 32-bit product is output. If FA is low, a left-shifted product is output, with the sign bit replicated in the LSP. FA must be high for two's complement integer, unsigned magnitude, and mixed mode multiplication.
MSPSEL	I	Output multiplexer control. When $\overline{\text{MSPSEL}}$ is low the MSP is available for output at the MSP output port, and the LSP is available at the Y input/LSP output port. When MSPSEL is high, the LSP is available at both ports (above) and the MSP is not available.
RND	I	Round control. When RND is high, a one is added to the MSP of the LSP. This position is dependent on the FA control; FA = high means RND adds to the 2 ⁻¹⁵ bit (P ₁₅), fa = low means RND added to the 2 ⁻¹⁶ bit (P ₁₄).
TCX	I	Two's complement control X. X input data is interpreted as two's complemented when TCX is high. TCX low means the data are interpreted as unsigned magnitude.
TCY	I	Two's complement control Y. Y input is interpreted as two's complement when TCY is high TCY low means the data is interpreted as unsigned magnitude.
$\overline{\text{OEP}}$	I	P ₃₁₋₁₆ /P ₁₅₋₀ output port three-state control. When $\overline{\text{OEP}}$ is low, the output port is enabled; when $\overline{\text{OEP}}$ is high, the drivers are in a high impedance state.
$\overline{\text{OEL}}$	I	Y-in/P ₁₅₋₀ port three-state control. When $\overline{\text{OEL}}$ is low, the timeshared port is enabled for LSP output. When $\overline{\text{OEL}}$ is high, the output drivers are in a high impedance state. This is required for Y input.
CLK	I	Clock. All enabled registers latch in their data at the rising edge of CLK.
$\overline{\text{ENX}}$	I	X-register enable. When $\overline{\text{ENX}}$ is low, the X register is enabled. X-input data and TCX will be latched in at rising edge of CLK when the register is enabled. When ENX is high, the X register is in hold mode.
$\overline{\text{ENY}}$	I	Y-register enable. $\overline{\text{ENY}}$ enables the Y-register (see $\overline{\text{ENX}}$).
$\overline{\text{ENP}}$	I	Product register enable. $\overline{\text{ENP}}$ enables the product register. Both the MSP and LSP sections are enabled by ENP (see ENX).

6.6.1 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 97-04-17

Approved sources of supply for SMD 87686 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8768601XX	3/	IDT7217L-40CB
5962-8768601YX	3/	7C517-42
5962-8768601ZX	3/	7C517-42 IDT7217L-40GB
5962-8768601UX	3/	7217L-40
5962-8768602XA	65896	LMU17DMB55
5962-8768602YA	65896	LMU217KMB55
5962-8768602ZA	3/	IDT7217L-55GB
5962-8768602UA	65896	LMU217RMB55
5962-8768602TA	65896	LMU17GMB55
5962-8768603XA	65896	LMU17DMB75
5962-8768603YA	65896	LMU217KMB75
5962-8768603ZX	3/	7C517-75

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Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962-8768603UA	65896	LMU217RMB75
5962-8768603TA	65896	LMU17GMB75
5962-8768604XA	65896	LMU17DMB25
5962-8768604YA	65896	LMU217KMB25
5962-8768604ZA	<u>3</u> /	7C517-25
5962-8768604UA	65896	LMU217RMB25
5962-8768604TA	65896	LMU17GMB25
5962-8768605XA	65896	LMU17DMB30
6962-8768605YA	65896	LMU217KMB30
5962-8768605ZA	<u>3</u> /	7C517-30
5962-8768605UA	65896	LMU217RMB30

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Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-8768605TA	65896	LMU17GMB30
5962-8768606XA	65896	LMU17DMB40
5962-8768606YA	65896	LMU217KMB40
5962-8768606ZA	<u>3/</u>	7C517-40
5962-8768606UA	65896	LMU217RMB40
5962-8768606TA	65896	LMU17GMB40

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. The device manufacturers listed herein are authorized to supply alternate lead finishes "A", "B", or "C" at their discretion. Contact the listed approved source of supply for further information.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ No approved source.

Vendor CAGE
number

65896

Vendor name
and address

Logic Devices Inc
1320 Orleans Drive
Sunnyvale, CA 94089

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.

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