

Full-Bridge Power Amplifier

FEATURES

- Precision Current Control
- $\pm 800\text{mA}$ Load Current
- 1.25V Total V_{SAT} at 800mA
- Controlled Velocity Head Parking
- Precision Dual Supply Monitor with Indicator
- Limit Input to Force Output Extremes
- Inhibit Input and UVLO
- 4V to 15V operation

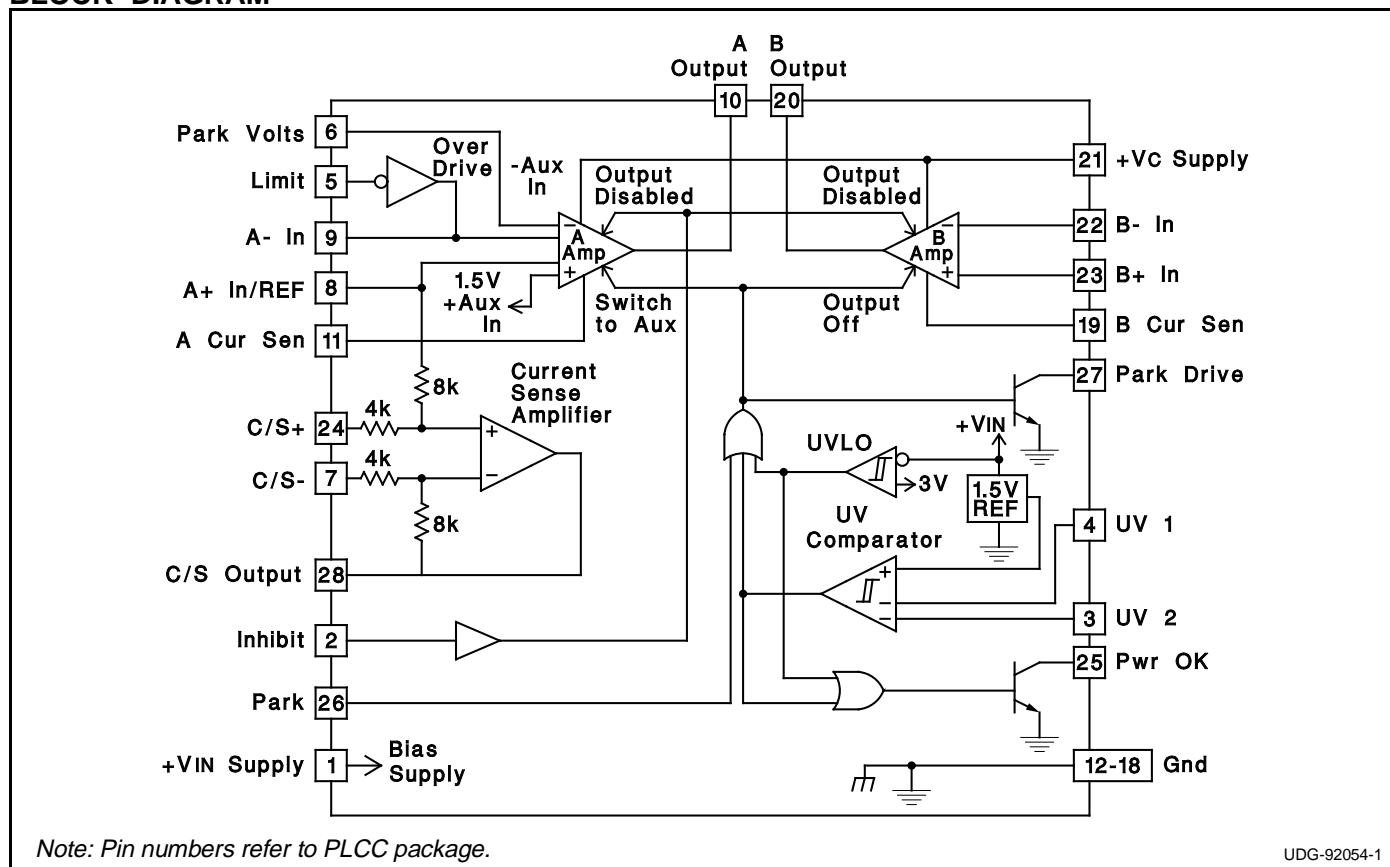
DESCRIPTION

This full-bridge power amplifier is rated for continuous output current of 0.8 Amperes and is intended for use in demanding servo applications such as head positioning for high-density disk drives. The device includes a precision current sense amplifier that provides accurate control of load current. Current is sensed with a single resistor in series with the load. The power amplifier has a very low output saturation voltage and will operate down to 4V supply levels. Power output stage protection includes current limiting and thermal shutdown.

Auxiliary functions on this device include a dual-input under-voltage comparator, which can monitor two independent supply voltages and force a built-in head park function when either is below minimum. When activated by either the UV comparator, or a command at the separate PARK input, the park circuitry will override the amplifier inputs to convert the power outputs to a programmable constant voltage source which will hold regulation as the supply voltage falls to below 3.0 Volts. Added features include a POWER OK flag output, a LIMIT input to force the drive output to its maximum level in either polarity, and a over-riding INHIBIT input to disable all amplifiers and reduce quiescent supply current.

This device is packaged in a power PLCC surface mount configuration which maintains a standard 28-pin outline, but with 7 pins along one edge allocated to ground for optimum thermal transfer. And is also available in a 24-pin surface mount SOIC package.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, (+VIN,+Vc)	20V
UV Comparator, and Digital Inputs	
Maximum forced voltage	-0.3V to 10V
Maximum forced current	±10mA
C/S Inputs	
Maximum forced voltage	-0.3V to 20V
A and B Amplifier Inputs	-0.3V to +VIN
Open Collector Output Voltages.	20V
A and B Output Currents (continuous)	
Source	Internally Limited
Sink	1.0A
Parking Drive Output Current	
Continuous	150mA
Pulsed	1A
Output Diode Current (pulsed)	1A
Power OK Output Current(continuous)	30mA
Operating Junction Temperature	-55°C to +150°C
Storage Temperature	-65°C to +150°C

Note 1: Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals.

"Pulsed" is defined as a less than 10% duty cycle pulse with a maximum duration of 500 μ s.

Note 2: See Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

Thermal Data**QP Package:**

Thermal Resistance Junction to Leads,

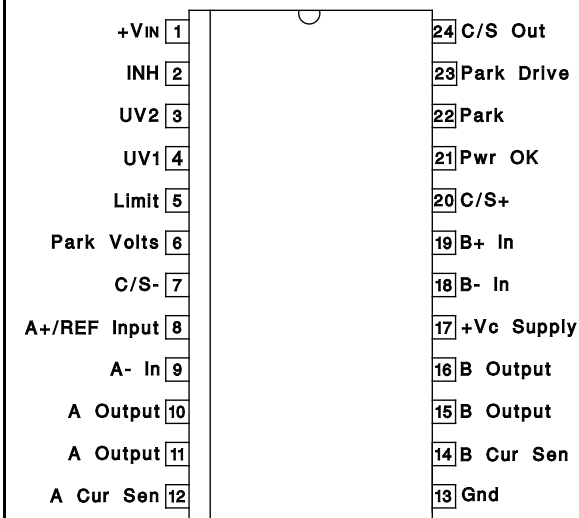
θ_{JL} 15°C/W

Thermal Resistance Junction to Ambient,

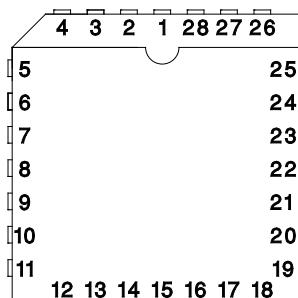
θ_{JA} 40°C/W

CONNECTION DIAGRAMS

SOIC-24 (Top View)
DW Package



PLCC-28 (Top View)
QP Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
+VIN	1
INH	2
UV2	3
UV1	4
Limit	5
Park Volts	6
C/S-	7
A+/REF Input	8
A- In	9
A Output	10
A Cur Sen	11
Gnd (Heat Dissipation Pins)	12-18
B Cur Sen	19
B Output	20
+Vc Supply	21
B- In	22
B+ In	23
C/S+	24
Pwr OK	25
Park	26
Park Drive	27
C/S Out	28

ELECTRICAL CHARACTERISTICS: Unless otherwise stated specifications apply for 0°C ≤ TA ≤ 70°C, +VIN = 12V, +Vc = +VIN, A+/REF Input = 6V. TA=TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY					
+VIN Supply Current	All Amplifier Outputs = 6V		35	42	mA
+Vc Supply Current	IOUT = 0A		1		mA
+VIN UVLO Threshold	Low to High		2.8	3.0	V
UVLO Threshold Hysteresis			200		mV

**ELECTRICAL
CHARACTERISTICS (cont.)**

Unless otherwise stated specifications apply for $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$, $+V_{IN} = 12\text{V}$, $+V_C = +V_{IN}$,
 $A+/REF$ INPUT = 6V. $T_A = T_J$.

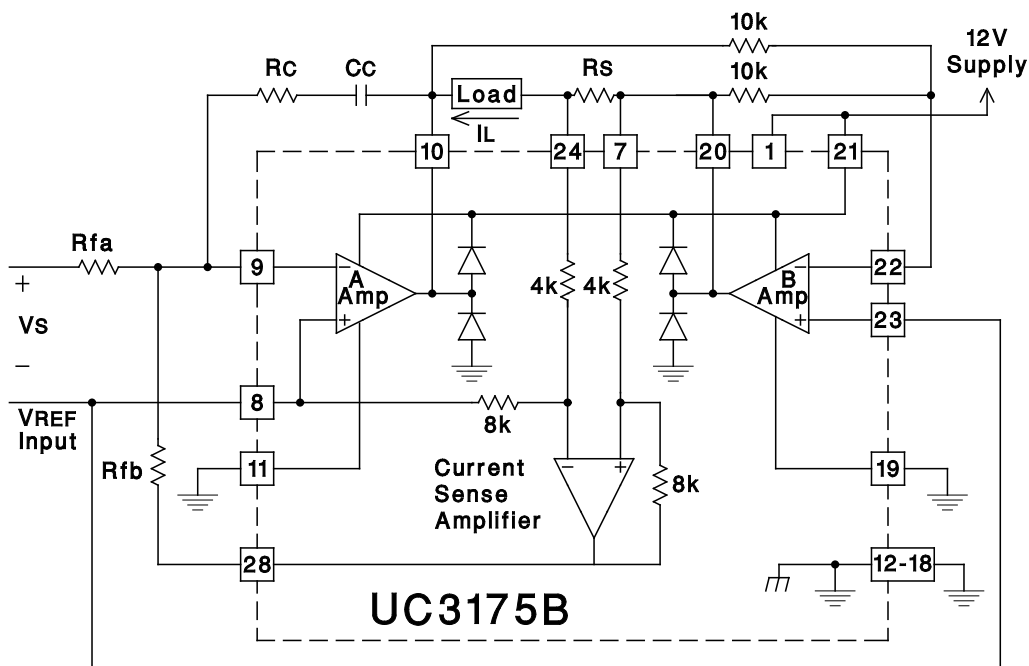
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UNDER VOLTAGE (UV) COMPARATOR					
Input Bias Current		-1.5	-0.5		μA
UV Thresholds	Low to High, Other Input = 5V	1.48	1.50	1.52	V
UV Threshold Hysteresis		15	25	40	mV
Pwr OK V_{SAT}	$I_{OUT} = 5\text{mA}$			0.45	V
Pwr OK Leakage	$V_{OUT} = 20\text{V}$			5	μA
POWER AMPLIFIERS A and B					
Input Offset Voltage	$V_{CM} = 6\text{V}$, A Amplifier			8	mV
	B Amplifier			12	mV
Input Offset Drift	Note 1, A Amplifier Only			25	$\mu\text{V}/^{\circ}\text{C}$
Input Bias Current	$V_{CM} = 6\text{V}$, except A+/REF Input	-500	-150		nA
Input Offset Current	$V_{CM} = 6\text{V}$, B Amplifier Only			200	nA
Input Bias Current at A+/Ref Input	$(A+/Ref-C/S+)/12k$, $T_J = 25^{\circ}\text{C}$	60	84	105	$\mu\text{A}/\text{V}$
CMRR	$1\text{V} \leq V_{CM} \leq 10\text{V}$	70	90		dB
PSRR	$+V_{IN} = 4\text{V}$ to 15V , $V_{CM} = 1.5\text{V}$	70	90		dB
Large Signal Voltage Gain	$V_{OUT} = 1\text{V}$, Sinking 500mA to $V_{OUT} = 11\text{V}$, Sourcing 500mA	3.0	15.0		V/mV
Slew Rate	1 to 13V, 13 to 1V, $T_J = 25^{\circ}\text{C}$		1	2.1	V/ μs
Unity Gain Bandwidth	Note 1, A Amplifier		2		MHz
	Note 1, B Amplifier		1		MHz
High-Side Current Limit		0.8	1.0		A
Output Saturation Voltage	High-Side, $I_{SOURCE} = 250\text{mA}$		0.7		V
	High-Side, $I_{SOURCE} = 800\text{mA}$		0.85		V
	Low-Side, $I_{SINK} = 250\text{mA}$		0.3		V
	Low-Side, $I_{SINK} = 800\text{mA}$		0.4		V
	Total, $I_{OUT} = 250\text{mA}$		1.0	1.2	V
	Total, $I_{OUT} = 800\text{mA}$		1.25	1.6	V
High Side Diode V_F	$I_D = 800\text{mA}$, Inhibit Activated		1.0		V
Low Side Diode V_F	$I_D = 800\text{mA}$, Inhibit Activated		1.0		V
CURRENT SENSE AMPLIFIER					
Input Offset Voltage	$V_{CM} = 6\text{V}$			2.0	mV
Input Offset Change with Common Mode Input	$0\text{V} \leq V_{CM} \leq 12\text{V}$			1500	$\mu\text{V}/\text{V}$
Input Offset Drift	Note 1			8	$\mu\text{V}/^{\circ}\text{C}$
Voltage Gain	$-1.0\text{V} \leq V_{DIFF} \leq +1.0\text{V}$, $V_{CM} = 6\text{V}$	1.95	2.00	2.05	V
Output Saturation Voltage	Low-Side, $I_{SINK} = 1.5\text{mA}$		0.3	0.5	V
	High-Side, $I_{SOURCE} = 1.5\text{mA}$		0.4	0.7	V
Maximum A+/Ref Input	Volts Below $+V_{IN}$, C/S+ & C/S- = BOUTPUT Max @ 10mA Output Current, $+V_{IN} = 4.5\text{V}$, C/S VIO $\leq 5\text{mV}$		2.6	3.0	V
PARKING FUNCTION					
Park Input Threshold		0.7	1.1	1.7	V
Park Input Current	Park Input = 1.7V		60	100	μA
Park Drive Saturation Voltage, PD_{VSAT}	$I_{SINK} = 100\text{mA}$		0.3	0.5	V
Parking Drive Leakage	$V_{OUT} = 20\text{V}$			100	μA
Amplifier A Aux Input Bias Current		-500	-150		nA

**ELECTRICAL
CHARACTERISTICS (cont.)**

Unless otherwise stated specifications apply for $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$, $+V_{\text{IN}} = 12\text{V}$, $+V_{\text{C}} = +V_{\text{IN}}$,
 $A+/\text{REF}$ Input = 6V. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PARKING FUNCTIONS (cont.)					
Amplifier A Saturation Voltage, A_{HVSAT}	$I_{\text{SOURCE}} = 50\text{mA}$, $+V_{\text{IN}} = 3\text{V}$		0.65	0.8	V
Regulating Voltage at Park Volts		1.47	1.50	1.53	V
Minimum Parking Supply Voltage	$A_{\text{HVSAT}} + P_{\text{DVSAT}} \leq 1.3\text{V}$ @ 50mA		1.7	1.9	V
AUXILIARY FUNCTIONS					
Limit Input Low Voltage	A Output Forced Low	0.7	0.8		V
Limit Input High Voltage	A Output Forced High		2.2	2.3	V
Limit Inactive		1.2		1.8	V
Limit Open Circuit Voltage		1.45	1.50	1.55	V
Limit Input Resistance	$1.2\text{V} \leq \text{Limit Input} \leq 1.8\text{V}$		10		$\text{k}\Omega$
Inhibit Input Threshold		0.7	1.1	1.7	V
Inhibit Input Current	Inhibit Input = 1.7V		400	700	μA
Supply Current when Inhibited	The sum of $+V_{\text{IN}}$ and $+V_{\text{C}}$ currents		2	6	mA
Thermal Shutdown Temperature			165		$^{\circ}\text{C}$

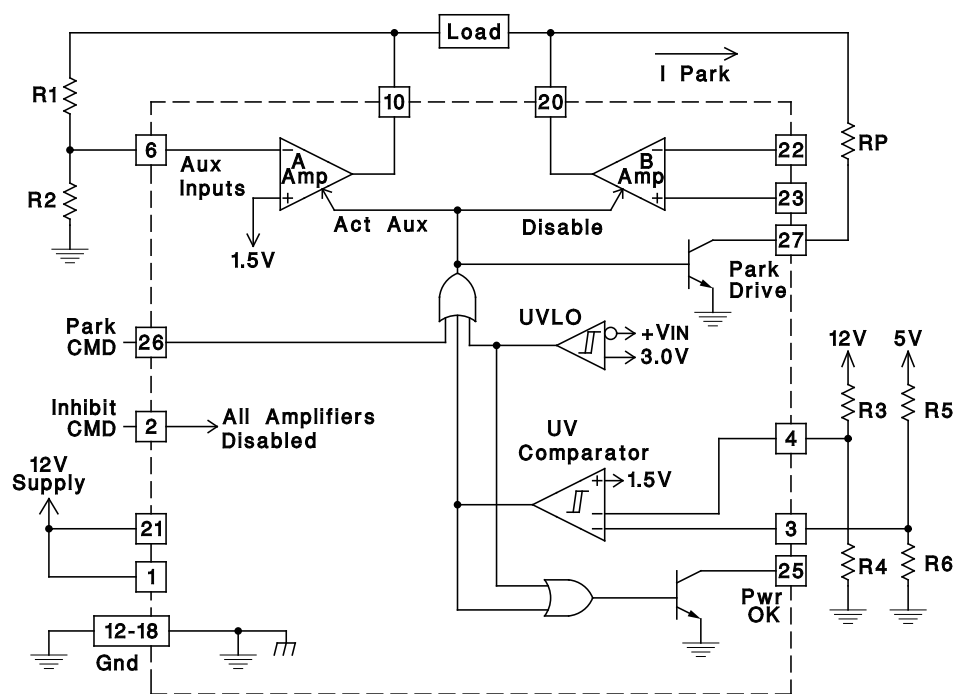
Note 1: This specification not tested in production.

UC3175B Series Current Sensing

UDG-92058

$$G_o = \frac{I_L}{V_s} = \frac{R_{fb}}{R_{fa} \cdot 2 \cdot R_s}$$

Parking Function



UDG-92059

Notes: $\text{Parking voltage} = \frac{1.5V \cdot R1 + R2}{R2 - (IL \cdot RP)}$
 RP is optional for current limiting.
 Inhibit and Park Inputs are active high.
 Pwr OK is low on power failure.

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.