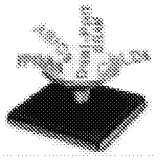
Integrator Series FPGAs – 1200XL and 3200DX Familes



Features

High Capacity

- 2,500 to 40,000 logic gates
- Up to 4 Kbits configurable dual-port SRAM
- Fast wide-decode circuitry
- Up to 288 user-programmable I/O Pins

High Performance

- 225 MHz performance
- 5 ns Dual-Port SRAM Access
- 100 MHz FIFOs
- 7.5 ns 35-bit Address Decode

Ease-of-Integration

- Synthesis-friendly architecture supports ASIC design methodologies
- 95–100% device utilization using automatic Place and Route Tools
- Deterministic, user-controllable timing via DirectTime software tools
- Supported by Actel Designer Series development system with interfaces to popular design environments such as Cadence, Escalade, Exemplar, IST, Mentor Graphics, Synopsys and Viewlogic
- JTAG 1149.1 Boundary Scan Testing

General Description

Actel's Integrator Series FPGAs are the first programmable logic devices optimized for high-speed system logic integration. Based on Actel's proprietary PLICE antifuse technology and state-of-the-art 0.6-micron double metal CMOS process, the Integrator Series devices offer a fine-grained, register-rich architecture with the industry's fastest embedded dual-port SRAM and wide decode circuitry.

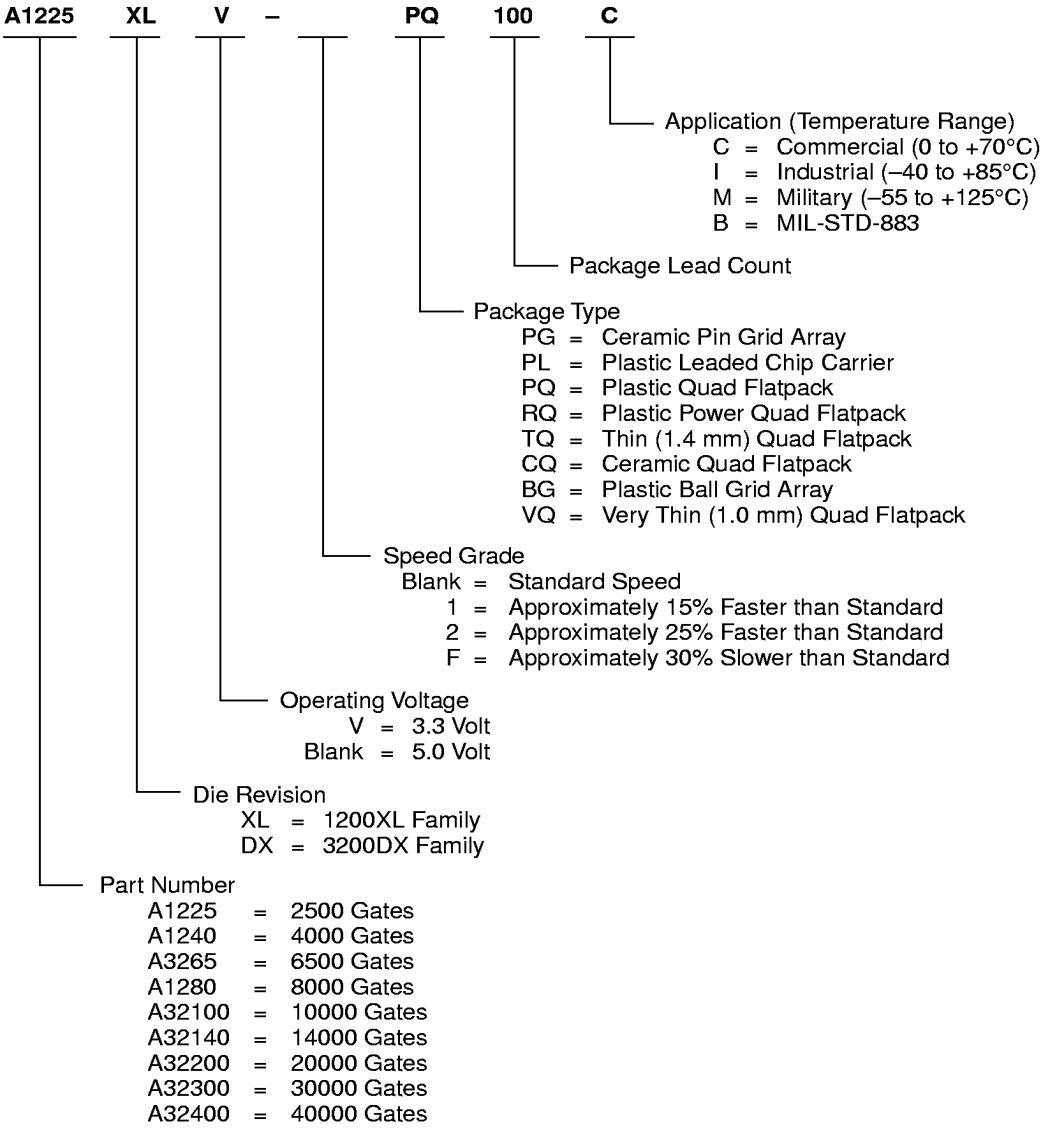
3200DX and 1200XL FPGAs were designed to integrate system logic which is typically implemented in multiple CPLDs, PALs and FPGAs. These devices provide the features and performance required for today's complex, high-speed digital logic systems. The 3200DX family offers the industry's fastest dual-port SRAM for implementing fast FIFOs, LIFOs and temporary data storage. The large number of storage elements can efficiently address applications requiring wide datapath manipulation and transformation functions such as telecommunications, networking and DSP.

Integrator Series Product Profile

Device	A1225XL	A1240XL	A3265DX	A1280XL	A32100DX	A32140DX	A32200DX	A32300DX	A32400DX
Capacity									
Logic Gates[1]	2,500	4,000	6,500	8,000	10,000	14,000	20,000	30,000	40,000
SRAM Bits	N/A	N/A	N/A	N/A	2,048	N/A	2,560	3,072	4,096
Logic Modules									
Sequential	231	348	510	624	700	954	1,230	1,888	2,526
Combinatorial	220	336	475	608	662	912	1,184	1,833	2,466
Decode	N/A	N/A	20	N/A	20	24	24	28	28
SRAM Modules (64x4 or 32x8)	NA	NA	NA	NA	8	NA	10	12	16
Dedicated Flip-Flops	231	348	510	624	700	954	1,230	1,888	2,526
Clocks	2	2	2	2	6	2	6	6	6
User I/O (maximum)	83	104	126	140	152	176	202	250	288
JTAG	No	No	No	No	Yes	Yes	Yes	Yes	Yes
Packages	PL84 PQ100 VQ100 PG100	PL84 PQ100 PQ144 TQ176 PG132	PL84 PQ100 PQ160 TQ176	PL84 PQ100 PQ160 PQ208 TQ176 PG176 CQ172	PL84 PQ160 PQ208 TQ176	PL84 PQ160 PQ208 TQ176	PQ208 RQ208 RQ240	RQ208 RQ240	RQ240

Note 1: *Logic gate capacity does not include SRAM bits as logic.*

Ordering Information



Product Plan

	Speed Grade				Application			
	–F	Std	–1*	–2*	C	I	M	B
A1225XL Device								
84-pin Plastic Leaded Chip Carrier (PLCC)	—	✔	✔	✔	✔	✔	—	—
100-pin Plastic Quad Flatpack (PQFP)	—	✔	✔	✔	✔	✔	—	—
100-pin Very Thin Plastic Quad Flatpack (VQFP)	—	✔	✔	✔	✔	✔	—	
100-pin Ceramic Pin Grid Array (CPGA)	—	✔	✔	✔	✔	—	—	—
A1225XLV Device								
84-pin Plastic Leaded Chip Carrier (PLCC)	—	✔	—	—	✔	—	—	—
100-pin Very Thin Plastic Quad Flatpack (VQFP)	—	✔	—	—	✔	—	—	—
A1240XL Device								
84-pin Plastic Leaded Chip Carrier (PLCC)	—	✔	✔	✔	✔	✔	—	—
100-pin Plastic Quad Flatpack (PQFP)	—	✔	✔	✔	✔	✔	—	—
132-pin Ceramic Pin Grid Array (CPGA)	—	✔	✔	✔	✔	—	—	—
144-pin Plastic Quad Flatpack (PQFP)	—	✔	✔	✔	✔	✔	—	—
176-pin Thin Plastic Quad Flatpack (TQFP)	—	✔	✔	✔	✔	✔	—	—
A1240XLV Device								
84-pin Plastic Leaded Chip Carrier (PLCC)	—	✔	—	—	✔	—	—	—
176-pin Thin Plastic Quad Flatpack (TQFP)	—	✔	—	—	✔	—	—	—
A3265DX Device								
84-pin Plastic Leaded Chip Carrier (PLCC)	—	✔	✔	✔	✔	✔	—	—
160-pin Plastic Quad Flatpack (PQFP)	—	✔	✔	✔	✔	✔	—	—
176-pin Thin Plastic Quad Flatpack (TQFP)	—	✔	✔	✔	✔	✔	—	—
A3265DXV Device								
84-pin Plastic Leaded Chip Carrier (PLCC)	—	✔	—	—	✔	—	—	—
176-pin Thin Plastic Quad Flatpack (TQFP)	—	✔	—	—	✔	—	—	—
A1280XL Device								
84-pin Plastic Leaded Chip Carrier (PLCC)	—	✔	✔	✔	✔	✔	—	—
160-pin Plastic Quad Flatpack (PQFP)	—	✔	✔	✔	✔	✔	—	—
172-pin Ceramic Quad Flatpack (CQFP)	—	✔	✔	✔	✔	—	P	P
176-pin Thin Plastic Quad Flatpack (TQFP)	—	✔	✔	✔	✔	✔	—	—
176-pin Ceramic Pin Grid Array (CPGA)	—	✔	✔	✔	✔	—	P	P
208-pin Plastic Quad Flatpack (PQFP)	—	✔	✔	✔	✔	✔	—	—
A1280XLV Device								
84-pin Plastic Leaded Chip Carrier (PLCC)	—	✔	—	—	✔	—	—	—
176-pin Thin Plastic Quad Flatpack (TQFP)	—	✔	—	—	✔	—	—	—

Applications: *C = Commercial, I = Industrial, M = Military, B = MIL-STD-883*

Availability: *✔ = Available, P = Planned, — = Not Planned*

** Speed Grade:* *–1 = Approx. 15% Faster than Standard, –2 = Approx. 25% Faster than Standard, –F = Approx. 30% Slower than Standard*

Product Plan (continued)

	Speed Grade				Application			
	–F	Std	–1*	–2*	C	I	M	B
A32100DX Device								
84-pin Plastic Leaded Chip Carrier (PLCC)	P	P	P	P	P	P	—	—
160-pin Plastic Quad Flatpack (PQFP)	P	P	P	P	P	P	—	—
208-pin Plastic Quad Flatpack (PQFP)	P	P	P	P	P	P	—	—
176-pin Thin Plastic Quad Flatpack (TQFP)	P	P	P	P	P	P	—	—
240-pin Plastic Super Ball Grid Array (SBGA)	P	P	P	P	P	P	—	—
A32140DX Device								
160-pin Plastic Quad Flatpack (PQFP)	P	✔	✔	✔	✔	✔	—	—
176-pin Thin Plastic Quad Flatpack (TQFP)	P	✔	✔	✔	✔	✔	—	—
208-pin Plastic Quad Flatpack (PQFP)	P	✔	✔	✔	✔	✔	—	—
240-pin Plastic Super Ball Grid Array (SBGA)	P	✔	✔	✔	✔	✔	—	—
A32140DXV Device								
176-pin Thin Plastic Quad Flatpack (TQFP)	—	✔	—	—	✔	—	—	—
208-pin Plastic Quad Flatpack (PQFP)	—	✔	—	—	✔	—	—	—
A32200DX Device								
208-pin Plastic Quad Flatpack (PQFP)	P	✔	✔	P	✔	✔	—	—
208-pin Plastic Power Quad Flatpack (RQFP)	P	✔	✔	P	✔	✔	—	—
240-pin Plastic Power Quad Flatpack (RQFP)	P	✔	✔	P	✔	✔	—	—
240-pin Plastic Super Ball Grid Array (SBGA)	P	P	P	P	P	P	—	—
432-pin Plastic Super Ball Grid Array (SBGA)	P	P	P	P	P	P	—	—
A32200DXV Device								
208-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔	✔	✔	✔	—	—
240-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔	✔	✔	✔	—	—
A32300DX Device								
240-pin Plastic Power Quad Flatpack (RQFP)	P	P	P	P	P	P	—	—
A32400DX Device								
240-pin Plastic Power Quad Flatpack (RQFP)	P	P	P	P	P	P	—	—

Applications: *C = Commercial, I = Industrial, M = Military, B = MIL-STD-883*

Availability: *✔ = Available, P = Planned, — = Not Planned*

** Speed Grade:* *–1 = Approx. 15% Faster than Standard, –2 = Approx. 25% Faster than Standard, –F = Approx. 30% Slower than Standard*

Integrator Series devices are supported by Actel's Designer Series Development software which provides a seamless integration into any ASIC design flow. The Designer Series development tools offer automatic placement and routing (even with pre-assigned pins), static timing analysis, user programming, and debug and diagnostic probe capabilities. In addition, the DirectTime tool provides deterministic as well as controllable timing. DirectTime allows the designer to specify the performance requirements of individual paths and system clock(s). Using these specifications, the software will automatically optimize the placement and routing of the logic to meet these constraints. Included with the Designer Series tools is Actel's ACTGen™ Macro Builder. ACTGen allows the designer to quickly build fast, efficient logic functions such as counters, adders, FIFOs, and RAM.

The Designer Series tools provide designers the capability to move up to High-Level Description Languages, such as VHDL and Verilog, or use schematic design entry with interfaces to most EDA tools. Designer Series is supported on the following development platforms: 486 and Pentium PC, Sun® and HP® workstations. The software provides CAE interfaces to Cadence, Mentor Graphics®, Escalade, OrCAD™ and Viewlogic® design environments. Additional development tools are supported through Actel's Industry Alliance Program, including DATA I/O (ABEL FPGA) and MINC.

Actel's FPGAs are an ideal solution for shortening the system design and development cycle and offers a cost-effective alternative for low volume production runs. The 3200DX and 1200XL devices are an excellent choice for integrating logic that is currently implemented in multiple PALs, CPLDs and FPGAs. Some example applications include high-speed controllers and address decoding, peripheral bus interfaces, DSP, and co-processor functions.

Plastic Device Resources

Device	User I/Os									
	PLCC 84-pin	VQFP 100-pin	PQFP 100-pin	PQFP 144-pin	PQFP 160-pin	PQFP 208-pin	RQFP 240-pin	TQFP 176-pin	SBGA 240-pin	SBGA 432-pin
A1225XL	72	83	83	—	—	—	—	—	—	—
A1240XL	72	—	83	104	—	—	—	103	—	—
A3265DX	72	—	83	—	125	—	—	126	—	—
A1280XL	72	—	83	—	125	140	—	140	—	—
A1280XLB										
A32100DX	72	—	—	—	125	152	—	142	152	—
A32140DX	72	—	—	—	125	176	—	150	176	—
A32200DX	—	—	—	—	—	176*	202	—	176	202
A32300DX	—	—	—	—	—	176	202	—	—	250
A32400DX	—	—	—	—	—	—	202	—	—	288

Package Definitions *(Consult your local Actel Sales Representative for product availability.)*

PLCC = Plastic Leaded Chip Carrier, PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, BGA = Ball Grid Array, VQFP = Very Thin Quad Flat Pack, RQFP = Plastic Power Quad Flat Pack

• Also available in RQFP 208-pin.

Hermetic Device Resources

Device	User I/Os	
	CPGA 176-pin	CQFP 172-pin
A1280XL	140	140
A32140DX		
A32200DX		

Package Definitions *(Consult your local Actel Sales Representative for product availability.)*

CPGA = Ceramic Pin Grid Array, CQFP = Ceramic Quad Flat Pack

Pin Description

CLKA, CLKB Clock A and Clock B (input)
TTL Clock inputs for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK Diagnostic Clock (Input)
TTL Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

GND Ground (Input)
Input LOW supply voltage.

I/O Input/Output (Input, Output)
I/O pin functions as an input, output, three-state or bi-directional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically driven LOW by the Designer Series software.

MODE Mode (Input)
The MODE pin controls the use of multi-function pins (DCLK, PRA, PRB, SDI, TDO). When the MODE pin is HIGH, the special functions are active. To provide Actionprobe capability, the MODE pin should be terminated to GND through a 10K resistor so that the MODE pin can be pulled high when required.

NC No Connection
This pin is not connected to circuitry within the device.

PRA/I/O Probe A (Output)
The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

PRB/I/O Probe B (Output)
The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

QCLKA/B,C,D Quadrant Clock (Input/Output)
These four pins are the quadrant clock inputs. When not used as a register control signal, these pins can function as general purpose I/O.

SDI Serial Data Input (Input)
Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

TCK Test Clock
Clock signal to shift the JTAG data into the device. This pin functions as an I/O when the JTAG fuse is not programmed.

TDI Test Data In
Serial data input for JTAG instructions and data. Data is shifted in on the rising edge of TCLK. This pin functions as an I/O when the JTAG fuse is not programmed.

TDO Test Data Out
Serial data output for JTAG instructions and test data. This pin functions as an I/O when the JTAG fuse is not programmed.

TMS Test Mode Select
Serial data input for JTAG test mode. Data is shifted in on the rising edge of TCLK. This pin functions as an I/O when the JTAG fuse is not programmed.

V_{CC} Supply Voltage (Input)
Input HIGH supply voltage.

Note: *TCK, TDI, TDO, TMS are only available on devices containing JTAG circuitry.*

Integrator Series Architectural Overview

The 1200XL and 3200DX architecture is composed of fine-grained building blocks which produce fast, efficient logic designs. All devices within the Integrator Series are composed of Logic Modules, Routing Resources, Clock Networks, and I/O modules which are the building blocks to design fast logic designs. In addition, a subset of devices contain embedded dual-port SRAM and wide decode modules. The dual-port SRAM modules are optimized for high-speed data path functions such as FIFOs, LIFOs, and scratchpad memory. "Integrator Series Product Profile" on page 1 lists the specific logic resources contained within each device.

Logic Modules

3200DX and 1200XL devices contain three types of logic modules: combinatorial (C-modules), sequential (S-modules), and decode (D-modules). 1200XL devices contain only the C-module and S-module, while the 3200DX devices contain D-modules and dual-port SRAM modules; in addition to the S-module and C-module.

The C-module is shown in Figure 1 and implements the following function:

Y=!S1*!S0*D00+!S1*S0*D01+S1*!S0*D01+S1*S0*D11

where:

S0=A0*B0

S1=A1+B1

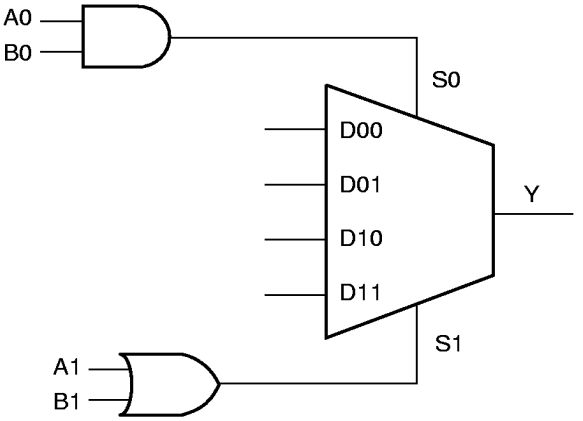


Figure 1 • C-module Implementation

The S-module shown in Figure 2 is designed to implement high-speed sequential functions within a single logic module. The S-module implements the same combinatorial logic function as the C-module while adding a sequential element. The sequential element can be configured as either a D flip-flop or a transparent latch. To increase flexibility, the S-module register can be by-passed so that it implements purely combinatorial logic.

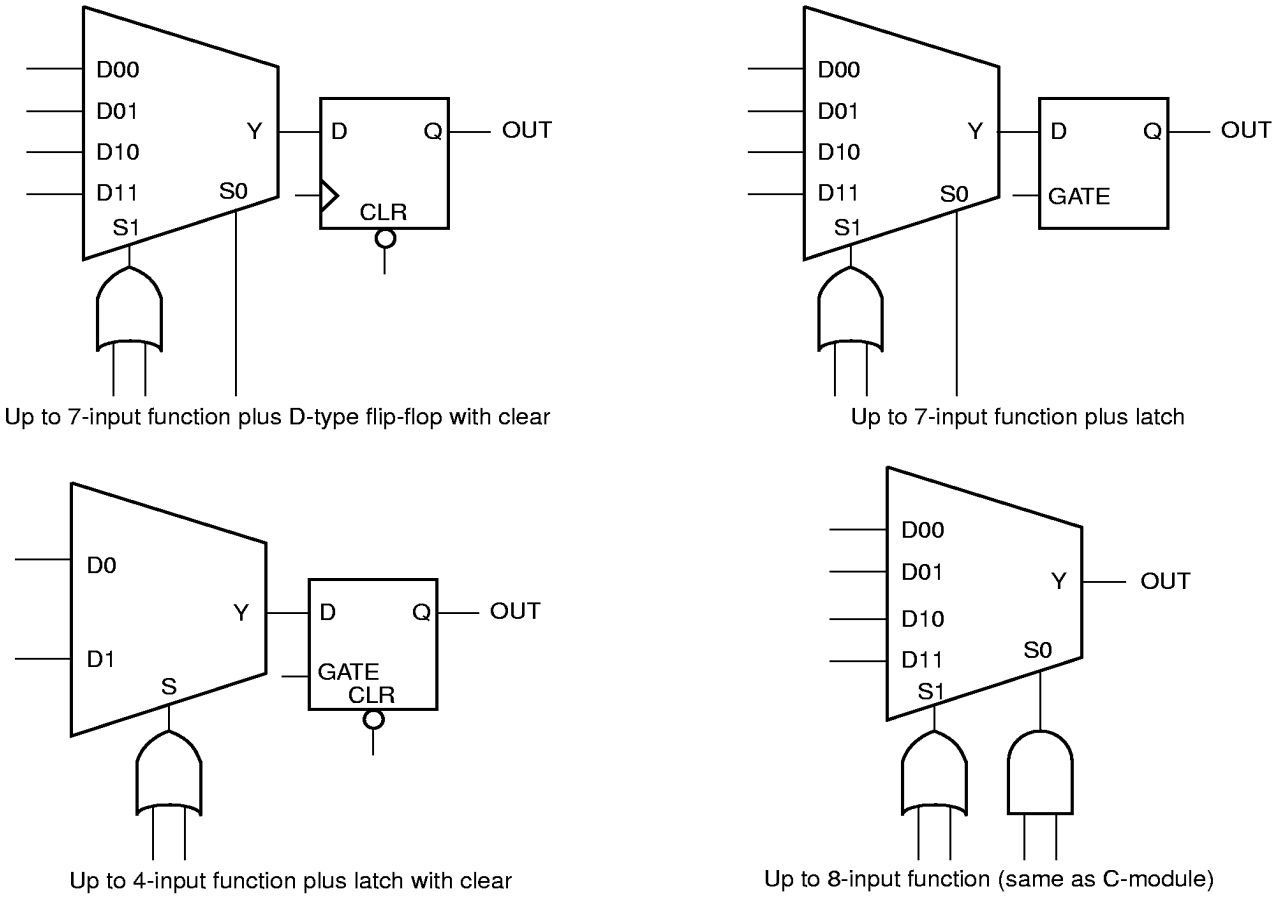


Figure 2 • S-module Implementation

3200DX devices contain a third type of logic module, D-modules, which are arranged around the periphery of device. D-modules contain wide decode circuitry which provides a fast, wide-input AND function similar to that found in product term architectures (Figure 3). The D-module allows 3200DX devices to perform wide decode functions at speeds comparable CPLDs and PAL devices. The output of the D-module has a programmable inverter for active HIGH or LOW assertion. The D-module output is hardwired to an output pin or can be fed back into the array to be incorporated into other logic.

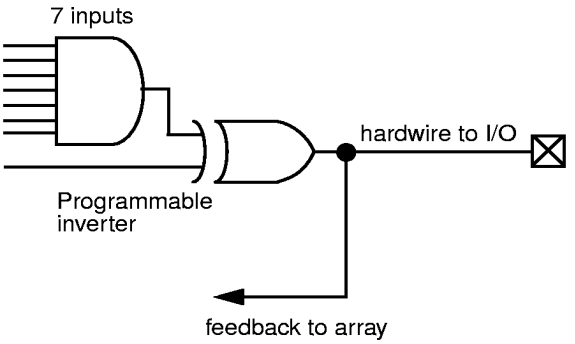


Figure 3 • *D-Module Implementation*

Dual-Port SRAM Modules

Several 3200DX devices contain dual-port SRAM modules that have been optimized for synchronous or asynchronous applications. The SRAM modules are arranged in 256 bit blocks which can be configured as 32 x 8 or 64 x 4 (refer to "Integrator Series Product Profile" on page 1 for the number of SRAM blocks within a particular device). SRAM modules can be cascaded together to form memory spaces of user-definable width and depth. A block diagram of the 3200DX dual-port SRAM block is shown in Figure 4.

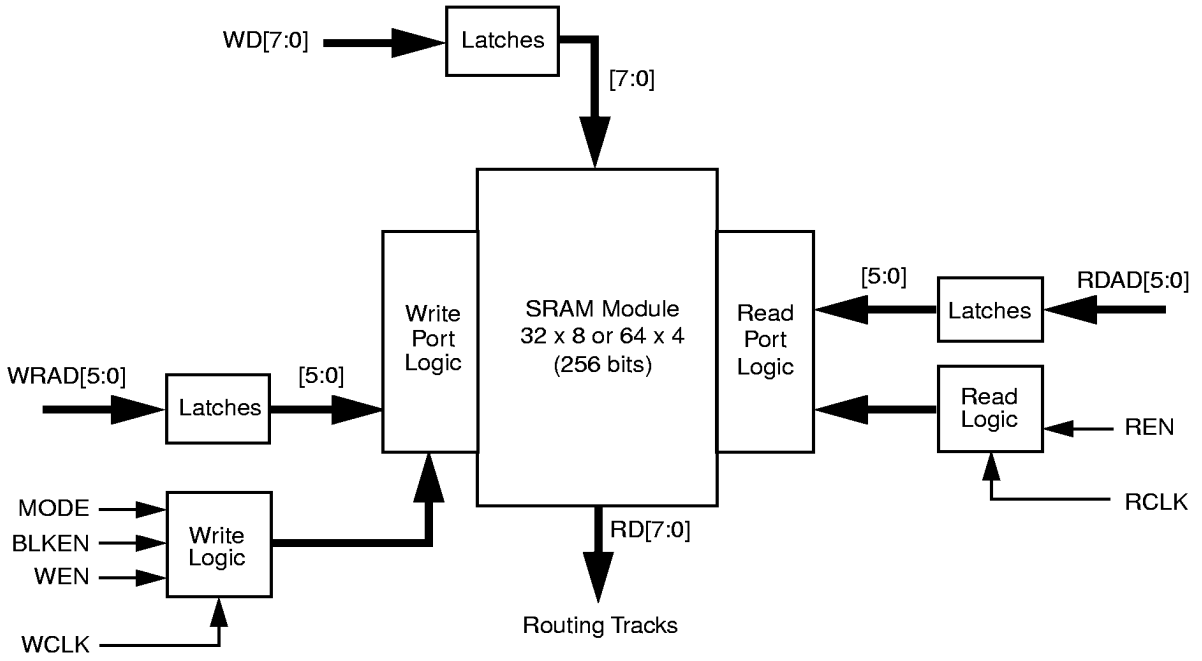


Figure 4 • *3200DX Dual-Port SRAM Block*

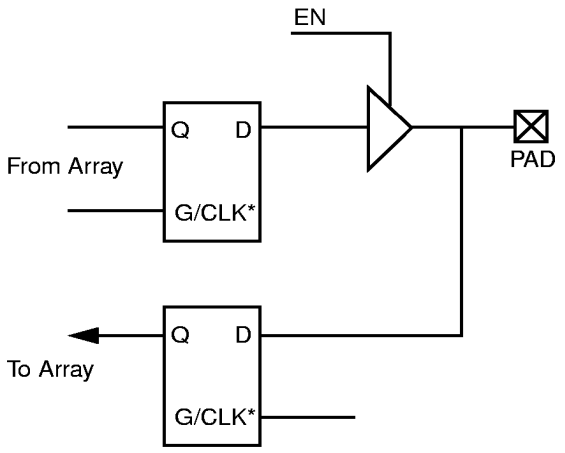
The 3200DX SRAM modules are true dual-port structures containing independent READ and WRITE ports. Each SRAM module contains six bits of read and write addressing (RDAD[5:0] and WRAD[5:0] respectively) for 64x4 bit blocks. When configured in byte mode, the highest order address bits (RDAD5 and WRAD5) are not used. The read and write ports of the SRAM block contain independent clocks (RCLK and WCLK) with programmable polarities offering active HIGH or LOW implementation. The SRAM block contains eight data inputs (WD[7:0]) and eight outputs (RD[7:0]) which are connected to segmented vertical routing tracks.

The 3200DX dual-port SRAM blocks are ideal for high-speed buffered applications requiring fast FIFO and LIFO queues. Actel's ACTGen Macro Builder provides the capability to quickly design memory functions, such as FIFOs, LIFOs, and

RAM arrays. Additionally, unused SRAM blocks need not be wasted since they can be used to implement registers for other logic within the design.

I/O Modules

The I/O modules provide the interface between the device pins and the logic array. Figure 5 is a block diagram of the I/O module. A variety of user functions, determined by a library macro selection, can be implemented in the module (refer to the Macro Library Guide for more information). I/O modules contain a tri-state buffer, input and output latches which can be configured for input, output, or bi-directional pins (Figure 5).



* Can be configured as a Latch or D Flip-Flop (using C-module)

Figure 5 • I/O Module

The Integrator Series devices contain flexible I/O structures in that each output pin has a dedicated output enable control. The I/O module can be used to latch input and/or output data, providing a fast setup time. In addition, the Actel Designer software tools can build a D flip-flop, using a C-module, to register input and/or output signals.

Actel's Designer Series development tools provide a design library of I/O macros. The I/O macro library provides macrofunctions which can implement all I/O configurations supported by the Integrator Series FPGAs.

Routing Structure

The Integrator Series architecture uses Vertical and Horizontal routing tracks to interconnect the various logic and I/O modules. These routing tracks are metal interconnects that may either be of continuous length or broken into pieces called segments. Varying segment lengths allows the interconnect of over 90% of design tracks to occur with only two antifuse connections. Segments can be joined together at the ends, using antifuses, to increase their lengths up to the full length of the track. All interconnects can be accomplished with a maximum of four antifuses.

Horizontal Routing

Horizontal channels are located between the rows of modules and are composed of several routing tracks. The horizontal routing tracks within the channel are divided into one or more segments. The minimum horizontal segment length is the width of a module-pair, and the maximum horizontal segment length is the full length of the channel. Any segment that spans more than one-third the row length is considered a long horizontal segment. A typical channel is shown in Figure 6. Non-dedicated horizontal routing tracks are used to route signal nets. Dedicated routing tracks are used for the global clock networks and for power and ground tie-off tracks.

Vertical Routing

Another set of routing tracks run vertically through the module. Vertical tracks are of three types: input, output, and long. Vertical tracks are also divided into one or more segments. Each segment in an input track is dedicated to the input of a particular module. Each segment in an output track is dedicated to the output of a particular module. Long segments are uncommitted and can be assigned during routing. Each output segment spans four channels (two above and two below), except near the top and bottom of the array where edge effects occur. LVTs contain either one or two segments. An example of vertical routing tracks and segments is shown in Figure 6.

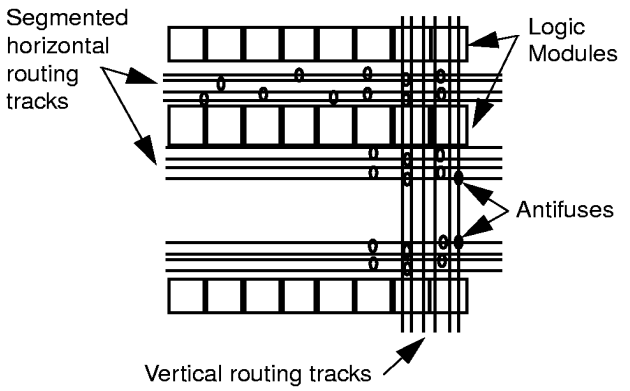


Figure 6 • Routing Structure

Antifuse Structures

An antifuse is a "normally open" structure as opposed to the normally closed fuse structure used in PROMs or PALs. The use of antifuses to implement a Programmable Logic Device results in highly testable structures as well as efficient programming algorithms. The structure is highly testable

because there are no pre-existing connections; therefore, temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed as well as isolate individual circuit structures to be tested. This can be done both before and after programming. For example, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

Clock Networks

Two low-skew, high fanout clock distribution networks are provided in each 3200DX device. These networks are referred to as CLK0 and CLK1. Each network has a clock module (CLKMOD) that selects the source of the clock signal and may be driven as follows:

1. Externally from the CLKA pad
2. Externally from the CLKB pad
3. Internally from the CLKINA input
4. Internally from the CLKINB input

The clock modules are located in the top row of I/O modules. Clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel.

The user controls the clock module by selecting one of two clock macros from the macro library. The macro CLKBUF is used to connect one of the two external clock pins to a clock network, and the macro CLKINT is used to connect an internally generated clock signal to a clock network. Since both clock networks are identical, the user does not care whether CLK0 or CLK1 is being used. The clock input pads may also be used as normal I/Os, bypassing the clock networks (see Figure 7).

The 3200DX devices which contain SRAM modules (all except A3265DX and A32140DX) have four additional register control resources, called Quadrant Clock Networks (Figure 8). Each quadrant clock provides a local, high-fanout resource to the contiguous logic modules within its quadrant of the device. Quadrant clock signals can originate from specific I/O pins or from the internal array and can be used as a secondary register clock, register clear, or output enable.

Test Circuitry

Both 3200DX and 1200XL devices provide the means to test and debug a design once it is programmed into a device. 3200DX and 1200XL devices contain Actel's Actionprobe® test facility. Once a device has been programmed, the Actionprobe test facility allows the designer to probe any internal node during device operation to aid in debugging a design. In addition, 3200DX devices contain JTAG 1149.1 Boundary Scan Test.

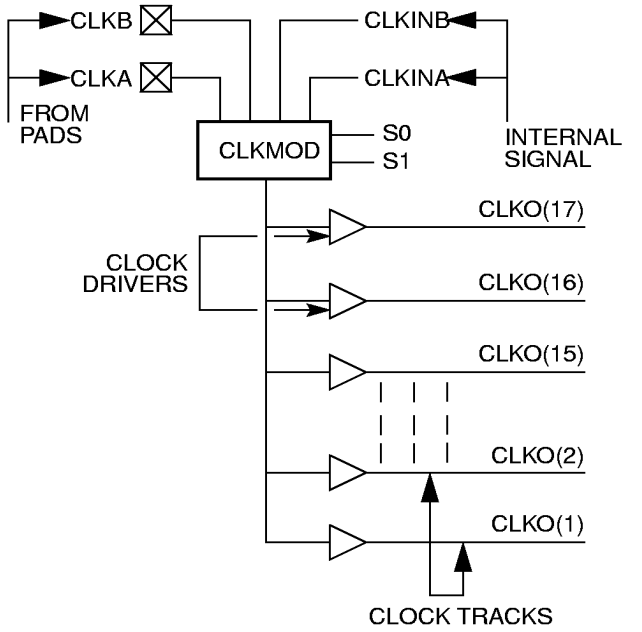


Figure 7 • *Clock Networks*

JTAG Boundary Scan Testing (BST)

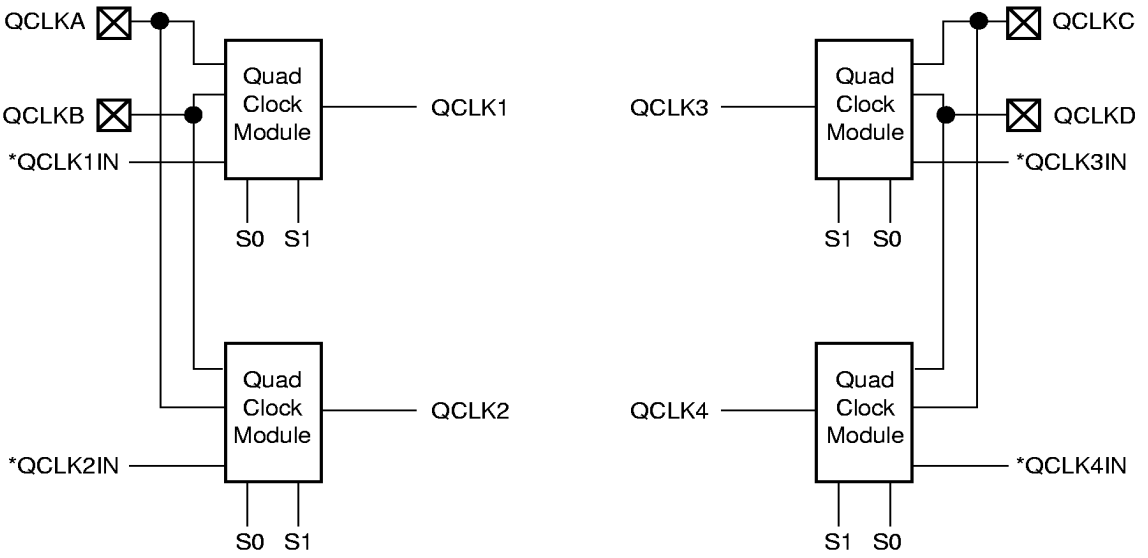
Device pin spacing is decreasing with the advent of fine-pitch packages such as TQFP and BGA packages and manufacturers are routinely implementing surface-mount technology with multi-layer PC boards. Boundary scan is becoming an attractive tool to help systems manufacturers test their PC boards. The Joint Test Action Group (JTAG) developed the IEEE Boundary Scan standard 1149.1 to facilitate board-level testing during manufacturing.

IEEE Standard 1149.1 defines a 4-pin Test Access Port (TAP) interface for testing integrated circuits in a system. The 3200DX family provides four JTAG BST pins: Test Data In (TDI), Test Data Out (TDO), Test Clock (TCLK) and Test Mode Select (TMS). Devices are configured in a JTAG "chain" where BST data can be transmitted serially between devices via TDO to TDI interconnections. The TMS and TCLK signals are shared between all devices in the JTAG chain so that all components operate in the same state.

The 3200DX family implements a subset of the IEEE 1149.1 Boundary Scan Test (BST) instruction in addition to a private instruction to allow the use of Actel's Actionprobe facility with JTAG BST. Refer to the IEEE 1149.1 specification for detailed information regarding JTAG testing.

JTAG Architecture

The 3200DX JTAG BST circuitry consist of a Test Access Port (TAP) controller, JTAG instruction register, JPROBE register, bypass register and boundary scan register. Figure 9 is a block diagram of the 3200DX JTAG circuitry.



**QCLK1IN, QCLK2IN, QCLK3IN, and QCKL4IN are internally generated signals.*

Figure 8 • *Quadrant Clock Network*

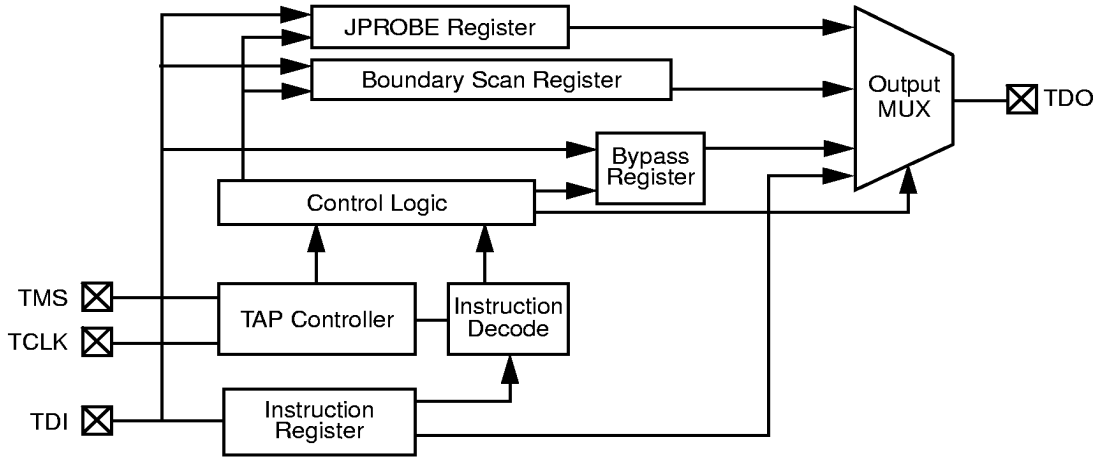


Figure 9 • *JTAG BST Circuitry*

When a device is operating in JTAG BST mode, four I/O pins are used for the TDI, TDO, TMS, and TCLK signals. An active reset (nTRST) pin is not supported, however the 3200DX contains power-on reset circuitry which resets the JTAG BST circuitry upon power-up. During normal device operation, the JTAG pins should be held LOW to disable the JTAG circuitry. The following table summarizes the functions of the JTAG BST signals.

JTAG Signal	Name	Function
TDI	Test Data In	Serial data input for JTAG instructions and data. Data is shifted in on the rising edge of TCLK.
TDO	Test Data Out	Serial data output for JTAG instructions and test data.
TMS	Test Mode Select	Serial data input for JTAG test mode. Data is shifted in on the rising edge of TCLK.
TCLK	Test Clock	Clock signal to shift the JTAG data into the device.

JTAG BST Instructions

JTAG BST testing within the 3200DX devices is controlled by a Test Access Port (TAP) state machine. The TAP controller drives the three-bit instruction register, a bypass register, and the boundary scan data registers within the device. The TAP controller uses the TMS signal to control the JTAG testing of the device. The JTAG test mode is determined by the bit stream entered on the TMS pin. The table in the next column describes the JTAG instructions supported by the 3200DX.

Test Mode	Code	Description
EXTEST	000	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
SAMPLE/ PRELOAD	001	Allows a snapshot of the signals at the device pins to be captured and examined during device operation.
INTEST	010	Refer to IEEE 1149.1 Specification
JPROBE	011	A private instruction allowing the user to connect Actel's Micro Probe registers to the JTAG chain.
USER INSTRUCTION	100	Allows the user to build application-specific instructions such as RAM READ and RAM WRITE.
HIGH Z	101	Refer to IEEE 1149.1 Specification
CLAMP	110	Refer to IEEE 1149.1 Specification
BYPASS	111	Enables the by bypass register between the TDI and TDO pins. The test data passes through the selected device to adjacent devices in the JTAG chain.

Actionprobe

If a device has been successfully programmed and the security fuse has not been programmed, any internal logic or I/O module output can be observed using the Actionprobe circuitry and the PRA and/or PRB pins. The Actionprobe diagnostic system provides the software and hardware required to perform real-time debugging. Refer to "Using the Actionprobe for System-Level Debug" application note on page 4-123 for further information.

5.0V Operating Conditions

Absolute Maximum Ratings[1]

Free air temperature range

Symbol	Parameter	Limits	Units
V_{CC}	DC Supply Voltage	–0.5 to +7.0	V
V_I	Input Voltage	–0.5 to V_{CC} +0.5	V
V_O	Output Voltage	–0.5 to V_{CC} +0.5	V
I_{IO}	I/O Source/Sink Current[2]	±20	mA
T_{STG}	Storage Temperature	–65 to +150	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.*
2. *Device inputs are normally high impedence and draw extremely low current. However, when input voltage is greater than V_{CC} + 0.5 V or less than GND – 0.5 V, the internal protection diode will be forward biased and can draw excessive current.*

Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature Range[1]	0 to +70	–40 to +85	–55 to +125	°C
Power Supply Tolerance	±5	±10	±10	%V_{CC}

Note:

1. *Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.*

Electrical Specifications

Symbol	Parameter	Commercial		Commercial –F		Industrial		Military		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}[1]	(I_{OH} = –10 mA)[2]	2.4		2.4						V
	(I_{OH} = –6 mA)	3.84		3.84						V
	(I_{OH} = –4 mA)					3.7		3.7		V
V_{OL}[1]	(I_{OL} = 10 mA)[2]		0.5		0.5					V
	(I_{OL} = 6 mA)		0.33		0.33		0.40		0.40	V
V_{IL}		–0.3	0.8	–0.3	0.8	–0.3	0.8	–0.3	0.8	V
V_{IH}		2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
Input Transition Time t_R, t_F[2]			500		500		500		500	ns
C_{IO} I/O Capacitance[2, 3]			10		10		10		10	pF
Standby Current, I_{CC}[4] (typical = 1 mA)			1.5		20		10		20	mA
$I_{CC(D)}$ Dynamic V_{CC} Supply Current		See "Power Dissipation" on page 1-21								

Notes:

1. *Only one output tested at a time. V_{CC} = min.*
2. *Not tested, for information only.*
3. *Includes worst-case 176 CPGA package capacitance. V_{OUT} = 0 V, f = 1 MHz.*
4. *All outputs unloaded. All inputs = V_{CC} or GND, typical I_{CC} = 1 mA. I_{CC} limit includes I_{PP} and I_{SV} during normal operation.*

3.3V Operating Conditions

Absolute Maximum Ratings[1]

Free air temperature range

Symbol	Parameter	Limits	Units
V_{CC}	DC Supply Voltage	–0.5 to +7.0	V
V_I	Input Voltage	–0.5 to V_{CC} +0.5	V
V_O	Output Voltage	–0.5 to V_{CC} +0.5	V
I_{IO}	I/O Source Sink Current[2]	±20	mA
T_{STG}	Storage Temperature	–65 to +150	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.*
2. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than V_{CC} + 0.5 V or less than GND – 0.5 V, the internal protection diodes will forward bias and can draw excessive current.*

Recommended Operating Conditions

Parameter	Commercial	Units
Temperature Range[1]	0 to +70	°C
Power Supply Tolerance	±5	%V

Note:

1. *Ambient temperature (T_A) is used for commercial.*

Electrical Specifications

Parameter		Commercial		Units
		Min.	Max.	
V_{OH}[1]	(I_{OH} = –4 mA)	2.15		V
	(I_{OH} = –3.2 mA)	2.4		V
V_{OL}[1]	(I_{OL} = 6 mA)		0.4	V
V_{IL}		–0.3	0.8	V
V_{IH}		2.0	V_{CC} + 0.3	V
Input Transition Time t_R, t_F[2]			500	ns
C_{IO} I/O Capacitance[2, 3]			10	pF
Standby Current, I_{CC}[4] (typical = 0.3 mA)			0.75	mA
$I_{CC(D)}$ Dynamic V_{CC} Supply Current		See "Power Dissipation" on page 1-21		

Notes:

1. *Only one output tested at a time. V_{CC} = min.*
2. *Not tested, for information only.*
3. *Includes worst-case 84-pin PLCC package capacitance. V_{OUT} = 0 V, f = 1 MHz.*
4. *Typical standby current = 0.3 mA. All outputs unloaded. All inputs = V_{CC} or GND.*

Package Thermal Characteristics

The device junction to case thermal characteristic is θjc, and the junction to ambient air characteristic is θja. The thermal characteristics for θja are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a PQFP 160-pin package at commercial temperature is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. commercial temp.}}{\theta ja\ (°C/W)} = \frac{150°C - 70°C}{30°C/W} = 2.6W$$

Package Type	Pin Count	θja		Maximum Power Dissipation	
		Still Air	300 ft/min	Still Air	300 ft/min
Plastic Quad Flatpack	160	36 °C/W	30 °C/W	2.2 W	2.6 W
Plastic Quad Flatpack	208	25 °C/W	16.2 °C/W	3.2 W	4.9 W
Plastic Leaded Chip Carrier	84	37 °C/W	28 °C/W	2.2 W	2.9 W
Thin Quad Flatpack	176	32 °C/W	25 °C/W	2.5 W	3.2 W
Power Quad Flatpack	208	16.8 °C/W	11.4 °C/W	4.8 W	7.0 W
Power Quad Flatpack	240	16.1 °C/W	10.6 °C/W	5.0 W	7.5 W
Ball Grid Array	240	14.0 °C/W	10.0 °C/W	5.7 W	8.0 W
Ball Grid Array	432	10.0 °C/W	8.0 ° C/W	8.0 W	10.0 W

Power Dissipation

General Power Equation

$$P = [I_{CC}standby + I_{CC}active] * V_{CC} + I_{OL} * V_{OL} * N + I_{OH} * (V_{CC} - V_{OH}) * M$$

where:

I_{CC}standby is the current flowing when no inputs or outputs are changing.

I_{CC}active is the current flowing due to CMOS switching.

I_{OL}, I_{OH} are TTL sink/source currents.

V_{OL}, V_{OH} are TTL level output voltages.

N equals the number of outputs driving TTL loads to V_{OL}.

M equals the number of outputs driving TTL loads to V_{OH}.

An accurate determination of N and M is problematic because their values depend on the family type, design details, and on the system I/O. The power can be divided into two components: static and active.

Static Power Component

Actel FPGAs have small static power components that result in lower power dissipation than PALs or PLDs. By integrating multiple PALs/PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. Standby power is calculated below for commercial, worst case conditions.

I_{CC}	V_{CC}	Power
2 mA	5.25 V	10.5 mW

The static power dissipation by TTL loads depends on the number of outputs driving high or low and the DC load current. Again, this number is typically small. For instance, a 32-bit bus sinking 4 mA at 0.33 V will generate 42 mW with all outputs driving low and 140 mW with all outputs driving high. The actual dissipation will average somewhere between as I/Os switch states with time.

Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency dependent, a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs. An additional component of the active power dissipation is the totem-pole current in the CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by Equation 1.

$$\text{Power } (\mu W) = C_{EQ} * V_{CC}^2 * F \quad (1)$$

where:

C_{EQ} is the equivalent capacitance expressed in picofarads (pF).

V_{CC} is power supply in volts (V).

F is the switching frequency in megahertz (MHz).

Equivalent capacitance is calculated by measuring $I_{CCactive}$ at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of V_{CC}. Equivalent capacitance is frequency independent so that the results may be used over a wide range of operating conditions. Equivalent capacitance values are shown below.

C_{EQ} Values for Actel FPGAs

Modules (C_{EQM})	5.2
Input Buffers (C_{EQI})	11.6
Output Buffers (C_{EQO})	23.8
Routed Array Clock Buffer Loads (C_{EQCR})	3.5

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. Equation 2 shows a piece-wise linear summation over all components.

$$\text{Power} = V_{CC}^2 * [(m \times C_{EQM} * f_m)_{Modules} + (n * C_{EQI} * f_n)_{Inputs} + (p * (C_{EQO} + C_L) * f_p)_{outputs} + 0.5 * (q_1 * C_{EQCR} * f_{q1})_{routed\_Clk1} + (r_1 * f_{q1})_{routed\_Clk1} + 0.5 * (q_2 * C_{EQCR} * f_{q2})_{routed\_Clk2} + (r_2 * f_{q2})_{routed\_Clk2} \quad (2)$$

where:

m = Number of logic modules switching at frequency f_m

n = Number of input buffers switching at frequency f_n

p = Number of output buffers switching at frequency f_p

q_1 = Number of clock loads on the first routed array clock

q_2 = Number of clock loads on the second routed array clock

r_1 = Fixed capacitance due to first routed array clock

r_2 = Fixed capacitance due to second routed array clock

C_{EQM} = Equivalent capacitance of logic modules in pF

C_{EQI} = Equivalent capacitance of input buffers in pF

C_{EQO} = Equivalent capacitance of output buffers in pF

C_{EQCR} = Equivalent capacitance of routed array clock in pF

C_L = Output load capacitance in pF

f_m = Average logic module switching rate in MHz

f_n = Average input buffer switching rate in MHz

f_p = Average output buffer switching rate in MHz

f_{q1} = Average first routed array clock rate in MHz

f_{q2} = Average second routed array clock rate in MHz

Fixed Capacitance Values for Actel FPGAs (pF)

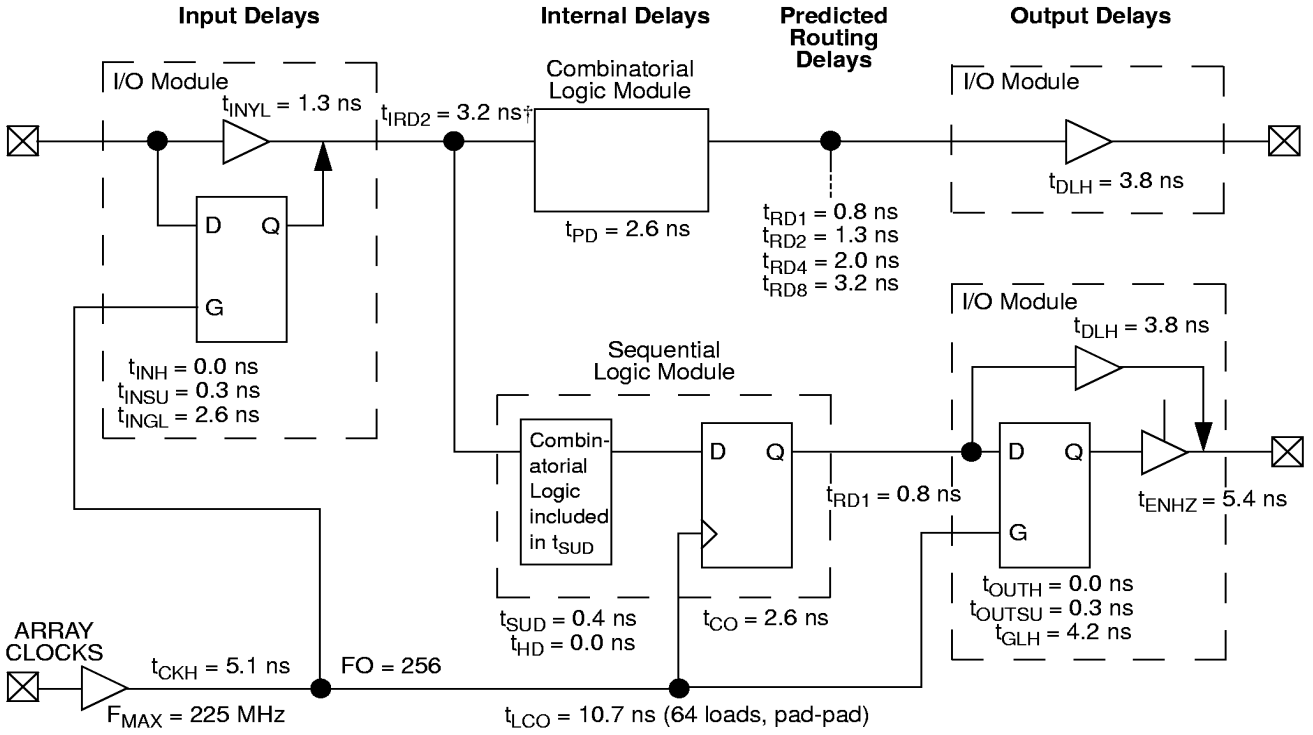
Device Type	r_1 routed_Clk1	r_2 routed_Clk2
A1225XL	106	106
A1240XL	134	134
A3265DX	158	158
A1280XL	168	168
A32100DX	178	178
A32140DX	190	190
A32200DX	230	230
A32300DX	285	285

Determining Average Switching Frequency

To determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are as follows:

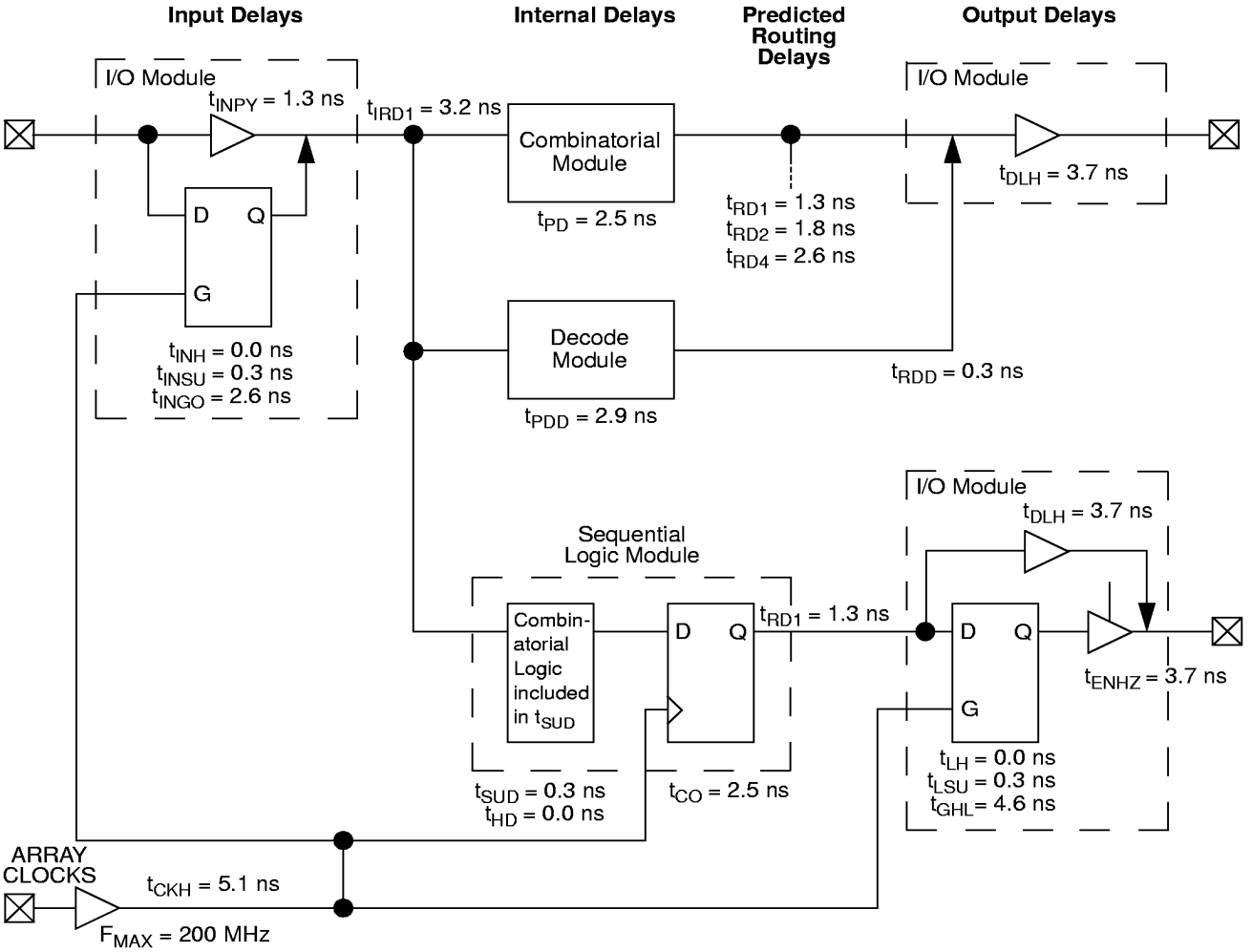
Logic Modules (m)	= 80% of combinatorial modules
Inputs switching (n)	= # of inputs/4
Outputs switching (p)	= # outputs/4
First routed array clock loads (q_1)	= 40% of sequential modules
Second routed array clock loads (q_2)	= 40% of sequential modules
Load capacitance (C_L)	= 35 pF
Average logic module switching rate (f_m)	= F/10
Average input switching rate (f_n)	= F/5
Average output switching rate (f_p)	= F/10
Average first routed array clock rate (f_{q1})	= F
Average second routed array clock rate (f_{q2})	= F/2

1200XL Timing Model*



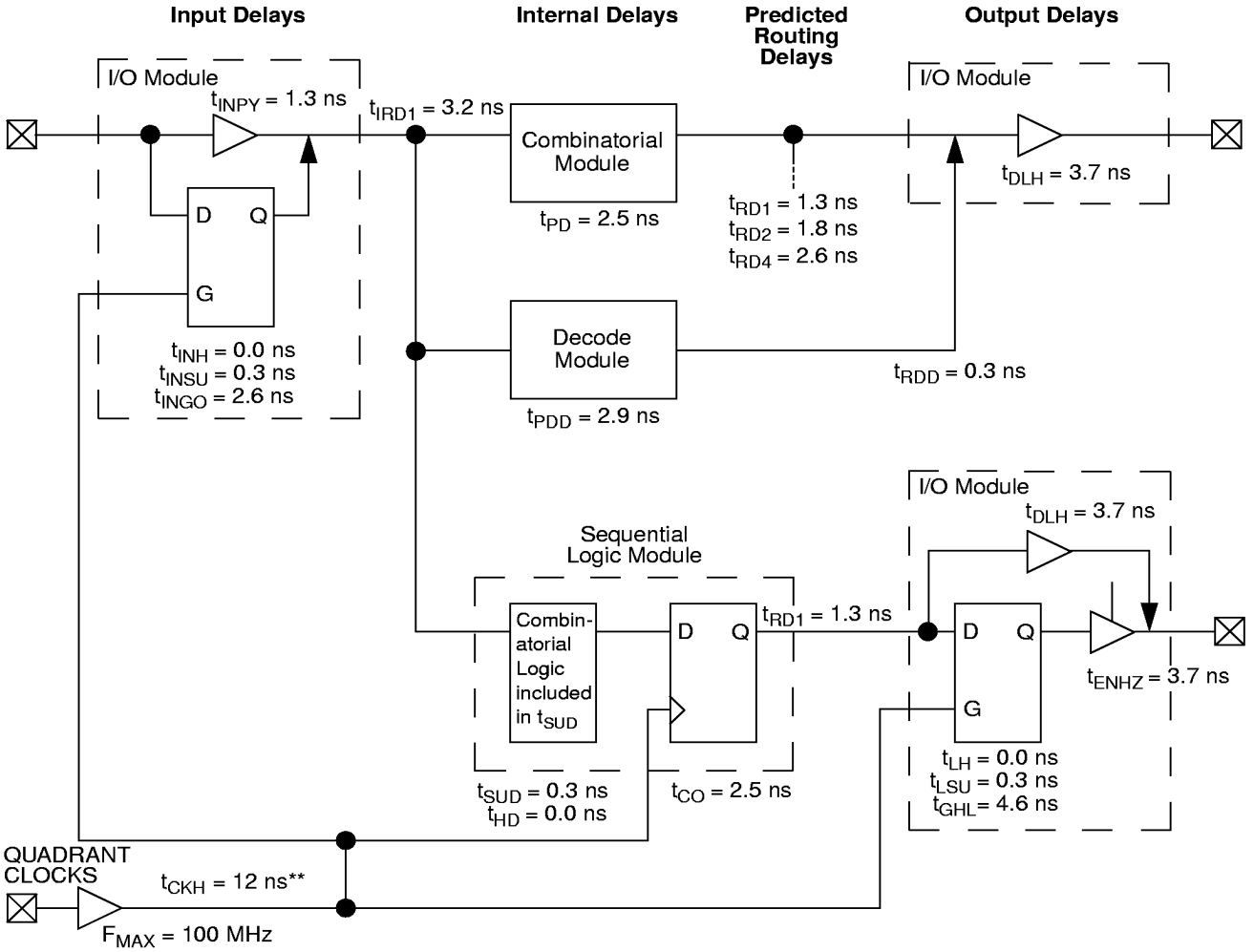
**Values shown for A1225XL-2 at worst-case commercial conditions.* *† Input Module Predicted Routing Delay*

3200DX Timing Model (Logic Functions using Array Clocks)*



**Values shown for A3265DX-2 at worst-case commercial conditions.*

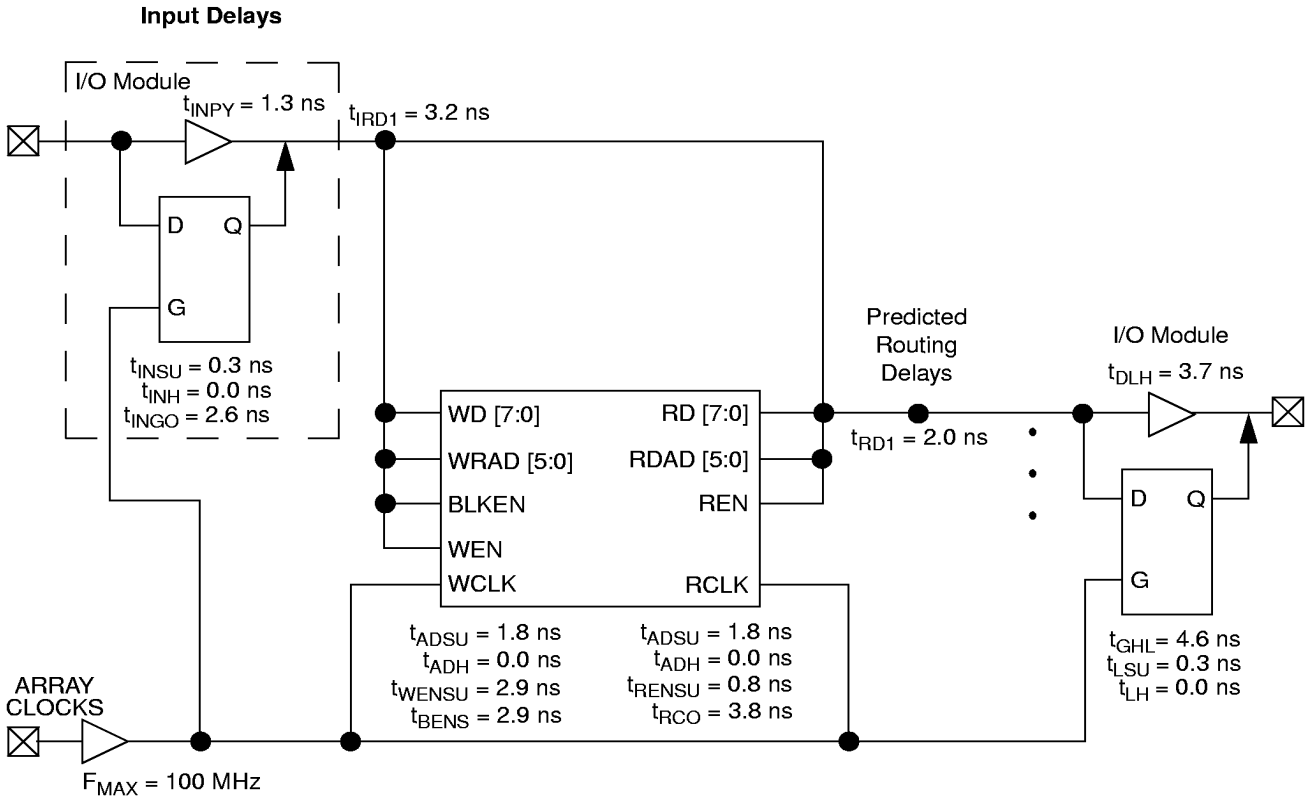
3200DX Timing Model (Logic Functions using Quadrant Clocks)*



** Preliminary values shown for A32200DX-2 at worst-case commercial conditions.*

*** Load dependent.*

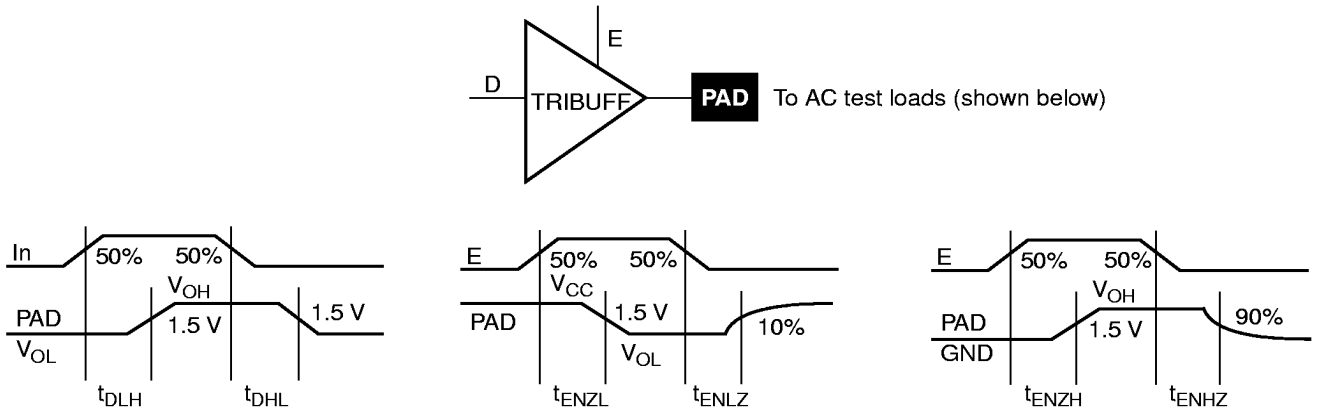
3200DX Timing Model (SRAM Functions)*



**Values shown for A32200DX-2 at worst-case commercial conditions.*

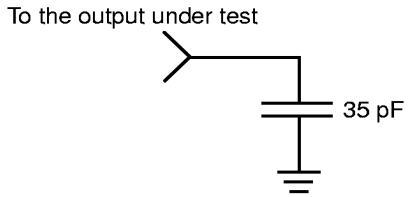
Parameter Measurement

Output Buffer Delays

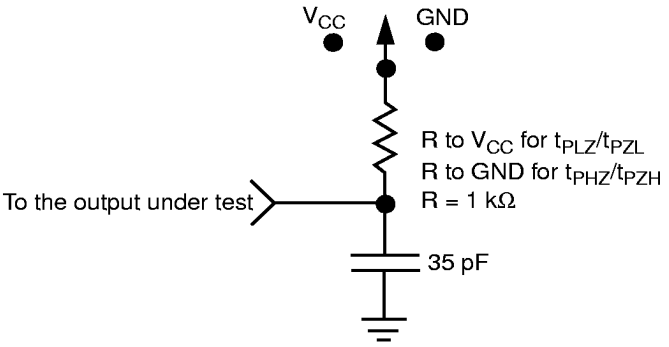


AC Test Loads

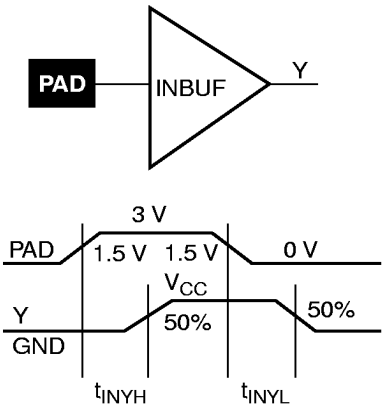
Load 1
(Used to measure propagation delay)



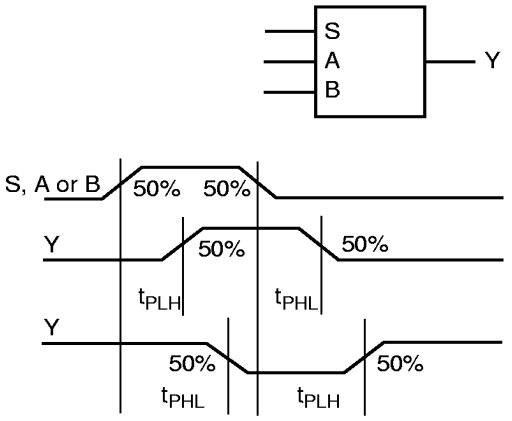
Load 2
(Used to measure rising/falling edges)



Input Buffer Delays

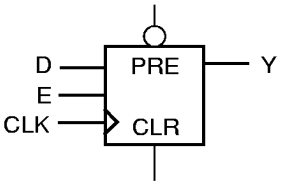


Module Delays

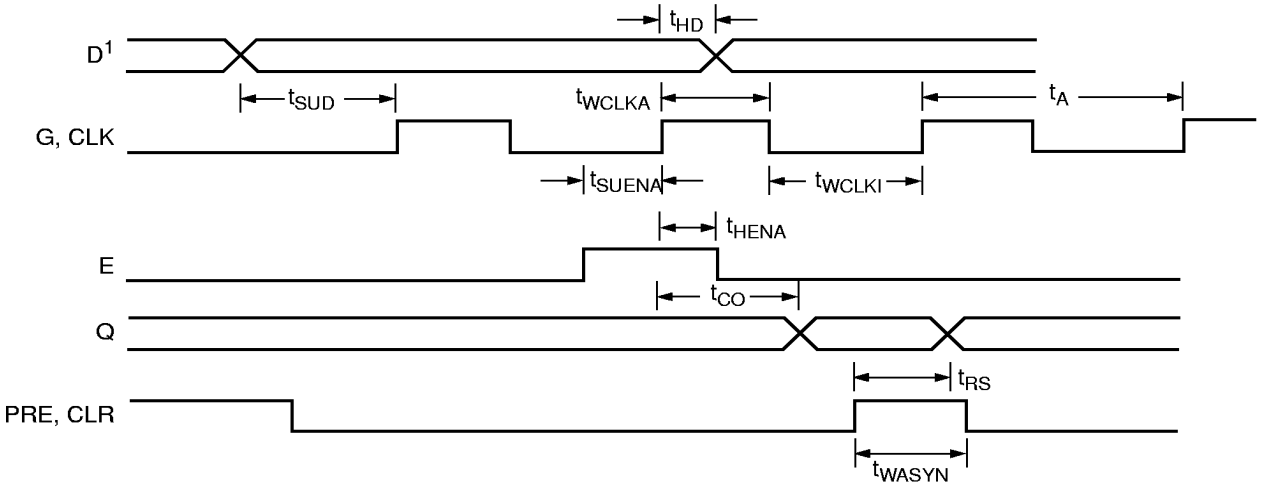


Sequential Module Timing Characteristics

Flip-Flops and Latches



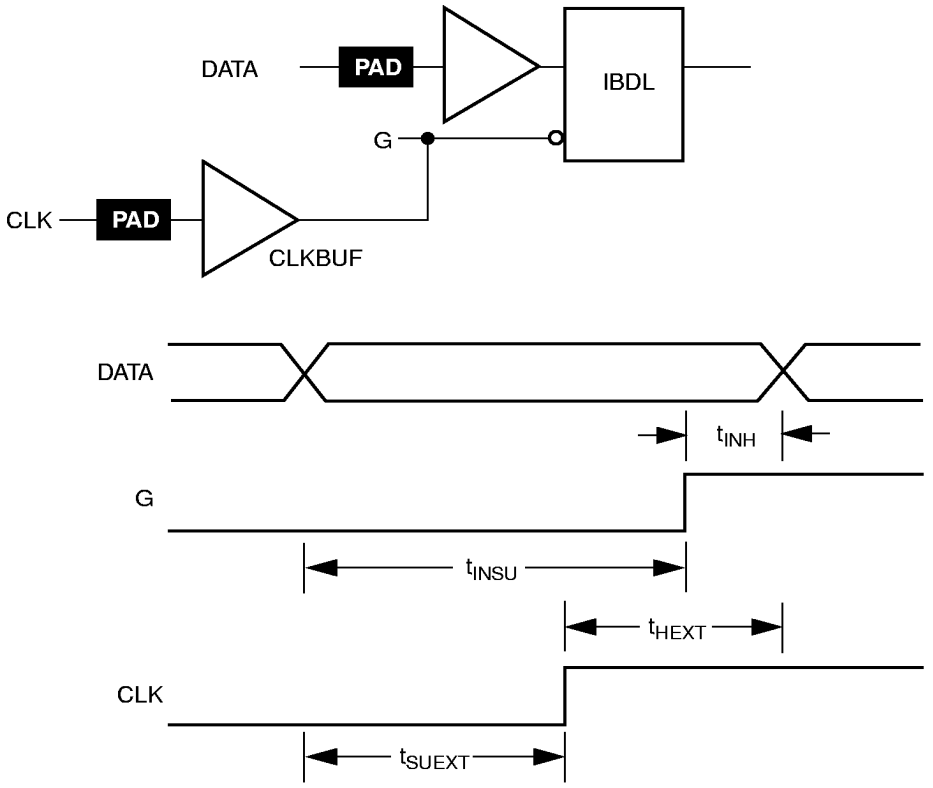
(Positive edge triggered)



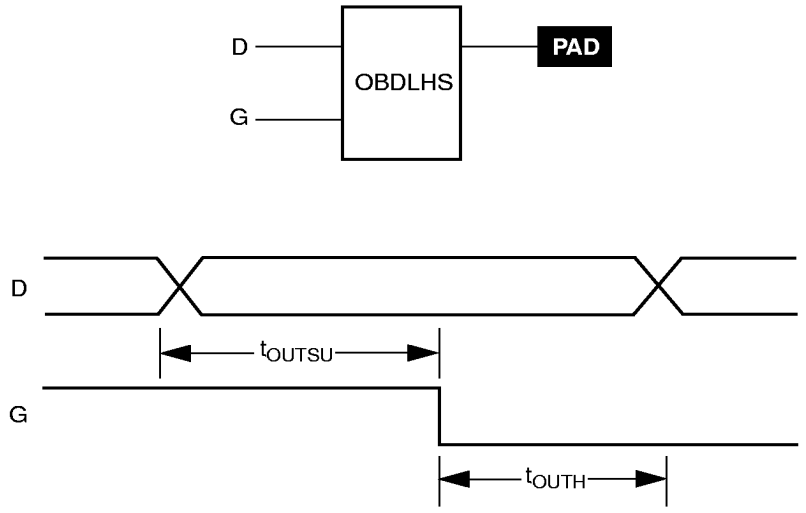
Note: *D represents all data functions involving A, B, and S for multiplexed flip-flops.*

Sequential Timing Characteristics (continued)

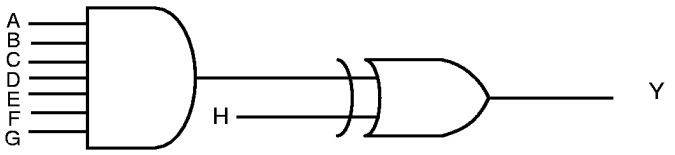
Input Buffer Latches

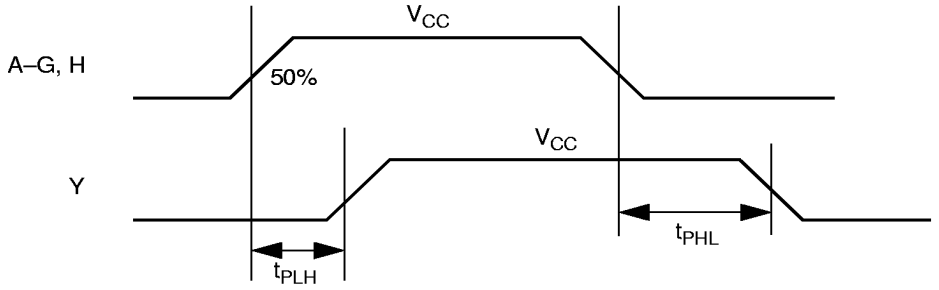


Output Buffer Latches

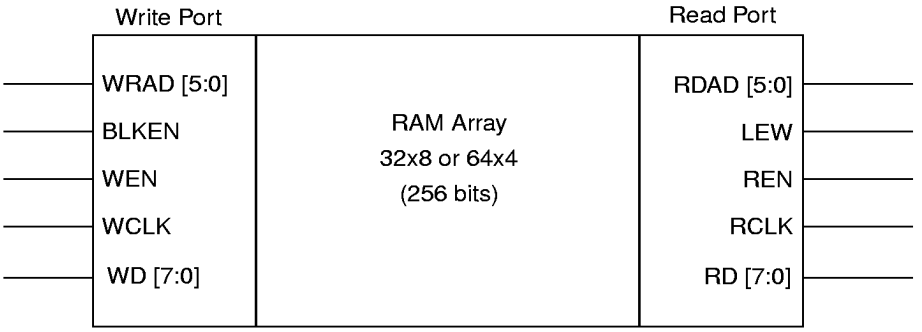


Decode Module Timing



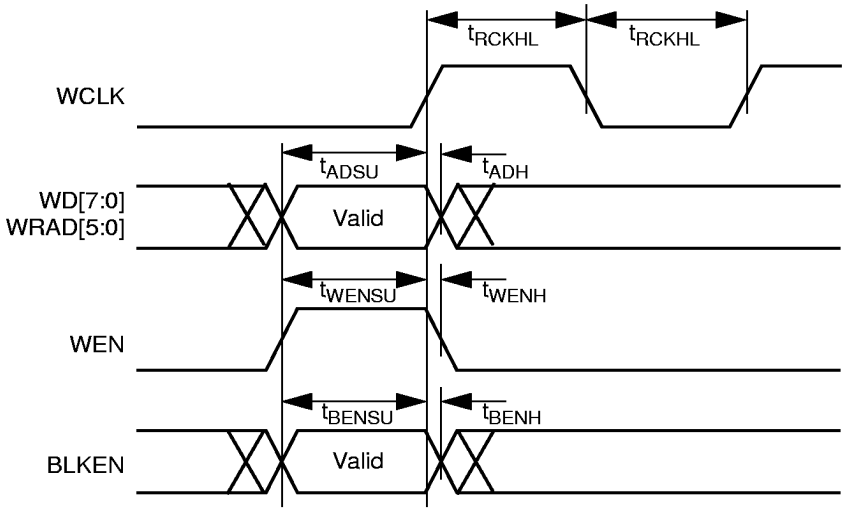


SRAM Timing Characteristics



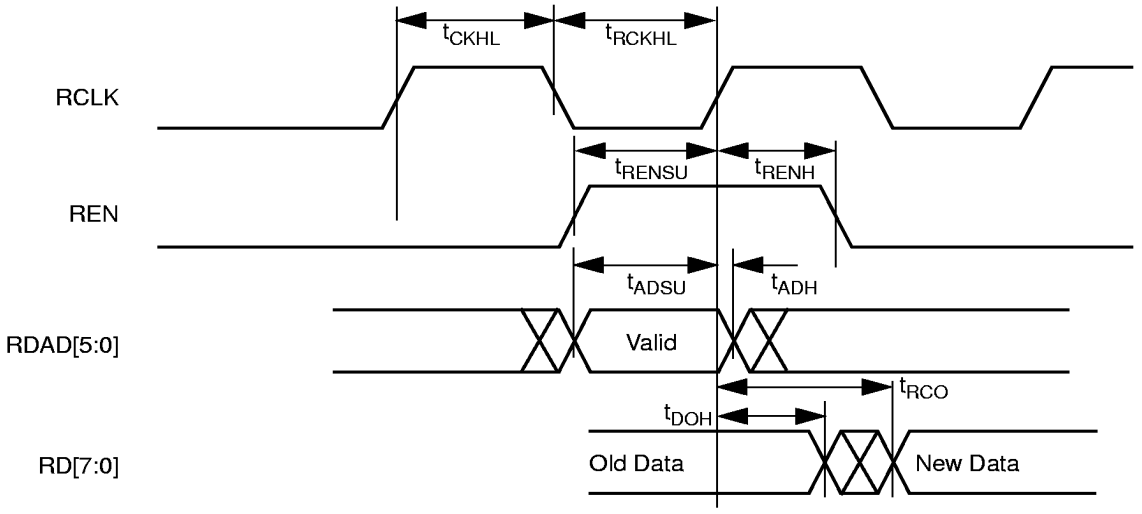
Dual-Port SRAM Timing Waveforms

3200DX SRAM Write Operation



Note: *Identical timing for falling-edge clock.*

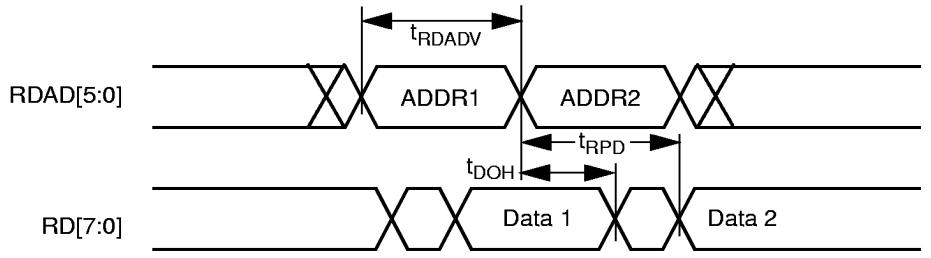
3200DX SRAM Synchronous Read Operation



Note: *Identical timing for falling-edge clock.*

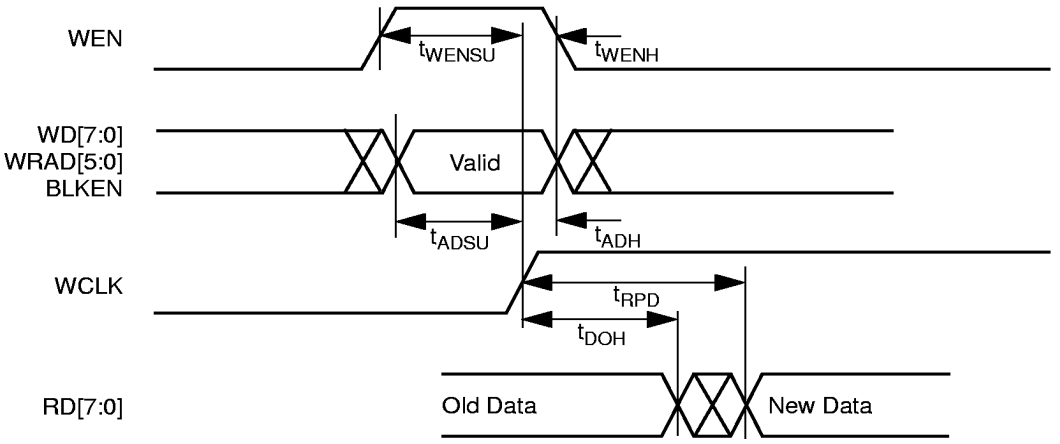
3200DX SRAM Asynchronous Read Operation—Type 1

(Read Address Controlled)



3200DX SRAM Asynchronous Read Operation—Type 2

(Write Address Controlled)



Predictable Performance: Tight Delay Distributions

Propagation delay between logic modules depends on the resistive and capacitive loading of the routing tracks, the interconnect elements, and the module inputs being driven. Propagation delay increases as the length of routing tracks, the number of interconnect elements, or the number of inputs increases.

From a design perspective, the propagation delay can be statistically correlated or modeled by the fanout (number of loads) driven by a module. Higher fanout usually requires some paths to have longer routing tracks.

The Integrator Series delivers a very tight fanout delay distribution. This tight distribution is achieved in two ways: by decreasing the delay of the interconnect elements and by decreasing the number of interconnect elements per path.

Actel's patented PLICE antifuse offers a very low resistive/capacitive interconnect. The antifuses, fabricated in 0.6 micron lithography, offer nominal levels of 100 ohms resistance and 7.0 femtofarad (fF) capacitance per antifuse.

The Integrator Series fanout distribution is also tight due to the low number of antifuses required for each interconnect path. The proprietary architecture limits the number of antifuses per path to a maximum of four, with 90% of interconnects using two antifuses.

Timing Characteristics

Timing characteristics for devices fall into three categories: family dependent, device dependent, and design dependent. The input and output buffer characteristics are common to all Integrator Series members. Internal routing delays are device dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design is complete. Delay values may then be determined by using the Designer Series utility or performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Since the architecture provides deterministic timing and abundant routing resources, Actel's Designer Series development tools offers DirectTime; a timing-driven place and route tool. Using DirectTime, the designer may specify timing-critical nets and system clock frequency. Using these timing specifications, the place and route software optimized the layout of the design to meet the user's specifications.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes four antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6% of nets in a fully utilized device require long tracks. Long tracks contribute approximately 3 ns to 6 ns delay. This additional delay is represented statistically in higher fanout (FO=8) routing delays in the data sheet specifications section.

Timing Derating

A best case timing derating factor of 0.45 is used to reflect best case processing. Note that this factor is relative to the "standard speed" timing parameters, and must be multiplied by the appropriate voltage and temperature derating factors for a given application.

Timing Derating Factor (Temperature and Voltage)

	Industrial		Military	
	Min.	**Max.**	**Min.**	**Max.**
(Commercial Specification) x	0.69	1.11	0.67	1.23

Timing Derating Factor for Designs at Typical Temperature (T_J = 25°C) and Voltage (5.0 V)

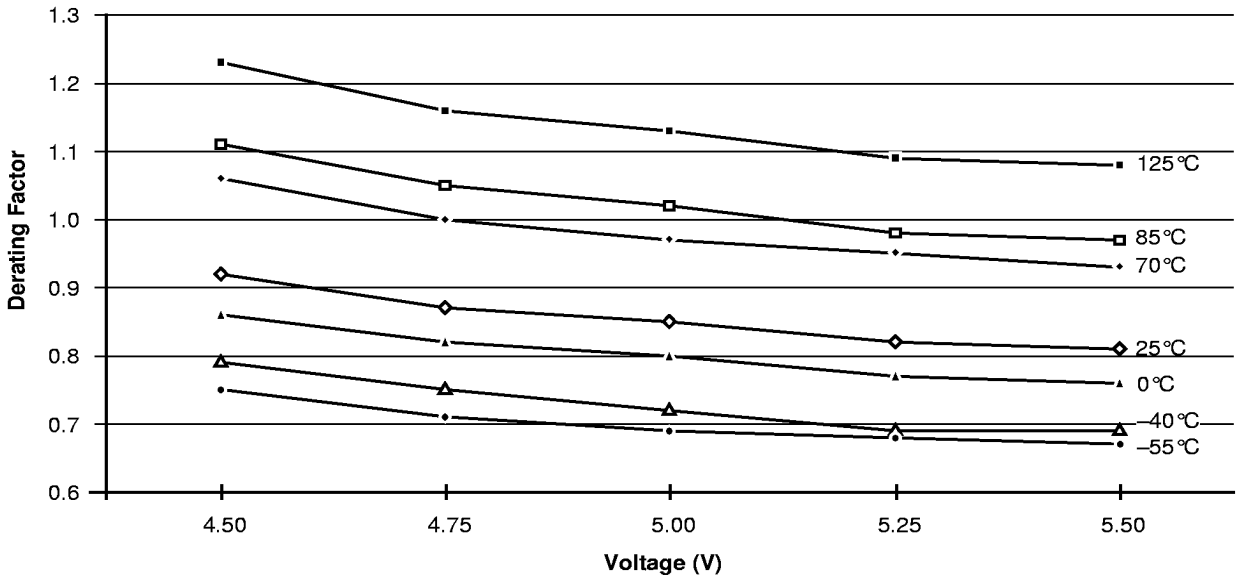
(Maximum Specification, Worst-Case Condition) x	0.85

Note: *This derating factor applies to all routing and propagation delays.*

Temperature and Voltage Derating Factors (normalized to Worst-Case Commercial, T_J = 4.75 V, 70°C)

	–55	–40	0	25	70	85	125
4.50	0.75	0.79	0.86	0.92	1.06	1.11	1.23
4.75	0.71	0.75	0.82	0.87	1.00	1.05	1.16
5.00	0.69	0.72	0.80	0.85	0.97	1.02	1.13
5.25	0.68	0.69	0.77	0.82	0.95	0.98	1.09
5.50	0.67	0.69	0.76	0.81	0.93	0.97	1.08

Junction Temperature and Voltage Derating Curves (normalized to Worst-Case Commercial, T_J = 4.75 V, 70°C)



Note: *This derating factor applies to all routing and propagation delays.*

A1225XL Timing Characteristics

(Worst-Case Commercial Conditions, V_{CC} = 4.75 V, T_J = 70°C)

Logic Module Propagation Delays[1]		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		3.3V Speed[5]		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD1}	Single Module		2.6		3.0		3.5		5.0		4.2	ns
t_{CO}	Sequential Clk to Q		2.6		3.0		3.5		5.0		4.2	ns
t_{GO}	Latch G to Q		2.6		3.0		3.5		5.0		4.2	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		2.6		3.0		3.5		5.0		4.2	ns
Predicted Routing Delays[2]												
t_{RD1}	FO=1 Routing Delay		0.8		0.9		1.1		1.57		1.3	ns
t_{RD2}	FO=2 Routing Delay		1.3		1.4		1.7		2.43		2.0	ns
t_{RD3}	FO=3 Routing Delay		1.7		1.8		2.2		3.15		2.6	ns
t_{RD4}	FO=4 Routing Delay		2.0		2.3		2.7		3.86		3.2	ns
t_{RD8}	FO=8 Routing Delay		3.2		3.5		4.2		6.00		5.0	ns
Sequential Timing Characteristics[3,4]												
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.4		0.4		0.5		0.7		0.6		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	0.8		0.9		1.0		1.4		1.2		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.2		3.6		4.3		6.1		5.2		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	3.2		3.6		4.3		6.1		5.2		ns
t_A	Flip-Flop Clock Input Period	6.5		7.4		8.7		12.4		10.4		ns
t_{INH}	Input Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Buffer Latch Setup	0.3		0.4		0.4		0.6		0.5		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Setup	0.3		0.4		0.4		0.6		0.5		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		225.0		200.0		170.0		120.0		115.0	MHz

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*
5. *V_{CC} = 3.0 V for 3.3V specifications.*

A1225XL Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

Input Module Propagation Delays			'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		3.3V Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Pad to Y High			1.1		1.2		1.4		2.0		1.7	ns
t_{INYL}	Pad to Y Low			1.3		1.4		1.7		2.4		2.0	ns
t_{INGH}	G to Y High			2.0		2.3		2.7		3.9		3.2	ns
t_{INGL}	G to Y Low			2.6		3.0		3.5		5.0		4.2	ns
Input Module Predicted Routing Delays[1]													
t_{IRD1}	FO=1 Routing Delay			2.9		3.3		3.9		5.6		4.7	ns
t_{IRD2}	FO=2 Routing Delay			3.2		3.6		4.3		6.1		5.2	ns
t_{IRD3}	FO=3 Routing Delay			3.8		4.2		5.0		7.2		6.0	ns
t_{IRD4}	FO=4 Routing Delay			4.1		4.6		5.4		7.7		6.5	ns
t_{IRD8}	FO=8 Routing Delay			5.2		5.9		6.9		9.9		8.3	ns
Global Clock Network													
t_{CKH}	Input Low to High	FO = 32		5.1		5.8		6.8		9.7		8.2	ns
		FO = 256		5.7		6.5		7.6		10.9		9.1	
t_{CKL}	Input High to Low	FO = 32		5.0		5.7		6.7		9.6		8.0	ns
		FO = 256		5.7		6.5		7.6		10.9		9.1	
t_{PWH}	Minimum Pulse Width High	FO = 32	2.6		3.0		3.5		5.0		4.2		ns
		FO = 256	2.7		3.1		3.6		5.1		4.3		
t_{PWL}	Minimum Pulse Width Low	FO = 32	2.6		3.0		3.5		5.0		4.2		ns
		FO = 256	2.7		3.1		3.6		5.1		4.3		
t_{CKSW}	Maximum Skew	FO = 32		0.8		0.9		1.0		1.4		1.2	ns
		FO = 256		0.8		0.9		1.0		1.4		1.2	
t_{SUEXT}	Input Latch External Setup	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 256	0.0		0.0		0.0		0.0		0.0		
t_{HEXT}	Input Latch External Hold	FO = 32	2.6		2.9		3.4		4.9		4.1		ns
		FO = 256	3.2		3.7		4.3		6.1		5.2		
t_P	Minimum Period	FO = 32	5.4		6.1		7.2		10.3		8.6		ns
		FO = 256	5.6		6.3		7.4		10.6		8.9		
f_{MAX}	Maximum Frequency	FO = 32		225.0		200.0		170.0		120.0		115.0	MHz
		FO = 256		200.0		180.0		155.0		105.0		105.0	

Note:

1. These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 3 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A1225XL Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

Output Module Timing		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		3.3V Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]												
t_{DLH}	Data to Pad High		3.8		4.3		5.0		7.1		6.0	ns
t_{DHL}	Data to Pad Low		4.1		4.6		5.4		7.7		6.5	ns
t_{ENZH}	Enable Pad Z to High		3.8		4.3		5.0		7.1		6.0	ns
t_{ENZL}	Enable Pad Z to Low		4.1		4.7		5.5		7.9		6.5	ns
t_{ENHZ}	Enable Pad High to Z		5.4		6.1		7.2		10.3		8.6	ns
t_{ENLZ}	Enable Pad Low to Z		5.4		6.1		7.2		10.3		8.6	ns
t_{GLH}	G to Pad High		4.2		4.8		5.6		8.0		6.7	ns
t_{GHL}	G to Pad Low		4.7		5.4		6.3		9.0		7.6	ns
t_{LCO}	I/O Latch Clock-Out (pad-to-pad), 64 clock loading		9.0		10.0		12.0		17.2		14.4	ns
t_{ACO}	Array Clock-Out (pad-to-pad), 64 clock loading		12.8		14.4		17.0		24.3		20.4	ns
d_{TLH}	Capacitive Loading, Low to High		0.04		0.04		0.05		0.06		0.06	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.05		0.06		0.07		0.08		0.08	ns/pF
CMOS Output Module Timing[1]												
t_{DLH}	Data to Pad High		4.8		5.4		6.4		9.1		7.7	ns
t_{DHL}	Data to Pad Low		3.4		3.8		4.5		6.4		5.4	ns
t_{ENZH}	Enable Pad Z to High		3.8		4.3		5.0		7.1		6.0	ns
t_{ENZL}	Enable Pad Z to Low		4.1		4.7		5.5		7.9		6.6	ns
t_{ENHZ}	Enable Pad High to Z		5.4		6.1		7.2		10.3		8.6	ns
t_{ENLZ}	Enable Pad Low to Z		5.4		6.1		7.2		10.3		8.6	ns
t_{GLH}	G to Pad High		4.2		4.8		5.6		8.0		6.7	ns
t_{GHL}	G to Pad Low		4.7		5.4		6.3		9.0		7.6	ns
t_{LCO}	I/O Latch Clock-Out (pad-to-pad), 64 clock loading		10.7		11.8		14.2		20.3		17.0	ns
t_{ACO}	Array Clock-Out (pad-to-pad), 64 clock loading		15.0		17.0		20.0		28.6		24.0	ns
d_{TLH}	Capacitive Loading, Low to High		0.05		0.06		0.07		0.08		0.08	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.05		0.05		0.06		0.07		0.07	ns/pF

Notes:

1. *Delays based on 35 pF loading.*
2. *SSO information can be found in the "Simultaneously Switching Output Limits for Actel FPGAs" application note on page 4-125.*

A1240XL Timing Characteristics

(Worst-Case Commercial Conditions, V_{CC} = 4.75 V, T_J = 70°C)

Logic Module Propagation Delays[1]		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		3.3V Speed[5]		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD1}	Single Module		2.6		3.0		3.5		5.0		4.2	ns
t_{CO}	Sequential Clk to Q		2.6		3.0		3.5		5.0		4.2	ns
t_{GO}	Latch G to Q		2.6		3.0		3.5		5.0		4.2	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		2.6		3.0		3.5		5.0		4.2	ns
Predicted Routing Delays[2]												
t_{RD1}	FO=1 Routing Delay		1.1		1.2		1.4		2.0		1.7	ns
t_{RD2}	FO=2 Routing Delay		1.3		1.4		1.7		2.4		2.0	ns
t_{RD3}	FO=3 Routing Delay		1.7		1.9		2.2		3.1		2.6	ns
t_{RD4}	FO=4 Routing Delay		2.3		2.6		3.0		4.3		3.6	ns
t_{RD8}	FO=8 Routing Delay		3.4		3.8		4.5		6.4		5.4	ns
Sequential Timing Characteristics[3, 4]												
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.4		0.4		0.5		0.7		0.6		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	0.8		0.9		1.0		1.4		1.2		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.4		3.8		4.5		6.4		5.4		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	3.4		3.8		4.5		6.4		5.4		ns
t_A	Flip-Flop Clock Input Period	6.8		7.7		9.1		13.0		10.9		ns
t_{INH}	Input Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Buffer Latch Setup	0.3		0.4		0.4		0.6		0.5		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Setup	0.3		0.4		0.4		0.6		0.5		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		215.0		190.0		160.0		110.0		105.0	MHz

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*
5. *V_{CC} = 3.0 V for 3.3V specifications.*

A1240XL Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

Input Module Propagation Delays			'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		3.3V Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Pad to Y High			1.1		1.2		1.4		2.0		1.7	ns
t_{INYL}	Pad to Y Low			1.3		1.4		1.7		2.4		2.0	ns
t_{INGH}	G to Y High			2.0		2.3		2.7		3.9		3.2	ns
t_{INGL}	G to Y Low			2.6		3.0		3.5		5.0		4.2	ns
Input Module Predicted Routing Delays[1]													
t_{IRD1}	FO=1 Routing Delay			2.9		3.3		3.9		5.6		4.7	ns
t_{IRD2}	FO=2 Routing Delay			3.4		3.8		4.5		6.4		5.4	ns
t_{IRD3}	FO=3 Routing Delay			3.8		4.3		5.1		7.3		6.1	ns
t_{IRD4}	FO=4 Routing Delay			4.1		4.7		5.5		7.9		6.6	ns
t_{IRD8}	FO=8 Routing Delay			5.6		6.3		7.4		10.6		8.9	ns
Global Clock Network													
t_{CKH}	Input Low to High	FO = 32		5.1		5.8		6.8		9.7		8.2	ns
		FO = 256		5.7		6.5		7.6		10.9		9.1	ns
t_{CKL}	Input High to Low	FO = 32		5.0		5.7		6.7		9.6		8.0	ns
		FO = 256		5.7		6.5		7.6		10.9		9.1	ns
t_{PWH}	Minimum Pulse Width High	FO = 32	2.7		3.1		3.6		5.1		4.3		ns
		FO = 256	2.9		3.3		3.9		5.6		4.7		ns
t_{PWL}	Minimum Pulse Width Low	FO = 32	2.7		3.1		3.6		5.1		4.3		ns
		FO = 256	2.9		3.3		3.9		5.6		4.7		ns
t_{CKSW}	Maximum Skew	FO = 32		0.8		0.9		1.0		1.4		1.2	ns
		FO = 256		0.8		0.9		1.0		1.4		1.2	ns
t_{SUEXT}	Input Latch External Setup	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
		FO = 256	0.0		0.0		0.0		0.0		0.0		ns
t_{HEXT}	Input Latch External Hold	FO = 32	2.6		2.9		3.4		4.9		4.1		ns
		FO = 256	3.2		3.7		4.3		6.1		5.2		ns
t_P	Minimum Period	FO = 32	5.6		6.3		7.4		10.6		8.9		ns
		FO = 256	6.0		6.8		8.0		11.4		9.6		ns
f_{MAX}	Maximum Frequency	FO = 32		215.0		190.0		160.0		110.0		105.0	MHz
		FO = 256		195.0		170.0		144.0		100.0		95.0	MHz

Note:

1. *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 3 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case*

A1240XL Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

Output Module Timing		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		3.3V Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]												
t_{DLH}	Data to Pad High		3.8		4.3		5.0		7.1		6.0	ns
t_{DHL}	Data to Pad Low		4.1		4.6		5.4		7.7		6.5	ns
t_{ENZH}	Enable Pad Z to High		3.8		4.3		5.0		7.1		6.0	ns
t_{ENZL}	Enable Pad Z to Low		4.1		4.7		5.5		7.9		6.6	ns
t_{ENHZ}	Enable Pad High to Z		5.4		6.1		7.2		10.3		8.6	ns
t_{ENLZ}	Enable Pad Low to Z		5.4		6.1		7.2		10.3		8.6	ns
t_{GLH}	G to Pad High		4.2		4.8		5.6		8.0		6.7	ns
t_{GHL}	G to Pad Low		4.7		5.4		6.3		9.0		7.6	ns
t_{LCO}	I/O Latch Clock-Out (pad-to-pad), 64 clock loading		9.2		10.5		12.3		17.6		14.8	ns
t_{ACO}	Array Clock-Out (pad-to-pad), 64 clock loading		12.9		14.6		17.2		24.6		20.6	ns
d_{TLH}	Capacity Loading, Low to High		0.04		0.04		0.05		0.06		0.06	ns/pF
d_{THL}	Capacity Loading, High to Low		0.05		0.06		0.07		0.08		0.08	ns/pF
CMOS Output Module Timing[1]												
t_{DLH}	Data to Pad High		4.8		5.4		6.4		9.1		7.7	ns
t_{DHL}	Data to Pad Low		3.4		3.8		4.5		6.4		5.4	ns
t_{ENZH}	Enable Pad Z to High		3.8		4.3		5.0		7.1		6.0	ns
t_{ENZL}	Enable Pad Z to Low		4.1		4.7		5.5		7.9		6.6	ns
t_{ENHZ}	Enable Pad High to Z		5.4		6.1		7.2		10.3		8.6	ns
t_{ENLZ}	Enable Pad Low to Z		5.4		6.1		7.2		10.3		8.6	ns
t_{GLH}	G to Pad High		4.2		4.8		5.6		8.0		6.7	ns
t_{GHL}	G to Pad Low		4.7		5.4		6.3		9.0		7.6	ns
t_{LCO}	I/O Latch Clock-Out (pad-to-pad), 64 clock loading		10.9		12.4		14.5		20.7		17.4	ns
t_{ACO}	Array Clock-Out (pad-to-pad), 64 clock loading		15.2		17.2		20.3		29.0		24.4	ns
d_{TLH}	Capacity Loading, Low to High		0.05		0.06		0.07		0.08		0.08	ns/pF
d_{THL}	Capacity Loading, High to Low		0.05		0.05		0.06		0.07		0.07	ns/pF

Notes:

1. *Delays based on 35 pF loading.*
2. *SSO information can be found in the "Simultaneously Switching Output Limits for Actel FPGAs" application note on page 4-125.*

A3265DX Timing Characteristics

(Worst-Case Commercial Conditions)

		Advanced Information		Preliminary Information							
Logic Module Propagation Delays[1]		**'–2' Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		**3.3V Speed[5]**	
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Combinatorial Functions												
t_{PD}	Internal Array Module Delay		1.8		2.4		2.9		3.7		3.2	ns
t_{PDD}	Internal Decode Module Delay		2.1		2.8		3.4		4.4		3.7	ns
Predicted Routing Delays[2]												
t_{RD1}	FO=1 Routing Delay		0.3		0.4		.05		0.6		0.5	ns
t_{RD2}	FO=2 Routing Delay		0.6		0.8		.09		1.2		1.0	ns
t_{RD3}	FO=3 Routing Delay		0.9		1.2		1.4		1.8		1.6	ns
t_{RD4}	FO=4 Routing Delay		1.2		1.6		1.9		2.4		2.1	ns
t_{RD5}	FO=8 Routing Delay		2.4		3.2		3.7		4.9		4.1	ns
t_{RDD}	Decode-to-Output Routing Delay		0.4		0.5		0.62		0.8		0.7	ns
Sequential Timing Chatacteristics[3, 4]												
t_{CO}	Flip-Flop Clock-to-Output		2.0		2.7		3.1		4.1		3.5	ns
t_{GO}	Latch Gate-to-Output		1.8		2.4		2.9		3.7		3.2	ns
t_{SU}	Flip-Flop (Latch) Setup Time	0.3		0.4		0.47		0.6		0.5		ns
t_{H}	Flip-Flop (Latch) Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t_{RO}	Flip-Flop (Latch) Reset to Output		2.0		2.7		3.1		4.1		3.5	ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	0.6		0.9		1.0		1.3		1.1		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.1		4.2		4.9		6.4		5.5		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.1		5.5		6.5		8.4		7.1		ns

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*
5. *V_{CC} = 3.0 V for 3.3V specifications.*

A3265DX Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

			Advanced Information		Preliminary Information						
Input Module Propagation Delays			**'–2' Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		**3.3V Speed**		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INPY}	Input Data Pad to Y			1.2		1.6		1.9		2.4		2.1	ns
t_{INGO}	Input Latch Gate-to-Output			2.8		3.7		4.4		5.7		4.8	ns
t_{INH}	Input Latch Hold		0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Latch Setup		0.4		0.6		0.7		0.9		0.8		ns
t_{ILA}	Latch Active Pulse Width		4.4		5.9		6.9		9.0		7.7		ns
Input Module Predicted Routing Delays[1]													
t_{IRD1}	FO=1 Routing Delay			2.7		3.7		4.3		5.6		4.8	ns
t_{IRD2}	FO=2 Routing Delay			3.1		4.2		4.9		6.4		5.4	ns
t_{IRD3}	FO=3 Routing Delay			3.4		4.5		5.3		6.9		5.9	ns
t_{IRD4}	FO=4 Routing Delay			3.9		5.2		6.1		7.9		6.7	ns
t_{IRD5}	FO=8 Routing Delay			5.6		7.5		8.8		11.4		9.7	ns
t_{IRDD}	Decode-to-Output Routing Delay			0.3		0.4		0.5		0.7		0.6	ns
Global Clock Network													
t_{CKH}	Input Low to High	FO=32		6.3		8.4		9.9		12.8		10.9	ns
		FO=256		5.3		7.1		8.4		10.9		9.2	ns
t_{CKL}	Input High to Low	FO=32		4.95		6.6		7.8		10.1		8.6	ns
		FO=256		5.5		7.3		8.6		11.2		9.5	ns
t_{PW}	Minimum Pulse Width	FO=32	2.7		3.7		4.3		5.6		4.8		ns
		FO=256	2.9		3.9		4.6		6.0		5.1		ns
t_{CKSW}	Maximum Skew	FO=32		0.6		0.9		1.0		1.3		1.1	ns
		FO=256		0.6		0.9		1.0		1.3		1.1	ns
t_{SUEXT}	Input Latch External Setup	FO=32	0.0		0.0		0.0		0.0		0.0		ns
		FO=256	0.0		0.0		0.0		0.0		0.0		ns
t_{HEXT}	Input Latch External Hold	FO=32	2.2		2.9		3.4		4.4		3.8		ns
		FO=256	2.2		2.9		3.4		4.4		3.8		ns
t_P	Minimum Period (1/fmax)	FO=32	12.5		10.0		8.7		6.1		9.6		ns
		FO=256	13.8		11.0		9.6		6.7		10.6		ns
f_{MAX}	Maximum Datapath Frequency	FO=32		172.5		138.0		120.0		84.0		108.0	MHz
		FO=256		150.9		120.8		105.0		73.5		94.5	MHz

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.

A3265DX Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

		Advanced Information		Preliminary Information							
Output Module Timing		**'–2' Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		**3.3V Speed**	
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]												
t_{DLH}	Data to Pad High		3.2		4.3		5.0		6.5		5.5	ns
t_{DHL}	Data to Pad Low		3.9		5.2		6.1		7.9		6.7	ns
t_{ENZH}	Enable Pad Z to High		4.1		5.4		6.4		8.3		7.1	ns
t_{ENZL}	Enable Pad Z to Low		4.4		5.9		6.9		9.0		7.6	ns
t_{ENHZ}	Enable Pad High to Z		7.1		9.5		11.1		14.5		12.3	ns
t_{ENLZ}	Enable Pad Low to Z		7.1		9.5		11.1		14.5		12.3	ns
t_{GLH}	G to Pad High		7.1		9.4		11.1		14.4		12.3	ns
t_{GHL}	G to Pad Low		6.5		8.7		10.2		13.3		11.3	ns
t_{LSU}	I/O Latch Output Setup	0.4		0.6		0.7		0.9		0.8		ns
t_{LH}	I/O Latch Output Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		8.4		11.1		13.1		17.0		14.5	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		11.8		15.7		18.5		24.1		20.5	ns
d_{TLH}	Capacitive Loading, Low to High		0.03		0.04		0.05		0.1		0.1	ns/pF
d_{TLL}	Capacitive Loading, High to Low		0.02		0.03		0.07		0.1		0.1	ns/pF
t_{WDO}	Hard-Wired Wide Decode Output		0.3		0.4		0.5		0.7		0.6	ns/pF
CMOS Output Module Timing[1]												
t_{DLH}	Data to Pad High		3.9		5.2		6.1		7.9		6.7	ns
t_{DHL}	Data to Pad Low		3.2		4.3		5.0		6.5		5.5	ns
t_{ENZH}	Enable Pad Z to High		4.1		5.5		6.4		8.4		7.1	ns
t_{ENZL}	Enable Pad Z to Low		4.4		5.9		6.9		9.0		7.6	ns
t_{ENHZ}	Enable Pad High to Z		7.1		9.5		11.1		14.5		12.3	ns
t_{ENLZ}	Enable Pad Low to Z		7.1		9.5		11.1		14.5		12.3	ns
t_{GLH}	G to Pad High		7.1		9.4		11.1		14.4		12.3	ns
t_{GHL}	G to Pad Low		7.7		10.2		12.0		15.6		13.3	ns
t_{LSU}	I/O Latch Setup	0.4		0.6		0.7		0.9		0.8		ns
t_{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		9.9		13.3		15.6		20.3		17.3	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		13.9		18.5		21.8		28.3		24.1	ns
d_{TLH}	Capacitive Loading, Low to High		0.04		0.06		0.07		0.1		0.1	ns/pF
d_{TLL}	Capacitive Loading, High to Low		0.04		0.05		0.06		0.1		0.1	ns/pF
t_{WDO}	Hard-Wired Wide Decode Output		0.3		0.4		0.5		0.7		0.6	ns/pF

Notes:

1. *Delays based on 35pF loading.*
2. *SSO information can be found in the "Simultaneously Switching Output Limits for Actel FPGAs" application note on page 4-125.*

A1280XL Timing Characteristics

(Worst-Case Commercial Conditions, V_{CC} = 4.75 V, T_J = 70°C)

Logic Module Propagation Delays[1]		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		3.3V Speed[5]		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD1}	Single Module		2.6		3.0		3.5		5.0		4.2	ns
t_{CO}	Sequential Clk to Q		2.6		3.0		3.5		5.0		4.2	ns
t_{GO}	Latch G to Q		2.6		3.0		3.5		5.0		4.2	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		2.6		3.0		3.5		5.0		4.2	ns
Predicted Routing Delays[2]												
t_{RD1}	FO=1 Routing Delay		1.3		1.4		1.7		2.4		2.0	ns
t_{RD2}	FO=2 Routing Delay		1.8		2.0		2.4		3.4		2.9	ns
t_{RD3}	FO=3 Routing Delay		2.2		2.5		2.9		4.1		3.5	ns
t_{RD4}	FO=4 Routing Delay		2.6		3.0		3.5		5.0		4.2	ns
t_{RD8}	FO=8 Routing Delay		5.0		5.7		6.7		9.6		8.0	ns
Sequential Timing Characteristics[3,4]												
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.4		0.4		0.5		0.7		0.6		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	0.8		0.9		1.0		1.4		1.2		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.7		4.3		4.9		7.0		5.9		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	3.7		4.3		4.9		7.0		5.9		ns
t_A	Flip-Flop Clock Input Period	8.0		8.7		10		14		12		ns
t_{INH}	Input Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Buffer Latch Setup	0.3		0.4		0.4		0.6		0.5		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Setup	0.3		0.4		0.4		0.6		0.5		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		200.0		167.0		130.0		90.0		110.0	MHz

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*
5. *V_{CC} = 3.0 V for 3.3V specifications.*

A1280XL Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

Input Module Propagation Delays			'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		3.3V Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Pad to Y High			1.1		1.2		1.4		2.0		1.7	ns
t_{INYL}	Pad to Y Low			1.3		1.4		1.7		2.4		2.0	ns
t_{INGH}	G to Y High			2.0		2.3		2.7		3.9		3.2	ns
t_{INGL}	G to Y Low			2.6		3.0		3.5		5.0		4.2	ns
Input Module Predicted Routing Delays[1]													
t_{IRD1}	FO=1 Routing Delay			3.2		3.7		4.3		6.1		5.2	ns
t_{IRD2}	FO=2 Routing Delay			3.7		4.2		4.9		7.0		5.9	ns
t_{IRD3}	FO=3 Routing Delay			4.0		4.5		5.3		7.6		6.4	ns
t_{IRD4}	FO=4 Routing Delay			4.6		5.2		6.1		8.7		7.3	ns
t_{IRD8}	FO=8 Routing Delay			6.6		7.5		8.8		12.6		10.6	ns
Global Clock Network													
t_{CKH}	Input Low to High	FO = 32		5.1		5.8		6.8		9.7		8.2	ns
		FO = 384		5.7		6.5		7.6		10.9		9.1	ns
t_{CKL}	Input High to Low	FO = 32		5.0		5.7		6.7		9.6		8.0	ns
		FO = 384		5.7		6.5		7.6		10.9		9.1	ns
t_{PWH}	Minimum Pulse Width	FO = 32	3.2		3.5		4.3		6.1		5.2		ns
	High	FO = 384	3.5		3.9		4.6		6.6		5.5		ns
t_{PWL}	Minimum Pulse Width	FO = 32	3.2		3.5		4.3		6.1		5.2		ns
	Low	FO = 384	3.5		3.9		4.6		6.6		5.5		ns
t_{CKSW}	Maximum Skew	FO = 32		0.8		0.9		1.0		1.4		1.2	ns
		FO = 384		0.8		0.9		1.0		1.4		1.2	ns
t_{SUEXT}	Input Latch External	FO = 32	0.0		0.0		0.0		0.0		0.0		ns
	Setup	FO = 384	0.0		0.0		0.0		0.0		0.0		ns
t_{HEXT}	Input Latch External	FO = 32	2.6		2.9		3.4		4.9		4.1		ns
	Hold	FO = 384	3.2		3.7		4.3		6.1		5.2		ns
t_P	Minimum Period	FO = 32	6.5		7.4		8.7		12.4		10.4		ns
		FO = 384	7.2		8.0		9.6		13.7		11.5		ns
f_{MAX}	Maximum Frequency	FO = 32		200.0		167.0		143.0		100.0		120.0	MHz
		FO = 384		180.0		150.0		130.0		90.0		110.0	MHz

Note:

1. *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A1280XL Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

Output Module Timing		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		3.3V Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]												
t_{DLH}	Data to Pad High		3.8		4.3		5.0		7.1		6.0	ns
t_{DHL}	Data to Pad Low		4.1		4.6		5.4		7.7		6.5	ns
t_{ENZH}	Enable Pad Z to High		3.8		4.3		5.0		7.1		6.0	ns
t_{ENZL}	Enable Pad Z to Low		4.1		4.7		5.5		7.7		6.6	ns
t_{ENHZ}	Enable Pad High to Z		5.4		6.1		7.2		10.3		8.6	ns
t_{ENLZ}	Enable Pad Low to Z		5.4		6.1		7.2		10.3		8.6	ns
t_{GLH}	G to Pad High		4.2		4.8		5.6		8.0		6.7	ns
t_{GHL}	G to Pad Low		4.7		5.4		6.3		9.0		7.6	ns
t_{LCO}	I/O Latch Clock-Out (pad-to-pad), 64 clock loading		9.8		11.0		13.1		18.7		15.7	ns
t_{ACO}	Array Clock-Out (pad-to-pad), 64 clock loading		13.9		15.7		18.5		26.4		22.2	ns
d_{TLH}	Capacitive Loading, Low to High		0.04		0.04		0.05		0.06		0.06	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.05		0.06		0.07		0.08		0.08	ns/pF
CMOS Output Module Timing[1]												
t_{DLH}	Data to Pad High		4.8		5.4		6.4		9.1		7.7	ns
t_{DHL}	Data to Pad Low		3.4		3.8		4.5		6.4		5.4	ns
t_{ENZH}	Enable Pad Z to High		3.8		4.3		5.0		7.1		6.0	ns
t_{ENZL}	Enable Pad Z to Low		4.1		4.7		5.5		7.9		6.6	ns
t_{ENHZ}	Enable Pad High to Z		5.4		6.1		7.2		10.3		8.6	ns
t_{ENLZ}	Enable Pad Low to Z		5.4		6.1		7.2		10.3		8.6	ns
t_{GLH}	G to Pad High		4.2		4.8		5.6		8.0		6.7	ns
t_{GHL}	G to Pad Low		4.7		5.4		6.3		9.0		7.6	ns
t_{LCO}	I/O Latch Clock-Out (pad-to-pad), 64 clock loading		11.6		13.0		15.5		22.2		18.6	ns
t_{ACO}	Array Clock-Out (pad-to-pad), 64 clock loading		16.4		18.5		21.8		31.2		26.2	ns
d_{TLH}	Capacitive Loading, Low to High		0.05		0.06		0.07		0.08		0.08	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.05		0.05		0.06		0.07		0.07	ns/pF

Notes:

1. *Delays based on 35 pF loading.*
2. *SSO information can be found in the "Simultaneously Switching Output Limits for Actel FPGAs" application note on page 4-125.*

A32140DX Timing Characteristics

(Worst-Case Commercial Conditions)

		Advanced Information		Preliminary Information						
Logic Module Propagation Delays[1]		**'–2 Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Combinatorial Functions										
t_{PD}	Internal Array Module Delay		1.8		2.3		2.8		3.6	ns
t_{PDD}	Internal Decode Module Delay		1.9		2.5		3.0		3.8	ns
Predicted Routing Delays[2]										
t_{RD1}	FO=1 Routing Delay		1.0		1.3		1.6		2.0	ns
t_{RD2}	FO=2 Routing Delay		1.4		1.9		2.2		2.8	ns
t_{RD3}	FO=3 Routing Delay		1.8		2.4		2.8		3.7	ns
t_{RD4}	FO=4 Routing Delay		2.2		2.9		3.4		4.5	ns
t_{RD5}	FO=8 Routing Delay		3.8		5.0		5.9		7.7	ns
t_{RDD}	Decode-to-Output Routing Delay		0.5		0.7		0.78		1.0	ns
Sequential Timing Characteristics[3, 4]										
t_{CO}	Flip-Flop Clock-to-Output		2.1		2.8		3.3		4.3	ns
t_{GO}	Latch Gate-to-Output		1.8		2.3		2.8		3.6	ns
t_{SU}	Flip-Flop (Latch) Setup Time	0.3		0.4		0.47		0.6		ns
t_{H}	Flip-Flop (Latch) Hold Time	0.0		0.0		0.0		0.0		ns
t_{RO}	Flip-Flop (Latch) Reset to Output		2.1		2.8		3.3		4.3	ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	0.6		0.9		1.0		1.3		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	2.6		3.5		4.1		5.4		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.1		5.5		6.5		8.4		ns

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

A32140DX Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

			Advanced Information		Preliminary Information						
Input Module Propagation Delays			**'–2' Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INPY}	Input Data Pad to Y			1.2		1.6		1.9		2.4	ns
t_{INGO}	Input Latch Gate-to-Output			2.3		3.1		3.7		4.7	ns
t_{INH}	Input Latch Hold		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Latch Setup		0.3		0.4		0.47		0.6		ns
t_{ILA}	Latch Active Pulse Width		3.1		4.2		4.9		6.4		ns
Input Module Predicted Routing Delays[1]											
t_{IRD1}	FO=1 Routing Delay			2.7		3.7		4.3		5.6	ns
t_{IRD2}	FO=2 Routing Delay			3.1		4.2		4.9		6.4	ns
t_{IRD3}	FO=3 Routing Delay			3.4		4.5		5.3		6.9	ns
t_{IRD4}	FO=4 Routing Delay			3.9		5.2		6.1		7.9	ns
t_{IRD5}	FO=8 Routing Delay			5.6		7.5		8.8		11.4	ns
t_{IRDD}	Decode-to-Output Routing Delay			0.3		0.4		0.5		0.7	ns
Global Clock Network											
t_{CKH}	Input Low to High	FO=32		6.2		8.3		9.7		12.7	ns
		FO=486		6.8		9.1		10.7		13.9	ns
t_{CKL}	Input High to Low	FO=32		6.12		8.2		9.6		12.5	ns
		FO=486		6.7		8.9		10.5		13.6	ns
t_{PW}	Minimum Pulse Width	FO=32	2.7		3.7		4.3		5.6		ns
		FO=486	2.9		3.9		4.6		6.0		ns
t_{CKSW}	Maximum Skew	FO=32		0.6		0.9		1.0		1.3	ns
		FO=486		0.6		0.9		1.0		1.3	ns
t_{SUEXT}	Input Latch External Setup	FO=32	0.0		0.0		0.0		0.0		ns
		FO=486	0.0		0.0		0.0		0.0		ns
t_{HEXT}	Input Latch External Hold	FO=32	2.2		2.9		3.4		4.4		ns
		FO=486	2.2		2.9		3.4		4.4		ns
t_P	Minimum Period (1/fmax)	FO=32	12.5		10.0		8.7		6.1		ns
		FO=486	13.8		11.0		9.6		6.7		ns
f_{MAX}	Maximum Datapath Frequency	FO=32		172.5		138.0		120.0		84.0	MHz
		FO=486		150.9		120.8		105.0		73.5	MHz

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.

A32140DX Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

		Advanced Information		Preliminary Information						
Output Module Timing		**'–2 Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]										
t_{DLH}	Data to Pad High		3.3		4.4		5.1		6.7	ns
t_{DHL}	Data to Pad Low		3.5		4.6		5.4		7.1	ns
t_{ENZH}	Enable Pad Z to High		4.1		5.5		6.4		8.4	ns
t_{ENZL}	Enable Pad Z to Low		4.4		5.9		6.9		9.0	ns
t_{ENHZ}	Enable Pad High to Z		7.1		9.5		11.1		14.5	ns
t_{ENLZ}	Enable Pad Low to Z		7.1		9.5		11.1		14.5	ns
t_{GLH}	G to Pad High		6.5		8.7		10.2		13.3	ns
t_{GHL}	G to Pad Low		6.5		8.7		10.2		13.3	ns
t_{LSU}	I/O Latch Output Setup	0.4		0.6		0.7		0.9		ns
t_{LH}	I/O Latch Output Hold	0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		8.4		11.1		13.1		17.0	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		11.8		15.7		18.5		24.1	ns
d_{TLH}	Capacitive Loading, Low to High		0.03		0.04		0.05		0.1	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.02		0.03		0.07		0.1	ns/pF
t_{WDO}	Hard-Wired Wide Decode Output		0.3		0.4		0.5		0.7	ns/pF
CMOS Output Module Timing[1]										
t_{DLH}	Data to Pad High		3.5		4.6		5.4		7.1	ns
t_{DHL}	Data to Pad Low		3.3		4.4		5.1		6.7	ns
t_{ENZH}	Enable Pad Z to High		4.1		5.5		6.4		8.4	ns
t_{ENZL}	Enable Pad Z to Low		4.4		5.9		6.9		9.0	ns
t_{ENHZ}	Enable Pad High to Z		7.1		9.5		11.1		14.5	ns
t_{ENLZ}	Enable Pad Low to Z		7.1		9.5		11.1		14.5	ns
t_{GLH}	G to Pad High		6.5		8.7		10.2		13.3	ns
t_{GHL}	G to Pad Low		6.5		8.7		10.2		13.3	ns
t_{LSU}	I/O Latch Setup	0.4		0.6		0.7		0.9		ns
t_{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		9.9		13.3		15.6		20.3	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		13.9		18.5		21.8		28.3	ns
d_{TLH}	Capacitive Loading, Low to High		0.04		0.06		0.07		0.1	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.04		0.05		0.06		0.1	ns/pF
t_{WDO}	Hard-Wired Wide Decode Output		0.3		0.4		0.5		0.7	ns/pF

Notes:

1. *Delays based on 35 pF loading.*
2. *SSO information can be found in the "Simultaneously Switching Output Limits for Actel FPGAs" application note on page 4-125.*

A32100DX Timing Characteristics

(Worst-Case Commercial Conditions)

		Advanced Information								
Logic Module Propagation Delays		**'–2 Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Combinatorial Functions										
t_{PD}	Internal Array Module Delay		2.2		3.0		3.5		5.2	ns
t_{PDD}	Internal Decode Module Delay		2.4		3.1		3.7		5.7	ns
Predicted Module Routing Delays										
t_{RD1}	FO=1 Routing Delay		1.0		1.3		1.5		3.3	ns
t_{RD2}	FO=2 Routing Delay		1.4		1.9		2.2		4.3	ns
t_{RD3}	FO=3 Routing Delay		1.8		2.5		2.9		5.2	ns
t_{RD4}	FO=4 Routing Delay		2.4		3.1		3.7		6.5	ns
t_{RD5}	FO=8 Routing Delay		4.2		5.6		6.6		10.0	ns
t_{RDD}	Decode-to-Output Routing Delay		0.3		0.4		0.5		0.4	ns
Sequential Timing Characteristics										
t_{CO}	Flip-Flop Clock-to-Output		2.2		3.0		3.5		5.0	ns
t_{GO}	Latch Gate-to-Output		2.2		3.0		3.5		5.0	ns
t_{SU}	Flip-Flop (Latch) Setup Time	0.3		0.4		0.5		0.7		ns
t_{H}	Flip-Flop (Latch) Hold Time	0.0		0.0		0.0		0.0		ns
t_{RO}	Flip-Flop (Latch) Reset to Output		2.2		3.0		3.5		5.0	ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	0.6		0.9		1.0		1.4		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.1		4.2		4.9		7.0		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.1		5.4		6.4		7.0		ns

A32100DX Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

		Advanced Information								
Logic Module Timing		**'–2 Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Synchronous SRAM Operations										
t_{RC}	Read Cycle Time	6.4		8.5		10.0		14.3		ns
t_{WC}	Write Cycle Time	6.4		8.5		10.0		14.3		ns
t_{RCKHL}	Clock High/Low Time	3.2		4.3		5.0		7.1		ns
t_{RCO}	Data Valid After Clock High/Low		3.2		4.3		5.0		7.1	ns
t_{ADSU}	Address/Data Setup Time	1.5		2.0		2.4		3.4		ns
t_{ADH}	Address/Data Hold Time	0.0		0.0		0.0		0.0		ns
t_{RENSU}	Read Enable Setup	0.6		0.8		0.9		1.4		ns
t_{RENH}	Read Enable Hold	3.2		4.3		5.0		0.7		ns
t_{WENSU}	Write Enable Setup	2.6		3.4		4.0		5.4		ns
t_{WENH}	Write Enable Hold	0.0		0.0		0.0		0.0		ns
t_{BENS}	Block Enable Setup	2.6		3.5		4.1		5.6		ns
t_{BENH}	Block Enable Hold	0.0		0.0		0.0		0.0		ns
Asynchronous SRAM Operations										
t_{RPD}	Asynchronous Access Time		7.7		10.2		12.0		17.2	ns
t_{RDADV}	Read Address Valid	8.3		11.1		13.0		18.6		ns
t_{ADSU}	Address/Data Setup Time	1.5		2.0		2.4		3.4		ns
t_{ADH}	Address/Data Hold Time	0.0		0.0		0.0		0.0		ns
t_{RENSUA}	Read Enable Setup to Address Valid	0.57		0.8		0.9		1.4		ns
t_{RENHA}	Read Enable Hold	3.2		4.3		5.0		7.1		ns
t_{WENSU}	Write Enable Setup	2.6		3.4		4.0		5.4		ns
t_{WENH}	Write Enable Hold	0.0		0.0		0.0		0.0		ns
t_{DOH}	Data Out Hold Time		1.1		1.5		1.8		2.6	ns

A32100DX Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

			Advanced Information								
Input Module Propagation Delays			**'–2' Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INPY}	Input Data Pad to Y			1.4		1.9		2.2		2.9	ns
t_{INGO}	Input Latch Gate-to-Output[1]			2.9		3.8		4.5		5.0	ns
t_{INH}	Input Latch Hold[1]		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Latch Setup[1]		0.45		0.6		0.7		0.6		ns
t_{ILA}	Latch Active Pulse Width[1]		4.4		5.9		6.9		7.0		ns
Input Module Predicted Routing Delays											
t_{IRD1}	FO=1 Routing Delay			1.6		2.1		2.5		6.1	ns
t_{IRD2}	FO=2 Routing Delay			2.0		2.7		3.2		7.0	ns
t_{IRD3}	FO=3 Routing Delay			2.6		3.4		4.0		7.6	ns
t_{IRD4}	FO=4 Routing Delay			2.6		3.4		4.0		8.7	ns
t_{IRD8}	FO=8 Routing Delay			4.1		5.4		6.4		12.6	ns
Global Clock Network											
t_{CKH}	Input Low to High	FO=32		4.7		6.3		7.4		8.4	ns
		FO=635		5.7		7.7		9.0		9.9	ns
t_{CKL}	Input High to Low	FO=32		4.8		6.4		7.5		8.4	ns
		FO=635		6.4		8.5		10.0		11.3	ns
t_{PWH}	Minimum Pulse Width High	FO=32	2.5		3.3		3.9		5.07		ns
		FO=635	2.7		3.7		4.3		5.59		ns
t_{PWL}	Minimum Pulse Width Low	FO=32	2.5		3.3		3.9		5.07		ns
		FO=635	2.7		3.7		4.3		5.59		ns
t_{CKSW}	Maximum Skew	FO=32		0.6		0.9		1.0		1.4	ns
		FO=635		0.6		0.9		1.0		1.4	ns
t_{SUEXT}	Input Latch External Setup	FO=32	0.0		0.0		0.0		0.0		ns
		FO=635	0.0		0.0		0.0		0.0		ns
t_{HEXT}	Input Latch External Hold	FO=32	2.2		2.9		3.4		4.9		ns
		FO=635	2.7		3.7		4.3		6.1		ns
t_P	Minimum Period (1/fmax)	FO=32	5.0		7.4		7.9		12.4		ns
		FO=635	5.5		8.2		8.6		13.7		ns
f_{HMAX}	Maximum Datapath Frequency	FO=32		182.6		146		127		88.9	MHz
		FO=635		166.8		133		116		81.2	MHz

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.

A32100DX Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

		Advanced Information								
Output Module Timing		**'–2' Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]										
t_{DLH}	Data to Pad High		3.7		4.9		5.8		4.8	ns
t_{DHL}	Data to Pad Low		4.5		6.0		7.1		6.2	ns
t_{ENZH}	Enable Pad Z to High		4.8		6.4		7.5		7.2	ns
t_{ENZL}	Enable Pad Z to Low		5.1		6.8		8.0		7.9	ns
t_{ENHZ}	Enable Pad High to Z		8.3		11.1		13.0		14.0	ns
t_{ENLZ}	Enable Pad Low to Z		8.3		11.1		13.0		14.0	ns
t_{GLH}	G to Pad High		8.3		11.1		13.0		8.0	ns
t_{GHL}	G to Pad Low		9.0		12.0		14.1		9.0	ns
t_{LSU}	I/O Latch Output Setup	0.26		0.3		0.4		0.6		ns
t_{LH}	I/O Latch Output Hold	0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		8.4		11.1		13.1		18.7	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		11.8		15.7		18.5		26.5	ns
d_{TLH}	Capacitive Loading, Low to High		0.03		0.0		0.05		0.07	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.04		0.1		0.07		0.10	ns/pF
t_{WDO}	Hard-Wired Wide Decode Output		0.04		0.1		0.06		0.09	ns
CMOS Output Module Timing[1]										
t_{DLH}	Data to Pad High		4.5		6.0		7.1		9.1	ns
t_{DHL}	Data to Pad Low		3.7		4.9		5.8		6.4	ns
t_{ENZH}	Enable Pad Z to High		4.8		6.4		7.5		7.2	ns
t_{ENZL}	Enable Pad Z to Low		5.1		6.8		8.0		7.9	ns
t_{ENHZ}	Enable Pad High to Z		8.3		11.1		13.0		14.0	ns
t_{ENLZ}	Enable Pad Low to Z		8.3		11.1		13.0		14.0	ns
t_{GLH}	G to Pad High		8.3		11.1		13.0		8.0	ns
t_{GHL}	G to Pad Low		9.0		12.0		14.1		9.0	ns
t_{LSU}	I/O Latch Setup	0.26		0.3		0.4		0.6		ns
t_{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		9.9		13.2		15.5		22.3	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		13.9		18.5		21.8		31.2	ns
d_{TLH}	Capacitive Loading, Low to High		0.04		0.1		0.07		0.10	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.04		0.1		0.06		0.09	ns/pF
t_{WDO}	Hard-Wired Wide Decode Output		0.04		0.1		0.06		0.09	ns

Notes:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.*
2. *SSO information can be found in the "Simultaneously Switching Output Limits for Actel FPGAs" application note on page 4-125.*

A32200DX Timing Characteristics

(Worst-Case Commercial Conditions)

		Advanced Information								
Logic Module Propagation Delays		**'–2 Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Combinatorial Functions										
t_{PD}	Internal Array Module Delay		2.0		2.7		3.2		5.2	ns
t_{PDD}	Internal Decode Module Delay		2.5		3.3		3.9		5.7	ns
Predicted Module Routing Delays										
t_{RD1}	FO=1 Routing Delay		1.1		1.5		1.8		3.3	ns
t_{RD2}	FO=2 Routing Delay		1.7		2.2		2.6		4.3	ns
t_{RD3}	FO=3 Routing Delay		2.1		2.8		3.3		5.2	ns
t_{RD4}	FO=4 Routing Delay		2.6		3.4		4.0		6.5	ns
t_{RD5}	FO=8 Routing Delay		4.5		6.0		7.0		10.0	ns
t_{RDD}	Decode-to-Output Routing Delay		0.6		0.8		0.9		0.4	ns
Sequential Timing Characteristics										
t_{CO}	Flip-Flop Clock-to-Output		2.3		3.1		3.6		5.0	ns
t_{GO}	Latch Gate-to-Output		2.0		2.7		3.2		5.0	ns
t_{SU}	Flip-Flop (Latch) Setup Time	0.3		0.4		0.47		0.7		ns
t_{H}	Flip-Flop (Latch) Hold Time	0.0		0.0		0.0		0.0		ns
t_{RO}	Flip-Flop (Latch) Reset to Output		2.3		3.1		3.6		5.0	ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	0.6		0.9		1.0		1.4		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.1		4.2		4.9		7.0		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.1		5.5		6.5		7.0		ns

A32200DX Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

		Advanced Information								
Logic Module Timing		**'–2 Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Synchronous SRAM Operations										
t_{RC}	Read Cycle Time	6.4		8.5		10.0		14.3		ns
t_{WC}	Write Cycle Time	6.4		8.5		10.0		14.3		ns
t_{RCKHL}	Clock High/Low Time	3.2		4.3		5.0		7.1		ns
t_{RCO}	Data Valid After Clock High/Low		3.2		4.3		5.0		7.1	ns
t_{ADSU}	Address/Data Setup Time	1.5		2.0		2.4		3.4		ns
t_{ADH}	Address/Data Hold Time	0.0		0.0		0.0		0.0		ns
t_{RENSU}	Read Enable Setup	0.6		0.8		0.9		1.4		ns
t_{RENH}	Read Enable Hold	3.2		4.3		5.0		0.7		ns
t_{WENSU}	Write Enable Setup	2.6		3.4		4.0		5.4		ns
t_{WENH}	Write Enable Hold	0.0		0.0		0.0		0.0		ns
t_{BENS}	Block Enable Setup	2.6		3.5		4.1		5.6		ns
t_{BENH}	Block Enable Hold	0.0		0.0		0.0		0.0		ns
Asynchronous SRAM Operations										
t_{RPD}	Asynchronous Access Time		7.7		10.2		12.0		17.2	ns
t_{RDADV}	Read Address Valid	8.3		11.1		13.0		18.6		ns
t_{ADSU}	Address/Data Setup Time	1.5		2.0		2.4		3.4		ns
t_{ADH}	Address/Data Hold Time	0.0		0.0		0.0		0.0		ns
t_{RENSUA}	Read Enable Setup to Address Valid	0.57		0.8		0.9		1.4		ns
t_{RENHA}	Read Enable Hold	3.2		4.3		5.0		7.1		ns
t_{WENSU}	Write Enable Setup	2.6		3.4		4.0		5.4		ns
t_{WENH}	Write Enable Hold	0.0		0.0		0.0		0.0		ns
t_{DOH}	Data Out Hold Time		1.1		1.5		1.8		2.6	ns

A32200DX Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

			Advanced Information								
Input Module Propagation Delays			**'–2' Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INPY}	Input Data Pad to Y			1.4		1.9		2.2		2.9	ns
t_{INGO}	Input Latch Gate-to-Output[1]			3.3		4.3		5.1		5.0	ns
t_{INH}	Input Latch Hold[1]		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Latch Setup[1]		0.45		0.6		0.7		0.6		ns
t_{ILA}	Latch Active Pulse Width[1]		4.4		5.9		6.9		7.0		ns
Input Module Predicted Routing Delays											
t_{IRD1}	FO=1 Routing Delay			1.9		2.6		3.0		6.1	ns
t_{IRD2}	FO=2 Routing Delay			2.5		3.3		3.9		7.0	ns
t_{IRD3}	FO=3 Routing Delay			3.3		4.4		5.2		7.6	ns
t_{IRD4}	FO=4 Routing Delay			3.9		5.2		6.1		8.7	ns
t_{IRD5}	FO=8 Routing Delay			5.0		6.7		7.9		8.7	ns
t_{IRDD}	Decode-to-Output Delay			0.3		0.4		0.5		12.6	ns
Global Clock Network											
t_{CKH}	Input Low to High	FO=32		5.3		7.1		8.3		8.4	ns
		FO=635		6.1		8.2		9.6		9.9	ns
t_{CKL}	Input High to Low	FO=32		5.2		7.0		8.2		8.4	ns
		FO=635		6.8		9.0		10.6		11.3	ns
t_{PWH}	Minimum Pulse Width High	FO=32	2.7		3.7		4.3		6.1		ns
		FO=635	2.9		3.9		4.6		6.6		ns
t_{PWL}	Minimum Pulse Width Low	FO=32	2.7		3.7		4.3		6.1		ns
		FO=635	2.9		3.9		4.6		6.6		ns
t_{CKSW}	Maximum Skew	FO=32		0.6		0.9		1.0		1.4	ns
		FO=635		0.6		0.9		1.0		1.4	ns
t_{SUEXT}	Input Latch External Setup	FO=32	0.0		0.0		0.0		0.0		ns
		FO=635	0.0		0.0		0.0		0.0		ns
t_{HEXT}	Input Latch External Hold	FO=32	2.2		2.9		3.4		4.9		ns
		FO=635	2.7		3.7		4.3		6.1		ns
t_P	Minimum Period (1/fmax)	FO=32	5.5		7.4		8.7		12.4		ns
		FO=635	6.1		8.2		9.6		13.7		ns
f_{HMAX}	Maximum Datapath Frequency	FO=32		165.3		132.3		115.0		80.0	MHz
		FO=635		150.9		120.8		105.0		73.0	MHz

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.

A32200DX Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

		Advanced Information								
Output Module Timing		**'–2' Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]										
t_{DLH}	Data to Pad High		3.7		4.9		5.8		4.8	ns
t_{DHL}	Data to Pad Low		4.5		6.0		7.1		6.2	ns
t_{ENZH}	Enable Pad Z to High		4.8		6.4		7.5		7.2	ns
t_{ENZL}	Enable Pad Z to Low		5.2		6.9		8.1		7.9	ns
t_{ENHZ}	Enable Pad High to Z		8.3		11.1		13.0		14.0	ns
t_{ENLZ}	Enable Pad Low to Z		8.3		11.1		13.0		14.0	ns
t_{GLH}	G to Pad High		8.3		11.1		13.0		8.0	ns
t_{GHL}	G to Pad Low		8.9		11.9		14.0		9.0	ns
t_{LSU}	I/O Latch Output Setup	0.26		0.3		0.4		0.6		ns
t_{LH}	I/O Latch Output Hold	0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		8.4		11.1		13.1		18.7	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		11.8		15.7		18.5		26.5	ns
d_{TLH}	Capacitive Loading, Low to High		0.03		0.0		0.05		0.07	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.04		0.1		0.07		0.10	ns/pF
t_{WDO}	Hard-Wired Wide Decode Output		0.04		0.1		0.06		0.09	ns
CMOS Output Module Timing[1]										
t_{DLH}	Data to Pad High		3.7		4.9		7.1		9.1	ns
t_{DHL}	Data to Pad Low		4.5		6.0		5.8		6.4	ns
t_{ENZH}	Enable Pad Z to High		4.8		6.4		7.5		7.2	ns
t_{ENZL}	Enable Pad Z to Low		5.2		6.9		8.1		7.9	ns
t_{ENHZ}	Enable Pad High to Z		8.3		11.1		13.0		14.0	ns
t_{ENLZ}	Enable Pad Low to Z		8.3		11.1		13.0		14.0	ns
t_{GLH}	G to Pad High		8.3		11.1		13.0		8.0	ns
t_{GHL}	G to Pad Low		8.9		11.9		14.0		9.0	ns
t_{LSU}	I/O Latch Setup	0.26		0.3		0.4		0.6		ns
t_{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		9.9		13.2		15.5		22.3	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		13.9		18.5		21.8		31.2	ns
d_{TLH}	Capacitive Loading, Low to High		0.04		0.1		0.07		0.10	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.04		0.1		0.06		0.09	ns/pF
t_{WDO}	Hard-Wired Wide Decode Output		0.04		0.1		0.06		0.09	ns

Notes:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.*
2. *SSO information can be found in the "Simultaneously Switching Output Limits for Actel FPGAs" application note on page 4-125.*

A32300DX Timing Characteristics

(Worst-Case Commercial Conditions)

		Advanced Information								
Logic Module Propagation Delays		**'–2 Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Combinatorial Functions										
t_{PD}	Internal Array Module Delay		2.2		2.9		3.4		5.2	ns
t_{PDD}	Internal Decode Module Delay		2.5		3.3		3.9		5.7	ns
Predicted Module Routing Delays										
t_{RD1}	FO=1 Routing Delay		1.1		1.5		1.8		3.3	ns
t_{RD2}	FO=2 Routing Delay		1.7		2.3		2.7		4.3	ns
t_{RD3}	FO=3 Routing Delay		2.4		3.1		3.7		5.2	ns
t_{RD4}	FO=4 Routing Delay		2.9		3.9		4.6		6.5	ns
t_{RD5}	FO=8 Routing Delay		5.2		7.0		8.2		10.0	ns
t_{RDD}	Decode-to-Output Routing Delay		0.6		0.8		0.9		0.4	ns
Sequential Timing Characteristics										
t_{CO}	Flip-Flop Clock-to-Output		2.3		3.1		3.6		5.0	ns
t_{GO}	Latch Gate-to-Output		2.2		2.9		3.4		5.0	ns
t_{SU}	Flip-Flop (Latch) Setup Time	0.3		0.3		0.5		0.7		ns
t_{H}	Flip-Flop (Latch) Hold Time	0.0		0.0		0.0		0.0		ns
t_{RO}	Flip-Flop (Latch) Reset to Output		2.2		3.0		3.5		5.0	ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	0.6		0.9		1.0		1.4		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.1		4.2		4.9		7.0		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	3.5		4.7		5.5		7.0		ns

A32300DX Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

		Advanced Information								
Logic Module Timing		**'–2 Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Synchronous SRAM Operations										
t_{RC}	Read Cycle Time	6.4		8.5		10.0		14.3		ns
t_{WC}	Write Cycle Time	6.4		8.5		10.0		14.3		ns
t_{RCKHL}	Clock High/Low Time	3.2		4.3		5.0		7.1		ns
t_{RCO}	Data Valid After Clock High/Low		3.2		4.3		5.0		7.1	ns
t_{ADSU}	Address/Data Setup Time	1.5		2.0		2.4		3.4		ns
t_{ADH}	Address/Data Hold Time	0.0		0.0		0.0		0.0		ns
t_{RENSU}	Read Enable Setup	0.6		0.8		0.9		1.4		ns
t_{RENH}	Read Enable Hold	3.2		4.3		5.0		0.7		ns
t_{WENSU}	Write Enable Setup	2.6		3.4		4.0		5.4		ns
t_{WENH}	Write Enable Hold	0.0		0.0		0.0		0.0		ns
t_{BENS}	Block Enable Setup	2.6		3.5		4.1		5.6		ns
t_{BENH}	Block Enable Hold	0.0		0.0		0.0		0.0		ns
Asynchronous SRAM Operations										
t_{RPD}	Asynchronous Access Time		7.7		10.2		12.0		17.2	ns
t_{RDADV}	Read Address Valid	8.3		11.1		13.0		18.6		ns
t_{ADSU}	Address/Data Setup Time	1.5		2.0		2.4		3.4		ns
t_{ADH}	Address/Data Hold Time	0.0		0.0		0.0		0.0		ns
t_{RENSUA}	Read Enable Setup to Address Valid	0.57		0.8		0.9		1.4		ns
t_{RENHA}	Read Enable Hold	3.2		4.3		5.0		7.1		ns
t_{WENSU}	Write Enable Setup	2.6		3.4		4.0		5.4		ns
t_{WENH}	Write Enable Hold	0.0		0.0		0.0		0.0		ns
t_{DOH}	Data Out Hold Time		1.1		1.5		1.8		2.6	ns

A32300DX Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

			Advanced Information								
Input Module Propagation Delays			**'–2' Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INPY}	Input Data Pad to Y			1.4		1.9		2.2		2.9	ns
t_{INGO}	Input Latch Gate-to-Output[1]			2.9		3.8		4.5		5.0	ns
t_{INH}	Input Latch Hold[1]		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Latch Setup[1]		0.45		0.6		0.7		0.6		ns
t_{ILA}	Latch Active Pulse Width[1]		4.4		5.9		6.9		7.0		ns
Input Module Predicted Routing Delays											
t_{IRD1}	FO=1 Routing Delay			1.9		2.6		3.0		6.1	ns
t_{IRD2}	FO=2 Routing Delay			2.5		3.3		3.9		7.0	ns
t_{IRD3}	FO=3 Routing Delay			3.3		4.4		5.2		7.6	ns
t_{IRD4}	FO=4 Routing Delay			3.9		5.2		6.1		8.7	ns
t_{IRD5}	FO=8 Routing Delay			5.0		6.7		7.9		8.7	ns
t_{RDD}	Decode-to-Output Routing Delay			0.6		0.8		0.9			ns
Global Clock Network											
t_{CKH}	Input Low to High	FO=32		6.4		8.6		10.1		8.4	ns
		FO=635		7.3		9.7		11.4		9.9	ns
t_{CKL}	Input High to Low	FO=32		6.6		8.8		10.3		8.4	ns
		FO=635		7.1		9.5		11.2		11.3	ns
t_{PWH}	Minimum Pulse Width High	FO=32	3.0		4.0		4.7		6.1		ns
		FO=635	3.3		4.3		5.1		6.6		ns
t_{PWL}	Minimum Pulse Width Low	FO=32	3.0		4.0		4.7		6.1		ns
		FO=635	3.3		4.3		5.1		6.6		ns
t_{CKSW}	Maximum Skew	FO=32		0.6		0.9		1.0		1.4	ns
		FO=635		0.6		0.9		1.0		1.4	ns
t_{SUEXT}	Input Latch External Setup	FO=32	0.0		0.0		0.0		0.0		ns
		FO=635	0.0		0.0		0.0		0.0		ns
t_{HEXT}	Input Latch External Hold	FO=32	2.2		2.9		3.4		4.9		ns
		FO=635	2.7		3.7		4.3		6.1		ns
t_P	Minimum Period (1/fmax)	FO=32	5.5		7.4		9.3		12.4		ns
		FO=635	6.1		8.2		10.2		13.7		ns
f_{HMAX}	Maximum Datapath Frequency	FO=32		153.8		123.1		107		74.9	MHz
		FO=635		140.9		112.7		98		68.6	MHz

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.

A32300DX Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

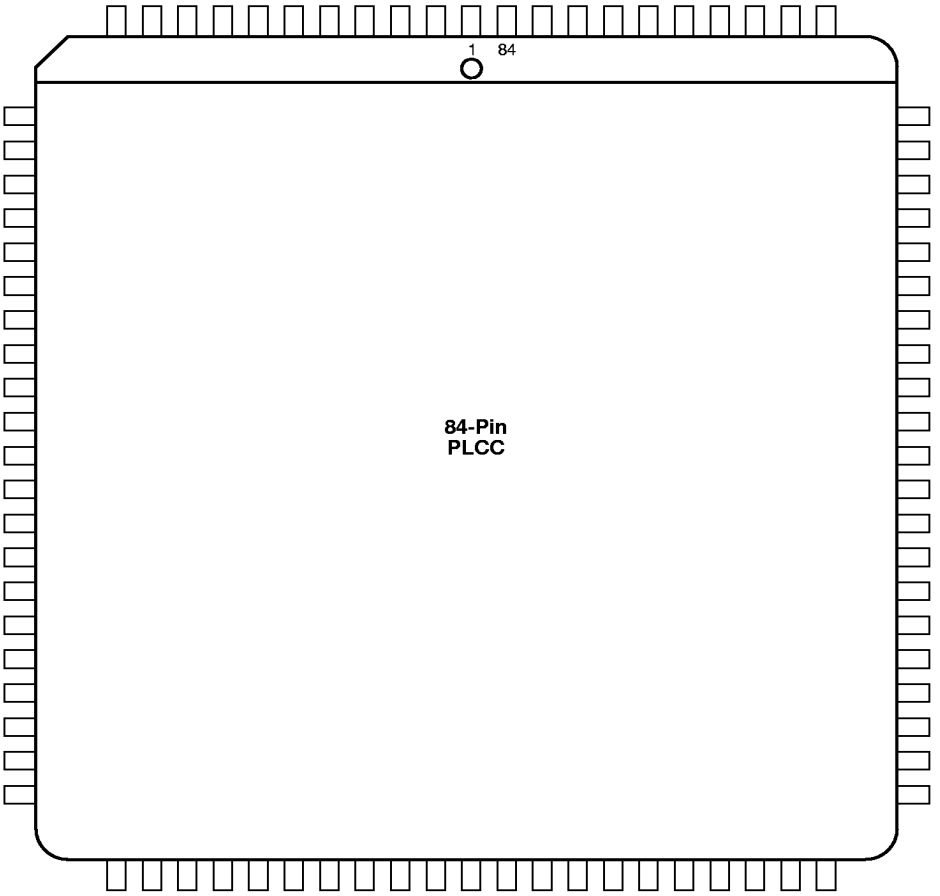
		Advanced Information								
Output Module Timing		**'–2' Speed**		**'–1' Speed**		**'Std' Speed**		**'–F' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]										
t_{DLH}	Data to Pad High		3.7		4.9		5.8		4.8	ns
t_{DHL}	Data to Pad Low		4.4		5.9		6.9		6.2	ns
t_{ENZH}	Enable Pad Z to High		4.8		6.4		7.5		7.2	ns
t_{ENZL}	Enable Pad Z to Low		5.1		6.8		8.0		7.9	ns
t_{ENHZ}	Enable Pad High to Z		8.3		11.1		13.0		14.0	ns
t_{ENLZ}	Enable Pad Low to Z		8.3		11.1		13.0		14.0	ns
t_{GLH}	G to Pad High		4.3		5.7		6.7		8.0	ns
t_{GHL}	G to Pad Low		5.4		7.1		8.4		9.0	ns
t_{LSU}	I/O Latch Output Setup	0.26		0.3		0.4		0.6		ns
t_{LH}	I/O Latch Output Hold	0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		8.4		11.1		13.1		18.7	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		11.8		15.7		18.5		26.5	ns
d_{TLH}	Capacitive Loading, Low to High		0.26		0.3		0.4		0.07	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.32		0.4		0.5		0.10	ns/pF
t_{WDO}	Hard-Wired Wide Decode Output		0.03		0.04		0.05		0.09	ns
CMOS Output Module Timing[1]										
t_{DLH}	Data to Pad High		4.4		5.9		6.9		9.1	ns
t_{DHL}	Data to Pad Low		3.7		4.9		5.8		6.4	ns
t_{ENZH}	Enable Pad Z to High		4.8		6.4		7.5		7.2	ns
t_{ENZL}	Enable Pad Z to Low		5.1		6.8		8.0		7.9	ns
t_{ENHZ}	Enable Pad High to Z		8.3		11.1		13.0		14.0	ns
t_{ENLZ}	Enable Pad Low to Z		8.3		11.1		13.0		14.0	ns
t_{GLH}	G to Pad High		4.3		5.7		6.7		8.0	ns
t_{GHL}	G to Pad Low		5.4		7.1		8.4		9.0	ns
t_{LSU}	I/O Latch Setup	0.26		0.34		0.4		0.6		ns
t_{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		9.9		13.2		15.5		22.3	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		13.9		18.5		21.8		31.2	ns
d_{TLH}	Capacitive Loading, Low to High		0.32		0.4		0.5		0.10	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.26		0.3		0.4		0.09	ns/pF
t_{WDO}	Hard-Wired Wide Decode Output		0.03		0.04		0.05		0.09	ns

Notes:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.*
2. *SSO information can be found in the "Simultaneously Switching Output Limits for Actel FPGAs" application note on page 4-125.*

Package Pin Assignments

84-Pin PLCC Package (Top View)



84-Pin PLCC Package

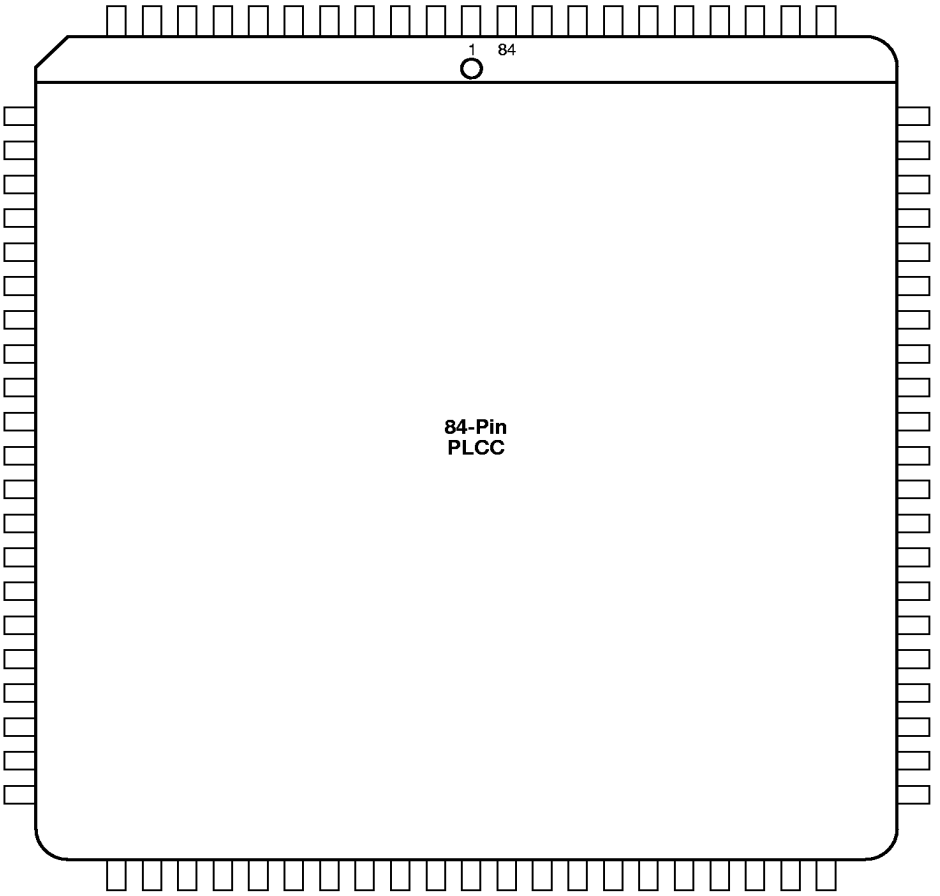
Pin Number	A1225XL Function	A1240XL Function	A3265DX Function	A1280XL Function	A32100DX Function
2	CLKB,I/O	CLKB,I/O	CLKB,I/O	CLKB,I/O	CLKB
4	PRB,I/O	PRB,I/O	PRB,I/O	PRB,I/O	PRB
5	I/O	I/O	I/O (WD)	I/O	I/O (WD)
6	GND	GND	GND	GND	—
7	—	—	—	—	QCLKC
8	I/O	I/O	I/O (WD)	I/O	I/O (WD)
9	I/O	I/O	I/O (WD)	I/O	I/O (WD)
10	DCLK,I/O	DCLK,I/O	DCLK,I/O	DCLK,I/O	DCLK
12	MODE (GND)	MODE (GND)	MODE (GND)	MODE (GND)	MODE (GND)
22	VCC	VCC	VCC	VCC	VCC
23	VCC	VCC	VCC	VCC	VSV (VCC)
28	GND	GND	GND	GND	GND
38	I/O	I/O	I/O (WD)	I/O	I/O
39	I/O	I/O	I/O (WD)	I/O	I/O
43	VCC	VCC	VCC	VCC	VCC
44	I/O	I/O	I/O (WD)	I/O	I/O
46	I/O	I/O	I/O (WD)	I/O	I/O
47	I/O	I/O	I/O (WD)	I/O	I/O
49	GND	GND	GND	GND	GND
63	GND	GND	GND	GND	GND
64	VCC	VCC	VCC	VCC	VCC
65	VCC	VCC	VCC	VCC	VCC
70	GND	GND	GND	GND	GND
76	SDI,I/O	SDI,I/O	SDI,I/O	SDI,I/O	SDI,I/O
78	I/O	I/O	I/O (WD)	I/O	I/O
79	I/O	I/O	I/O (WD)	I/O	I/O
80	I/O	I/O	I/O (WD)	I/O	I/O
81	PRA,I/O	PRA,I/O	PRA,I/O	PRA,I/O	PRA,I/O
83	CLKA,I/O	CLKA,I/O	CLKA,I/O	CLKA,I/O	CLKA,I/O
84	VCC	VCC	VCC	VCC	VCC

Notes:

1. *I/O (WD) : Denotes I/O pin with an associated Wide Decode Module*
2. *Wide Decode I/O (WD) can also be general purpose user I/O*
3. *NC : Denotes No Connection*
4. *All unlisted pin numbers are user I/O's*
5. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

Package Pin Assignments

84-Pin PLCC Package (Top View)



84-Pin PLCC Package

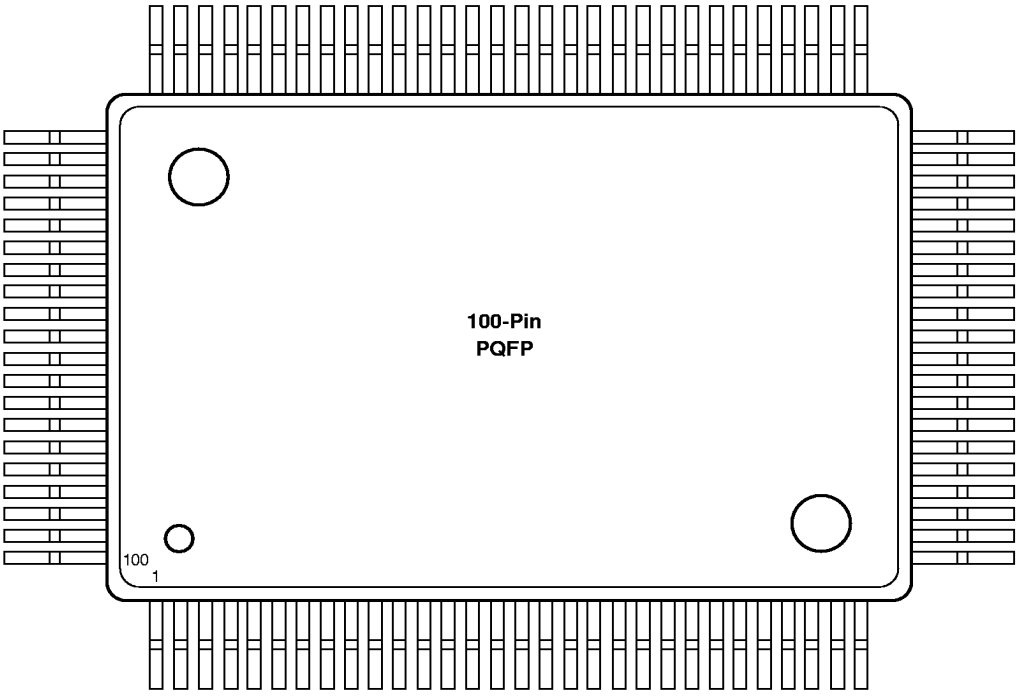
Pin Number	A32100DX Function
2	CLKB, I/O
4	PRB, I/O
5	I/O (WD)
7	QCLKC, I/O
8	I/O (WD)
9	I/O (WD)
10	DCLK, I/O
12	MODE (GND)
22	VCC
23	VSV (VCC)
28	GND
34	TMS, I/O
35	TDI, I/O
36	I/O (WD)
37	QCLKA, I/O
38	I/O (WD)
39	I/O (WD)
43	VCC
44	I/O (WD)
45	QCLKB, I/O
46	I/O (WD)
47	I/O (WD)
50	GND
51	I/O (WD)
52	SDI
53	TCK, I/O
63	VKS (GND)
64	VPP (VCC)
65	VCC
70	GND
76	SDI, I/O
78	I/O (WD)
79	I/O (WD)
80	QCLKD, I/O
81	PRA, I/O
83	CLKA, I/O
84	VCC

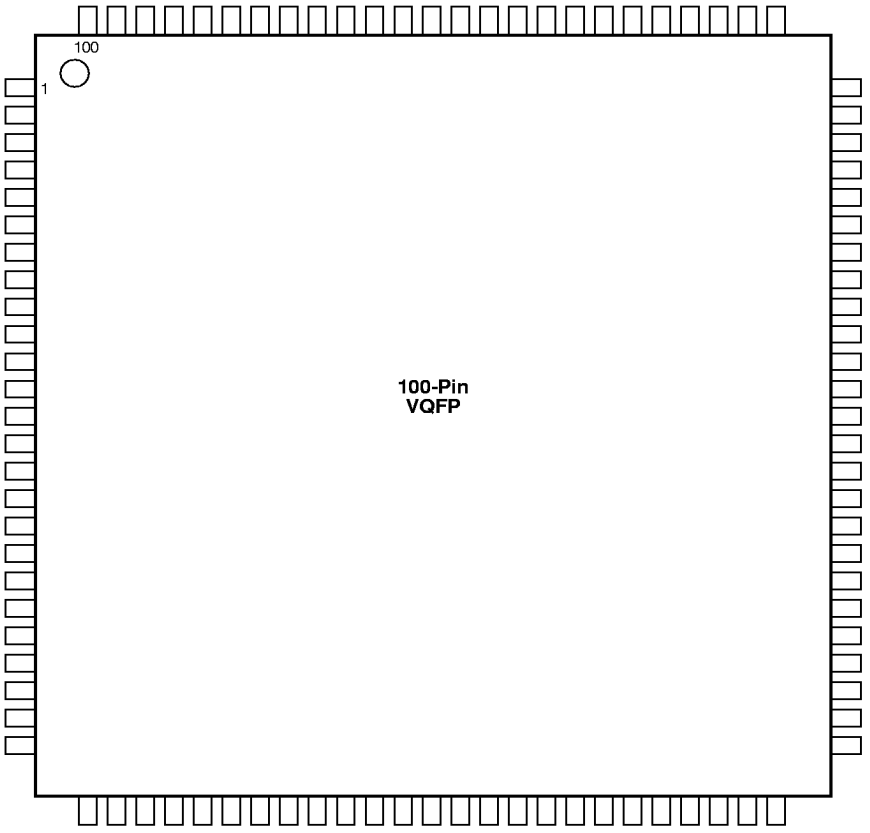
Notes:

1. *I/O (WD) : Denotes I/O pin with an associated Wide Decode Module*
2. *Wide Decode I/O (WD) can also be general purpose user I/O*
3. *NC : Denotes No Connection*
4. *All unlisted pin numbers are user I/O's*
5. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

Package Pin Assignments (continued)

100-pin PQFP Package, 100-pin VQFP Package (Top View)





100-pin PQFP Package, 100-pin VQFP Package

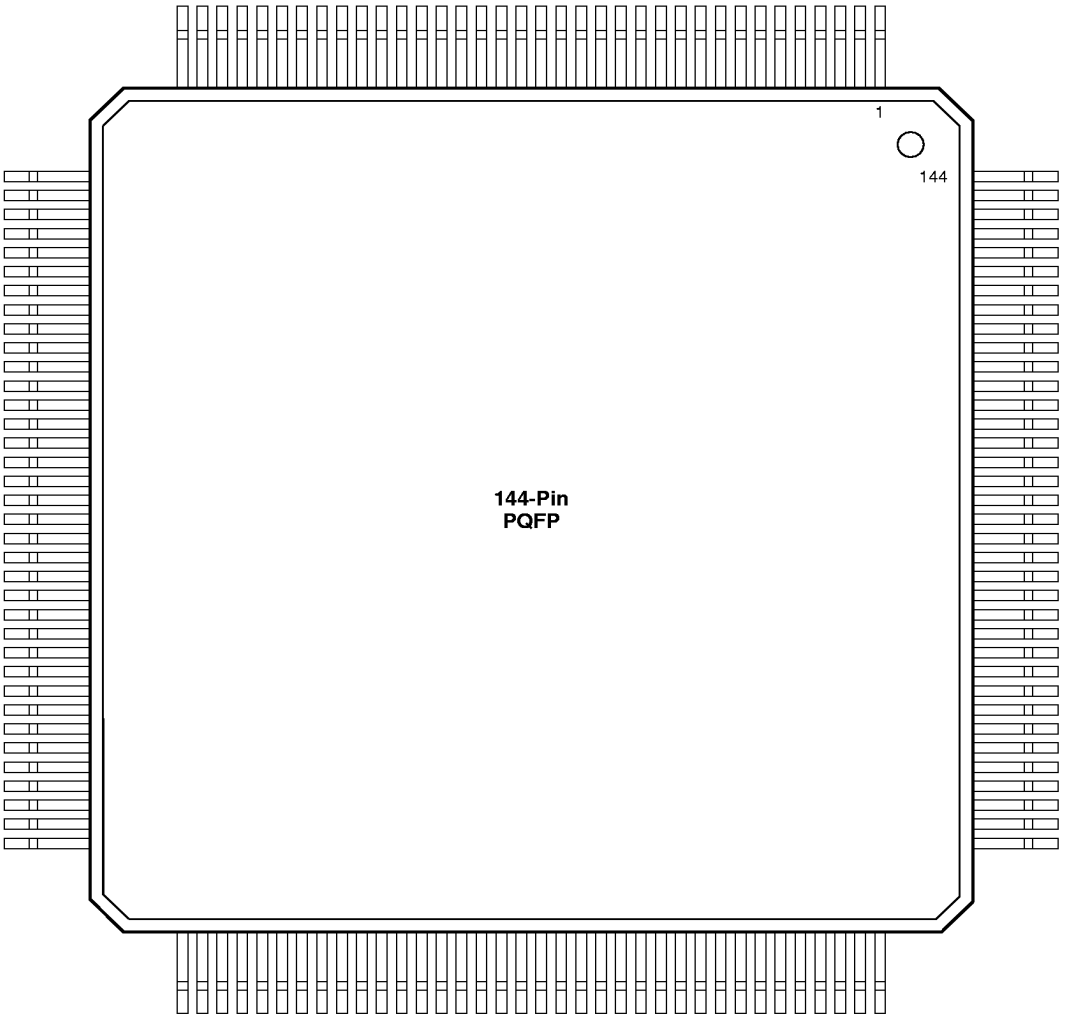
Pin Number	A1225XL-PQ100 Function	A1225XL-VQ100 Function	A1240XL-PQ100 Function
2	DCLK, I/O	MODE (GND)	DCLK, I/O
4	MODE	I/O	MODE (GND)
7	I/O	GND	I/O
9	GND	I/O	GND
14	I/O	VCC	I/O
15	I/O	VCC	I/O
16	VCC	I/O	VCC
17	VCC	I/O	VCC
20	I/O	GND	I/O
22	GND	I/O	GND
32	I/O	GND	I/O
34	GND	I/O	GND
38	I/O	VCC	I/O
40	VCC	I/O	VCC
44	I/O	GND	I/O
46	GND	I/O	GND
55	I/O	GND	I/O
57	GND	I/O	GND
62	I/O	GND	I/O
63	I/O	VCC	I/O
64	GND	VCC	GND
65	VCC	VCC	VCC
66	VCC	I/O	VCC
67	VCC	I/O	VCC
70	I/O	GND	I/O
72	GND	I/O	GND
77	I/O	SDI, I/O	I/O
79	SDI, I/O	I/O	SDI, I/O
82	I/O	GND	I/O
84	GND	I/O	GND
85	I/O	PRA, I/O	I/O
87	PRA, I/O	CLKA, I/O	PRA, I/O
88	I/O	VCC	I/O
89	CLKA, I/O	I/O	CLKA, I/O
90	VCC	CLKB, I/O	VCC
92	CLKB, I/O	PRB, I/O	CLKB, I/O
94	PRB, I/O	GND	PRB, I/O
96	GND	I/O	GND
100	I/O	DCLK, I/O	I/O

Notes:

1. *NC : Denotes No Connection*
2. *All unlisted pin numbers are user I/O's*
3. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

Package Pin Assignments (continued)

144-Pin PQFP Package (Top View)



144-Pin PQFP Package

Pin Number	A1240XL Function
2	MODE (GND)
9	GND
10	GND
11	GND
18	VCC
19	VCC
20	VCC
21	VCC
28	GND
29	GND
30	GND
44	GND
45	GND
46	GND
54	VCC
55	VCC
56	VCC
64	GND
65	GND
79	GND
80	GND
81	GND
88	GND

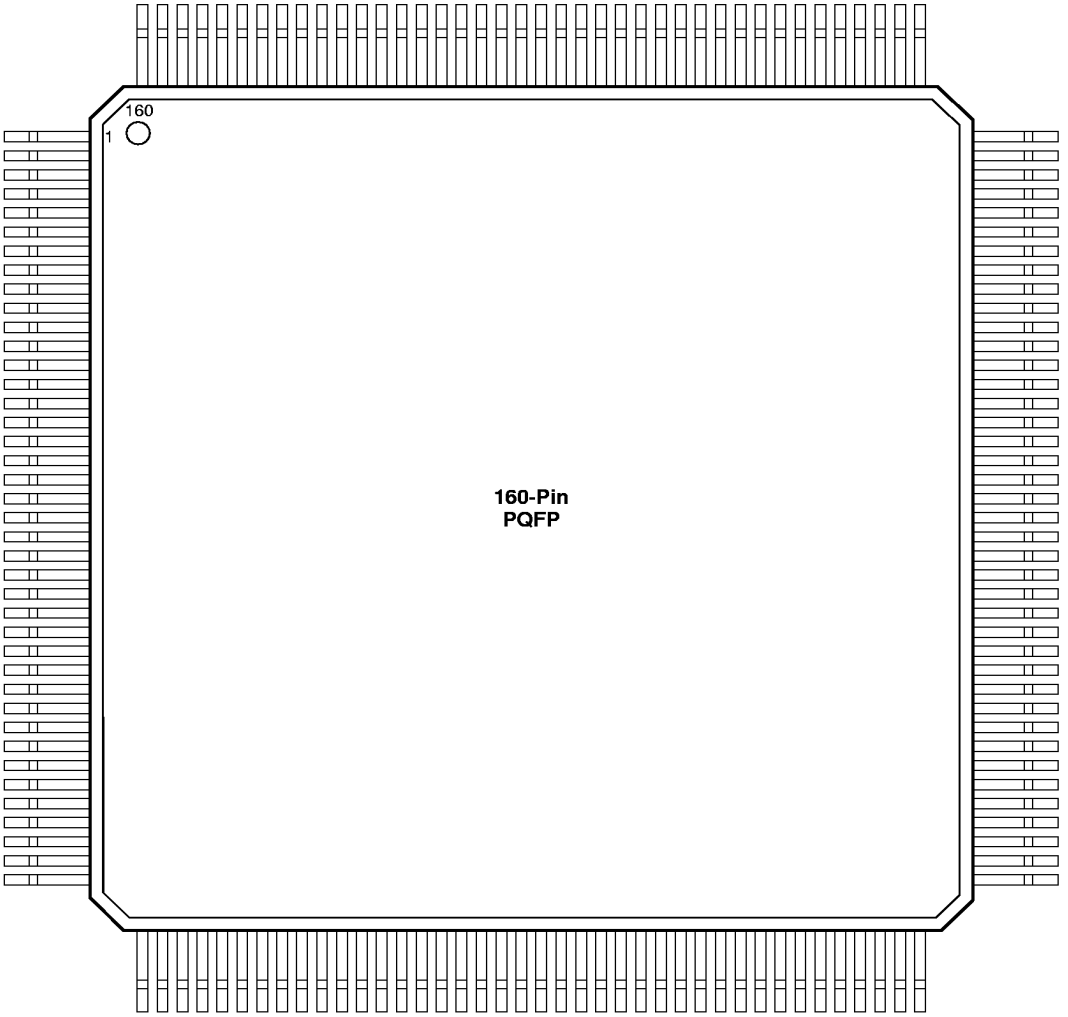
Pin Number	A1240XL Function
89	VCC
90	VCC
91	VCC
92	VCC
93	VCC
100	GND
101	GND
102	GND
110	SDI, I/O
116	GND
117	GND
118	GND
123	PRA, I/O
125	CLKA, I/O
126	VCC
127	VCC
128	VCC
130	CLKB, I/O
132	PRB, I/O
136	GND
137	GND
138	GND
144	DCLK, I/O

Notes:

1. *NC : Denotes No Connection*
2. *All unlisted pin numbers are user I/O's*
3. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

Package Pin Assignments (continued)

160-pin PQFP Package (Top View)



Notes:

1. *I/O (WD) : Denotes I/O pin with an associated Wide Decode Module*
2. *Wide Decode I/O (WD) can also be general purpose user I/O*
3. *NC : Denotes No Connection*
4. *All unlisted pin numbers are user I/O's*
5. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

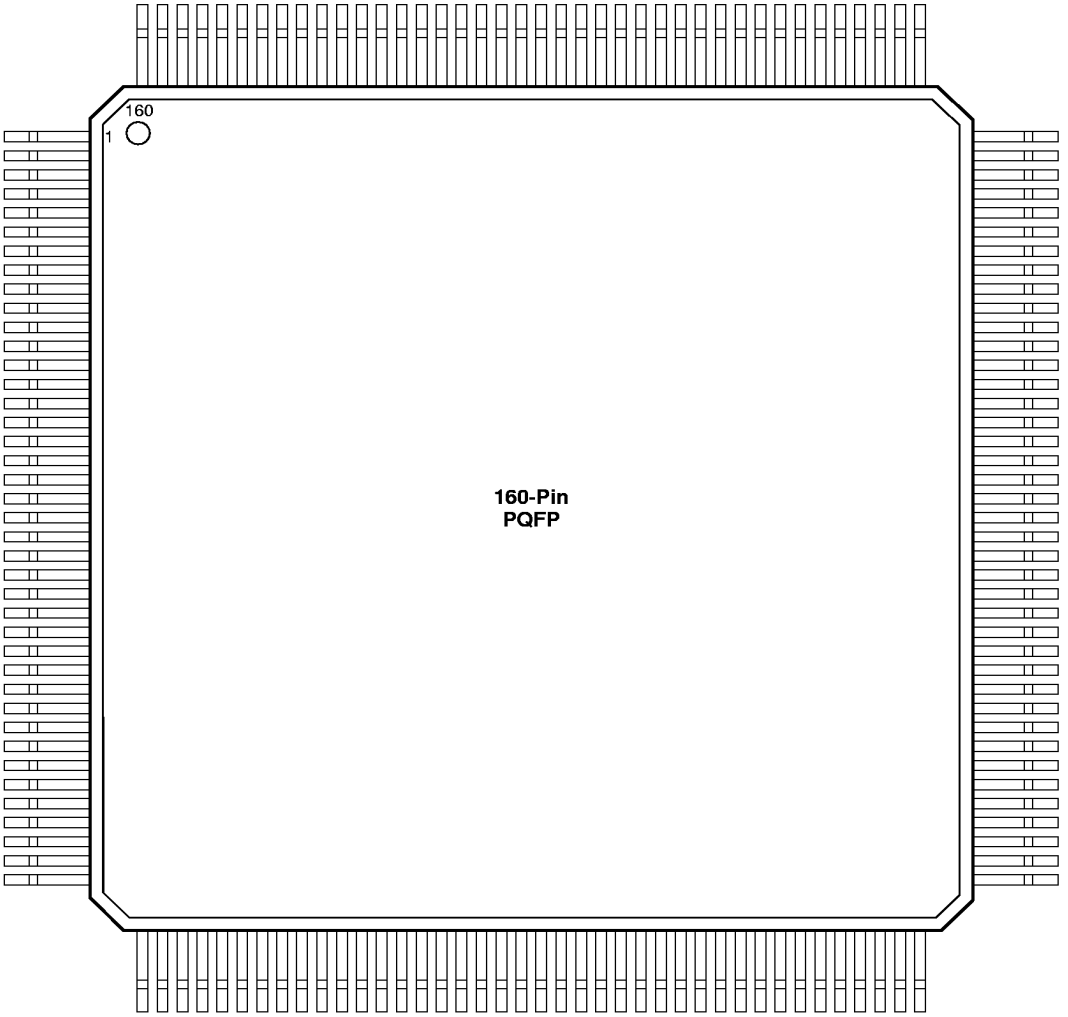
160-Pin PQFP Package

Pin Number	A3265DX Function	A1280XL Function	A32140DX Function
2	DCLK,I/O	DCLK,I/O	DCLK,I/O
4	I/O	I/O	I/O (WD)
5	I/O (WD)	I/O	I/O (WD)
6	VCC	VCC	VCC
7	I/O (WD)	I/O	I/O
11	GND	GND	GND
13	I/O (WD)	I/O	I/O (WD)
14	I/O (WD)	I/O	I/O (WD)
16	PRB,I/O	PRB,I/O	PRB,I/O
18	CLKB,I/O	CLKB,I/O	CLKB,I/O
20	VCC	VCC	VCC
21	CLKA,I/O	CLKA,I/O	CLKA,I/O
23	PRA,I/O	PRA,I/O	PRA,I/O
24	I/O	I/O	I/O (WD)
25	I/O (WD)	I/O	I/O (WD)
26	I/O (WD)	I/O	I/O
29	I/O (WD)	I/O	I/O (WD)
30	GND	GND	GND
31	I/O (WD)	I/O	I/O (WD)
34	I/O (WD)	I/O	I/O
35	VCC	VCC	VCC
36	I/O (WD)	I/O	I/O (WD)
37	I/O	I/O	I/O (WD)
38	SDI,I/O	SDI,I/O	SDI,I/O
40	GND	GND	GND
44	GND	GND	GND
49	GND	GND	GND
54	VCC	VCC	VCC
57	VCC	VCC	VCC
58	VCC	VCC	VCC
59	GND	GND	GND
60	VCC	VCC	VCC
61	GND	GND	GND
62	I/O	I/O	TCK, I/O
64	GND	GND	GND
69	GND	GND	GND

Pin Number	A3265DX Function	A1280XL Function	A32140DX Function
80	GND	GND	GND
82	I/O	I/O	TDO, I/O
83	I/O	I/O	I/O (WD)
84	I/O	I/O	I/O (WD)
86	VCC	VCC	VCC
87	I/O (WD)	I/O	I/O
88	I/O (WD)	I/O	I/O (WD)
89	GND	GND	GND
92	I/O (WD)	I/O	I/O
93	I/O (WD)	I/O	I/O
96	I/O (WD)	I/O	I/O (WD)
97	I/O (WD)	I/O	I/O
98	VCC	VCC	VCC
99	GND	GND	GND
106	I/O (WD)	I/O	I/O (WD)
107	I/O (WD)	I/O	I/O (WD)
109	GND	GND	GND
111	I/O (WD)	I/O	I/O (WD)
112	I/O (WD)	I/O	I/O (WD)
114	VCC	VCC	VCC
115	I/O	I/O	I/O (WD)
116	I/O	I/O	I/O (WD)
118	I/O	I/O	TDI, I/O
119	I/O	I/O	TMS, I/O
120	GND	GND	GND
125	GND	GND	GND
130	GND	GND	GND
135	VCC	VCC	VCC
138	VCC	VCC	VCC
139	VCC	VCC	VCC
140	GND	GND	GND
145	GND	GND	GND
150	VCC	VCC	VCC
155	GND	GND	GND
159	MODE (GND)	MODE (GND)	MODE (GND)
160	GND	GND	GND

Package Pin Assignments (continued)

160-pin PQFP Package (Top View)



Notes:

1. *I/O (WD) : Denotes I/O pin with an associated Wide Decode Module*
2. *Wide Decode I/O (WD) can also be general purpose user I/O*
3. *NC : Denotes No Connection*
4. *All unlisted pin numbers are user I/O's*
5. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

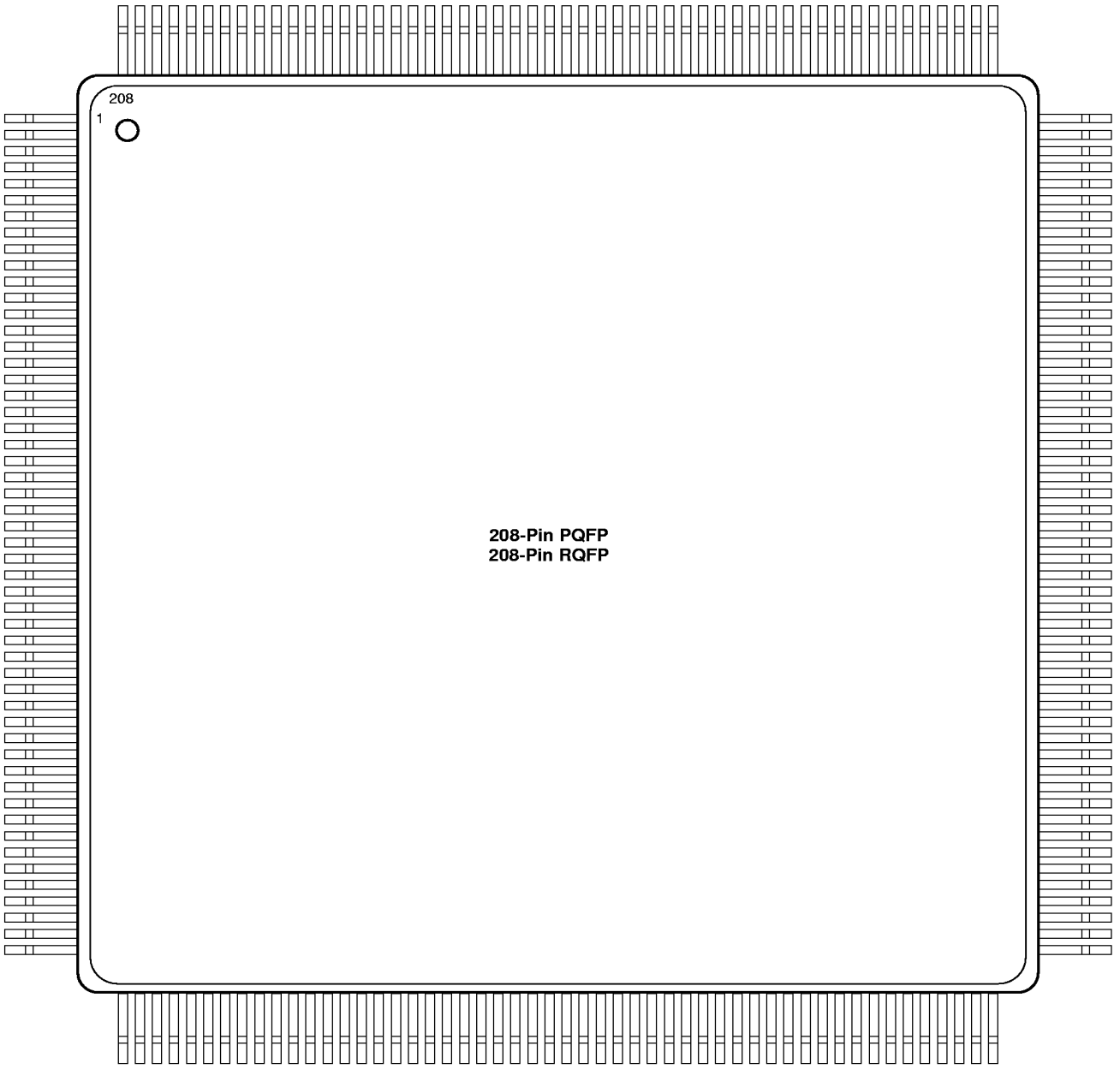
160-Pin PQFP Package

Pin Number	A32100DX Function
2	DCLK
4	I/O (WD)
5	I/O (WD)
6	VCC
11	GND
12	QCLKC, I/O
13	I/O (WD)
14	I/O (WD)
16	PRB, I/O
18	CLKB, I/O
20	VCC
21	CLKA, I/O
23	PRA, I/O
24	I/O (WD)
25	I/O (WD)
28	QCLKD
29	I/O (WD)
30	GND
31	I/O (WD)
35	VCC
36	I/O (WD)
37	I/O (WD)
38	SDI, I/O
40	GND
54	VCC
57	VSV (VCC)
58	VCC
59	GND
60	VPP (VCC)
61	VKS (GND)
62	TCK, I/O
64	GND
69	GND

Pin Number	A32100DX Function
80	GND
82	SDO, I/O
83	I/O (WD)
84	I/O (WD)
86	VCC
88	I/O (WD)
89	GND
90	I/O (WD)
91	QCLKB, I/O
95	I/O (WD)
96	I/O (WD)
98	VCC
99	GND
106	I/O (WD)
107	I/O (WD)
110	QCLKA, I/O
114	VCC
115	I/O (WD)
116	I/O (WD)
118	TDI, I/O
119	TMS, I/O
120	GND
125	GND
135	VCC
138	VSV (VCC)
139	VCC
140	GND
145	GND
150	VCC
155	GND
159	MODE (GND)
160	GND

Package Pin Assignments (continued)

208-Pin PQFP Package, 208-pin RQFP Package (Top View)



Notes:

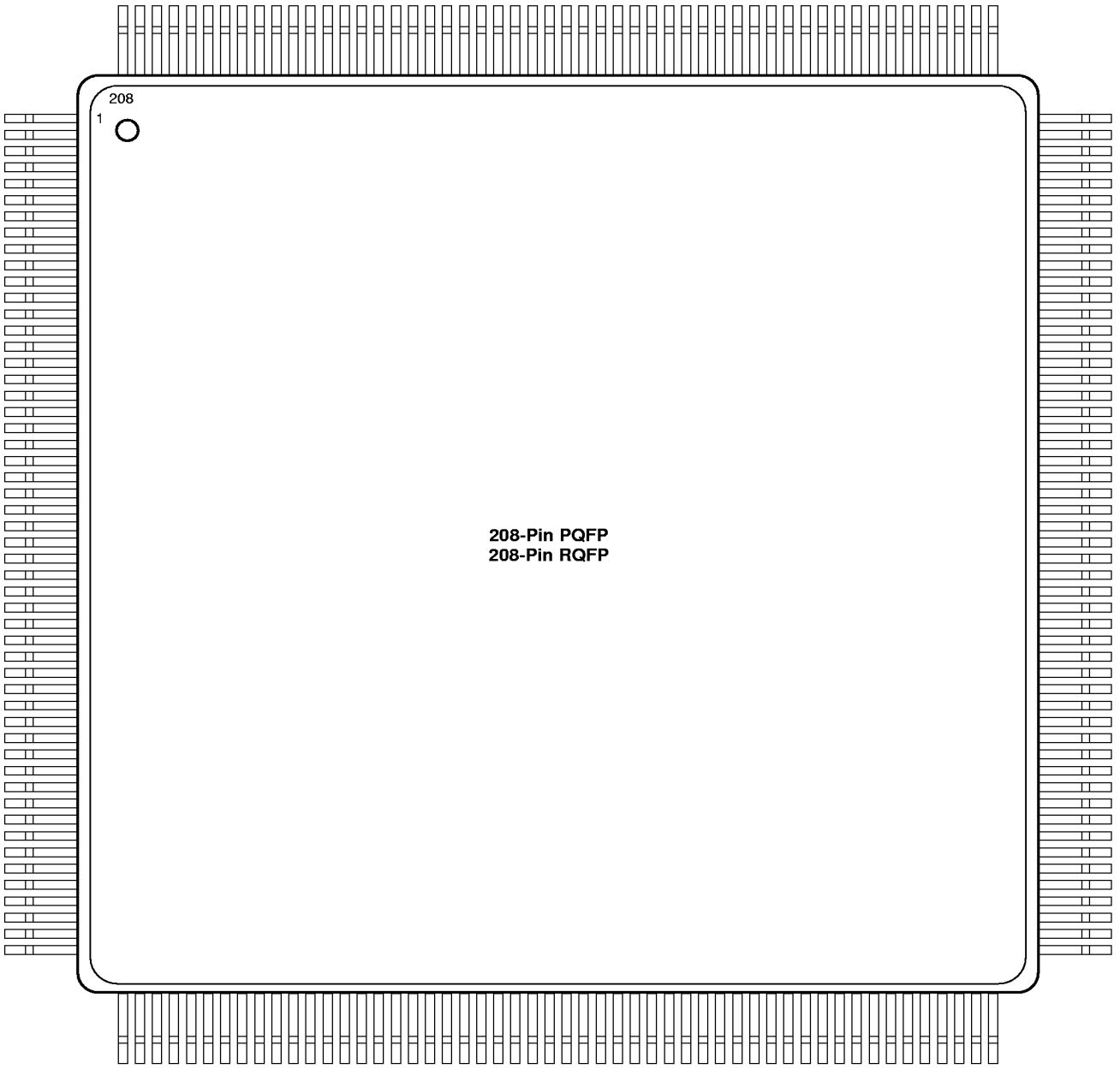
1. *I/O (WD) : Denotes I/O pin with an associated Wide Decode Module*
2. *Wide Decode I/O (WD) can also be general purpose user I/O*
3. *NC : Denotes No Connection*
4. *All unlisted pin numbers are user I/O's*
5. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*
6. *RQFP has an exposed circular metal heatsink on the top surface.*

208-Pin PQFP Package, 208-pin RQFP Package

Pin Number	A1280XL Function	A32140DX Function	A32200DX-PQ208 Function	A32200DX-RQ208 Function
1	GND	GND	GND	I/O
2	NC	VCC	VCC	DCLK, I/O
3	MODE (GND)	MODE (GND)	MODE (GND)	I/O
5	I/O	I/O	I/O	I/O (WD)
6	I/O	I/O	I/O	I/O (WD)
7	I/O	I/O	I/O	VCC
9	NC	I/O	I/O	I/O
10	NC	I/O	I/O	I/O
11	NC	I/O	I/O	I/O
13	I/O	I/O	I/O	QCLKC, I/O
15	I/O	I/O	I/O	I/O (WD)
16	NC	I/O	I/O	I/O (WD)
17	VCC	VCC	VCC	I/O
19	I/O	I/O	I/O	I/O (WD)
20	I/O	I/O	I/O	I/O (WD)
22	GND	GND	GND	PRB, I/O
24	I/O	I/O	I/O	CLKB, I/O
26	I/O	I/O	I/O	GND
27	GND	GND	GND	VCC
28	VCC	VCC	VCC	I/O
29	VCC	VCC	VCC	CLKA, I/O
30	I/O	I/O	I/O	PRA, I/O
32	VCC	VCC	VCC	I/O (WD)
33	I/O	I/O	I/O	I/O (WD)
38	I/O	I/O	I/O	QCLKD, I/O
40	I/O	I/O	I/O	I/O (WD)
41	NC	I/O	I/O	I/O (WD)
42	NC	I/O	I/O	I/O
43	NC	I/O	I/O	I/O
45	I/O	I/O	I/O	VCC
47	I/O	I/O	I/O	I/O (WD)
48	I/O	I/O	I/O	I/O (WD)
50	NC	I/O	I/O	SDI, I/O
51	NC	I/O	I/O	I/O
52	GND	GND	GND	GND
53	GND	GND	GND	I/O
54	I/O	TMS, I/O	TMS, I/O	I/O
55	I/O	TDI, I/O	TDI, I/O	I/O
57	I/O	I/O (WD)	I/O (WD)	I/O
58	I/O	I/O (WD)	I/O (WD)	I/O
59	I/O	I/O	I/O	GND
60	VCC	VCC	VCC	I/O
61	NC	I/O	I/O	I/O
62	NC	I/O	I/O	I/O
65	I/O	I/O	QCLKA, I/O	I/O
66	I/O	I/O (WD)	I/O (WD)	I/O
67	NC	I/O (WD)	I/O (WD)	I/O
68	NC	I/O	I/O	I/O
70	I/O	I/O (WD)	I/O (WD)	I/O
71	I/O	I/O (WD)	I/O (WD)	I/O
74	I/O	I/O	I/O	VCC
77	I/O	I/O	I/O	VCC
78	GND	GND	GND	VCC
79	VCC	VCC	VCC	VCC
80	NC	VCC	VCC	GND
81	I/O	I/O	I/O	TCK, I/O
83	I/O	I/O	I/O	GND
85	I/O	I/O (WD)	I/O (WD)	I/O
86	I/O	I/O (WD)	I/O (WD)	I/O
89	NC	I/O	I/O	I/O
90	NC	I/O	I/O	I/O
91	I/O	I/O	QCLKB, I/O	I/O
93	I/O	I/O (WD)	I/O (WD)	I/O
94	I/O	I/O (WD)	I/O (WD)	I/O
95	NC	I/O	I/O	I/O
96	NC	I/O	I/O	I/O
97	NC	I/O	I/O	I/O
98	VCC	VCC	VCC	I/O
100	I/O	I/O (WD)	I/O (WD)	I/O
101	I/O	I/O (WD)	I/O (WD)	I/O
103	I/O	TDO, I/O	TDO, I/O	VCC
104	I/O	I/O	I/O	GND
105	GND	GND	GND	I/O
106	NC	VCC	VCC	TDO, I/O
107	I/O	I/O	I/O	I/O (WD)
108	I/O	I/O	I/O	I/O (WD)
110	I/O	I/O	I/O	VCC
112	NC	I/O	I/O	I/O
113	NC	I/O	I/O	I/O
114	NC	I/O	I/O	I/O (WD)
115	NC	I/O	I/O	I/O (WD)
117	I/O	I/O	I/O	QCLKB, I/O
121	I/O	I/O	I/O	I/O (WD)
122	I/O	I/O	I/O	I/O (WD)
126	GND	GND	GND	I/O
128	I/O	TCK, I/O	TCK, I/O	I/O
129	GND	GND	GND	VCC
130	VCC	VCC	VCC	GND
131	GND	GND	GND	I/O
132	VCC	VCC	VCC	I/O
133	VCC	VCC	VCC	I/O
136	VCC	VCC	VCC	I/O
137	I/O	I/O	I/O	I/O (WD)
138	I/O	I/O	I/O	I/O (WD)
141	NC	I/O	I/O	I/O (WD)
142	I/O	I/O	I/O	I/O (WD)
144	I/O	I/O	I/O	QCLKA, I/O
146	NC	I/O	I/O	I/O
147	NC	I/O	I/O	I/O
148	NC	I/O	I/O	I/O
149	NC	I/O	I/O	VCC
150	GND	GND	GND	I/O
151	I/O	I/O	I/O	I/O (WD)
152	I/O	I/O	I/O	I/O (WD)
154	I/O	I/O	I/O	TDI, I/O
155	I/O	I/O	I/O	TMS, I/O
156	I/O	I/O	I/O	GND
157	GND	GND	GND	VCC
159	SDI,I/O	SDI,I/O	SDI,I/O	I/O
161	I/O	I/O (WD)	I/O (WD)	I/O
162	I/O	I/O (WD)	I/O (WD)	I/O
164	VCC	VCC	VCC	I/O
165	NC	I/O	I/O	I/O
166	NC	I/O	I/O	I/O
168	I/O	I/O (WD)	I/O (WD)	I/O
169	I/O	I/O (WD)	I/O (WD)	I/O
171	NC	I/O	QCLKD, I/O	I/O
176	I/O	I/O (WD)	I/O (WD)	I/O
177	I/O	I/O (WD)	I/O (WD)	I/O
178	PRA,I/O	PRA,I/O	PRA,I/O	VCC
180	CLKA,I/O	CLKA,I/O	CLKA,I/O	I/O
181	NC	I/O	I/O	VCC
182	NC	VCC	VCC	VCC
183	VCC	VCC	VCC	I/O
184	GND	GND	GND	I/O
186	CLKB,I/O	CLKB,I/O	CLKB,I/O	I/O
187	I/O	I/O	I/O	GND
188	PRB,I/O	PRB,I/O	PRB,I/O	I/O
190	I/O	I/O (WD)	I/O (WD)	I/O
191	I/O	I/O (WD)	I/O (WD)	I/O
193	NC	I/O	I/O	I/O
194	NC	I/O (WD)	I/O (WD)	I/O
195	NC	I/O (WD)	I/O (WD)	I/O
196	I/O	I/O	QCLKC, I/O	I/O
197	NC	I/O	I/O	I/O
201	NC	I/O	I/O	I/O
202	VCC	VCC	VCC	I/O
203	I/O	I/O (WD)	I/O (WD)	I/O
204	I/O	I/O (WD)	I/O (WD)	I/O
206	I/O	I/O	I/O	MODE
207	DCLK,I/O	DCLK,I/O	DCLK,I/O	VCC
208	I/O	I/O	I/O	GND

Package Pin Assignments (continued)

208-Pin PQFP Package, 208-pin RQFP Package (Top View)



Notes:

1. *I/O (WD) : Denotes I/O pin with an associated Wide Decode Module*
2. *Wide Decode I/O (WD) can also be general purpose user I/O*
3. *NC : Denotes No Connection*
4. *All unlisted pin numbers are user I/O's*
5. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*
6. *RQFP has an exposed circular metal heatsink on the top surface.*

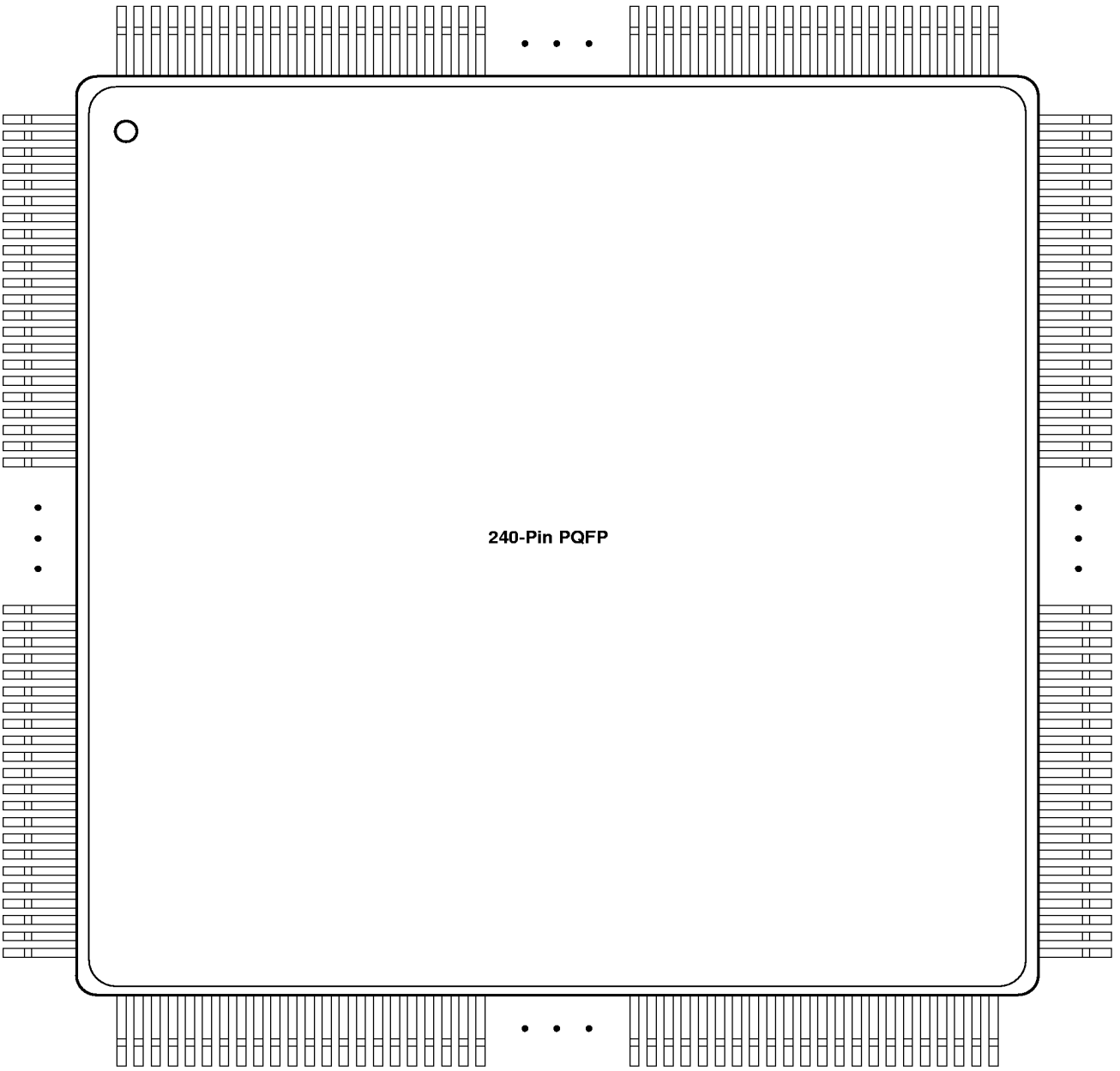
208-Pin PQFP Package, 208-pin RQFP Package

Pin Number	A32100DX-PQ208 Function	A32300DX-RQ208 Function
1	GND	
2	VCC	DCLK, I/O
3	MODE (GND)	
5		I/O (WD)
6		I/O (WD)
7		VCC
9		
10		
11		
13	I/O	QCLKC, I/O
15		I/O (WD)
16		I/O (WD)
17	VCC	
19		I/O (WD)
20		I/O (WD)
22	GND	PRB, I/O
24		CLKB, I/O
26		GND
27	GND	VCC
28	VCC	
29	VSV (VCC)	CLKA, I/O
30		PRA, I/O
32	VCC	I/O (WD)
33		I/O (WD)
38		QCLKD, I/O
40		I/O (WD)
41		I/O (WD)
42		
43		
45		VCC
47		I/O (WD)
48		I/O (WD)
50		SDI, I/O
51		
52	GND	GND
53	GND	
54	TMS, I/O	
55	TDI, I/O	
57		
58	I/O (WD)	
59	I/O (WD)	GND
60	VCC	
61		
62		
65	QCLKA, I/O	
66		
67		
68		
70	I/O (WD)	
71	I/O (WD)	
74		VCC
77		VSV (VCC)
78	GND	VCC
79	VCC	VPP (VCC)
80	VCC	VKS (GND)
81		TCK, I/O
83		GND
85	I/O (WD)	
86	I/O (WD)	
89		
90		
91	QCLKB, I/O	
93	I/O (WD)	
94	I/O (WD)	
95		
96		
97		
98	VCC	
100	I/O (WD)	
101	I/O (WD)	
103	SDO, I/O	VCC

Pin Number	A32100DX-PQ208 Function	A32300DX-RQ208 Function
104		GND
105	GND	
106	VCC	SDO/TDO, I/O
107		I/O (WD)
108		I/O (WD)
110		VCC
112		
113		
114		I/O (WD)
115		I/O (WD)
117		QCLKB, I/O
121		I/O (WD)
122		I/O (WD)
126	GND	I/O (WD)
127		I/O (WD)
128	TCK, I/O	
129	VKS (GND)	VCC
130	VPP (VCC)	GND
131	GND	
132	VCC	
133	VSV (VCC)	
136	VCC	
137		I/O (WD)
138		I/O (WD)
141		I/O (WD)
142		I/O (WD)
144		QCLKA, I/O
146		
147		
148		
149		VCC
150	GND	
151		I/O (WD)
152		I/O (WD)
154		TDI, I/O
155		TMS, I/O
156		GND
157	GND	VCC
159	SDI, I/O	
161	I/O (WD)	
162	I/O (WD)	
164	VCC	
165		
166		
168	I/O (WD)	
169	I/O (WD)	
171	QCLKD, I/O	
176	I/O (WD)	
177	I/O (WD)	
178	PRA, I/O	VCC
180	CLKA, I/O	
181		VSV (VCC)
182	VCC	VCC
183	VCC	
184	GND	
186	CLKB	
187		GND
188	PRB, I/O	
190	I/O (WD)	
191	I/O (WD)	
193		
194		
196	QCLKC, I/O	
197		
201		
202	VCC	
203	I/O (WD)	
204	I/O (WD)	
206		MODE (GND)
207	DCLK, I/O	VCC
208		GND

Package Pin Assignments (continued)

240-Pin PQFP Package (Top View)



Notes:

1. *I/O (WD) : Denotes I/O pin with an associated Wide Decode Module*
2. *Wide Decode I/O (WD) can also be general purpose user I/O*
3. *NC : Denotes No Connection*
4. *All unlisted pin numbers are user I/O's*
5. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*
6. *RQFP has an exposed circular metal heatsink on the top surface.*

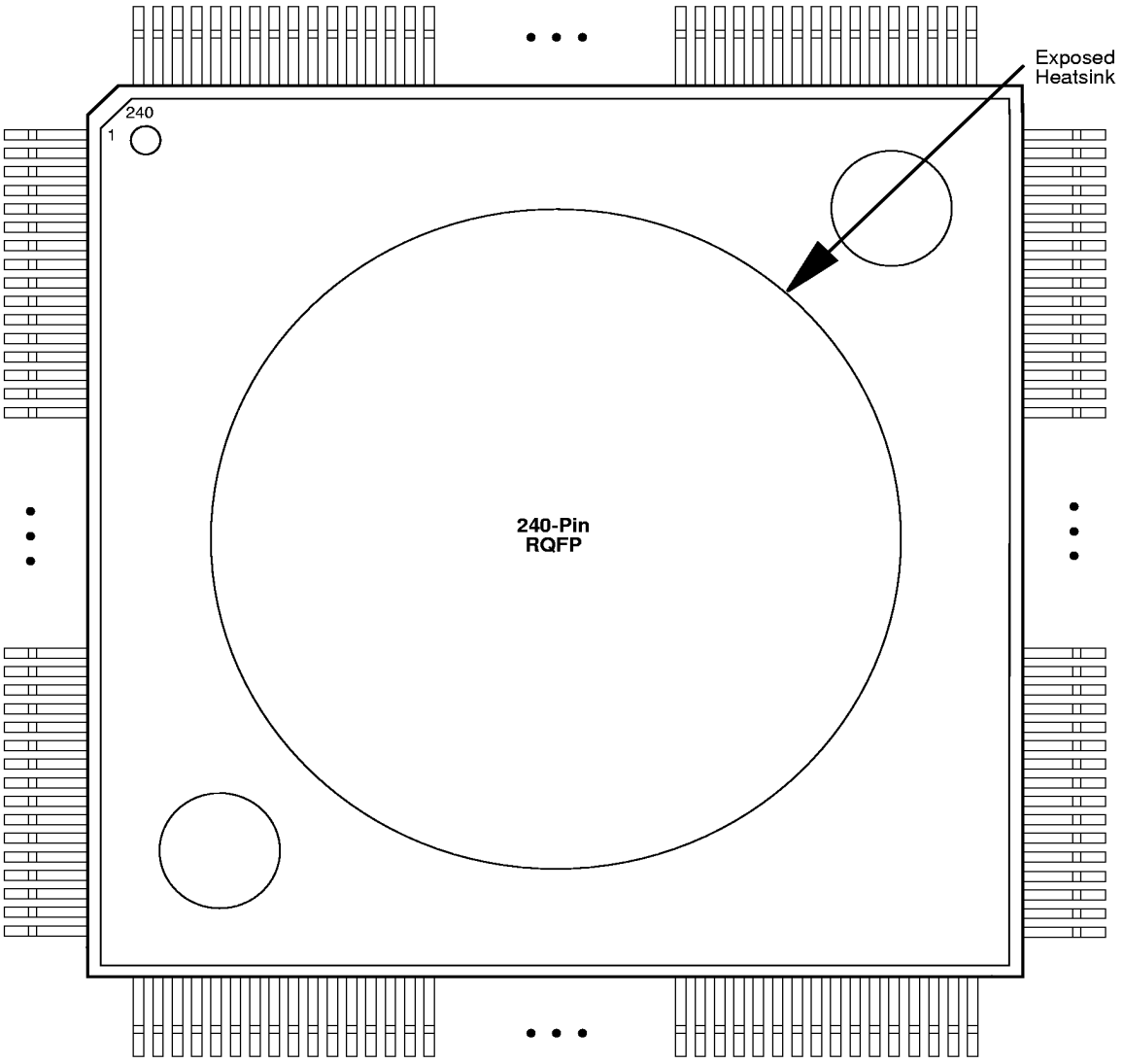
240-Pin PQFP Package

Pin Number	A32300DX Function
2	DCLK
6	I/O (WD)
7	I/O (WD)
8	VCC
15	QCLKC
17	I/O (WD)
18	I/O (WD)
21	I/O (WD)
22	I/O (WD)
24	PROBB
26	CLKB
28	GND
29	VCC
30	VCC
32	CLKA
33	I/O (WD)
34	PROBA
37	I/O (WD)
38	I/O (WD)
45	QCLKD
47	I/O (WD)
48	I/O (WD)
52	VCC
54	I/O (WD)
55	I/O (WD)
57	SDI
59	VCC
60	GND
61	GND
71	VCC
85	VCC
88	VSV (VCC)
89	VCC
90	VPP (VCC)
91	VKS (GND)
92	TCK
94	GND
108	VCC
118	VCC
119	GND

Pin Number	A32300DX Function
120	GND
121	GND
123	SDO/TDO
125	I/O (WD)
126	I/O (WD)
128	VCC
132	I/O (WD)
133	I/O (WD)
135	QCLKB
142	I/O (WD)
143	I/O (WD)
147	I/O (WD)
148	I/O (WD)
150	VCC
151	VCC
152	GND
159	I/O (WD)
160	I/O (WD)
163	I/O (WD)
164	I/O (WD)
166	QCLKA
172	VCC
174	I/O (WD)
175	I/O (WD)
178	BINOUT/TMS
179	BININ/TMS
180	GND
181	VCC
182	GND
192	VCC
206	VCC
209	VSV (VCC)
210	VCC
219	VCC
227	VCC
237	GND
238	MODE (GND)
239	VCCA
240	GND

Package Pin Assignments (continued)

240-Pin RQFP Package (Top View)



Notes:

1. *I/O (WD) : Denotes I/O pin with an associated Wide Decode Module*
2. *Wide Decode I/O (WD) can also be general purpose user I/O*
3. *NC : Denotes No Connection*
4. *All unlisted pin numbers are user I/O's*
5. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*
6. *RQFP has an exposed circular metal heatsink on the top surface.*

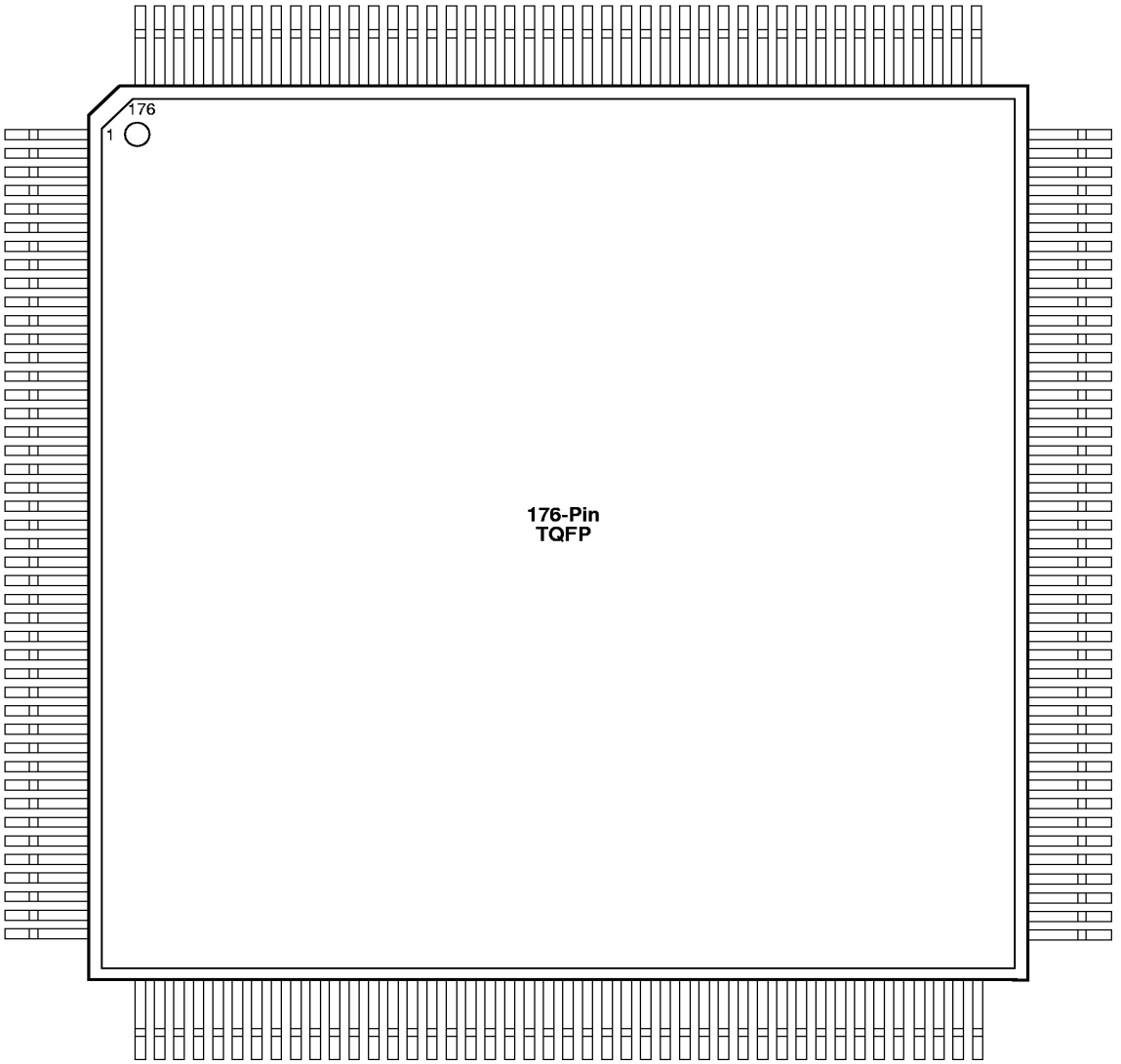
240-Pin RQFP Package

Pin Number	A32200DX Function
2	DCLK, I/O
6	I/O (WD)
7	I/O (WD)
8	VCC
15	QCLKC, I/O
17	I/O (WD)
18	I/O (WD)
21	I/O (WD)
22	I/O (WD)
24	PRB, I/O
26	CLKB, I/O
28	GND
29	VCC
30	VCC
32	CLKA, I/O
34	PRA, I/O
37	I/O (WD)
38	I/O (WD)
45	QCLKD, I/O
47	I/O (WD)
48	I/O (WD)
52	VCC
54	I/O (WD)
55	I/O (WD)
57	SDI, I/O
59	VCC
60	GND
61	GND
71	VCC
85	VCC
88	VCC
89	VCC
90	VCC
91	GND
92	TCK, I/O
94	GND
108	VCC
118	VCC

Pin Number	A32200DX Function
119	GND
120	GND
121	GND
123	TDO, I/O
125	I/O (WD)
126	I/O (WD)
128	VCC
132	I/O (WD)
133	I/O (WD)
135	QCLKB, I/O
142	I/O (WD)
143	I/O (WD)
150	VCC
151	VCC
152	GND
159	I/O (WD)
160	I/O (WD)
163	I/O (WD)
164	I/O (WD)
166	QCLKA, I/O
172	VCC
174	I/O (WD)
175	I/O (WD)
178	TDI, I/O
179	TMS, I/O
180	GND
181	VCC
182	GND
192	VCC
206	VCC
209	VCC
210	VCC
219	VCC
227	VCC
237	GND
238	MODE (GND)
239	VCC
240	GND

Package Pin Assignments (continued)

176-Pin TQFP Package (Top View)



Notes:

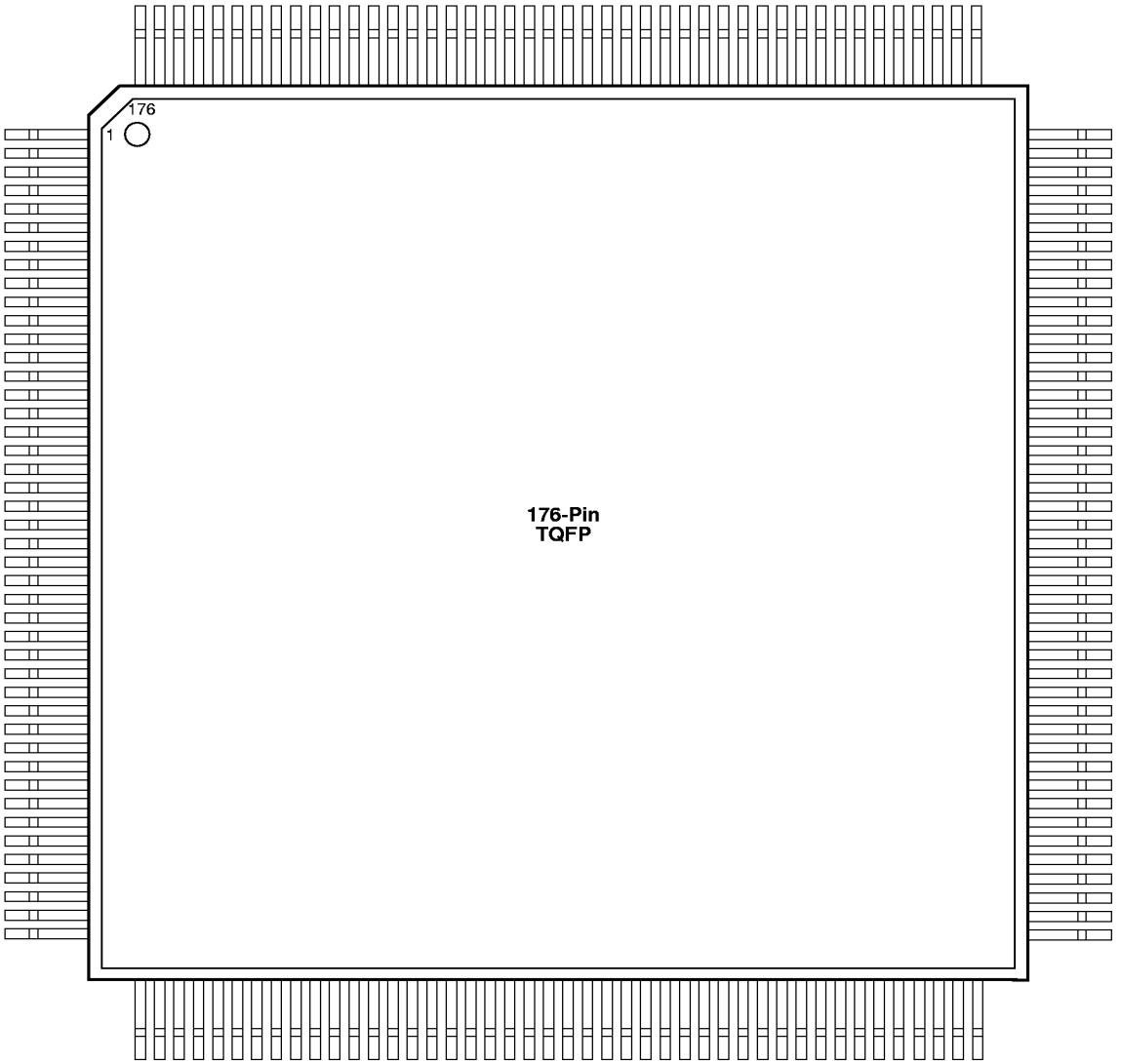
1. *I/O (WD) : Denotes I/O pin with an associated Wide Decode Module*
2. *Wide Decode I/O (WD) can also be general purpose user I/O*
3. *NC : Denotes No Connection*
4. *All unlisted pin numbers are user I/O's*
5. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

176-pin TQFP Package

Pin Number	A1240XL Function	A3265DX Function	A1280XL Function	A32140DX Function
1	GND	GND	GND	GND
2	MODE	MODE	MODE	MODE
8	NC	NC	NC	I/O
10	NC	NC	I/O	I/O
11	NC	NC	I/O	I/O
13	NC	VCC	VCC	VCC
18	GND	GND	GND	GND
19	NC	I/O	I/O	I/O
20	NC	I/O	I/O	I/O
22	NC	I/O	I/O	I/O
23	GND	GND	GND	GND
24	NC	VCC	VCC	VCC
25	VCC	VCC	VCC	VCC
26	NC	I/O	I/O	I/O
27	NC	I/O	I/O	I/O
28	VCC	VCC	VCC	VCC
29	NC	NC	I/O	I/O
33	NC	NC	NC	I/O
37	NC	NC	I/O	I/O
38	NC	NC	NC	I/O
45	GND	GND	GND	GND
46	I/O	I/O	I/O	TMS, I/O
47	I/O	I/O	I/O	TDI, I/O
48	I/O	NC	I/O	I/O
49	I/O	I/O	I/O	I/O (WD)
50	I/O	I/O	I/O	I/O (WD)
52	NC	VCC	VCC	VCC
54	NC	I/O (WD)	I/O	I/O
55	NC	I/O (WD)	I/O	I/O (WD)
56	I/O	I/O	I/O	I/O (WD)
57	NC	NC	NC	I/O
59	I/O	I/O (WD)	I/O	I/O (WD)
60	I/O	I/O (WD)	I/O	I/O (WD)
61	NC	I/O	I/O	I/O
64	NC	I/O	I/O	I/O
66	NC	I/O	I/O	I/O
67	GND	GND	GND	GND
68	VCC	VCC	VCC	VCC
69	I/O	I/O (WD)	I/O	I/O (WD)
70	I/O	I/O (WD)	I/O	I/O (WD)
73	I/O	I/O (WD)	I/O	I/O
74	NC	NC	I/O	I/O
75	I/O	I/O (WD)	I/O	I/O
77	NC	NC	NC	I/O (WD)
78	NC	NC	I/O	I/O (WD)
80	NC	I/O (WD)	I/O	I/O
81	I/O	I/O (WD)	I/O	I/O
82	NC	VCC	VCC	VCC
84	I/O	I/O	I/O	I/O (WD)
85	I/O	I/O	I/O	I/O (WD)
86	NC	NC	I/O	I/O
87	I/O	I/O	I/O	TDO, I/O
89	GND	GND	GND	GND
96	NC	NC	I/O	I/O
97	NC	I/O	I/O	I/O
101	NC	NC	NC	I/O
103	NC	I/O	I/O	I/O
106	GND	GND	GND	GND
107	NC	I/O	I/O	I/O
108	NC	I/O	I/O	TCK, I/O
109	GND	GND	GND	GND
110	VCC	VCC	VCC	VCC
111	GND	GND	GND	GND
112	VCC	VCC	VCC	VCC
113	VCC	VCC	VCC	VCC
114	NC	I/O	I/O	I/O
115	NC	I/O	I/O	I/O
116	NC	VCC	VCC	VCC
117	I/O	NC	I/O	I/O
121	NC	NC	NC	I/O
124	NC	NC	I/O	I/O
125	NC	NC	I/O	I/O
126	NC	NC	NC	I/O
133	GND	GND	GND	GND
135	SDI,I/O	SDI,I/O	SDI,I/O	SDI,I/O
136	NC	NC	I/O	I/O
137	I/O	I/O	I/O	I/O (WD)
138	I/O	I/O	I/O	I/O (WD)
139	I/O	I/O (WD)	I/O	I/O
140	NC	VCC	VCC	VCC
141	I/O	I/O (WD)	I/O	I/O
143	NC	I/O	I/O	I/O
144	NC	I/O (WD)	I/O	I/O (WD)
145	NC	NC	NC	I/O (WD)
146	I/O	I/O (WD)	I/O	I/O
147	NC	I/O	I/O	I/O
149	I/O	I/O (WD)	I/O	I/O
150	I/O	I/O (WD)	I/O	I/O (WD)
151	NC	I/O	I/O	I/O (WD)
152	PRA,I/O	PRA,I/O	PRA,I/O	PRA,I/O
154	CLKA,I/O	CLKA,I/O	CLKA,I/O	CLKA,I/O
155	VCC	VCC	VCC	VCC
156	GND	GND	GND	GND
158	CLKB,I/O	CLKB,I/O	CLKB,I/O	CLKB,I/O
160	PRB,I/O	PRB,I/O	PRB,I/O	PRB,I/O
161	NC	I/O	I/O	I/O (WD)
162	I/O	I/O (WD)	I/O	I/O (WD)
163	I/O	I/O (WD)	I/O	I/O
165	NC	NC	NC	I/O (WD)
166	NC	I/O	I/O	I/O (WD)
168	NC	I/O	I/O	I/O
169	I/O	I/O (WD)	I/O	I/O
170	NC	VCC	VCC	VCC
171	I/O	I/O (WD)	I/O	I/O (WD)
172	I/O	I/O	I/O	I/O (WD)
173	NC	NC	I/O	I/O
175	DCLK,I/O	DCLK,I/O	DCLK,I/O	DCLK,I/O

Package Pin Assignments (continued)

176-Pin TQFP Package (Top View)



Notes:

1. *I/O (WD) : Denotes I/O pin with an associated Wide Decode Module*
2. *Wide Decode I/O (WD) can also be general purpose user I/O*
3. *NC : Denotes No Connection*
4. *All unlisted pin numbers are user I/O's*
5. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.*

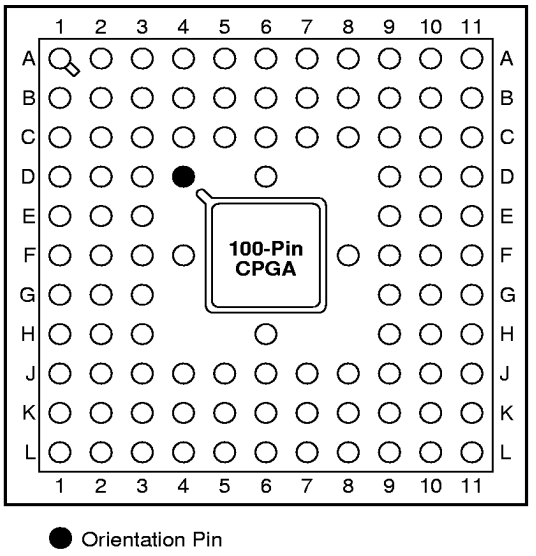
176-pin TQFP Package

Pin Number	A32100DX Function
2	MODE (GND)
13	VCC
18	GND
23	GND
24	VCC
25	VSV (VCC)
28	VCC
45	GND
46	TMS, I/O
47	TDI, I/O
50	I/O (WD)
51	I/O (WD)
52	VCC
57	QCLKA, I/O
59	I/O (WD)
60	I/O (WD)
67	GND
68	VCC
72	I/O (WD)
73	I/O (WD)
76	QCLKB, I/O
78	I/O (WD)
79	I/O (WD)
82	VCC
84	I/O (WD)
85	I/O (WD)
87	SDO, I/O
89	GND
106	GND

Pin Number	A32100DX Function
108	TCK, I/O
109	VKS (GND)
110	VPP (VCC)
111	GND
112	VCC
113	VSV (VCC)
116	VCC
133	GND
135	SDI, I/O
137	I/O (WD)
138	I/O (WD)
140	VCC
142	I/O (WD)
143	I/O (WD)
146	QCLKD, I/O
150	I/O (WD)
151	I/O (WD)
152	PRA, I/O
154	CLKA, I/O
155	VCC
158	CLKB, I/O
160	PRB, I/O
161	I/O (WD)
162	I/O (WD)
164	QLCKC, I/O
170	VCC
171	I/O (WD)
172	I/O (WD)
175	DCLK, I/O

Package Pin Assignments (continued)

100-Pin CPGA (Top View)



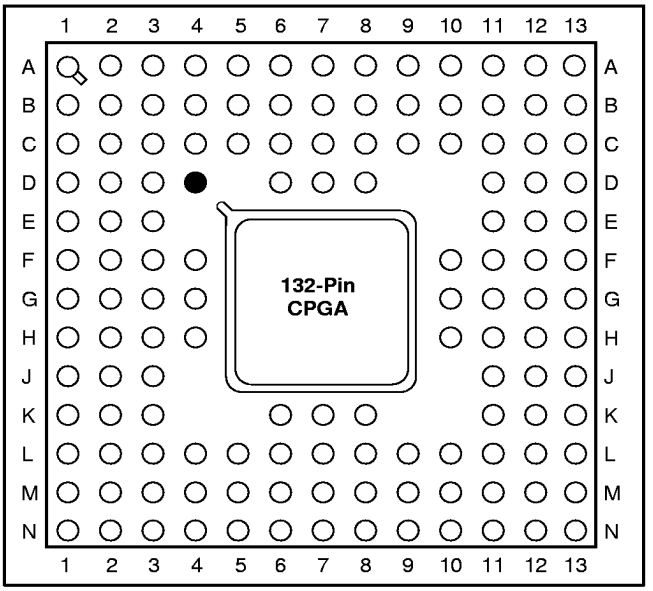
Signal	Pad Number	Location
PRA or I/O	85	A7
PRB or I/O	92	A4
MODE	2	C2
SDI or I/O	77	C8
DCLK or I/O	100	C3
CLKA or I/O	87	C6
CLKB or I/O	90	D6
GND	7, 20, 32, 44, 55, 70, 82, 94	E3, G3, J5, J7, G9, F11, D10, C7, C5
V_{CC}	15, 38, 64, 88	F3, G1, K6, F9, F10, E11, B6

Notes:

1. *Unused I/O pins are designated as outputs by ALS and are driven low.*
2. *All unassigned pins are available for use as I/Os.*
3. *MODE = GND, except during device programming or debugging.*

Package Pin Assignments (continued)

132-Pin CPGA (Top View)



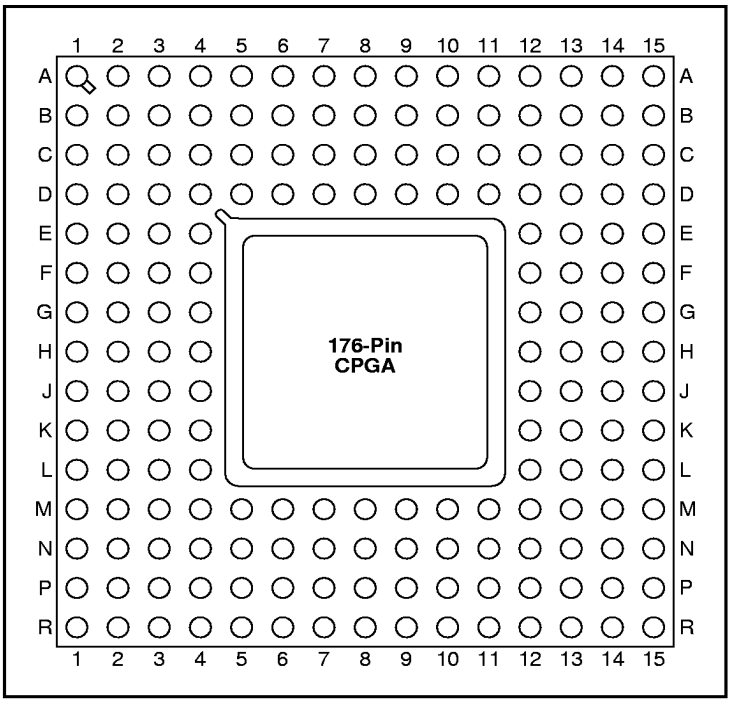
Signal	Pad Number	Location
PRA or I/O	113	B8
PRB or I/O	121	C6
MODE	2	A1
SDI or I/O	101	B12
DCLK or I/O	132	C3
CLKA or I/O	115	B7
CLKB or I/O	119	B6
GND	9, 10, 26, 27, 41, 58, 59, 73, 74, 92, 93, 107, 108, 125, 126	E3, F4, J2, J3, L5, L9, M9, K12, J11, H13, E12, E11, C9, B9, B5, C5
V_{CC}	18, 19, 49, 50, 83, 84, 116, 117	G3, G2, G4, L7, K7, G10, G11, G12, G13, D7, C7

Notes:

1. *Unused I/O pins are designated as outputs by ALS and are driven low.*
2. *All unassigned pins are available for use as I/Os.*
3. *MODE = GND, except during device programming or debugging.*

Package Pin Assignments (continued)

176-Pin CPGA (Top View)



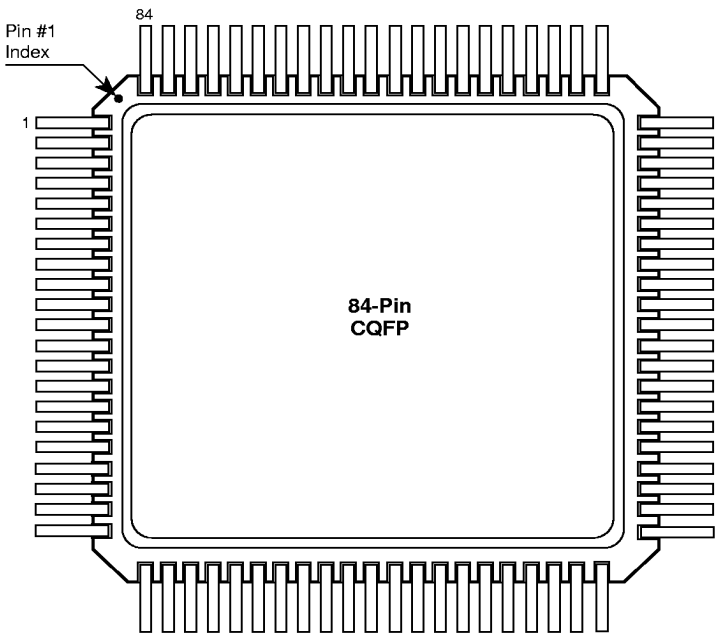
Signal	Pad Number	Location
PRA or I/O	152	C9
PRB or I/O	160	D7
MODE	2	C3
SDI or I/O	135	B14
DCLK or I/O	175	B3
CLKA or I/O	154	A9
CLKB or I/O	158	B8
GND	1, 8, 18, 23, 33, 38, 45, 57, 67, 77, 89 101, 106, 111, 121, 126, 133, 145, 156, 165	D4, E4, G4, H4, K4, L4, M4, M6, M8, M10, M12 K12, J12, J13, H12, F12, E12, D12, D10, C8, D6
V_{CC}	13, 24, 28, 52, 68, 82, 112, 116, 140, 155, 170	F4, H2, H3, J4, M5, N8, M11, J14, H13, H14, G12, D11, D8, D5

Notes:

1. *Unused I/O pins are designated as outputs by ALS and are driven low.*
2. *All unassigned pins are available for use as I/Os.*
3. *MODE = GND, except during device programming or debugging.*

Package Pin Assignments (continued)

84-Pin CQFP



Notes:

1. *Unused I/O pins are designated as outputs by ALS and are driven low.*
2. *All unassigned pins are available for use as I/Os.*
3. *MODE = GND, except during device programming or debugging.*

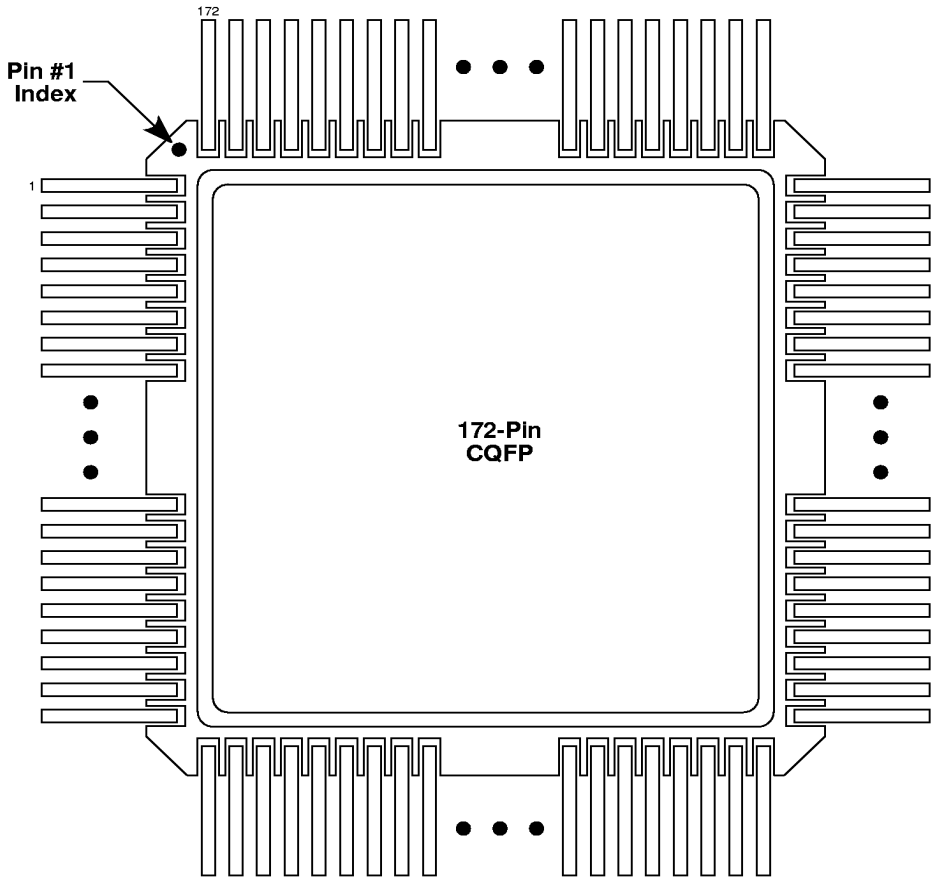
84-pin CQFP Package

Pin Number	A32100DX Function
1	GND
2	MODE (GND)
7	VCC
10	GND
11	VCC
12	VSV (VCC)
17	GND
22	GND
23	TMS, I/O
24	TDI, I/O
25	I/O (WD)
26	I/O (WD)
28	QCLKA, I/O
30	I/O (WD)
32	GND
33	VCC
34	I/O (WD)
35	I/O (WD)
36	QCLKB, I/O
37	I/O (WD)
38	GND
39	I/O (WD)
40	I/O (WD)
41	I/O (WD)
42	SDO, I/O
43	GND
50	GND

Pin Number	A32100DX Function
51	TCK, I/O
52	VKS (GND)
53	VPP (VCC)
55	VSV (VCC)
56	VCC
59	GND
63	GND
64	SDI
65	I/O (WD)
66	I/O (WD)
67	I/O (WD)
68	I/O (WD)
69	QCLKD, I/O
70	I/O (WD)
71	I/O (WD)
72	PRA, I/O
73	CLKA, I/O
74	VCC
76	CLKB, I/O
77	PRB, I/O
78	I/O (WD)
79	I/O (WD)
80	QCLKC, I/O
81	GND
82	I/O (WD)
83	I/O (WD)
84	DCLK, I/O

Package Pin Assignments (continued)

172-Pin CQFP



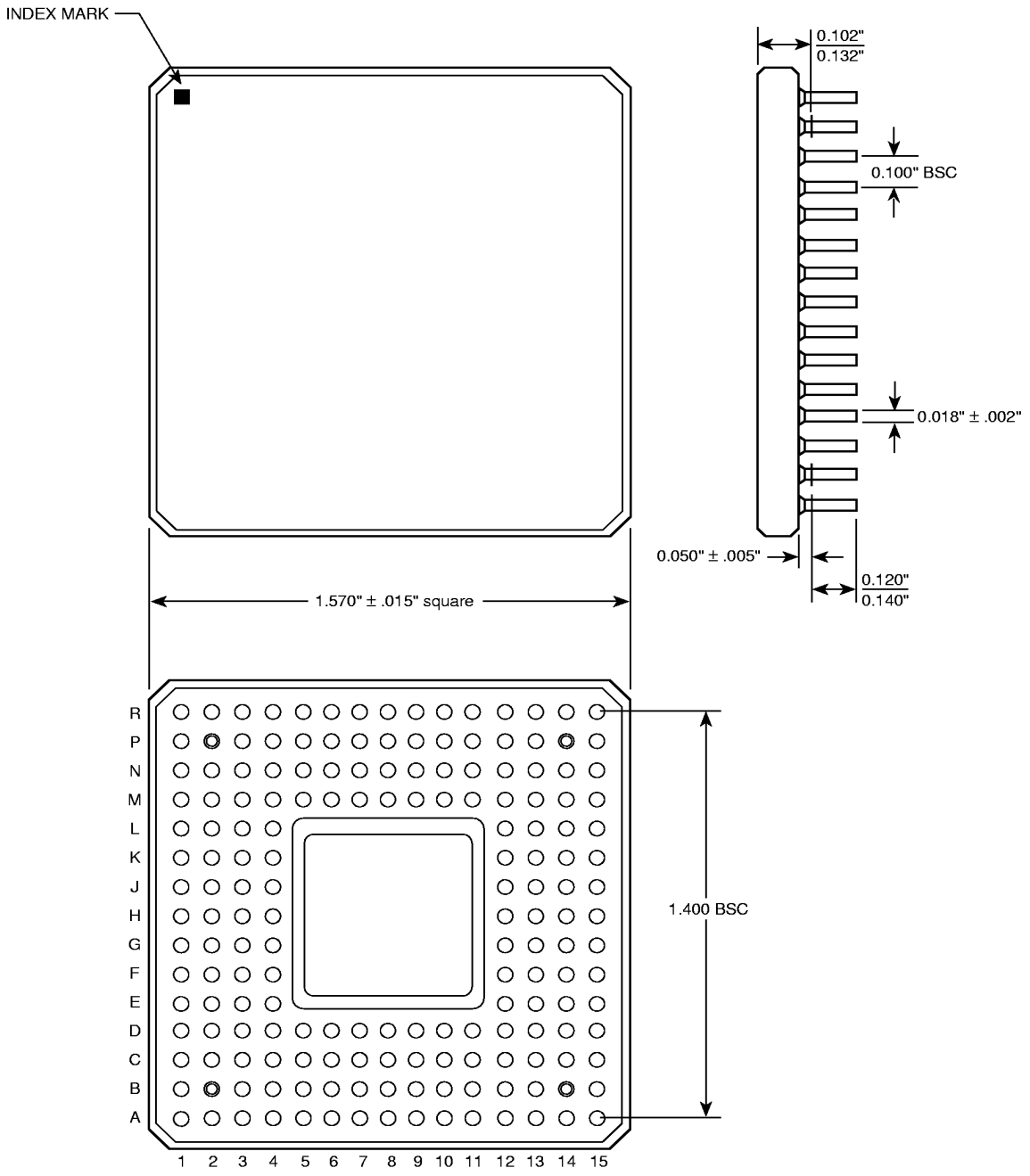
Signal	Pad Number
CLKA or I/O	150
CLKB or I/O	154
DCLK or I/O	171
GND	7, 17, 22, 32, 37, 55, 65, 75, 98, 103, 106, 118, 123, 141, 152, 161
MODE	1
PRA or I/O	148
PRB or I/O	156
SDI or I/O	131
V_{CC}	12, 23, 24, 27, 66, 80, 107, 109, 110, 113, 136, 151, 166

Notes:

1. *Unused I/O pins are designated as outputs by ALS and are driven low.*
2. *All unassigned pins are available for use as I/Os.*
3. *MODE = GND, except during device programming or debugging.*

Package Mechanical Drawings

176-Pin CPGA (Ceramic Pin Grid Array)

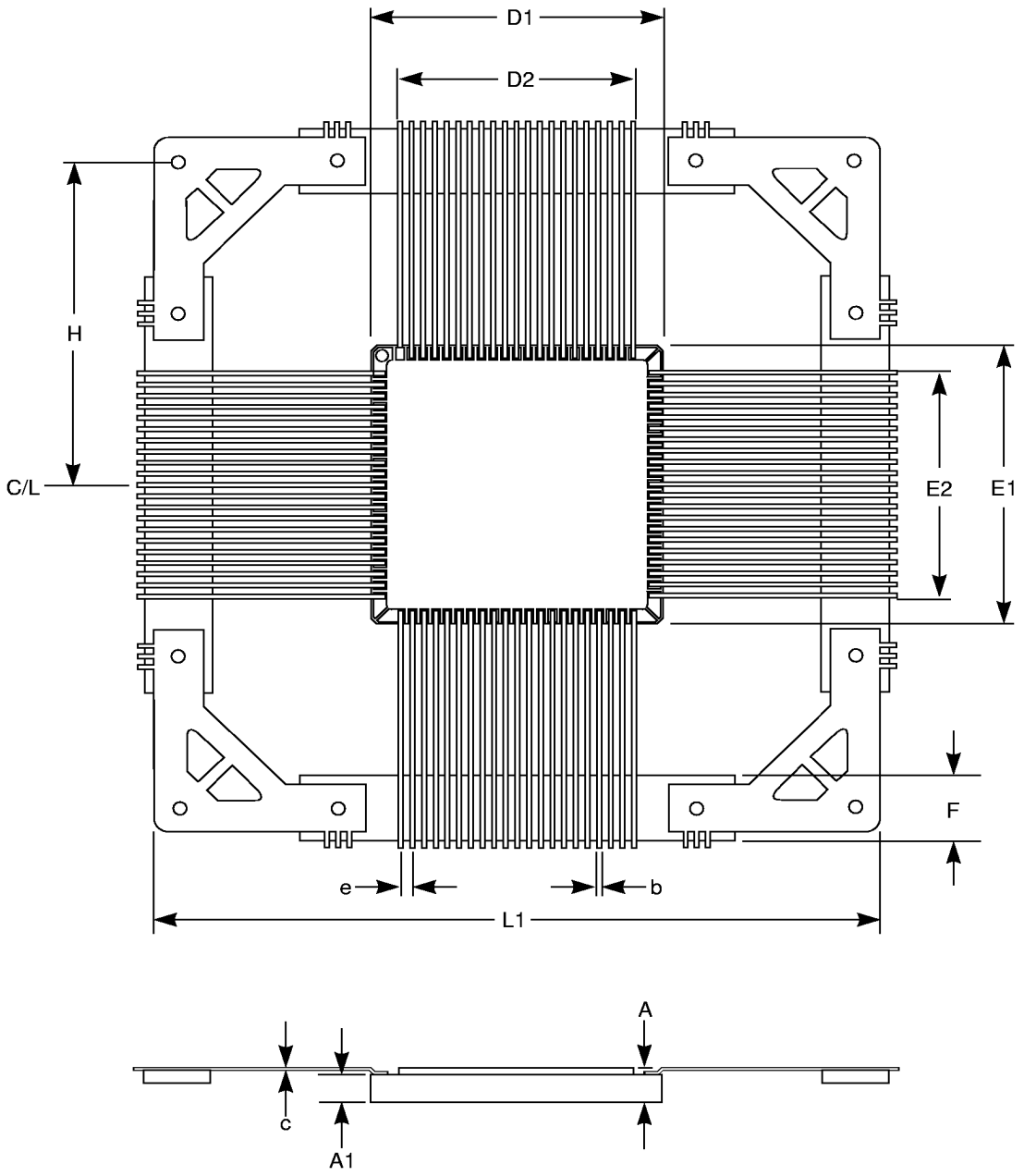


Notes:

1. *All dimensions are in inches unless otherwise stated.*
2. *BSC—Basic Spacing between Centers.*

Package Mechancial Drawings (continued)

Ceramic Quad Flatpack (CQFP)



Cermamic Quad Flatpack (CQFP)

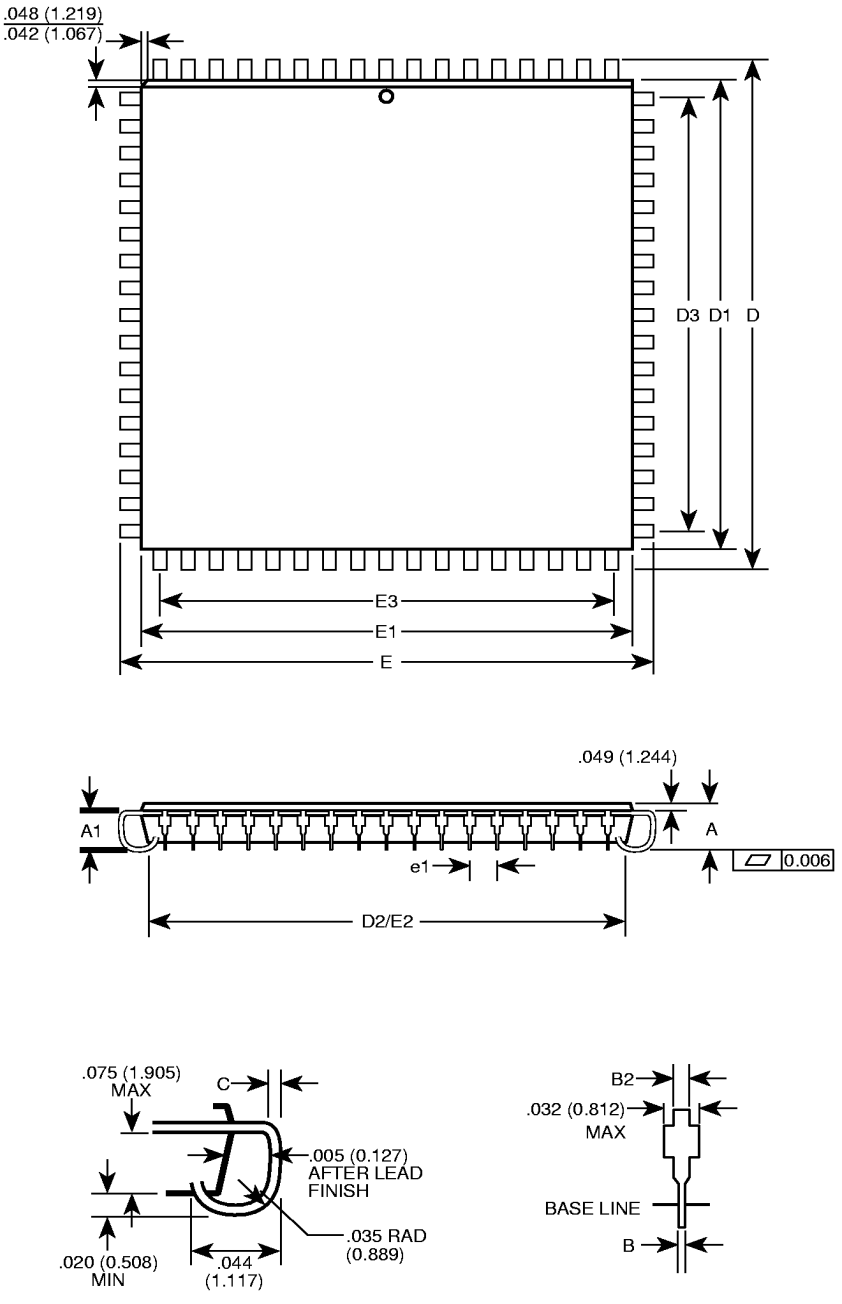
JEDEC	CQ172 MO-113	
Symbol	**Min**	**Max**
A	0.086	0.140
A1	0.078	0.125
b	0.007	0.010
c	0.004	0.008
D1/E1	1.165	1.195
D2/E2	1.050 BSC	
e	.025 BSC	
F	0.175	0.225
H	1.150 BSC	
L1	2.485	2.505

Note:

1. *All dimensions are in inches except CQ256, which is in millimeters.*
2. *BSC—Basic Spacing between Centers.*

Package Mechancial Drawings (continued)

Plastic Leaded Chip Carrier (PLCC)



Plastic Leaded Chip Carrier Packages (PLCC)

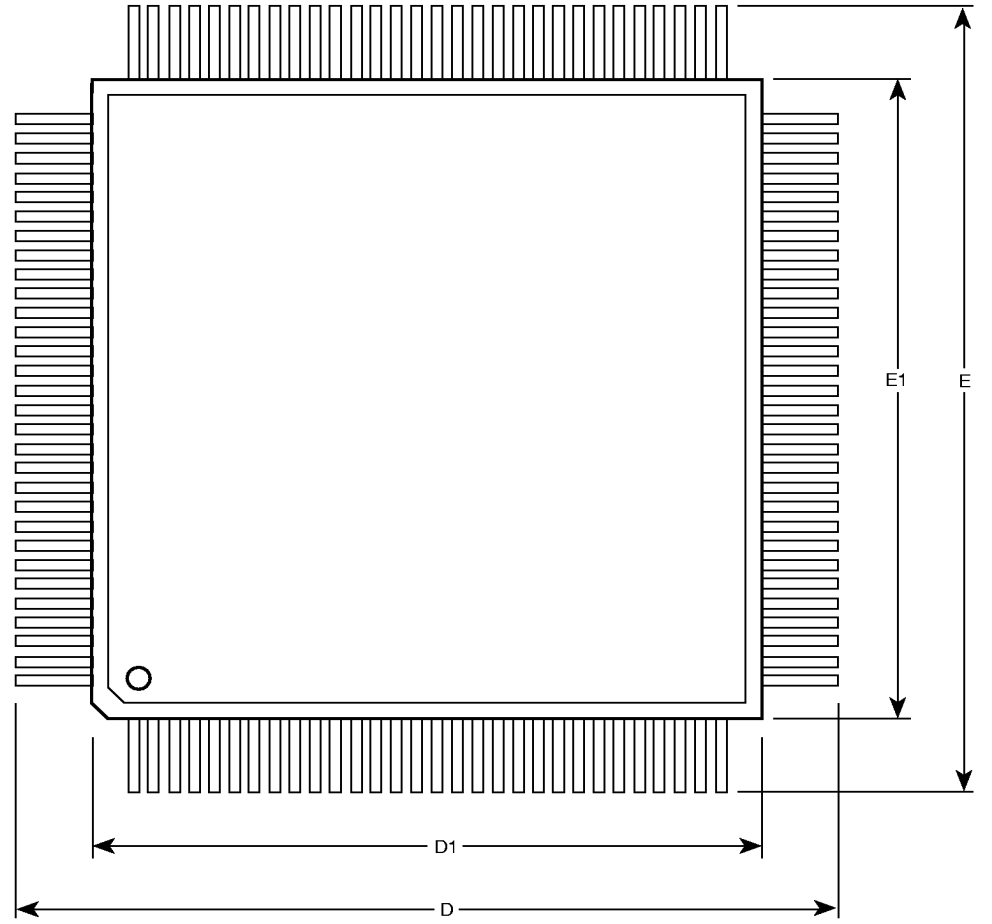
Jedec Equiv	PLCC 84 MS007 AE VAR	
Dimension	**Min**	**Max**
A	0.155	0.175
A1	0.090	0.130
B	0.013	0.027
B2	0.026	0.032
C	0.005	0.011
D/E	1.170	1.210
D1/E1	1.140	1.160
D2/E2	1.090	1.130
D3/E3	1.00 nominal	
e1	0.050 BSC	

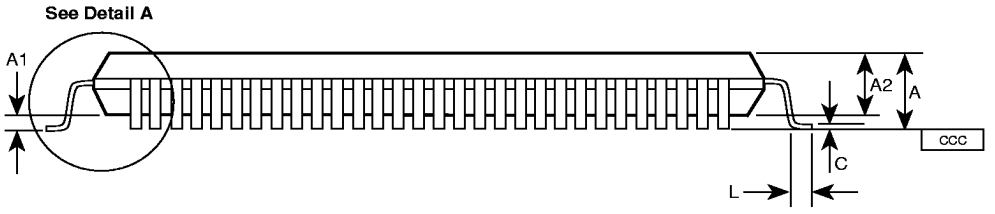
Notes:

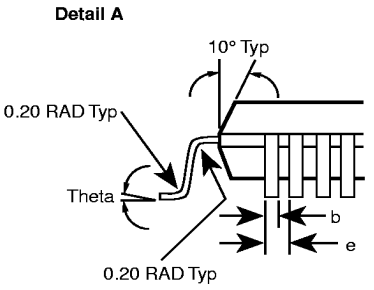
1. *All dimensions are in inches.*
2. *BSC—Basic Spacing between Centers.*

Package Mechancial Drawings (continued)

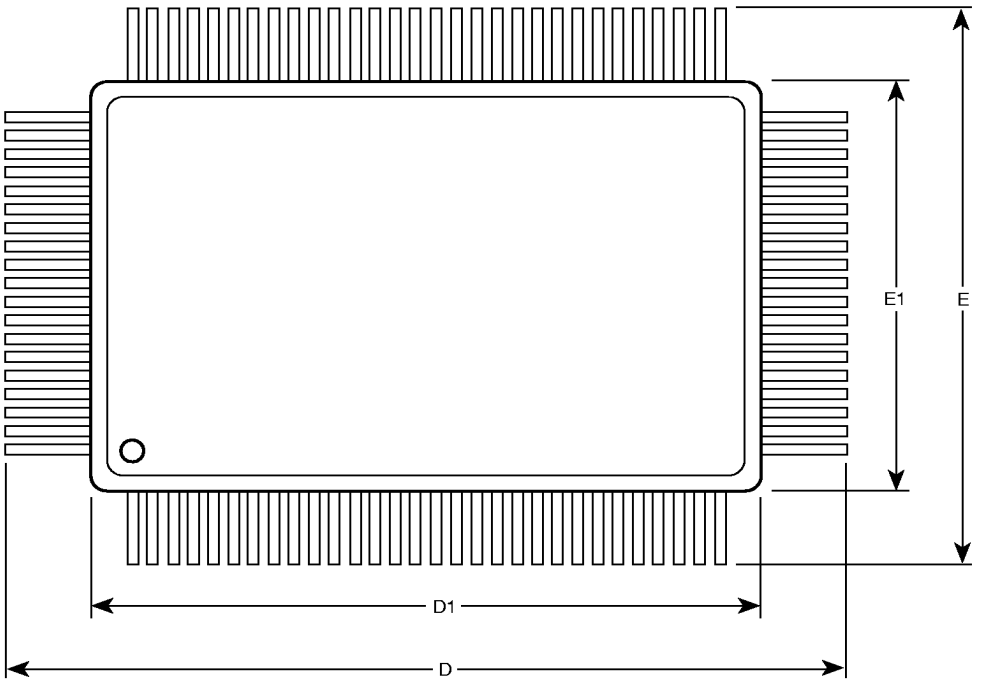
Plastic Quad Flatpack (PQFP, RQFP, TQFP, VQFP)

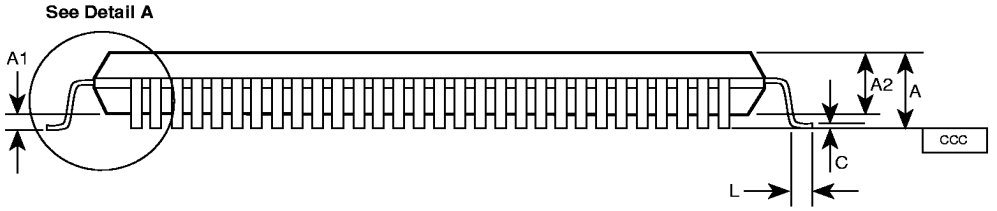




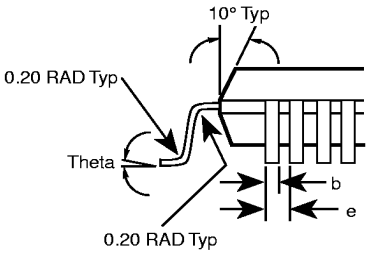


Plastic Quad Flatpack
Rectangular Package (PQ100)





Detail A



Plastic Quad Flat Packages (PQFP)

Jedec Equiv	PQFP 100 MO-108		PQFP 144 MO-108		1200XL, 3200DX PQFP 160 MO-112		PQFP 208 MO-143	
Dimension	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
A		3.40		4.07		4.07		4.10
A1	0.25		0.25		0.25		0.25	
A2	2.55	3.05	3.20	3.60	3.17	3.67	3.20	3.60
b	0.22	0.38	0.22	0.38	0.22	0.38	0.17	0.27
c	0.13	0.23	0.13	0.23	0.13	0.23	0.09	0.20
D	23.20 BSC		31.20 BSC		31.90 BSC		30.60 BSC	
D1	20.00 BSC		28.00 BSC		28.00 BSC		28.00 BSC	
E	17.20 BSC		31.20 BSC		31.90 BSC		30.60 BSC	
E1	14.00 BSC		28.00 BSC		28.00 BSC		28.00 BSC	
e	0.65 BSC		0.65 BSC		0.65 BSC		0.50 BSC	
L	0.73	1.03	0.73	1.03	0.65	0.95	0.50	0.75
ccc		0.10		0.08		0.10		0.08
Theta	0	7 deg	0	7 deg	0	7 deg	0	7 deg

Notes:

1. *All dimensions are in millimeters.*
2. *BSC—Basic Spacing between Centers.*

Plastic Quad Flat Packages (RQFP)

Jedec Equiv	RQFP 208 MO-143		RQFP 240 MO-143	
Dimension	**Min**	**Max**	**Min**	**Max**
A		4.10		4.10
A1	0.25		0.25	
A2	3.20	3.60	3.20	3.60
b	0.17	0.27	0.17	0.27
c	0.09	0.20	0.09	0.20
D/E	30.60 BSC		34.60 BSC	
D1/E1	28.00 BSC		32.00 BSC	
e	0.50 BSC		0.50 BSC	
L	0.50	0.75	0.50	0.75
ccc		0.08		0.08
Theta	0	7 deg	0	7 deg

Notes:

1. *All dimensions are in millimeters.*
2. *BSC—Basic Spacing between Centers.*

Thin Quad Flatpacks (TQFP and VQFP)

Jedec Equiv	TQFP 176 MO-136		VQFP 100 MO-136	
Dimension	**Min**	**Max**	**Min**	**Max**
A		1.60		1.20
A1	0.05	0.15	0.05	0.15
A2	1.35	1.45	0.95	1.05
b	0.17	0.27	0.17	0.27
c	0.09	0.20	0.09	0.20
D/E	26.00 BSC		16.00 BSC	
D1/E1	24.00 BSC		14.00 BSC	
e	0.50 BSC		0.50 BSC	
L	0.45	0.75	0.45	0.75
ccc		0.08		0.08
Theta	0	7 deg	0	7 deg

Notes:

1. *All dimensions are in millimeters.*
2. *BSC—Basic Spacing between Centers.*