ACE ACE25C100 Flash Memory Datasheet

http://www.manuallib.com/ace/ace25c100-flash-memory-datasheet.html

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The ACE25C100 can be programmed 1 to 256 bytes at a time, using the Page Program instruction. It is designed to allow either single Sector/Block at a time or full chip erase operation. The ACE25C100 can be configured to protect part of the memory as the software protected mode. The device can sustain a minimum of 100K program/erase cycles on each sector or block.

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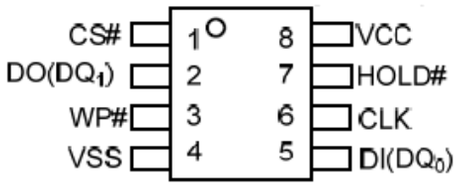
Features

- 1M-BIT of Flash memory
  - 32 uniform sectors with 4K-byte each
  - 2 uniform blocks with 64K-byte each
  - 4 uniform blocks with 32K-byte each
  - 256 bytes per programmable page
- Wide Operation Range
  - 2.7V~3.6V single voltage supply
  - Industrial temperature range
- Serial Interface
  - Standard SPI: CLK, CS#, DI, DO, WP#
  - Dual SPI: CLK, CS#, DQ_0, DQ_1, WP#
  - Continuous READ mode support
- High Performance
  - Max FAST_READ clock frequency: 100MHz
  - Max READ clock frequency: 50MHz
  - Typical page program time: 1.5ms
  - Typical sector erase time: 90ms
  - Typical block erase time: 500ms
  - Typical chip erase time: 1.5s
- Low Power Consumption
  - Typical standby current: 1μA
- Security
  - Software and hardware write protection
  - Lockable 256-Byte OTP security sectors
  - Low Voltage Write Inhibit
  - 64-BIT Unique ID for each device
- High Reliability
  - Endurance: 100,000program/erase cycles
  - Data retention: 20years

Packaging Type

SOP-8



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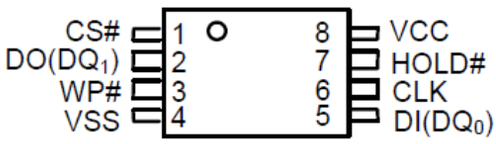
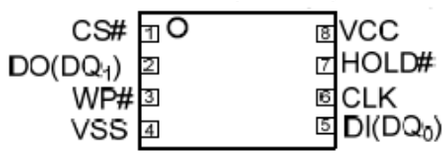


TDFN (2*3mm)



Pin Configurations

Pin No	Pin Number	I/O	Function
1	CS#	I	Chip select input
2	DO(DQ_1)	I/O	Data output (Data input output 1)(1)
3	WP#	I	Write protect input
4	GND		Ground
5	DI(DQ_0)	I/O	Data input (Data input output 0)(1)
6	CLK	I	Serial clock input
7	HOLD#	I	Hold input
8	VCC		Power supply

Note: 1. DQ0 and DQ1 are used for Dual SPI instructions.

Block Diagram

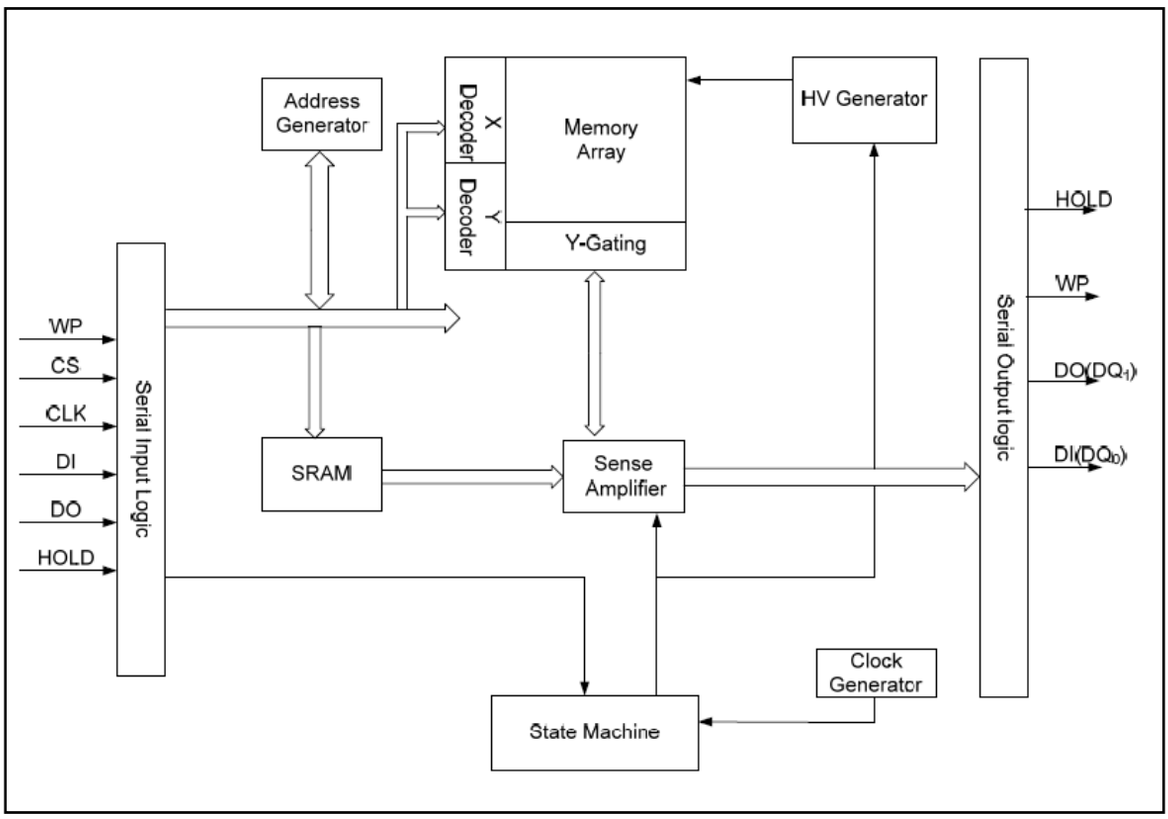


Figure 1 ACE25C100 serial flash memory block diagram

Ordering information

ACE25C100 XX + X H

- Halogen-free
- U : Tube
  T : Tape and Reel
- Pb - free
- FM: SOP-8
  TM: TSSOP-8
  DM : TDFN-8

Pin descriptions

Serial Clock (CLK): The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations.

Serial Data Input, Output and I/Os (DI, DO and DQ_0, DQ_1): The ACE25C100 supports standard SPI and Dual SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK.

Dual SPI instructions use the bidirectional DQ pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK.

Chip Select (CS#): The SPI Chip Select (CS#) pin enables and disables device operation. When CS# is high, the device is deselected and the Serial Data Output (DO, or DQ_0, DQ_1) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When CS# is brought low, the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, CS# must transition from high to low before a new instruction will be accepted. The CS# input must track the VCC supply level at power-up (see “9 Write Protection” and Figure 25). If needed a pull-up resister on CS# can be used to accomplish this.

HOLD (HOLD#): The HOLD# pin allows the device to be paused while it is actively selected. When HOLD# is brought low, while CS# is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don’t care). When HOLD# is brought high, device operation can resume. The HOLD# function can be useful when multiple devices are sharing the same SPI signals. The HOLD# pin is active low.

Write Protect (WP#): The Write Protect (WP#) pin can be used to prevent the Status Registers from being written. Used in conjunction with the Status Register’s Block Protect (BP2, BP1 and BP0) bits and Status Register Protect (SRP) bits, a portion as small as a 4KB sector or the entire memory array can be hardware protected. The WP# pin is active low.

Memory Organization

The ACE25C100 array is organized into 512 programmable pages of 256-bytes each. Up to 256 bytes can be programmed (bits are programmed from 1 to 0) at a time. Pages can be erased in groups of 16 (4KB sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase). The ACE25C100 has 32 erasable sectors 4 erasable 32-k byte blocks and 2 erasable 64-k byte block respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage.

Block (64KB)	Sector (4KB)	Address Range	
1	31	01F000h	01FFFFh
	. .	. .	. .
	16	010000h	010FFFh
0	15	00F000h	00FFFFh
	. .	. .	. .
	3	003000h	003FFFh
	2	002000h	002FFFh
	1	001000h	001FFFh
	0	000000h	000FFFh

Block (32KB)	Sector (4KB)	Address Range	
3	31	01F000h	01FFFFh
	. .	. .	. .
	25	019000h	019FFFh
	24	018000h	018FFFh
2	23	017000h	017FFFh
	. .	. .	. .
	17	011000h	011FFFh
	16	010000h	010FFFh
1	15	00F000h	00FFFFh
	. .	. .	. .
	9	009000h	009FFFh
	8	008000h	008FFFh
0	7	007000h	007FFFh
	. .	. .	. .
	1	001000h	001FFFh
	0	000000h	003FFFh

Table 1 Memory organization

Device Operations

Standard SPI

The ACE25C100 is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (CS#), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of CS#. For Mode 3, the CLK signal is normally high on the falling and rising edges of CS#.

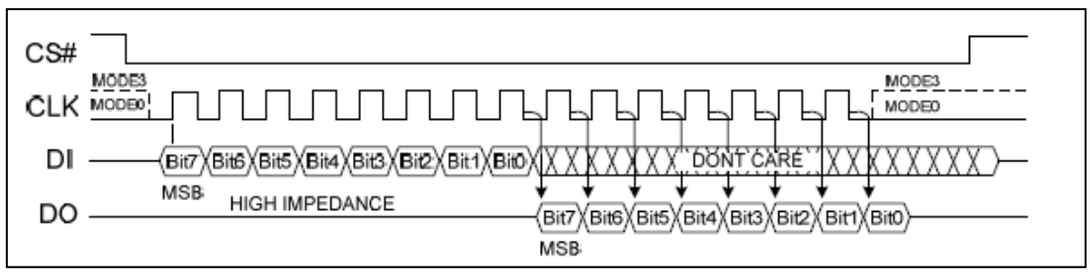


Figure 2 The difference between Mode 0 and Mode 3

Dual SPI

The ACE25C100 supports Dual SPI operation when using instructions such as “Fast Read Dual Output (3Bh)” and “Fast Read Dual I/O (BBh)”. These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual SPI Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed- critical code directly from the SPI bus (XIP). When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: DQ_0 and DQ_1.

Hold

For Standard SPI and Dual SPI operations, the HOLD# signal allows the ACE25C100 operation to be paused while it is actively selected (when CS# is low). The HOLD# function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the HOLD# function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again.

To initiate a HOLD# condition, the device must be selected with CS# low. A HOLD# condition will activate on the falling edge of the HOLD# signal if the CLK signal is already low. If the CLK is not already low the HOLD# condition will activate after the next falling edge of CLK. The HOLD# condition will terminate on the rising edge of the HOLD# signal if the CLK signal is already low. If the CLK is not already low the HOLD# condition will terminate after the next falling edge of CLK. During a HOLD# condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and Serial Clock (CLK) are ignored. The Chip Select (CS#) signal should be kept active (low) for the full duration of the HOLD# operation to avoid resetting the internal logic state of the device.

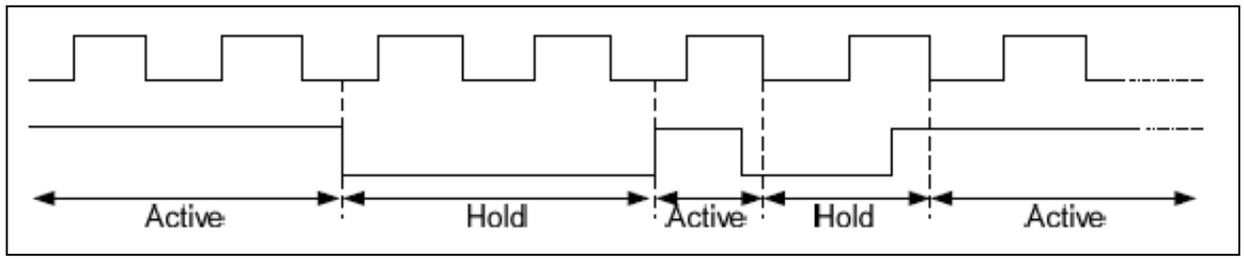


Figure 3 Hold condition waveform

Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the ACE25C100 provides several means to protect the data from inadvertent writes.

Write Protect Features

- Device resets when VCC is below threshold
- Time delay write disable after Power-up
- Write enable/disable instructions and automatic write disable after erase or program
- Software and Hardware (WP# pin) write protection using Status Register
- Write Protection using Power-down instruction
- Lock Down write protection for Status Register until the next power-up
- One Time Program (OTP) write protection for array and Security Sectors using Status Register.

Upon power-up or at power-down, the ACE25C100 will maintain a reset condition while VCC is below the threshold value of VWI, (See “12.3 Power-up Timing” and Figure 25). While reset, all operations are disabled and no instructions are recognized. During power-up and after the VCC voltage exceeds VWI, all program and erase related instructions are further disabled for a time delay of t_{PUW}. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register instructions. Note that the chip select pin (CS#) must track the VCC supply level at power-up until the VCC-min level and t_{VSL} time delay is reached. If needed a pull-up resister on CS# can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register instruction will be accepted. After completing a program, erase or write instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP) and Block Protect (BP2, BP1 and BP0) bits. These settings allow a portion as small as a 4KB sector or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (WP#) pin, changes to the Status Register can be enabled or disabled under hardware control. See Status Register section for further information. Additionally, the Power-down instruction offers an extra level of write protection as all instructions are ignored except for the Release Power-down instruction.

Status Register

The Read Status Register instruction can be used to provide status on the availability of the Flash memory array, if the device is write enabled or disabled, the state of write protection, Security Sector lock status. The Write Status Register instruction can be used to configure the device write protection features and Security Sector OTP lock. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bit (SRP), the Write Enable instruction, and the WP# pin.

Factory default for all Status Register bits are 0.

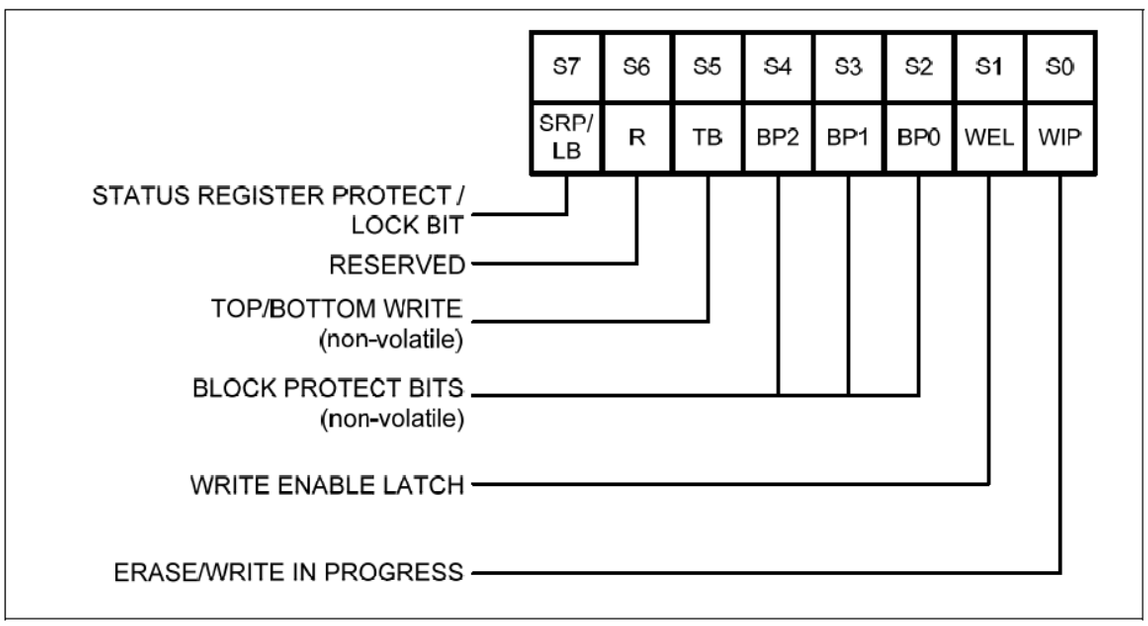


Figure 4 Status Register

WIP Bit

WIP is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register. During this time the device will ignore further instructions except for the Read Status Register and Erase/Program Suspend instruction (see t_W, t_{PP}, t_{SE}, t_{BE}, and t_{CE} in “12.6 AC Electrical Characteristics”). When the program, erase or write status register (or security sector) instruction has completed, the WIP bit will be cleared to a 0 state indicating the device is ready for further instructions.

Write Enable Latch bit (WEL)

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register.

Block Protect Bits (BP2, BP1,BP0)

The Block Protect Bits (BP2, BP1, BP0) are non-volatile read/write bits in the status register (S4, S3, and S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see t_W in "12.6 AC Electrical Characteristics"). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Table 2 Status Register Memory Protection). The factory default setting for the Block Protection Bits is 0, none of the array protected.

Top/Bottom Block Protect (TB)

The non-volatile Top/Bottom bit (TB) controls if the Block Protect Bits (BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in Table 2 Status Register Memory Protection table. The factory default setting is TB=0. The TB bit can be set with the write Status Register Instruction depending on the state of the SRP0, SRP1 and WEL bits.

Status Register Protect bit / Lock_bit (SRP/LB)

The Status Register Protect (SRP) bit is operated in conjunction with the Write Protect (WP#) signal. The Status Register Write Protect (SRP) bit and Write Protect (WP#) signal allow the device to be put in the Hardware Protected mode (when the Status Register Protect (SRP) bit is set to 1, and Write Protect (WP#) is driven Low). In this mode, the non-volatile bits of the Status Register (SRP, BP2, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is no longer accepted for execution.

In OTP mode, this bit is served as Lock_bit (LB), user can read/program/erase security sector as normal sector while LB value is equal 0, after LB is programmed with 1 by WRSR command, the security sector is protected from program and erase operation. The LB can only be programmed once.

Note: In OTP mode, the WRSR command will ignore any input data and program LB to 1, user must clear the protect bits before enter OTP mode and program the OTP code, then execute WRSR command to lock the security sector before leaving OTP mode.

Status Register Memory Protection

Status Register Content				Memory Content		
TB bit	**BP2 bit**	**BP1 bit**	**BP0 bit**	**Address**	**Density**	**Portion**
X	X	0	0	None	None	None
0	X	0	1	010000h~01FFFFh	64KB	Upper 1/2
1	X	0	1	000000h~00FFFFh	64KB	Lower 1/2
X	X	1	X	000000h~01FFFFh	128KB	All

Table 2 Status Register Memory Protection

Instructions

The Standard/Dual SPI instruction set of the ACE25C100 consists of 17 basic instructions that are fully controlled through the SPI bus (see Table 4~Table 5 Instruction Set). Instructions are initiated with the falling edge of Chip Select (CS#). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB) first.

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge CS#. Clock relative timing diagrams for each instruction are included in Figure 5 through Figure 29. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (CS# driven high after a full 8-bits have been clocked) otherwise the instruction will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

Manufacturer and Device Identification

OP Code	MF7-MF0	ID15-ID0	ID7-DO
ABh	x	x	10h
90h	A1h	x	10h
9Fh	A1h	3111h	x

Table 3 Manufacturer and Device Identification

Standard SPI Instructions Set(1)

Instruction Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
Clock number	(0-7)	(8-15)	(16-23)	(24-31)	(32-39)	(40-47)
Write enable	06h					
Write disable	04h					
Read status register	05h	(S7-S0)(2)				
Write status Register	01h	(S7-S0)	(S15-S8)			
Page program	02h	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0(3)
Sector erase (4KB)	20h	A23-A16	A15-A8	A7-A0		
Block erase (32KB)	52h	A23-A16	A15-A8	A7-A0		
Block erase (64KB)	D8h	A23-A16	A15-A8	A7-A0		
Chip erase	C7h/60h					
Power-down	B9h					
Read data	03h	A23-A16	A15-A8	A7-A0	D7-D0	
Fast read	0Bh	A23-A16	A15-A8	A7-A0	dummy	D7-D0
Release powerdown/ID (4)	ABh	dummy	dummy	dummy	(ID7-D0)(2)	
Read Unique ID)	4Bh	dummy	dummy	dummy	dummy	(UID63-UID0)
Manufacturer/Device ID (4)	90h	dummy	dummy	00h	(MF7-MF0)	(ID7-D0)
JEDEC ID (4)	9Fh	(MF7-MF0) Manufacturer	(ID15-ID8) Memory Type	(ID7-D0) Capacity		
Enter OTP mode	3Ah					

Table 4 Standard SPI Instruction Set [1]

Dual SPI instructions Set

Instruction Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
Clock number	(0-7)	(8-15)	(16-23)	(24-31)	(32-39)	(40-47)
Fast read dual output	3Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0,…)[6]
Fast read dual I/O	BBh	A23-A8 [5]	A7-A0, M7-M0 [5]	(D7-DO,…)[6]		

Notes:

1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis “( )” indicate data output from the device on 1 or 2 DQ pins.
2. The Status Register contents and Device ID will repeat continuously until CS# terminates the instruction.
3. At least one byte of data input is required for Page Program and Program Security Sectors, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing will wrap to the beginning of the page and overwrite previously sent data.
4. See Table 3 Manufacturer and Device Identification table for device ID information.
5. Dual SPI address input format:
   DQ_0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0
   DQ_1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1
6. Dual SPI data output format: DQ_0 = (D6, D4, D2, D0) DQ_1 = (D7, D5, D3, D1)

Write Enable (WREN) (06h)

The Write Enable (WREN) instruction (Figure 5) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register instruction. The Write Enable (WREN) instruction is entered by driving CS# low, shifting the instruction code “06h” into the Data Input (DI) pin on the rising edge of CLK, and then driving CS# high.

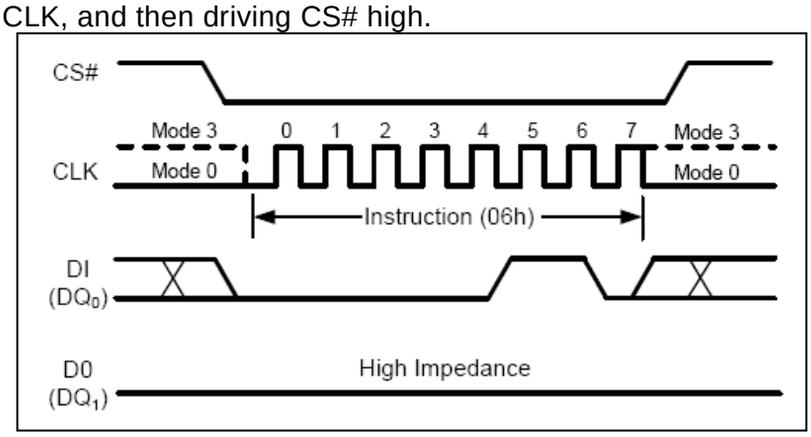


Figure 5 Write enable instruction

Write disable (WRDI) (04h)

The Write Disable (WRDI) instruction (Figure 6) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable (WRDI) instruction is entered by driving CS# low, shifting the instruction code “04h” into the DI pin and then driving CS# high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase, Chip Erase instructions.

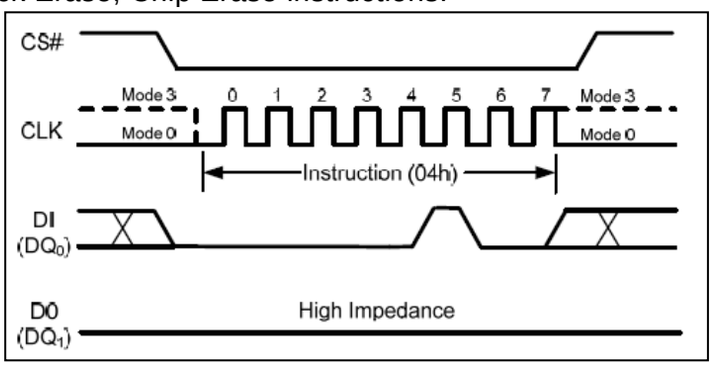


Figure 6 Write disable instruction

Read status register (RDSR) (05h)

The Read Status Register instructions allow the 8-bit Status Registers to be read. The instruction is entered by driving CS# low and shifting the instruction code “05h” into the DI pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 7. The Status Register bits are shown in Figure 4 and include the WIP, WEL, BP2-BP0 and SRP bits.

The Read Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the WIP status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously. The instruction is completed by driving CS# high.

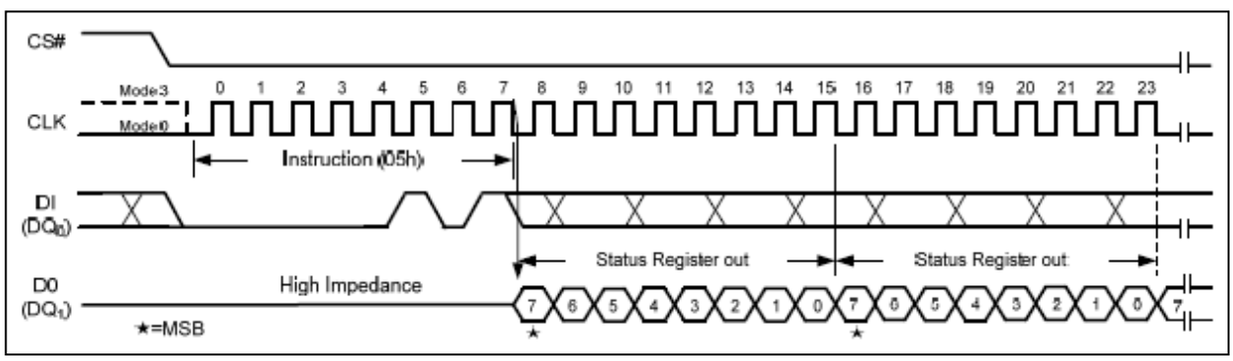


Figure 7 Read status register instruction

Write Status Register (WRSR) (01h)

The Write Status Register (WRSR) instruction allows the Status Register to be written. Only non-volatile Status Register bits SRP, BP2, BP1, BP0 can be written to. All other Status Register bit locations are read-only and will not be affected by the Write Status Register (WRSR) instruction. The Status Register bits are shown in Figure 4, and described in 10 Status Register.

To write non-volatile Status Register bits, a standard Write Enable (06h) instruction must previously have been executed for the device to accept the Write Status Register (WRSR) instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving CS# low, sending the instruction code “01h”, and then writing the status register data byte as illustrated in Figure 8.

To complete the Write Status Register (WRSR) instruction, the CS# pin must be driven high after the eighth or sixteenth bit of data that is clocked in. If this is not done the Write Status Register (WRSR) instruction will not be executed.

During non-volatile Status Register write operation (06h combined with 01h), after CS# is driven high, the self-timed Write Status Register cycle will commence for a time duration of t_W (See “12.6 AC Electrical Characteristics”). While the Write Status Register cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the WIP bit. The WIP bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Status Register cycle has finished, the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

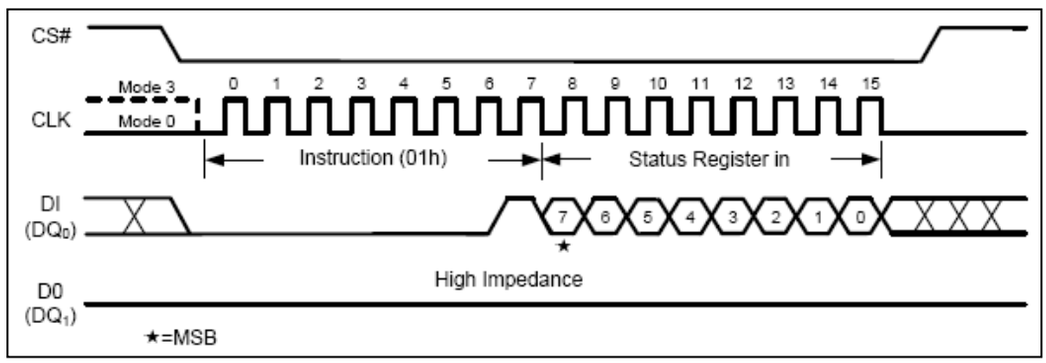


Figure 8 Writes status register instruction

Read Data (03h)

The Read Data instruction allows one or more data bytes to be sequentially read from the memory. The instruction is initiated by driving the CS# pin low and then shifting the instruction code “03h” followed by a 24-bit address A23-A0 into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving CS# high.

The Read Data instruction sequence is shown in Figure 9. If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (WIP =1) the instruction is ignored and will not have any effects on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of f_R (see “12.6 AC Electrical Characteristics”).

The Read Data (03h) instruction is only supported in Standard SPI mode.

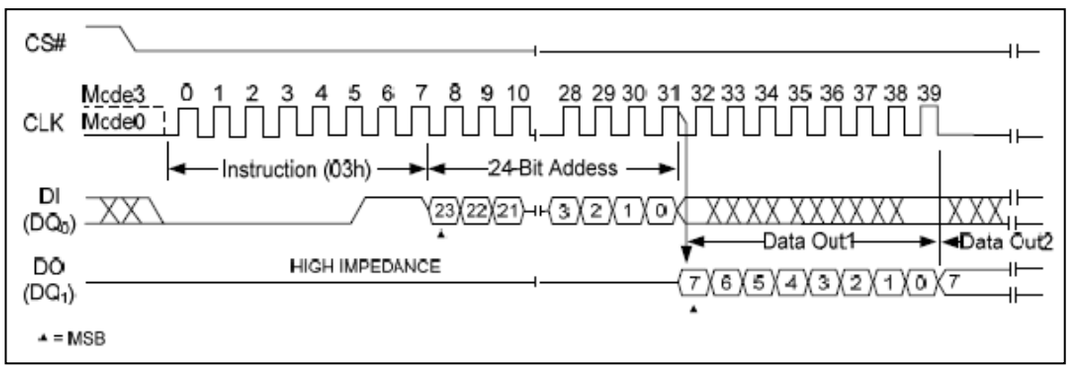


Figure 9 Read data instruction

Fast Read (0Bh)

The Fast Read instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of FR (see “12.6 AC Electrical Characteristics”). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 10. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the DO pin is a “don’t care”.

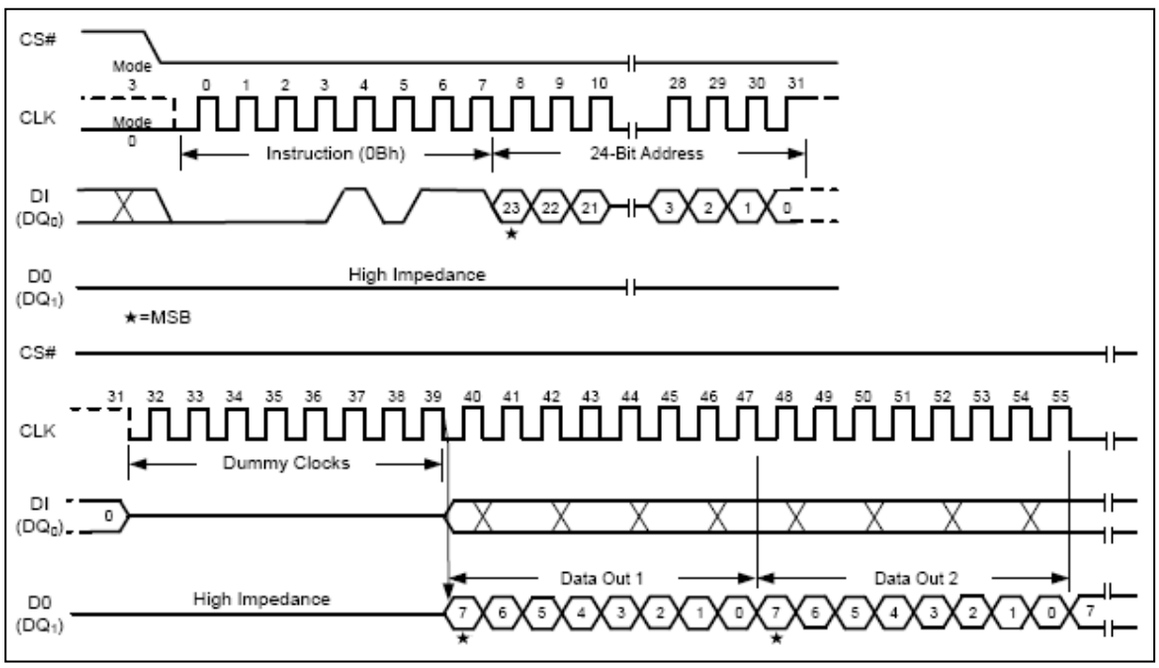


Figure 10 Fast read instruction

Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins; DQ_0 and DQ_1. This allows data to be transferred from the ACE25C100 at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Fast Read Dual Output instruction can operate at the highest possible frequency of FR (see “12.6 AC Electrical Characteristics”). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 11. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the DQ_0 pin should be high-impedance prior to the falling edge of the first data out clock.

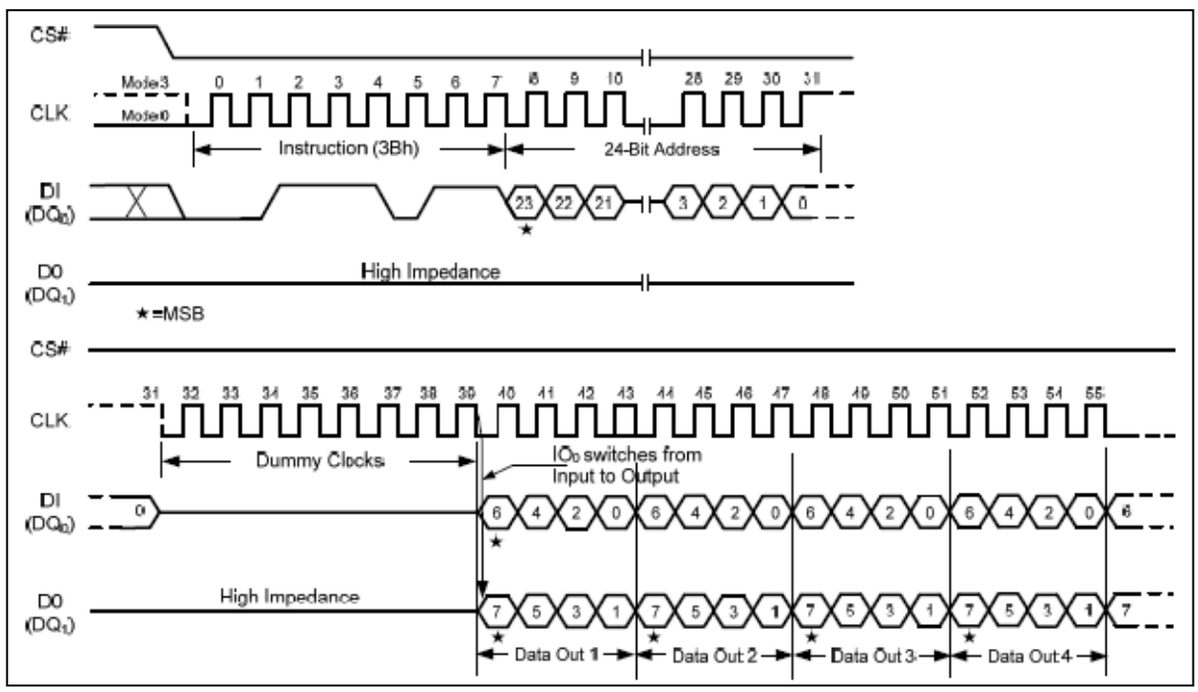


Figure 11 Fast read dual output instruction

Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) instruction allows for improved random access while maintaining two I/O pins, DQ_0 and DQ_1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Address bits A23-A0 two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

Fast Read Dual I/O with “Continuous Read Mode”

The Fast Read Dual I/O instruction can further reduce instruction overhead through setting the “Continuous Read Mode” bits (M7-0) after the input Address bits A23-A0, as shown in Figure 12. The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don’t care (“x”). However, the DQ pins should be high-impedance prior to the falling edge of the first data out clock.

If the “Continuous Read Mode” bits M5-4 = (1,0), then the next Fast Read Dual I/O instruction (after CS# is raised and then lowered) does not require the BBh instruction code, as shown in Figure 13. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after CS# is asserted low. If the “Continuous Read Mode” bits M5-4 do not equal to (1,0), the next instruction (after CS# is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFFFh on DQ_0 for the next.

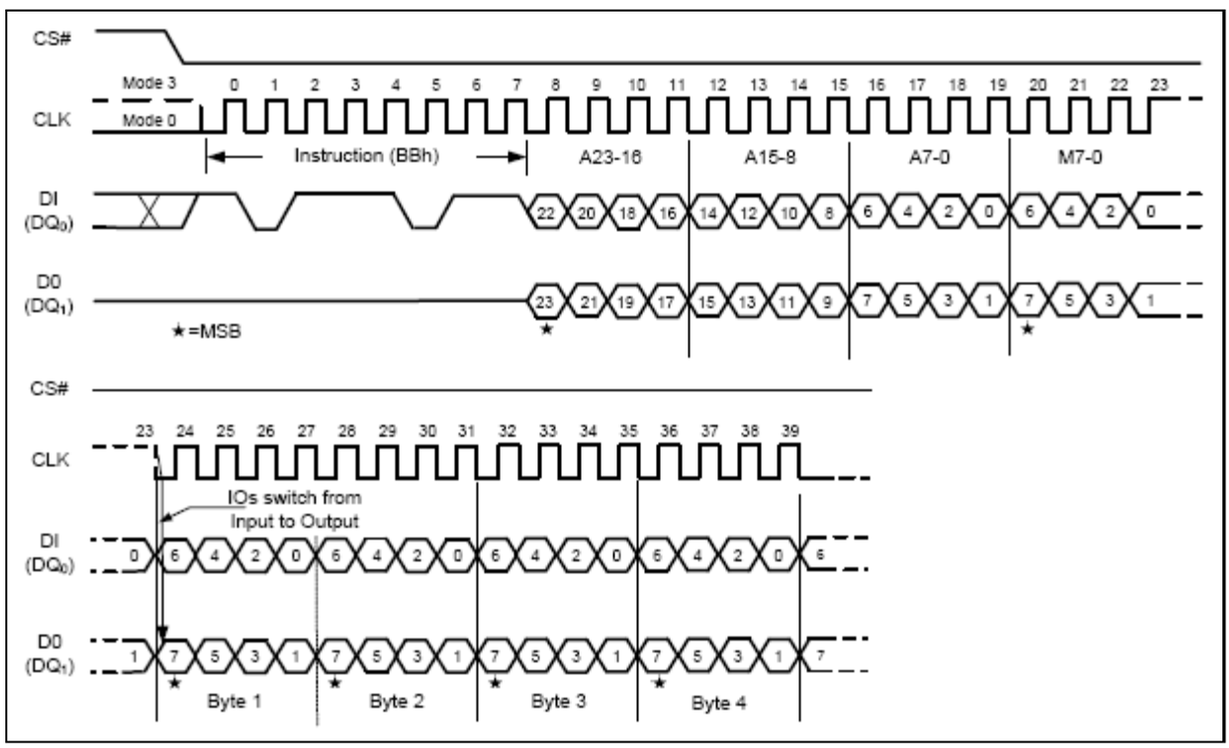


Figure 12 Fast read dual I/O instruction (initial instruction or previous M5-4≠10)

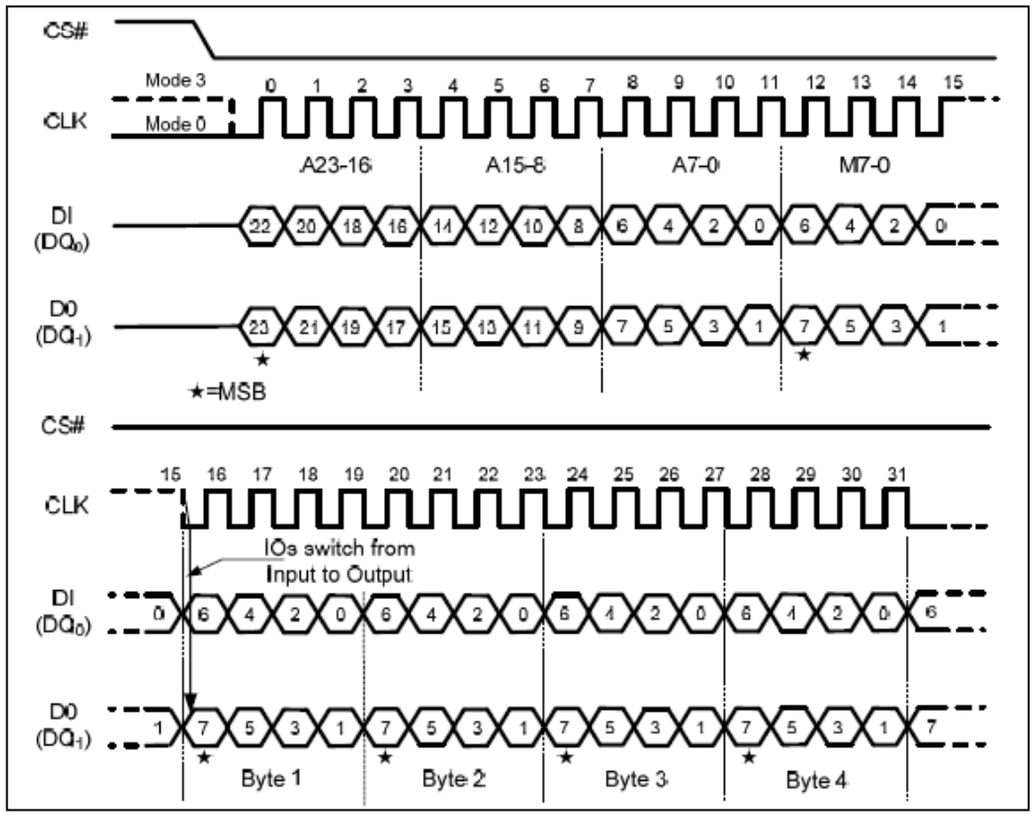


Figure 13 Fast read dual I/O instruction (previous instruction set M5-4=10)

Page Program (02h)

The Page Program instruction allows from one byte to 256 bytes (a page) of data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Page Program Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the CS# pin low then shifting the instruction code “02h” followed by a 24-bit address A23-A0 and at least one data byte, into the DI pin. The CS# pin must be held low for the entire length of the instruction while data is being sent to the device. The Page Program instruction sequence is shown in Figure 14.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceeds the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks can not exceed the remaining page length. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase instructions, the CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program instruction will not be executed. After CS# is driven high, the self-timed Page Program instruction will commence for a time duration of t_{PP} (See “12.6 AC Electrical Characteristics”). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is

ready to accept other instructions again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program instruction will not be executed if the addressed page is protected by the Block Protect (BP2, BP1, and BP0) bits.

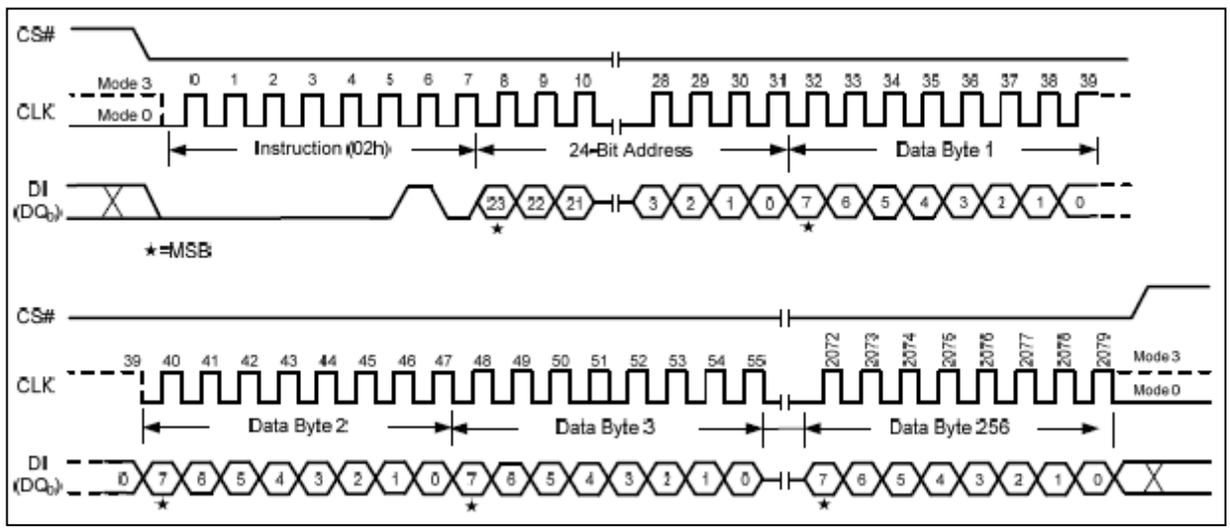


Figure 14 Page program instruction

Sector Erase (20h)

The Sector Erase instruction sets all memory within a specified sector (4K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code “20h” followed a 24-bit sector address A23-A0 (see Figure 1). The Sector Erase instruction sequence is shown in Figure 15 .

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase instruction will not be executed. After CS# is driven high, the self-timed Sector Erase instruction will commence for a time duration of t_{SE} (See “12.6 AC Electrical Characteristics”). While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase instruction will not be executed if the addressed page is protected by the Block Protect (BP2, BP1, and BP0) bits (see Table 2 Status Register Memory Protection table).

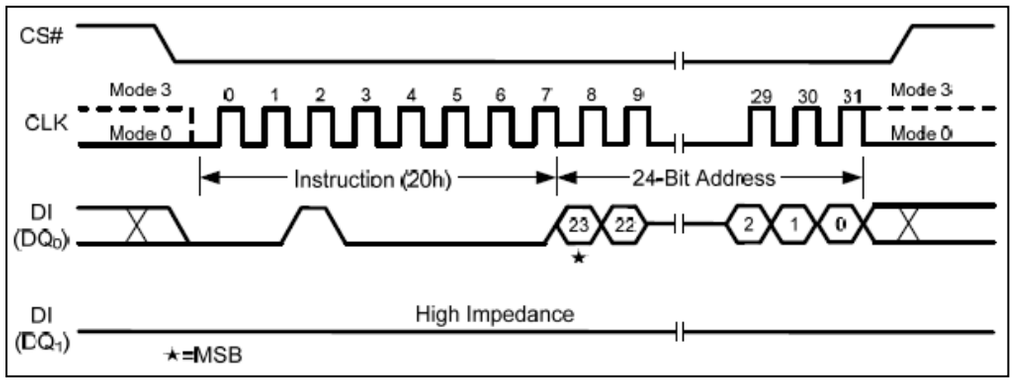


Figure 15 Sector erase instruction

32KB Block Erase (BE32) (52h)

The 32KB Block Erase instruction sets all memory within a specified block (32K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code “52h” followed a 24-bit block address A23-A0. The Block Erase instruction sequence is shown in Figure 16.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase Instruction will commence for a time duration of t_{BE2} (See 12.6 AC Electrical Characteristics”). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (BP2, BP1, and BP0) bits (see Table 2 Status Register Memory Protection table).

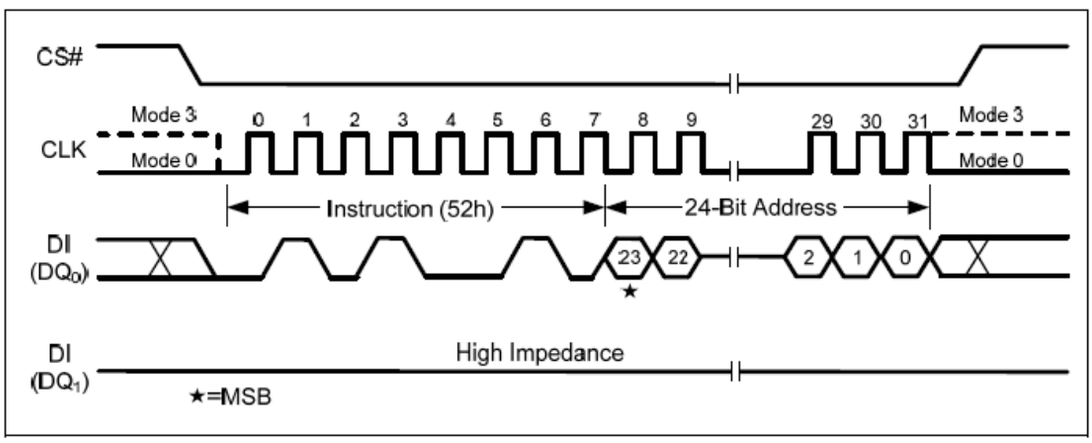


Figure 16 32KB Block Erase Instruction (SPI Mode)

64K Block Erase (BE) (D8h)

The 64KB Block Erase instruction sets all memory within a specified block (64K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code “D8h” followed a 24-bit block address A23-A0. The Block Erase instruction sequence is shown in Figure 17.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After CS# is driven high, the self-timed Block Erase instruction will commence for a time duration of t_{BE} (See 12.6 AC Electrical Characteristics”). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (BP2, BP1, and BP0) bits (see Table 2 Status Register Memory Protection table).

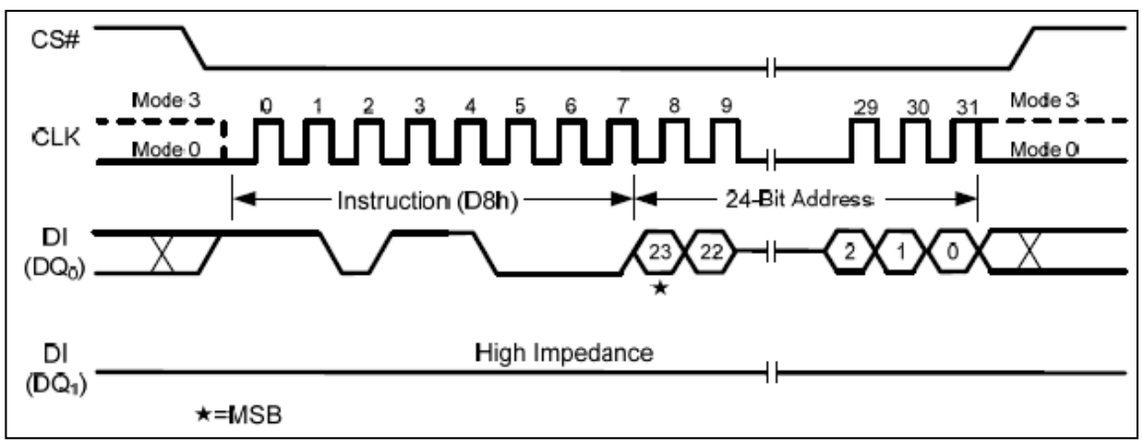


Figure 17 Block erase instruction

Chip Erase (CE) (C7h / 60h)

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code “C7h” or “60h”. The Chip Erase instruction sequence is shown in Figure 18.

The CS# pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After CS# is driven high, the self-timed Chip Erase instruction will commence for a time duration of t_{CE} (See “12.6 AC Electrical Characteristics”). While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the WIP bit. The WIP bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction will not be executed if any page is protected by the Block Protect (BP2, BP1, and BP0) bits.

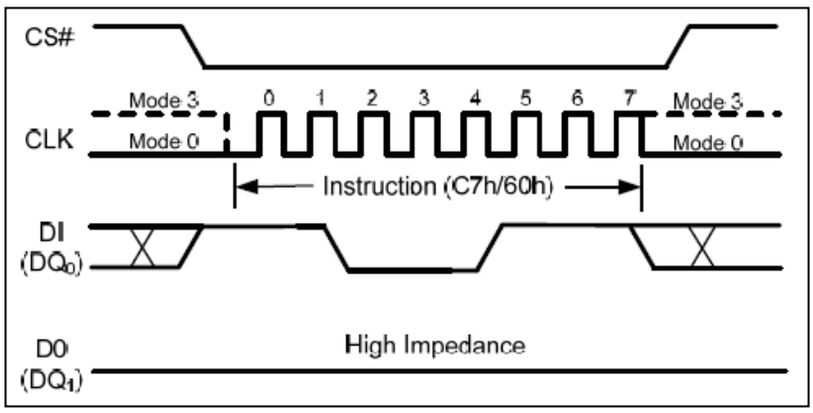


Figure 18 Chip erase instruction

Power-down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Power-down instruction. The lower power consumption makes the Power-down instruction especially useful for battery powered applications (See I_{CC1} and I_{CC2} in "12.6 AC Electrical Characteristics"). The instruction is initiated by driving the CS# pin low and shifting the instruction code "B9h" as shown in Figure 19.

The CS# pin must be driven high after the eighth bit has been latched. If this is not done the Power-down instruction will not be executed. After CS# is driven high, the power-down state will enter within the time duration of t_{DP} (See "12.6 AC Electrical Characteristics"). While in the power-down state only the Release from Power- down / Device ID instruction, which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of I_{CC1}.

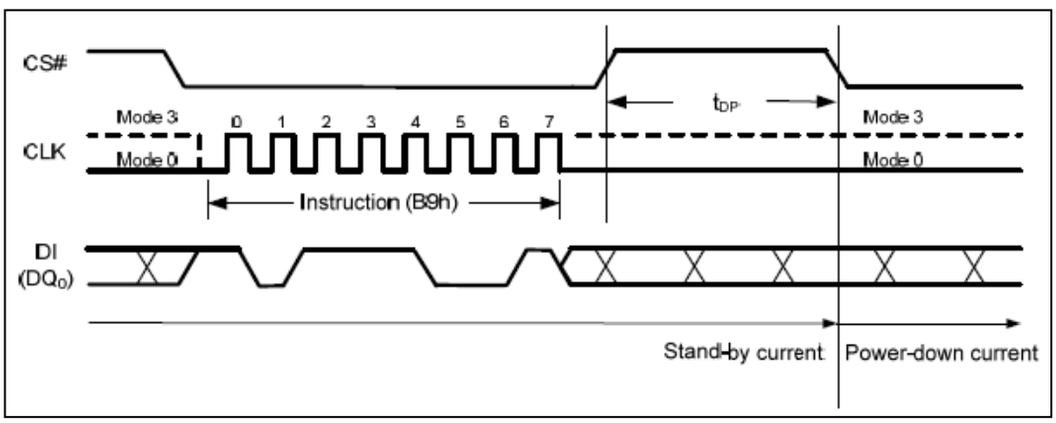


Figure 19 Deep power-down instruction

Release Power-down / Device ID (ABh)

The Release from Power-down / Device ID instruction is a multi-purpose instruction. It can be used to release the device from the power-down state, or obtain the devices electronic identification (ID) number.

To release the device from the power-down state, the instruction is issued by driving the CS# pin low, shifting the instruction code “ABh” and driving CS# high as shown in Figure 20. Release from power-down will take the time duration of tRES1 (See “12.6 AC Electrical Characteristics”) before the device will resume normal operation and other instructions are accepted. The CS# pin must remain high during the tRES1 time duration.

When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the CS# pin low and shifting the instruction code “ABh” followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 19. The Device ID value for the ACE25C100 is listed in Table 3 Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving CS# high.

When used to release the device from the power-down state and obtain the Device ID, the instruction is the same as previously described, and shown in Figure 21, except that after CS# is driven high it must remain high for a time duration of t_{RES2} (See “12.6 AC Electrical Characteristics”). After this time duration the device will resume normal operation and other instructions will be accepted. If the Release from Power-down / Device ID instruction is issued while an Erase, Program or Write cycle is in process (when WIP equals 1) the instruction is ignored and will not have any effects on the current cycle.

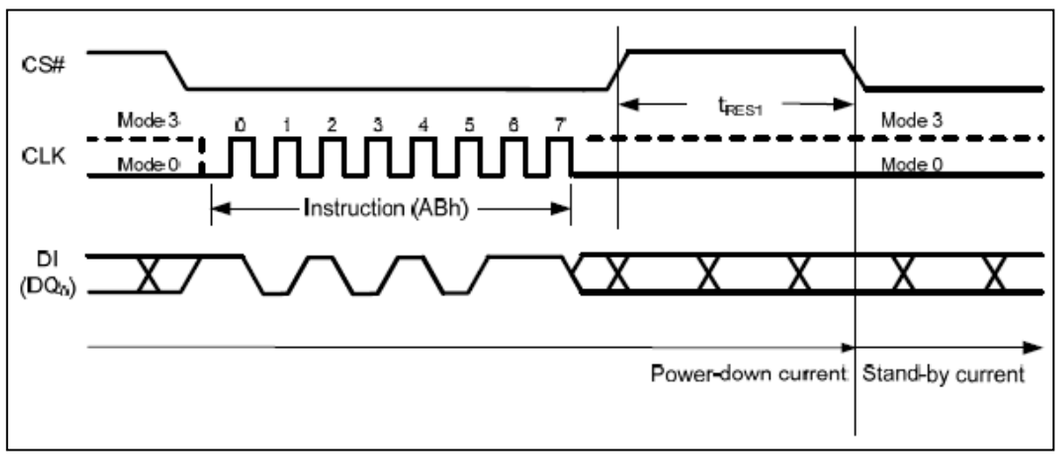


Figure 20 Release power-down instruction

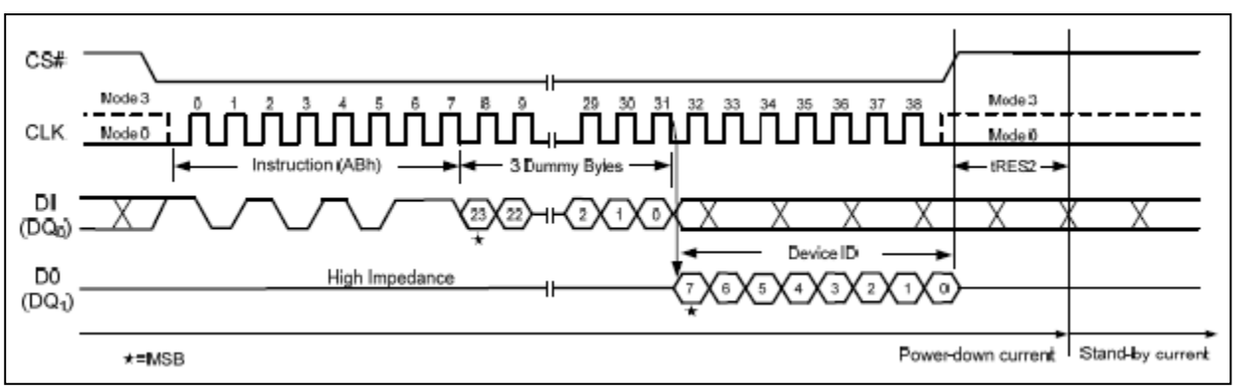


Figure 21 Release power-down / device ID instruction

Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the CS# pin low and shifting the instruction code “90h” followed by a 24-bit address A23-A0 of 000000h. After which, the Manufacturer ID for ACE Technology CO., LTD. (A1h) and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 22. The Device ID value for the ACE25C100 is listed in Table 3 Manufacturer and Device Identification table. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

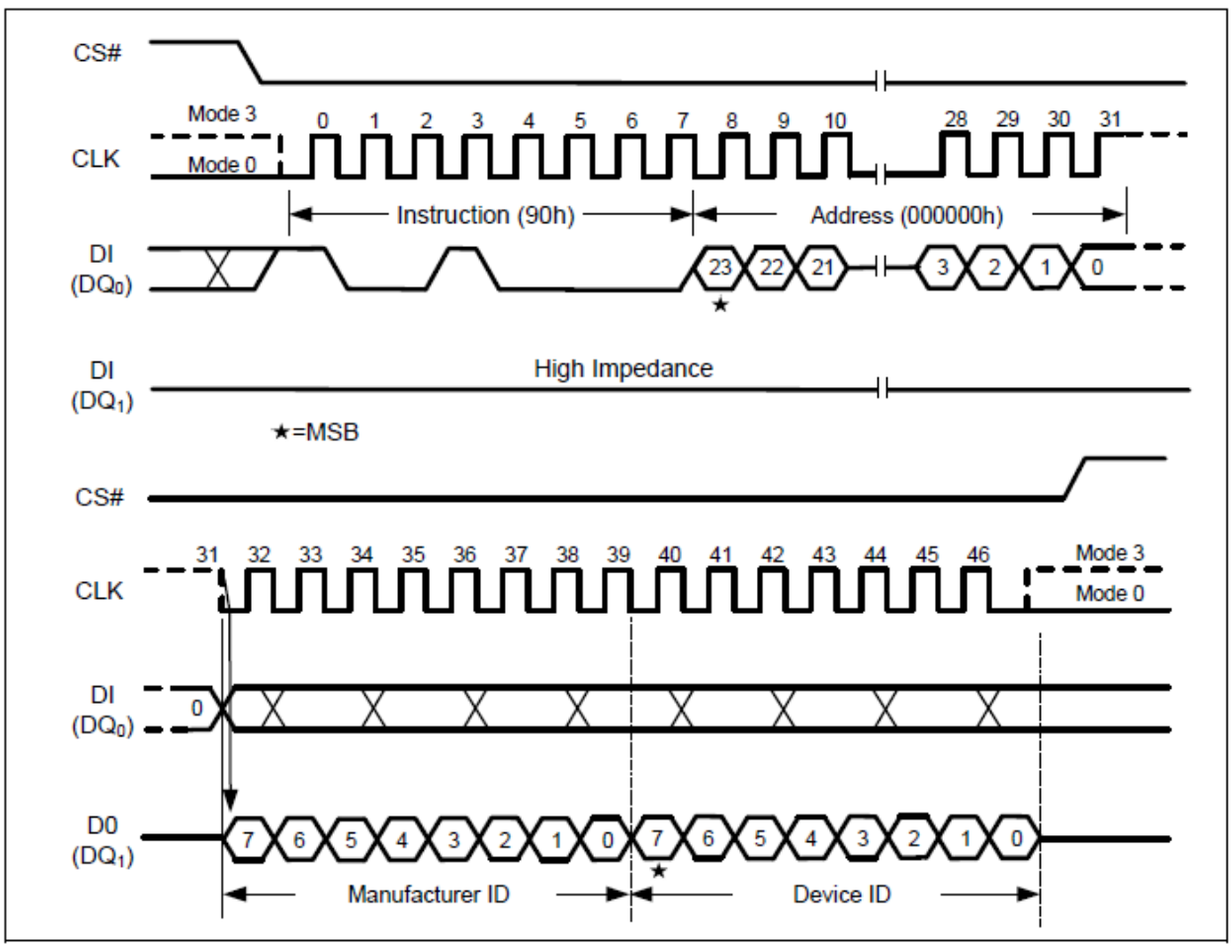


Figure 22 Read manufacturer / device ID instruction

Read Unique ID Number(4Bh)

The Read Unique ID Number instruction accesses a factory-set read-only 64-bit number that is unique to each ACE25C100 device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the CS# pin low and shifting the instruction code “4Bh” followed by a four bytes of dummy clocks. After which, the 64- bit ID is shifted out on the falling edge of CLK as shown in Figure 23.

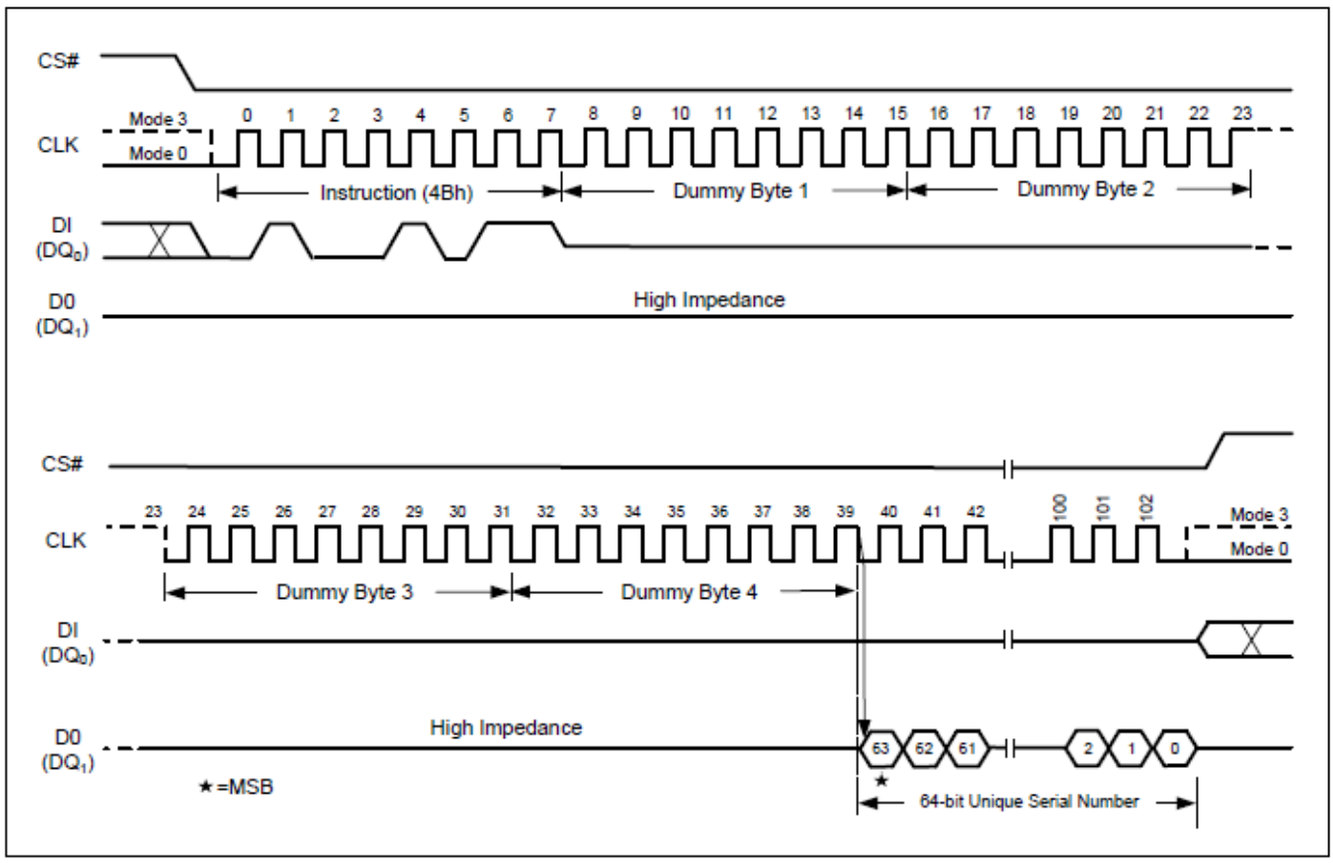


Figure 23 Read Unique ID Number Instruction (SIP Mode only)

Read JEDEC ID (9Fh)

For compatibility reasons, the ACE25C100 provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories. The instruction is initiated by driving the CS# pin low and shifting the instruction code “9Fh”. The JEDEC assigned Manufacturer ID byte for ACE Technology Co., LTD. (A1h) and two Device ID bytes, Memory Type (ID15-ID8) and Capacity ID7-D0 are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 24. For memory type and capacity values refer to Table 3 Manufacturer and Device Identification table.

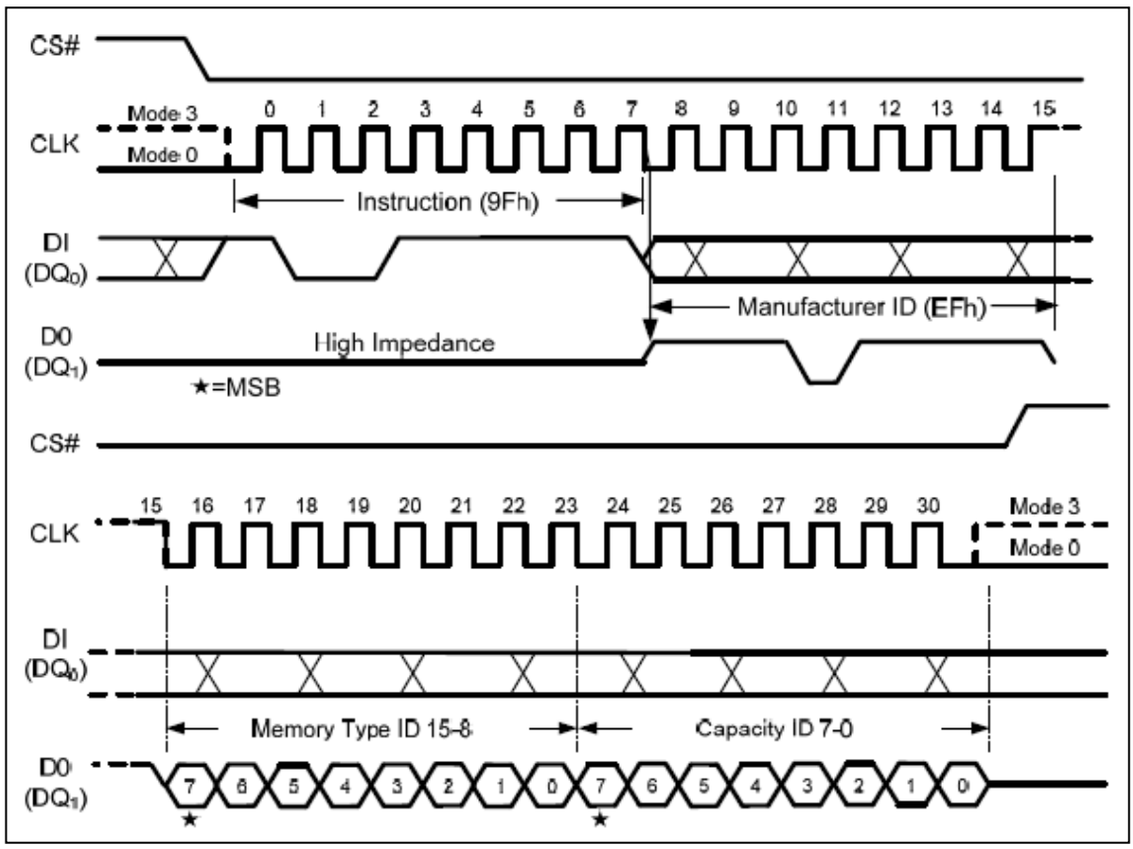


Figure 24 Read JEDEC ID instruction

Enter OTP Mode (3Ah)

This Flash has an extra 256 bytes security sector, user must issue ENTER OTP MODE command to read, program or erase security sector. After entering OTP mode, the security sector is mapping to sector 31, SRP bit becomes LB and can be read with RDSR command. Program / Erase command will be disabled when LB is '1'

WRSR command will ignore the input data and program LB to 1. User must clear the protect bits before enter OTP mode.

Security sector can only be program and erase before LB equal '1' and BP[2:0] = '000'. In OTP mode, user can read other sectors, but program/erase other sectors only allowed when LB equal '0'.

User can use WRDI (04h) command to exit OTP mode.

Sector	Sector size	Adress range
15	256 byte	01F000h-01F0FFh

Table 6 Security sector address

Note: The secruty sector is mapping to sector 31

While in OTP mode, user can use Sector Erase (20h) command only to erase OTP data.

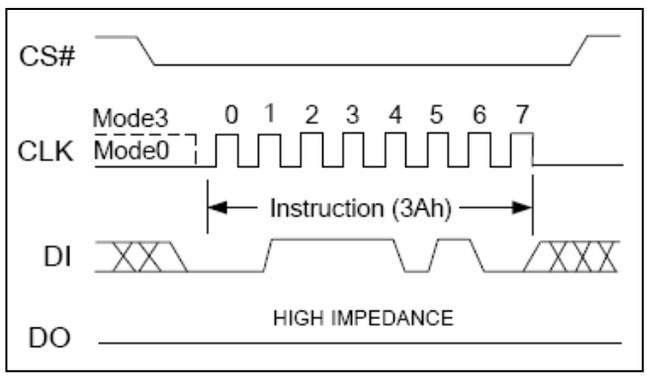


Figure 23 Enter OTP Mode

Electrical Characteristics

Absolute Maximum Ratings

Operating Temperature	-40 to 85℃
Storage Temperature	-65 to 150℃
Voltage on I/O pin with respect to ground	-0.5 to V_{CC}+0.4V
V_{CC}	-0.5 to 4.0V

Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Capacitance

Applicable over recommended operating range from: V_{IN}=0V, T_A=25°C, f=5 MHz, V_{CC}=2.7V

Symbol	Test condition	Max	Units	Conditions
C_{IN}(1)	Input Capacitance	6	pF	V_{IN}=0V
C_{OUT}(1)	Output Capacitance	8	pF	V_{OUT}=0V

Note: This parameter is characterized and is not 100% tested.

Power-up Timing

Applicable over recommended operating range from: T_A=-40°C to 85°C, V_{CC}=2.7V to 3.6V, (unless otherwise noted)

Parameter	Symbol	Spec		Unit
		Min	Max	
VCC (min) to CS# Low	T_{VSL}	10		us
Time delay before write instruction	t_{PUW}	1	10	ms

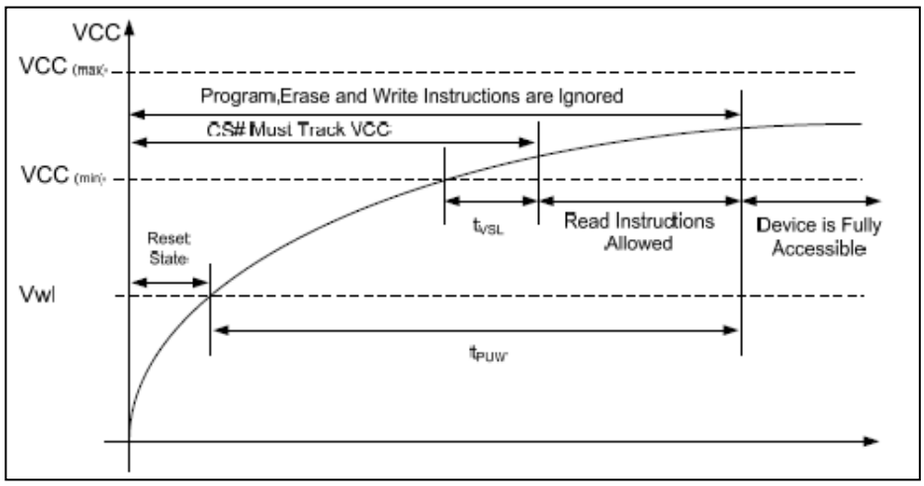


Figure 25 Power-up Timing

DC Electrical Characteristics

Applicable over recommended operating range from: T_A=-40°C to 85°C, V_{CC}=2.7V to 3.6V, (unless otherwise noted).

Symbol	Parameter	Conditions	Spec			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2.7		3.6	V
I_{LI}	Input leakage current				±2	uA
I_{LO}	Output leakage current				±2	uA
I_{CC1}	Standby current	V_{CC}=3.6V, CS#=V_{CC} V_{IN}=V_{SS} or V_{CC}		1	5	uA
I_{CC2}	Deep power-down current	V_{CC}=3.6V, CS#=V_{CC} V_{IN}=V_{SS} or V_{CC}		1	5	uA
I_{CC3}(1)	Operating Current (READ)	V_{CC}=3.6V, CLK=0.1, V_{CC}/0.9V_{CC}, at 100MHz, DQ open			25	mA
I_{CC4}	Operating current (WRSR)	V_{CC}=3.6V, CS#=V_{CC}		8	12	mA
I_{CC5}	Operating current (PP)	V_{CC}=3.6V, CS#=V_{CC}		20	25	mA
I_{CC6}	Operating current (SE)	V_{CC}=3.6V, CS#=V_{CC}		20	25	mA
I_{CC7}	Operating current (BE)	V_{CC}=3.6V, CS#=V_{CC}		20	25	mA
V_{IL}(2)	Input low voltage		-0.5		0.3V_{CC}	V
V_{IH}(2)	Input high voltage		0.7V_{CC}		V_{CC}+0.4	V
V_{OL}	Output low voltage	I_{OL}=1.6mA				V
V_{OH}	Output high voltage	I_{OH}=-100uA	V_{CC}-0.2			V
V_{WI}	Write inhibit threshold voltage		1.0		2.2	V

Table 7 DC Characteristics

Notes: 1. Checker Board Pattern

2. V_{IL} min and V_{IH} max are reference only and are not tested

AC Measurement Conditions

Symbol	Parameter	Spec		Unit
		Min	Max	
CL	Load capacitance		20	pF
TR, TF	Input rise and fall times		5	ns
VIN	Input pulse voltage	0.2 V_{CC} to 0.8 V_{CC}		V
IN	Input timing reference voltages	0.3 V_{CC} to 0.7 V_{CC}		V
OUT	Output timing reference voltages	0.5 V_{CC}		V

Table 8 AC Measurement Conditions

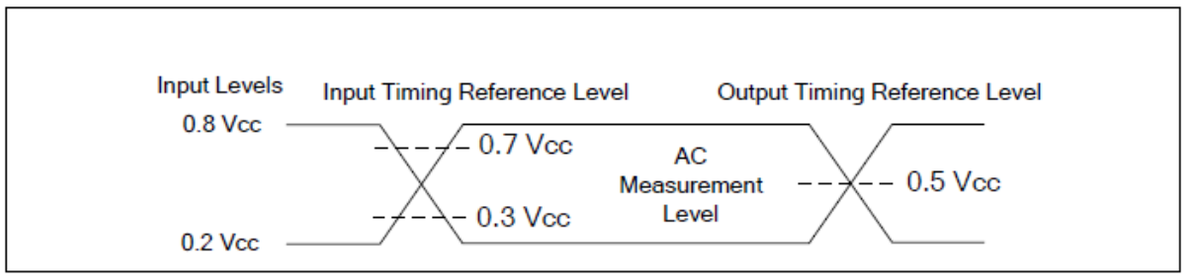


Figure 26 AC Measurement I/O waveform

AC Electrical Characteristics

Applicable over recommended operating range from: T_A=-40°C to 85°C, V_{CC}=2.7V to 3.6V, (unless otherwise noted).

Symbol	Parameter	Spec			Unit
		Min	Typ	Max	
F_R	Serial Clock Frequency for: FAST_READ, PP, SE, BE, DP, RES, WREN, WRDI, WRSR			100	MHz
f_R	Serial Clock Frequency for READ, RDSR, RDID			50	MHz
t_{CH}(1)	Serial Clock High Time	4			ns
t_{CL}(1)	Serial Clock Low Time	4			ns
t_{CLCH}(2)	Serial Clock Rise Time (Slew Rate)	0.1			V/ns
t_{CHCL}(2)	Serial Clock Fall Time (Slew Rate)	0.1			V/ns
t_{SLCH}	CS# Active Setup Time	5			ns
t_{CHSH}	CS# Active Hold Time	5			ns
t_{SHCH}	CS# Not Active Setup Time	5			ns
t_{CHSL}	CS# Not Active Hold Time	5			ns
t_{SHSL}	CS# Deselect Time (for Array Read → Array Read / Erase or Program → Read Status Register)	10/50			ns
t_{SHQZ}(2)	Output Disable Time			6	ns
t_{CLQX}	Output Hold Time	0			ns
t_{DVCH}	Data In Setup Time	2			ns

t_{CHDX}	Data In Hold Time	5			ns
t_{HLCH}	HOLD# Low Setup Time (relative to CLK)	5			ns
t_{HHCH}	HOLD# High Setup Time (relative to CLK)	5			ns
t_{CHHH}	HOLD# Low Hold Time (relative to CLK)	5			ns
t_{CHHL}	HOLD# High Hold Time (relative to CLK)	5			ns
t_{HLQZ}(2)	HOLD# Low to High-Z Output			6	ns
t_{HHQX}(2)	HOLD# High to Low-Z Output			6	ns
t_{CLQV}	Output Valid from CLK			8	ns
t_{WHSL}	Write Protect Setup Time before CS# Low	20			ns
t_{SHWL}	Write Protect Hold Time after CS# High	100			ns
t_{DP}(2)	CS# High to Deep Power-down Mode			3	us
t_{RES1}(2)	CS# High to Standby Mode without Electronic Signature Read			3	us
t_{RES2}(2)	CS# High to Standby Mode with Electronic Signature Read			1.8	us
t_W	Write Status Register Cycle Time		10	15	ms
t_{PP}	Page Programming Time		1.5	5	ms
t_{SE}	Sector Erase Time		0.09	0.3	s
t_{BE1}	Block Erase Time (64KB)		0.5	2	s
t_{BE2}	Block Erase Time (32KB)		0.3	1.2	s
t_{CE}	Chip Erase Time		1.5	4	s

Notes: 1. $t_{CH}+t_{CL} >= 1 / F_R$ or $1/f_R$

2. This parameter is characterized and is not 100% tested.

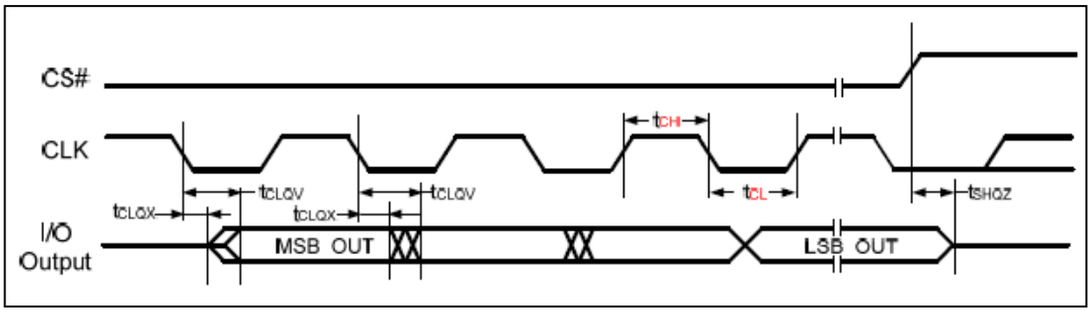


Figure 27 Serial output timing

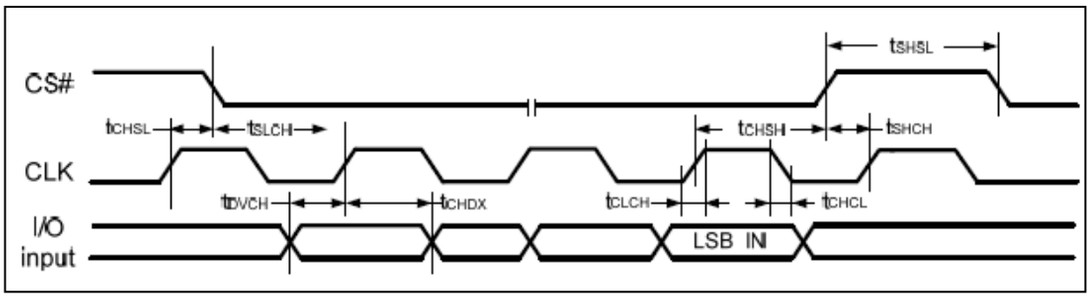


Figure 28 Serial Input timing

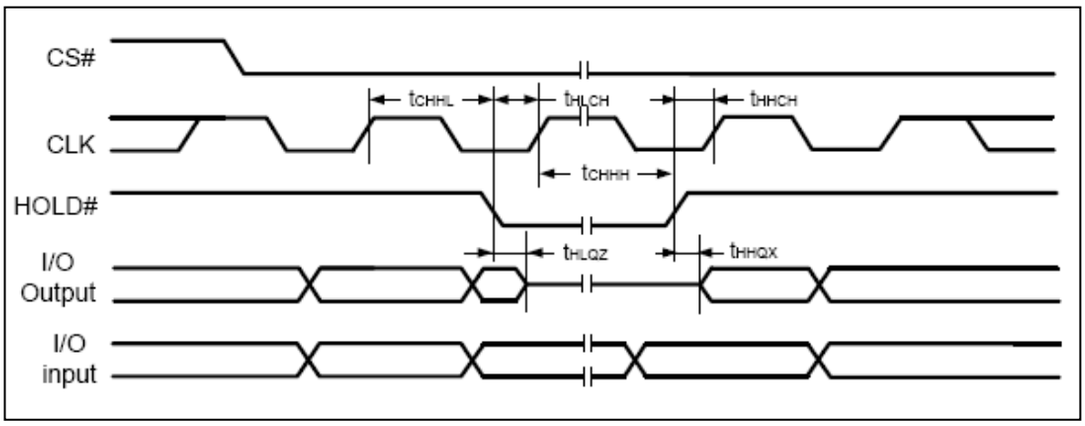
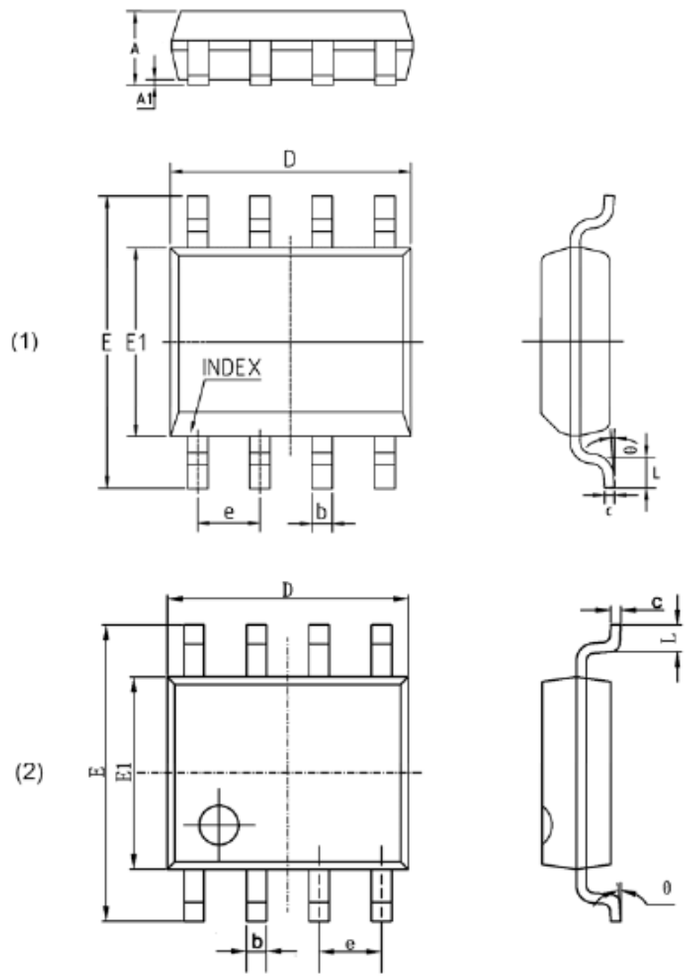


Figure 29 Hold timing

Packaging information

SOP-8

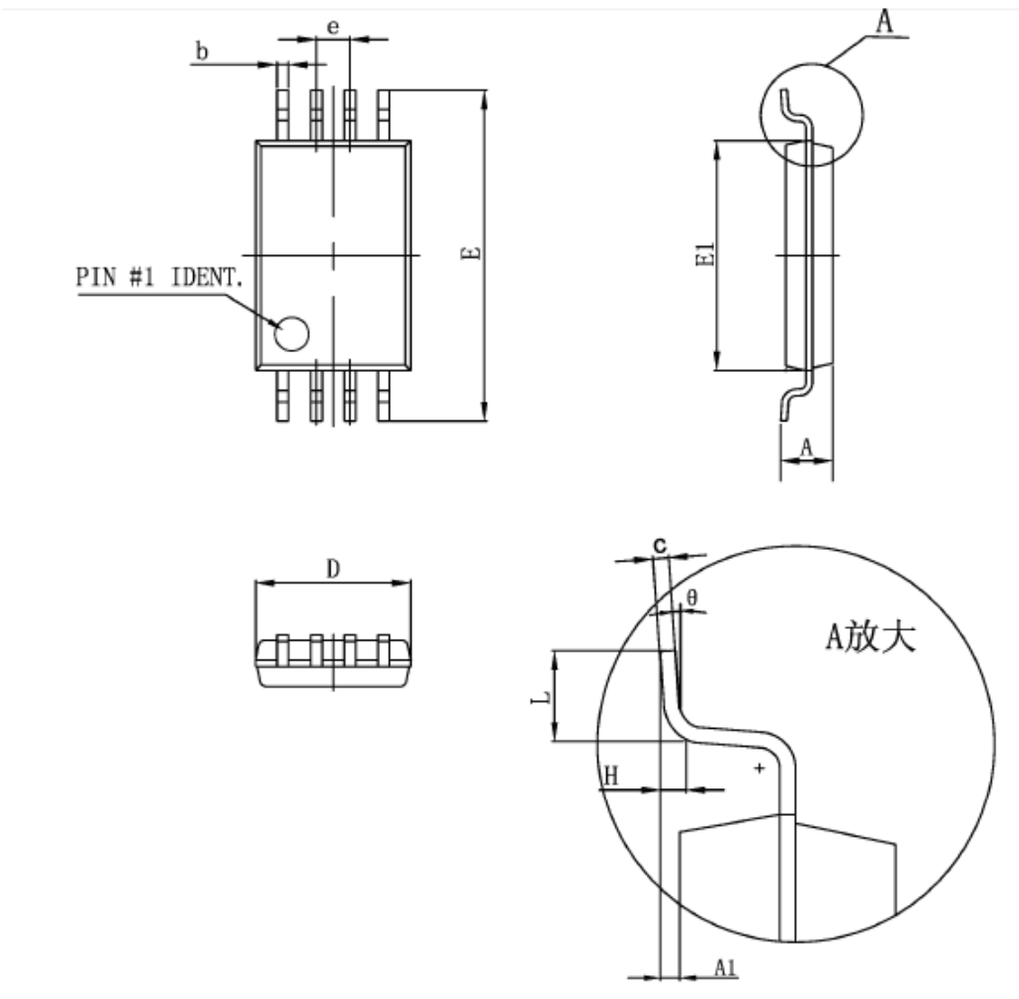


Symbol	MIN	MAX
A	1.350	1.750
A1	0.050	0.250
b	0.330	0.510
c	0.150	0.250
D	4.700	5.150
E1	3.800	4.000
E	5.800	6.200
e	1.270(BSC)	
L	0.400	1.270
θ	0°	8°

NOTE:
1. Dimensions are in Millimeters.

Packaging information

TSSOP-8

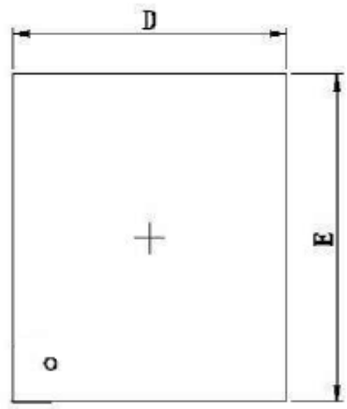


Symbol	MIN	MAX
D	2.900	3.100
E1	4.300	4.500
b	0.190	0.300
c	0.090	0.200
E	6.250	6.550
A		1.200
A1	0.050	0.150
e	0.650 (BSC)	
L	0.450	0.750
θ	0°	8°

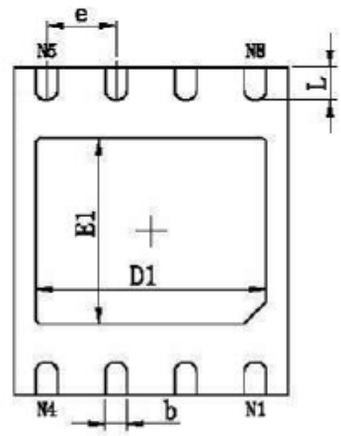
NOTE:
1. Dimensions are in Millimeters.

Packaging information

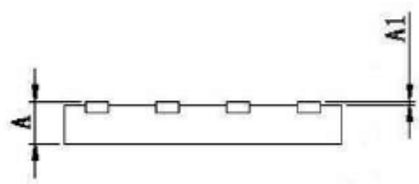
TDFN-8



Top View



Bottom View



Side View

Symbol	MIN	MAX
A	0.700	0.800
A1	0.000	0.050
D	4.924	5.076
E1	3.300	3.500
E	5.924	6.076
b	0.350	0.450
e	1.270TYP	
L	0.524	0.676

NOTE:
1. Dimensions are in Millimeters.

Notes

ACE does not assume any responsibility for use as critical components in life support devices or systems without the express written approval of the president and general counsel of ACE Electronics Co., LTD. As sued herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and shoes failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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